# NI PCI-5640R Specifications

## Reconfigurable IF Transceiver

このドキュメントには、日本語ページも含まれています。

This document lists the specifications of the NI PCI-5640R IF transceiver. These specifications are warranted at 0 to 40 °C ambient unless otherwise specified and include a 10 minute warm-up time from ambient conditions. Typical values are valid over 25 °C ± 10 °C. All figures show typical performance at 25 °C. All specifications are subject to change without notice. Visit `ni.com/manuals` for the most current specifications and product documentation.

## Analog Input

Number of channels ..... 2

Resolution ..... 14 bits

Maximum sample rate ..... 100 MSamples/second (MS/s)

Maximum bandwidth ..... 20 MHz (limited by digital downconverter)

Input impedance ..... 50 Ω nominal

Input return loss ..... < –15 dB

Input coupling ..... AC-coupled

AC coupling cutoff frequency (–3dB) ..... 50 kHz typical

Full-scale input range ..... +8.5 dBm peak (1.68 $V_{pk-pk}$ sine) at 10 MHz (± 0.5 dB max calibration data uncertainty; <±1 dB typical without calibration)

Maximum input overload ..... +24 dBm peak (10 $V_{pk-pk}$ sine, 3.5 $V_{RMS}$)

Passband flatness (referenced at 10 MHz) 250 to 80 MHz ..... <±0.5 dB (calibration data uncertainty) +0.25 dB, –0.75 dB (without calibration)

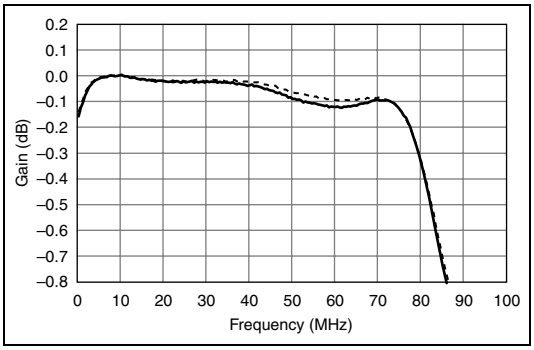


**Figure 1.** Input Frequency Response for Both Channels (Passband)

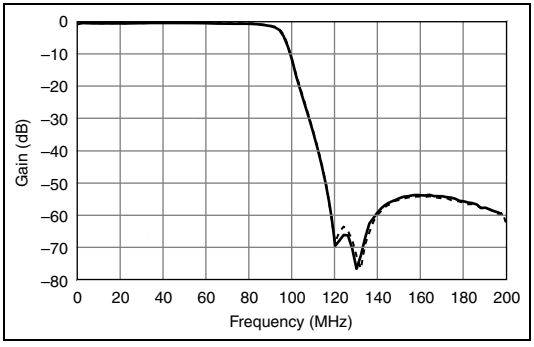


**Figure 2.** Input Frequency Response for Both Channels (Broadband)

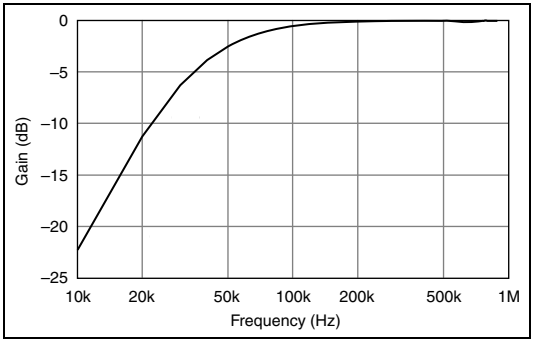


**Figure 3.** Input Frequency Response (Low Frequency)

Input group delay variation .....10 ns typical, up to 80 MHz

Stopband rejection.....>50 dB at 120 MHz typical

Channel-to-channel crosstalk

<40 MHz.....<–70 dB typical

≥40 to 80 MHz.....<–60 dB typical

## Spectral Characteristics

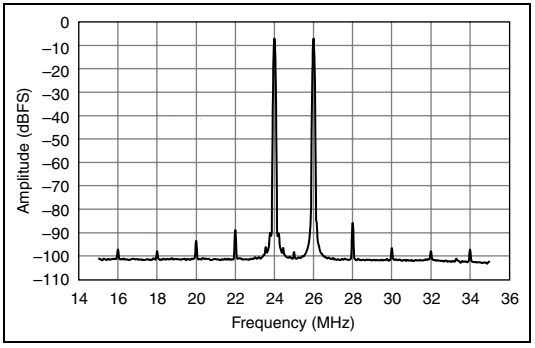


**Figure 4.** Analog Input Two-Tone Intermodulation Distortion (IMD)

**Note** Phase noise skirts in Figure 4 are due to signal generators and do not represent NI PCI-5640R performance.

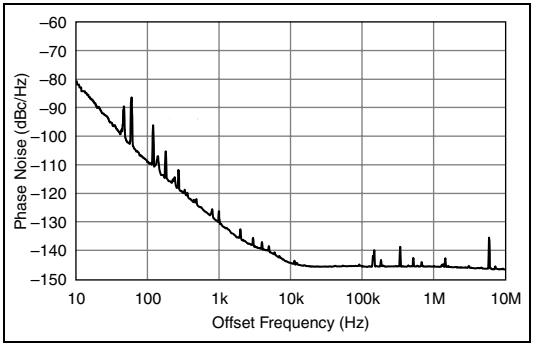


**Figure 5.** Phase Noise at Carrier Frequency = 68.659 MHz

Signal to noise ratio .....>76 dB typical (–1 dBfs at 68 MHz tone, bandwidth = 5 MHz)

Average noise density (100 kHz to 80 MHz) ..... –143 dBm/Hz typical

## Digital Downconverter (DDC)

Number of channels..... Up to 6 per ADC

Bandwidth..... Up to 20 MHz using all six processing channels

Decimation

Using NI-5640R driver..... ÷4 to ÷2,048

Using LabVIEW FPGA ..... ÷4 to ÷32,768*

* Decimation rate is referenced to a maximum of 100 MS/s complex (I/Q) data.

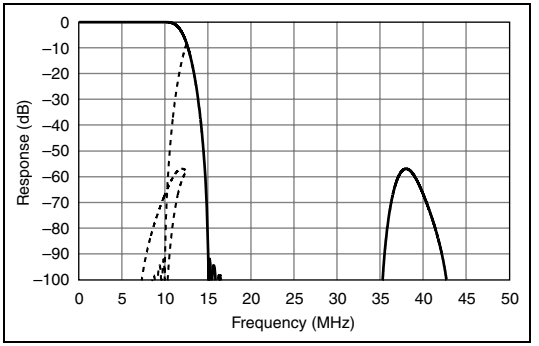


**Figure 6.** DDC Filter Performance, 20 MHz Span

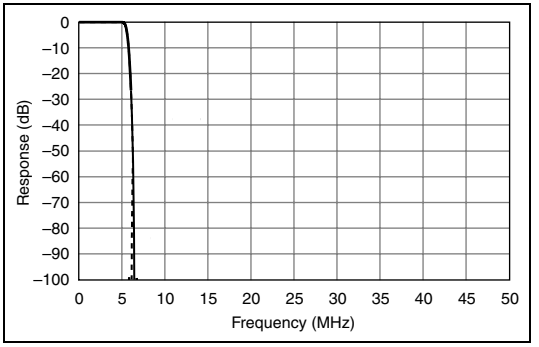


**Figure 7.** DDC Filter Performance, 10 MHz Span

Sample DDC filter performance plots using NI-5640R 1.0 library example filter designs: Figure 6 depicts a 20 MHz span; Figure 7 depicts a 10 MHz span. The dark lines show the true response of the digital filter in the DDC. The dashed lines show the effect of aliasing after decimation. Notice that for a 10 MHz span, the DDC filter aliasing artifacts have virtually no impact; whereas for a full 20 MHz span, signals at frequency offsets near ±40 MHz can alias back up to –66 dBc within the ±10 MHz passband near the band edges.

## Analog Output

Number of channels ..... 2

Resolution ..... 14 bits

Maximum update rate ..... 200 MS/s

Output impedance ..... 50 Ω nominal

Output return loss..... <–15 dB

Output coupling ..... AC-coupled

AC coupling cutoff frequency
(–3dB).....50 kHz typical

Full-scale output range

Using NI-5640R driver .....–4 dBm peak

Using LabVIEW FPGA .....+2 dBm peak (0.8 $V_{pk-pk}$) nominal into 50 Ω, –1.5 dBm with sinc and total interpolation factor = 4 at 10 MHz (± 0.5 dB max calibration data uncertainty, <± 1 dB typical without calibration)*

Tuning speed .....1 ms

Output protection.....Indefinite duration short to ground

Reverse power protection.....+24 dBm peak (10 $V_{pk-pk}$, 3.5 $V_{RMS}$)

Passband flatness
(referenced at 10 MHz) ..... <±1 dB typical, 250 kHz to 80 MHz (With CIC and sinc compensation filter engaged)

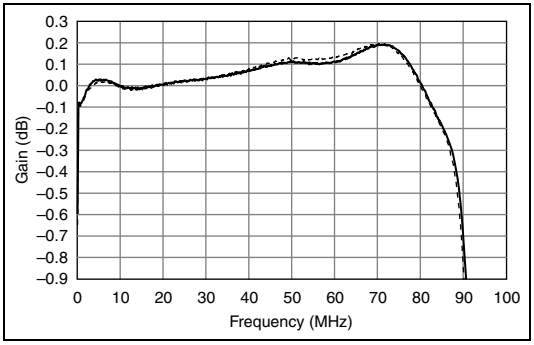


**Figure 8.** Analog Output Passband Flatness (Referenced to 10 MHz)

Channel-to-channel crosstalk

<40 MHz.....<–70 dB typical

≥40 to 80 MHz.....<–60 dB typical

* CIC compensation filter lowers the level by 0.59 dB when the total interpolation factor equals 8 and by 0.79 when the total interpolation factor >8.

## Spectral Characteristics

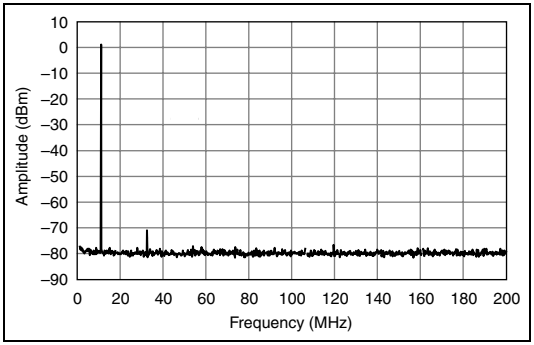


**Figure 9.** Analog Output Single-Tone Distortion

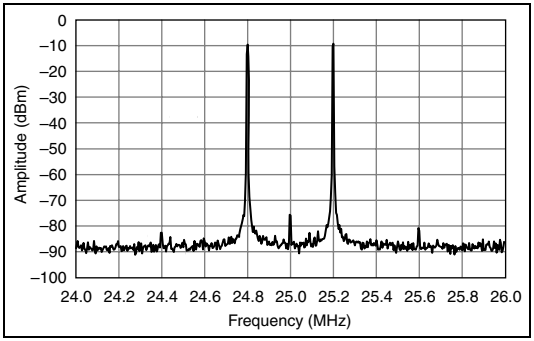


**Figure 10.** Analog Output Two-Tone IMD

**Note** Phase noise skirts and noise floor in Figure 10 are a limitation of the spectrum analyzer used for measurement.

# Digital Upconverter

Number of channels.....1 per DAC

Modulation bandwidth

Using NI-5640R driver .....Up to 20 MHz

Using LabVIEW FPGA .....Up to 40 MHz

Interpolation .....4× to 252×

## System Level Performance

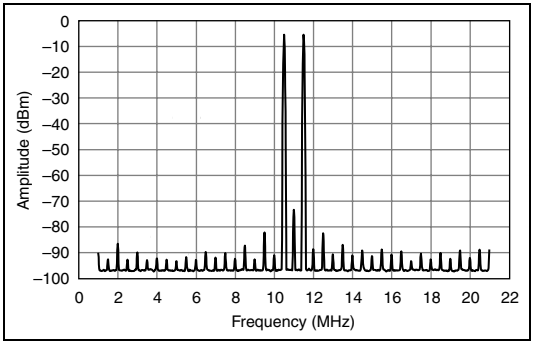


**Figure 11.** System-level Two-Tone IMD, Center Frequency = 11 MHz

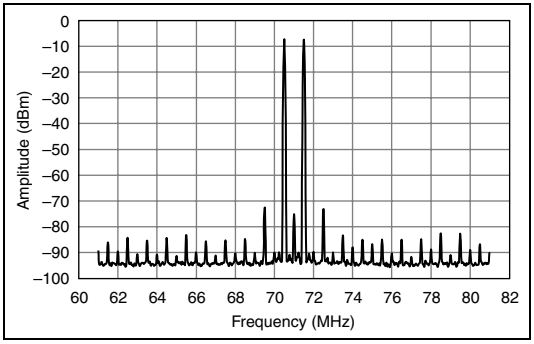


**Figure 12.** System-Level Two-Tone IMD, Center Frequency = 71 MHz

**Note** Figures 11 and 12 depict analog output signals routed to analog input terminals at various center frequencies.

## System Level Modulation Quality

Analog output connected to analog input

Conditions ..... QAM 256, Carrier = 25 MHz, Symbol Rate = 12.5 MS/s, Filter alpha = 0.5, raised cosine filter

Modulation Error Ratio..... >43 dB typical

Error Vector Magnitude..... <0.4% typical

## Timebase System

Timebase options

Using NI-5640R driver ..... Internal, External reference clock input (CLK IN)

Using LabVIEW FPGA ..... Internal, External (CLK IN), External reference clock input (CLK IN)

### Internal

Timebase frequency ..... 200 MHz with division by *N*, where *N* = 1, 2, 4, 8, or 16

**Note** ADC is clocked at 100 MHz max (200 MHz ÷ 2). ADC data output is further decimated by the DDC. DAC is clocked at 200 MHz maximum. DAC data is interpolated in the digital upconverter.

Timebase frequency accuracy ..... ±25 ppm

### External

External sample clock sources ..... CLK IN (SMB connector)

External sample clock range ..... 30 to 200 MHz

**Note** Set programmable clock divider (*N* = 1, 2, 4, 8, or 16) appropriately to ensure ADC sample rate ≤100 MS/s, and DAC update rate ≤ 200 MS/s.

External reference clock sources

Using NI-5640R driver ..... CLK IN (SMB connector)

Using LabVIEW FPGA ..... CLK IN (SMB connector), RTSI

External reference clock range ..... 1 to 100 MHz in 1 MHz increments, ± 100 ppm (RTSI limited to 20 MHz)

PLL lock time ..... < 250 ms

External clock input amplitude

Sine wave ..... 0.63 to 2.8 $V_{pk-pk}$ (0 to 13 dBm)

Square wave ..... 0.25 to 2.8 $V_{pk-pk}$

External clock input impedance ..... 50 Ω nominal, AC-coupled

## Trigger System

Modes ..... Digital input, software

Sources

Using NI-5640R driver ..... TRIG, software

Using LabVIEW FPGA ..... TRIG, RTSI <0..6>, software

Slope

Using NI-5640R driver ..... Rising

Using LabVIEW FPGA ..... Rising or falling

### External Trigger Channel (TRIG)

Impedance ..... 10 kΩ nominal, DC-coupled

Range ..... 0 to 5 V, TTL-compatible

Overvoltage protection ..... –3.5 to + 8 V continuous

## Digital I/O Connector (AUX I/O)

Number of digital lines ..... 6

I/O direction ..... Pin-configurable

Input voltage range ..... 0 to 5 V, TTL-compatible

Overvoltage protection ..... –0.5 to +5.5 V

Output type ..... 3.3 V CMOS

Output current ..... ±24 mA

## FPGA

Model ..... Xilinx Virtex-II Pro P30 (XC2VP30)

Logic cells ..... 30,816 (~ 3 million system gates)

Multipliers (18x18) ..... 136

Block RAM ..... 2,448 Kbits

## Power Requirements

Typical

| +3.3 VDC | +5 VDC | +12 VDC | Total Power |
|---|---|---|---|
| 1.8 to 3.5 A | 2.3 A | 200 mA | 20 to 25.5 W, depending on FPGA configuration |

## Calibration

Self-calibration parameters.....Analog input gain, Analog output gain, VCXO

External calibration interval .....2 years

## Physical Dimensions

NI PCI-5640R module.....35.5 × 2.0 × 11.3 cm (13.4 × 0.8 × 4.4 in.)

Weight .....263 g (9.2 oz)

## Environment

Maximum altitude .....2,000 m (at 25 °C ambient temperature)

Pollution Degree.....2

**Note** The NI PCI-5640R is intended for indoor use only.

### Operating Environment

Ambient temperature range .....0 to 40 ºC (Tested in accordance with IEC 60068-2-1 and IEC 60068-2-2.)

Relative humidity range .....10 to 90%, noncondensing (Tested in accordance with IEC 60068-2-56.)

### Storage Environment

Ambient temperature range .....–40 to 70 ºC (Tested in accordance with IEC 60068-2-1 and IEC 60068-2-2.)

Relative humidity range .....5 to 95%, noncondensing (Tested in accordance with IEC 60068-2-56.)

## Safety

This product is designed to meet the requirements of the following standards of safety for electrical equipment for measurement, control, and laboratory use:

- IEC 61010-1, EN 61010-1
- UL 61010-1
- CAN/CSA-C22.2 No. 61010-1

**Note** For UL and other safety certifications, refer to the product label, or visit `ni.com/certification`, search by model number or product line, and click the appropriate link in the Certification column.

## Electromagnetic Compatibility

Emissions ..... EN 55011 Class A at 10 m. FCC Part 15A above 1 GHz

Immunity..... EN 61326:1997 + A2:2001, Table 1

CE, C-Tick, and FCC Part 15 (Class A) Compliant

**Note** For EMC compliance, operate this device with shielded cabling.

## CE Compliance

This product meets the essential requirements of applicable European Directives, as amended for CE marking, as follows:

Low-Voltage Directive (safety)…….....73/23/EEC

Electromagnetic Compatibility Directive (EMC) ..... 89/336/EEC

**Note** Refer to the Declaration of Conformity (DoC) for this product for any additional regulatory compliance information. To obtain the DoC for this product, visit `ni.com/certification`, search by model number or product line, and click the appropriate link in the Certification column.

## Waste Electrical and Electronic Equipment (WEEE)

**EU Customers** At the end of their life cycle, all products must be sent to a WEEE recycling center. For more information about WEEE recycling centers and National Instruments WEEE initiatives, visit `ni.com/environment/weee.htm`.

371620C Dec07