AT-AO-6/10
User Manual

Expansion Board for the PC AT/EISA

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About This Manual

This manual describes the mechanical and electrical aspects of the AT-AO-6/10 board and contains information concerning its operation and programming. The AT-AO-6/10 is a high-performance, analog output and digital I/O board for the IBM PC AT and compatibles and EISA personal computers (PCs). The AT-AO-6/10 refers to two versions of the board: the six-digital-to-analog converter (DAC) AT-AO-6 and the ten-DAC AT-AO-10. It contains six/ten 12-bit DACs with both voltage and current outputs, and eight lines of transistor-transistor logic (TTL)-compatible digital I/O.

Organization of This Manual

The *AT-AO-6/10 User Manual* is organized as follows:

- Chapter 1, *Introduction*, describes the AT-AO-6/10; lists the contents of your AT-AO-6/10 kit, the optional software, and optional equipment; and explains how to unpack the AT-AO-6/10 kit.
- Chapter 2, *Configuration and Installation*, describes the AT-AO-6/10 jumper configuration, installation of the AT-AO-6/10 in the PC, signal connections to the AT-AO-6/10, and cable wiring.
- Chapter 3, *Theory of Operation*, contains a functional overview of the AT-AO-6/10 and explains the operation of each functional unit making up the AT-AO-6/10.
- Chapter 4, *Programming*, describes in detail the address and function of each of the AT-AO-6/10 registers. This chapter also includes important information about programming the AT-AO-6/10.
- Chapter 5, *Calibration Procedures*, discusses the calibration procedures for the AT-AO-6/10 analog output circuitry.
- Appendix A, *Specifications*, lists the specifications for the AT-AO-6/10.
- Appendix B, *I/O Connector*, shows the pinout and signal names for the AT-AO-6/10 50-pin I/O connector, including a description of each connection.
- Appendix C, *MSM82C53 Data Sheet*, contains the *MSM82C53 Programmable Interval Timer* (Oki Semiconductor) data sheet. This counter/timer is used on the AT-AO-6/10.
- Appendix D, *Customer Communication*, contains forms for you to complete to facilitate communication with National Instruments concerning our products.
- The *Index* alphabetically lists topics covered in this manual, including the page where the topic can be found.

Conventions Used in This Manual

The following conventions are used in this manual:

italic	Italic text denotes emphasis, a cross reference, or an introduction to a key concept.
NI-DAQ	NI-DAQ is used throughout this manual to refer to the NI-DAQ software for DOS/Windows/LabWindows unless otherwise noted.
PC	PC refers to the IBM PC AT and compatibles, and to EISA personal computers.
AT-AO-6/10	AT-AO-6/10 refers to the AT-AO-6 and the AT-AO-10 boards.

Related Documentation

The following document contains information that you may find helpful as you read this manual:

- *IBM Personal Computer AT Technical Reference* manual

You may also want to consult the following Oki Semiconductor manual if you plan to program the MSM82C53 Counter/Timer used on the AT-AO-6/10:

- *Oki 82C53 Programmable Interval Timer* technical manual

Customer Communication

National Instruments want to receive your comments on our products and manuals. We are interested in the applications you develop with our products, and we want to help if you have problems with them. To make it easy for you to contact us, this manual contains comment and configuration forms for you to complete. These forms are in Appendix D, *Customer Communication*, at the end of this manual.

Chapter 1
Introduction

This chapter describes the AT-AO-6/10; lists the contents of your AT-AO-6/10 kit, the optional software, and optional equipment; and explains how to unpack the AT-AO-6/10 kit.

The AT-AO-6/10 is a high-performance analog output and digital I/O board for the PC. There are two versions of the AT-AO-6/10: a version with six analog output channels and a version with ten analog output channels. In this manual, the descriptions of analog output Channels 6 through 9 apply to the AT-AO-10 only. The AT-AO-6/10 has six/ten double-buffered, multiplying, 12-bit DACs; unipolar and bipolar voltage output; 4 to 20 mA current output; an onboard DAC reference voltage of 10 V; internal timer and external signal update capability for waveform generation; an onboard 1,024-word FIFO buffer; transfer rates up to 200 ksamples/sec per channel; onboard analog output auto calibration circuitry; eight digital I/O lines able to sink up to 24 mA of current; timer-generated and externally generated interrupts; a high-performance RTSI bus interface; analog output auto-initialization at startup; and full PC I/O channel DMA capability with analog output.

The AT-AO-6/10 is designed for applications such as automation of machine and process control, instrumentation, and electronic test signal generation. The analog voltage outputs can be used for functions such as 12-bit resolution voltage sourcing, analog function generation, and control signal output. The 4 to 20 mA current outputs can be used in industrial control loops or any other application that benefits from the inherent noise immunity of two-wire current loop communication. The eight TTL-compatible digital I/O lines can be used for machine and process control, intermachine communication, and relay switching control.

The AT-AO-6/10 is interfaced to the National Instruments RTSI bus. With this bus, National Instruments AT Series boards can send timing signals to each other. The AT-AO-6/10 can send signals from the onboard counter/timer to another board, or another board can send control signals to the AT-AO-6/10.

Detailed specifications for the AT-AO-6/10 are listed in Appendix A, *Specifications*.

What Your Kit Should Contain

Each version of the AT-AO-6/10 board has a different part number and kit part number, listed as follows.

Kit Name	Kit Part Number	Kit Component	Board Part Number
AT-AO-6	776541-01	AT-AO-6 board	181435-06
AT-AO-10	776542-02	AT-AO-10 board	181435-10

The board part number is printed on your board along the top edge on the component side. You can identify which version of the AT-AO-6/10 board you have by looking up the part number in the preceding table.

In addition to the board, each version of the AT-AO-6/10 kit contains the following components.

Kit Component	Part Number
AT-AO-6/10 User Manual	320379-01
NI-DAQ software for DOS/Windows/LabWindows, with manuals	776250-01
NI-DAQ Software Reference Manual for DOS/Windows/LabWindows	320498-01
NI-DAQ Function Reference Manual for DOS/Windows/LabWindows	320499-01

If your kit is missing any of the components or if you received the wrong version, contact National Instruments.

Your AT-AO-6/10 is shipped with the NI-DAQ software for DOS/Windows/LabWindows. NI-DAQ has a library of functions that can be called from your application programming environment. These functions include routines for analog input (A/D conversion), buffered data acquisition (high-speed A/D conversion), analog output (D/A conversion), waveform generation, digital I/O, counter/timer, SCXI, RTSI, and self-calibration. NI-DAQ maintains a consistent software interface among its different versions so you can switch between platforms with minimal modifications to your code. NI-DAQ comes with language interfaces for Professional BASIC, Turbo Pascal, Turbo C, Turbo C++, Borland C++, and Microsoft C for DOS; and Visual Basic, Turbo Pascal, Microsoft C with SDK, and Borland C++ for Windows. NI-DAQ software is on high-density 5.25 in. and 3.5 in. diskettes.

Optional Software

This manual contains complete instructions for directly programming the AT-AO-6/10. Normally, however, you should not need to read the low-level programming details in the user manual because the NI-DAQ software package for controlling the AT-AO-6/10 is included with the board. Using NI-DAQ is quicker and easier than and as flexible as using the low-level programming described in Chapter 4, *Programming*.

You can use the AT-AO-6/10 with LabVIEW for Windows or LabWindows for DOS. LabVIEW and LabWindows are innovative program development software packages for data acquisition and control applications. LabVIEW uses graphical programming, whereas LabWindows enhances Microsoft C and QuickBASIC. Both packages include extensive libraries for data acquisition, instrument control, data analysis, and graphical data presentation.

Part numbers for these software packages are listed in the following table.

Software	Part Number
LabVIEW for Windows	776670-01
LabWindows for DOS	
Standard package	776473-01
Advanced Analysis Library	776474-01
Standard package with the Advanced Analysis Library	776475-01

Optional Equipment

Equipment	Part Number
CB-50 I/O connector block (50 screw terminals)	
with 0.5-m type NB1 cable	776164-01
with 1.0-m type NB1 cable	776164-02
AT Series RTSI bus cables for	
2 boards	776249-02
3 boards	776249-03
4 boards	776249-04
5 boards	776249-05

Unpacking

Your AT-AO-6/10 board is shipped packaged in an antistatic package to prevent electrostatic damage to the board. Several components on the board can be damaged by electrostatic discharge. To avoid such damage in handling the board, take the following precautions:

- Touch the antistatic package to a metal part of your PC chassis before removing the board from the pacakge.
- Remove the board from the package and inspect the board for loose components or any other sign of damage. Notify National Instruments if the board appears damaged in any way. *Do not* install a damaged board into your computer.

Chapter 2
Configuration and Installation

This chapter describes the AT-AO-6/10 jumper configuration, installation of the AT-AO-6/10 in the PC, signal connections to the AT-AO-6/10, and cable wiring.

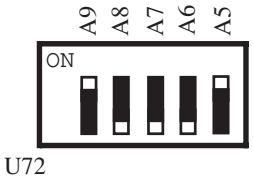
Board Configuration

The AT-AO-6/10 contains 24 jumpers (only 16 are used on the AT-AO-6 version) and one DIP switch. Jumpers W22, W23, and W24 on the AT-AO-6/10 select the DMA channel and the interrupt level. Jumpers W1 through W13 on the AT-AO-6 and Jumpers W1 through W20 on the AT-AO-10 configure the analog output circuitry. Jumper W21 is used for initial calibration functions and should not be changed, so it is removed from the board prior to shipping. The DIP switch is used to set the base I/O address. The jumpers and DIP switch are shown in the parts locator diagram in Figure 2-1.

AT Bus Interface

The AT-AO-6/10 is configured at the factory to a base I/O address of 1C0 hex, to use DMA Channel 5, and to use interrupt levels 11 and 12. These settings (shown in Table 2-1) are suitable for most systems. However, if your system has other hardware at this base I/O address, DMA channel, or interrupt level, you need to change these factory settings on the AT-AO-6/10 (as described in the following pages) or on the other hardware.

Table 2-1. AT Bus Interface Factory Settings

Base I/O Address	Hex 1C0 (factory setting)	 (The white portion indicates the position of the raised part of the slide switch.)
DMA Channel	DMA Channel 5 (factory setting)	**W22:** DRQ5, DACK5 **W24:** no jumpers
Interrupt Level	Group 1 interrupt level 11 selected Group 2 interrupt level 12 selected (factory setting)	**W23:** Row 11 **W23:** Row 12

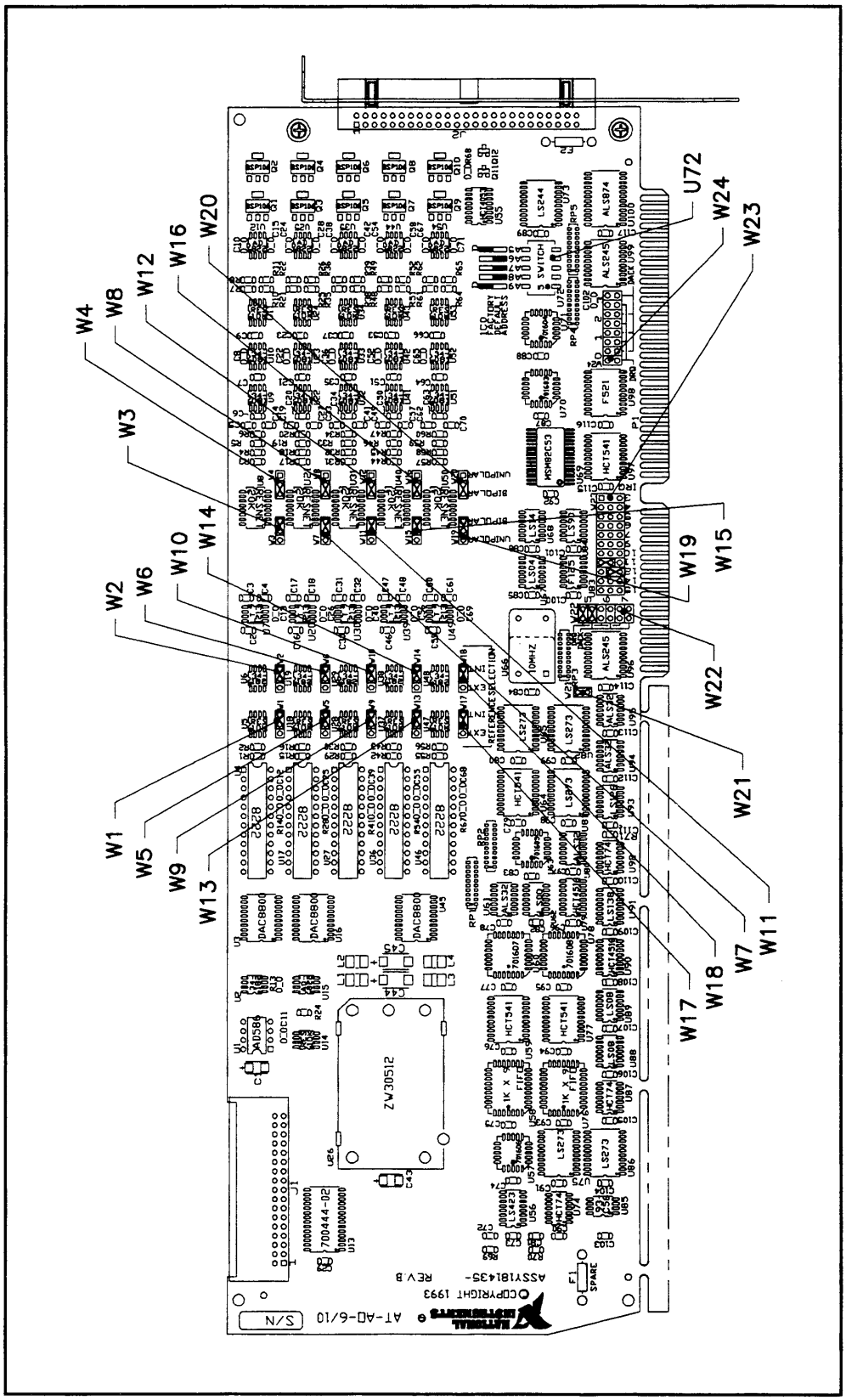


Figure 2-1. AT-AO-6/10 Parts Locator Diagram

Base I/O Address Selection

The base I/O address for the AT-AO-6/10 is determined by the switches at position U72 (see Figure 2-1). The switches are set at the factory for the base I/O address 1C0 hex. This factory setting is used by National Instruments software packages as the default base I/O address value for the AT-AO-6/10. The AT-AO-6/10 uses the base I/O address space 1C0 hex through 1DF hex with the factory setting.

Note: Verify that this space is not already used by other equipment installed in your computer. If any equipment in your computer uses this base I/O address space, change the base I/O address of the AT-AO-6/10 or of the other device. If you change the AT-AO-6/10 base I/O address, make a corresponding change to any software packages you use with the AT-AO-6/10. Table 2-2 lists the default settings of other National Instruments products for the PC. For more information about the I/O address of your PC, refer to the technical reference manual for your computer.

Table 2-2. Default Settings of National Instruments Products for the PC

Board	DMA Channel	Interrupt Level	Base I/O Address
AT-A2150	None*	None*	120 hex
AT-AO-6/10	Channel 5	Line 11, 12	1C0 hex
AT-DIO-32F	Channels 5, 6	Lines 11, 12	240 hex
AT-DSP2200	None*	None*	120 hex
AT-GPIB	Channel 5	Line 11	2C0 hex
AT-MIO-16	Channels 6, 7	Line 10	220 hex
AT-MIO-16D	Channels 6, 7	Line 10	220 hex
AT-MIO-16F-5	Channels 6, 7	Line 10	220 hex
AT-MIO-16X	None*	None*	220 hex
AT-MIO-64F-5	None*	None*	220 hex
GPIB-PCII	Channel 1	Line 7	2B8 hex
GPIB-PCIIA	Channel 1	Line 7	02E1 hex
GPIB-PCIII	Channel 1	Line 7	280 hex
Lab-PC	Channel 3	Line 5	260 hex
Lab-PC+	Channel 3	Line 5	260 hex
PC-DIO-24	None	Line 5	210 hex
PC-DIO-96	None	Line 5	180 hex
PC-LPM-16	None	Line 5	260 hex
PC-TIO-10	None	Line 5	1A0 hex

* These settings are software configurable and are disabled at startup time.

The base address DIP switch is arranged so that you select a logical 1 or *true* state from the associated address selection bit by pushing the toggle switch down, or toward the bottom of the board. Alternately, you select a logical 0 or *false* state by pushing the toggle switch up, or toward the top of the board. In Figure 2-2B, for example, A9 is up (false), A8 through A6 are down (true), and A5 is up (false). This represents a hex value of IC0. The AT-AO-6/10 decodes the five least significant bits of the address (A4 through A0) to select the appropriate AT-AO-6/10 register. Table 2-3 lists the possible switch settings, the corresponding base I/O address, and the base I/O address space used for that setting.

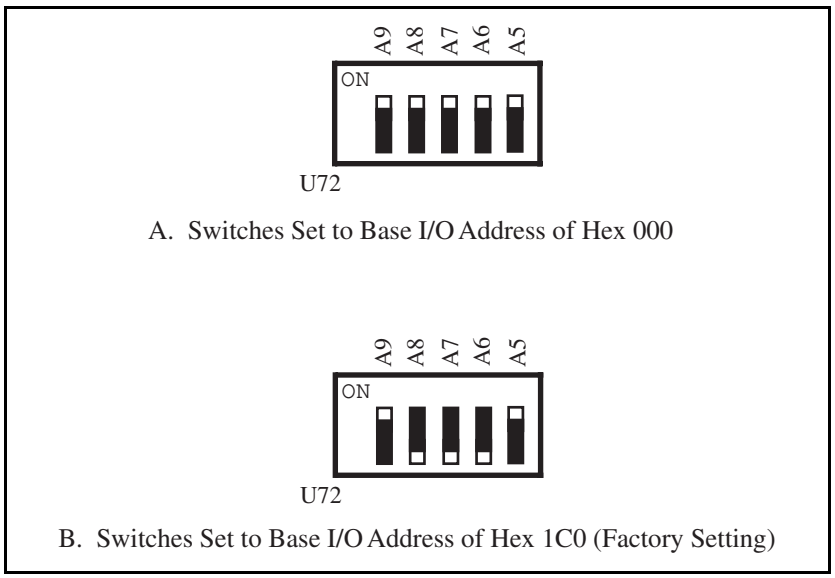


Figure 2-2. Example Base I/O Address Switch Settings

Table 2-3. Switch Settings with Corresponding Base I/O Address and Base I/O Address Space

Switch Setting A9	A8	A7	A6	A5	Base I/O Address (hex)	Base I/O Address Space Used (hex)
0	0	0	0	0	000	000 - 01F
0	0	0	0	1	020	020 - 03F
0	0	0	1	0	040	040 - 05F
0	0	0	1	1	060	060 - 07F
0	0	1	0	0	080	080 - 09F
0	0	1	0	1	0A0	0A0 - 0BF
0	0	1	1	0	0C0	0C0 - 0DF
0	0	1	1	1	0E0	0E0 - 0FF
0	1	0	0	0	100	100 - 11F
0	1	0	0	1	120	120 - 13F
0	1	0	1	0	140	140 - 15F
0	1	0	1	1	160	160 - 17F
0	1	1	0	0	180	180 - 19F
0	1	1	0	1	1A0	1A0 - 1BF
0	1	1	1	0	1C0	1C0 - 1DF
0	1	1	1	1	1E0	1E0 - 1FF
1	0	0	0	0	200	200 - 21F
1	0	0	0	1	220	220 - 23F
1	0	0	1	0	240	240 - 25F
1	0	0	1	1	260	260 - 27F
1	0	1	0	0	280	280 - 29F
1	0	1	0	1	2A0	2A0 - 2BF
1	0	1	1	0	2C0	2C0 - 2DF
1	0	1	1	1	2E0	2E0 - 2FF
1	1	0	0	0	300	300 - 31F
1	1	0	0	1	320	320 - 33F
1	1	0	1	0	340	340 - 35F
1	1	0	1	1	360	360 - 37F
1	1	1	0	0	380	380 - 39F
1	1	1	0	1	3A0	3A0 - 3BF
1	1	1	1	0	3C0	3C0 - 3DF
1	1	1	1	1	3E0	3E0 - 3FF

Note: Base I/O address values 000 through 0FF hex are reserved for system use. Base I/O address values 100 through 3FF hex are available on the I/O channel.

DMA Channel Selection

The DMA channels used by the AT-AO-6/10 are selected by jumpers W22 and W24 (see Figure 2-1). The AT-AO-6/10 is set at the factory to use DMA Channel 5. This channel is the default DMA channel used by the AT-AO-6/10 software handler. Verify that this DMA channel is not also used by equipment already installed in your computer. If any device uses DMA Channel 5, change the DMA channel used by either the AT-AO-6/10 or the other device. (Unless the appropriate DMA modes have been enabled on the AT-AO-6/10 through software, the DMA channel is by default in the high-impedance state at startup.) The DMA channels supported by the AT-AO-6/10 hardware are Channel 0 through Channel 3 and Channel 5 through Channel 7. If the AT-AO-6/10 is used in an AT-type computer, only DMA Channels 5 through 7 should be used because these channels are the only 16-bit channels. If the board is used in an EISA computer, all of the channels are 16-bit and can be used. The AT-AO-6/10 *does not* use and *cannot* be configured to use the 8-bit DMA channels on the PC I/O channel.

Each DMA channel consists of two signal lines, as shown in Table 2-4.

Table 2-4. DMA Channels for the AT-AO-6/10

DMA Channel	DMA Acknowledge	DMA Request
0 (EISA bus)	DACK0	DRQ0
1 (EISA bus)	DACK1	DRQ1
2 (EISA bus)	DACK2	DRQ2
3 (EISA bus)	DACK3	DRQ3
5 (EISA and AT bus)	DACK5	DRQ5
6 (EISA and AT bus)	DACK6	DRQ6
7 (EISA and AT bus)	DACK7	DRQ7

Two jumpers must be installed to select a single DMA channel. The DMA acknowledge and DMA request lines selected must have the same number suffix for proper operation. Figure 2-3 shows the jumper positions for selecting DMA Channel 5.

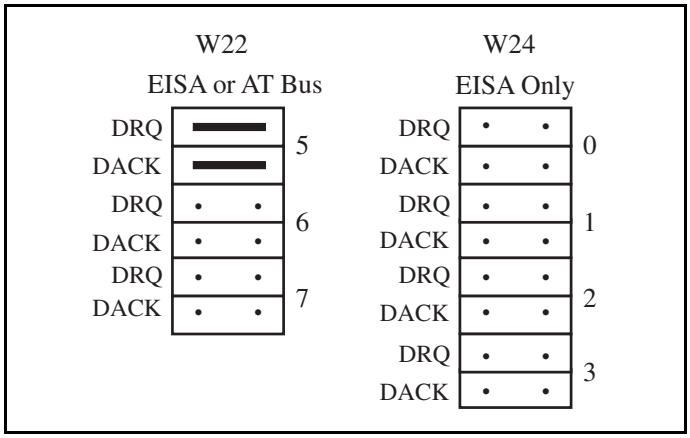


Figure 2-3. DMA Jumper Settings for DMA Channel 5 (Factory Setting)

The DMA channel circuitry can be programmed for high-impedance state.

Interrupt Selection

The AT-AO-6/10 board can connect to any two of the eleven interrupt lines of the PC I/O channel. Each interrupt line is selected by a jumper with the triple rows of pins located above the I/O slot edge connector on the AT-AO-6/10 (refer to Figure 2-1). To use the interrupt capability of the AT-AO-6/10, select an interrupt line and place the jumper in the appropriate position to enable that particular interrupt line. The jumper on the upper two rows of interrupt line 11 selects the interrupt level for Group 1 of the analog output channel, and the jumper on the lower two rows of interrupt line 12 selects the interrupt level for Group 2 of the analog output channel.

The AT-AO-6/10 can share interrupt lines with other devices. Unless the appropriate interrupt modes have been enabled on the AT-AO-6/10 through software, the interrupt line is by default in the high-impedance state at startup. The interrupt lines supported by the AT-AO-6/10 hardware are IRQ3, IRQ4, IRQ5, IRQ6, IRQ7, IRQ9, IRQ10, IRQ11, IRQ12, IRQ14, and IRQ15.

Note: *Do not* use interrupt line 6 or 14. Interrupt line 6 is used by the diskette drive controller, and interrupt line 14 is used by the hard disk controller on most PCs.

Once you have selected an interrupt level, place the interrupt jumper on the appropriate pins to enable the interrupt line.

The interrupt jumper set is W23. The default interrupt lines are IRQ11 for Group 1 and IRQ12 for Group 2. These interrupt lines are selected by placing one jumper on the upper pins in row 11 and the other jumper on the lower pins in row 12. Figure 2-4 shows the default interrupt jumper settings IRQ11 and IRQ12. To change to other lines, remove the jumpers from IRQ11 and IRQ12 and place them on the new pins.

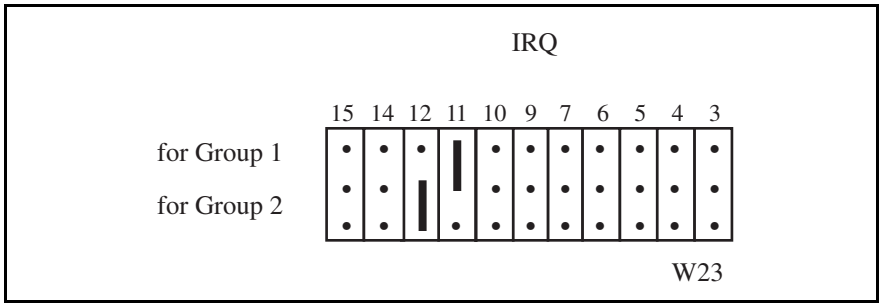


Figure 2-4. Interrupt Jumper Setting IRQ11 and IRQ12 (Factory Setting)

Interrupts for both groups can be enabled or disabled via control bits on the AT-AO-6/10. These control bits are described in the programming configuration registers. See Chapter 4, *Programming*, for more information.

Analog Output Configuration

The AT-AO-6/10 is shipped from the factory with the following configuration–±10 V analog output range with internal reference selected.

You can select different analog output configurations by using the jumper settings shown in Table 2-5. Table 2-5 lists all the available analog output configuration jumpers and notes the factory settings. The following paragraphs describe each of the analog output configurations in detail.

Table 2-5. Analog Output Jumper Settings

Output Channel	Configuration	Jumper Settings
Channel 0	Reference: Internal (factory setting) External	W1: B-C W1: A-B
	Unipolar Bipolar (factory setting)	W3: A-B W3: B-C
Channel 1	Reference: Internal (factory setting) External	W2: B-C W2: A-B
	Unipolar Bipolar (factory setting)	W4: B-C W4: A-B
Channel 2	Reference: Internal (factory setting) External	W5: B-C W5: A-B
	Unipolar Bipolar (factory setting)	W7: A-B W7: B-C
Channel 3	Reference: Internal (factory setting) External	W6: B-C W6: A-B
	Unipolar Bipolar (factory setting)	W8: B-C W8: A-B
Channel 4	Reference: Internal (factory setting) External	W9: B-C W9: A-B
	Unipolar Bipolar (factory setting)	W11: A-B W11: B-C
Channel 5	Reference: Internal (factory setting) External	W10: B-C W10: A-B
	Unipolar Bipolar (factory setting)	W12: B-C W12: A-B

(continues)

Table 2-5. Analog Output Jumper Settings (continued)

Output Channel	Configuration	Jumper Settings
Channel 6	Reference: Internal (factory setting) External	W13: B-C W13: A-B
	Unipolar Bipolar (factory setting)	W15: A-B W15: B-C
Channel 7	Reference: Internal (factory setting) External	W14: B-C W14: A-B
	Unipolar Bipolar (factory setting)	W16: B-C W16: A-B
Channel 8	Reference: Internal (factory setting) External	W17: B-C W17: A-B
	Unipolar Bipolar (factory setting)	W19: A-B W19: B-C
Channel 9	Reference: Internal (factory setting) External	W18: B-C W18: A-B
	Unipolar Bipolar (factory setting)	W20: B-C W20: A-B

Internal and External Reference

Each DAC can be connected to the AT-AO-6/10 internal reference of 10 V or to the external reference signal connected to the EXTREFX pin on the I/O connector. This signal applied to EXTREFX must be between -10 V and +10 V. Each EXTREFX signal is shared by two DACs that are in the same chip; that is, DAC0 and DAC1 share EXTREF0, DAC2 and DAC3 share EXTREF2, etc. Both channels need not be configured the same way.

External Reference Selection

You select the external reference signal for each analog output channel by setting the following jumpers as shown in Table 2-6:

Table 2-6. External Reference Selection

Channel	Jumper	Setting	External Reference Configuration
Analog Output Channel 0	W1	A - B	
Analog Output Channel 1	W2	A - B	
Analog Output Channel 2	W5	A - B	
Analog Output Channel 3	W6	A - B	
Analog Output Channel 4	W9	A - B	
Analog Output Channel 5	W10	A - B	
Analog Output Channel 6	W13	A - B	
Analog Output Channel 7	W14	A - B	
Analog Output Channel 8	W17	A - B	
Analog Output Channel 9	W18	A - B	

Internal Reference Selection (Factory Setting)

You select the onboard 10 V reference for each analog output channel by setting the following jumpers as shown in Table 2-7.

Table 2-7. Internal Reference Selection

Channel	Jumper	Factory Setting	Internal Reference Configuration
Analog Output Channel 0	W1	B - C	
Analog Output Channel 1	W2	B - C	
Analog Output Channel 2	W5	B - C	
Analog Output Channel 3	W6	B - C	
Analog Output Channel 4	W9	B - C	
Analog Output Channel 5	W10	B - C	
Analog Output Channel 6	W13	B - C	
Analog Output Channel 7	W14	B - C	
Analog Output Channel 8	W17	B - C	
Analog Output Channel 9	W18	B - C	

Analog Output Polarity Selection

Each analog output channel can be configured for either unipolar or bipolar output. A unipolar configuration has a range of 0 to V_{ref} at the analog output. A bipolar configuration has a range of

$-V_{ref}$ to $+V_{ref}$ at the analog output. V_{ref} is the voltage reference used by the DACs in the analog output circuitry and can be either the 10 V onboard reference or an externally supplied reference between -10 V and +10 V. Each channel is configured independently; at the factory, all channels are configured for bipolar output.

Bipolar Output Selection (Factory Setting)

You select the bipolar output configuration for each analog output channel by setting the following jumpers as shown in Table 2-8.

Table 2-8. Bipolar Output Selection

Channel	Jumper	Factory Setting	Bipolar Output Configuration
Analog Output Channel 0	W3	B - C	
Analog Output Channel 1	W4	A - B	
Analog Output Channel 2	W7	B - C	
Analog Output Channel 3	W8	A - B	
Analog Output Channel 4	W11	B - C	
Analog Output Channel 5	W12	A - B	
Analog Output Channel 6	W15	B - C	
Analog Output Channel 7	W16	A - B	
Analog Output Channel 8	W19	B - C	
Analog Output Channel 9	W20	A - B	

Data can be written to the DAC in either straight binary mode or two's complement mode depending on certain configuration register bits. When you use bipolar configuration, you must select whether to write to the DAC in straight binary mode or two's complement mode. In straight binary mode, data values written to the analog output channel range from 0 to 4,095 decimal (0 to 0FFF hex). In two's complement mode, data values written to the analog output channel range from -2,048 to +2,047 decimal (F800 to 07FF hex).

Unipolar Output Selection

You select the unipolar output configuration for each analog output channel by setting the following jumpers as shown in Table 2-9.

Table 2-9. Unipolar Output Selection

Channel	Jumper	Setting	Unipolar Output Configuration
Analog Output Channel 0	W3	A - B	
Analog Output Channel 1	W4	B - C	
Analog Output Channel 2	W7	A - B	
Analog Output Channel 3	W8	B - C	
Analog Output Channel 4	W11	A - B	
Analog Output Channel 5	W12	B - C	
Analog Output Channel 6	W15	A - B	
Analog Output Channel 7	W16	B - C	
Analog Output Channel 8	W19	A - B	
Analog Output Channel 9	W20	B - C	

Notice that the straight binary format for data should be used when in unipolar output mode.

Hardware Installation

The AT-AO-6/10 can be installed in any available 16-bit expansion slot (AT Series) in your computer. The AT-AO-6/10 *does not* work if installed in an 8-bit expansion slot (PC Series). After you have made any necessary changes, verified, and recorded the switch and jumper settings (a form is included for this purpose in Appendix D, *Customer Communication*), you are ready to install the AT-AO-6/10. The following are general installation instructions, but consult the user manual or technical reference manual of your PC for specific instructions and warnings.

1. Turn off your computer.
2. Remove the top cover or access port to the I/O channel.
3. Remove the expansion slot cover on the back panel of the computer.
4. Insert the AT-AO-6/10 into a 16-bit slot. Do not force the board into place.
5. Screw the mounting bracket of the AT-AO-6/10 to the back panel rail of the computer.
6. Check the installation.
7. Replace the cover.

The AT-AO-6/10 board is installed and ready for operation.

Signal Connections

This section describes input and output signal connections to the AT-AO-6/10 board via the AT-AO-6/10 I/O connector, and includes specifications and connection instructions for the signals given on the AT-AO-6/10 I/O connector.

Warning: Connections that exceed any of the maximum ratings of input or output signals on the AT-AO-6/10 can result in damage to the AT-AO-6/10 board and to the PC. Maximum input ratings for each signal are given in this chapter under the discussion of that signal. National Instruments is not liable for any damages resulting from such signal connections.

Figure 2-5 shows the pin assignments for the AT-AO-6/10 I/O connector.

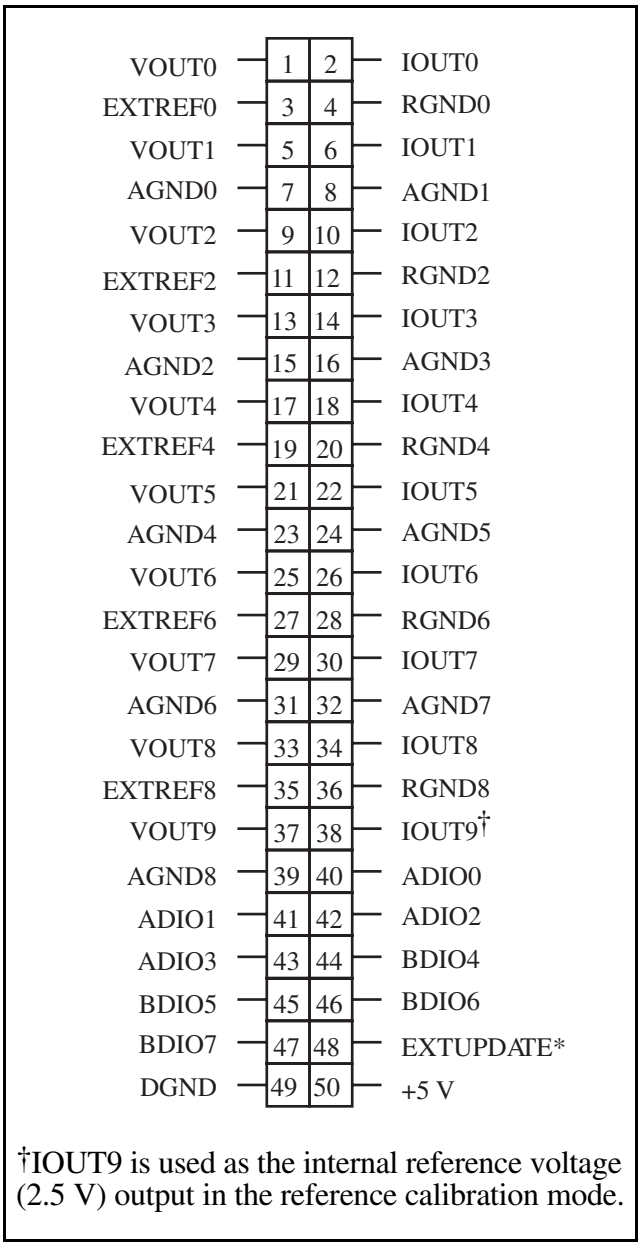


Figure 2-5. AT-AO-6/10 I/O Connector

Signal Connection Descriptions

Pin	Signal Name	Description
1, 5, 9, 13, 17, 21, 25, 29, 33, 37	VOUT0 through VOUT9	These pins are the analog voltage outputs of Channel 0 through Channel 9.

Pin	Signal Name	Description (continued)
2, 6, 10, 14, 18, 22, 26, 30, 34, 38	IOUT0 through IOUT9†	These pins are the analog current outputs of Channel 0 through Channel 9. The IOUT9 signal is programmable and can be either analog current output from Channel 9 or the 2.5 V onboard reference signal. In the reference calibration mode, this pin is used to monitor the internal 2.5 V_{ref}.
3, 11, 19, 27, 35	EXTREF0 through EXTREF8	These pins are the analog external reference inputs for Channel 0 through Channel 9. Each external reference input signal is shared by two channels. Channel 0 and Channel 1 share EXTREF0, Channel 2 and Channel 3 shares EXTREF2, etc.
4, 12, 20, 28, 36	RGND0 through RGND8	These pins are the analog external reference ground pins. Each of these five ground pins is the ground reference to the corresponding EXTREFX signal.
7, 8, 15, 16, 23, 24, 31, 32, 39	AGND0 through AGND8	These pins are the analog output ground pins for each channel. Channel 8 and Channel 9 share one ground pin, AGND8.
40, 41, 42, 43	ADIO0 through ADIO3	These pins are the digital I/O Port A signals.
44, 45, 46, 47	BDIO0 through BDIO3	These pins are the digital I/O Port B signals.
48	EXTUPDATE*	This pin is the external DAC Update. If selected, a high-to-low edge on EXTUPDATE* results in the selected outputs of DACs being updated with the value written to them.
49	DGND	This pin is the digital ground. This pin supplies the reference for the digital signals at the I/O connector as well as the +5 VDC supply.
50	+5 V	This pin is the +5 VDC source. This pin is fused for up to 1 A of +5 V supply.

The signals on the connector can be classified as analog output signals, digital I/O signals, digital power connections, or update timing signals. Signal connection guidelines for each of these groups are given in the following section.

Analog Output Signal Connections

Pins 1 through 39 of the I/O connector are analog output signal pins.

Pins 1, 5, 9, 13, 17, 21, 25, 29, 33 and 37 are the analog voltage output signal pins for analog output Channels 0 through 9, respectively. Pins 2, 6, 10, 14, 18, 22, 26, 30, 34 and 38 are the analog current output signal pins for Channels 0 through 9.

Pins 3, 11, 19, 27, and 35 are the external reference inputs for analog output channels. Each analog output channel must be configured individually for external reference selection so the signal applied at the external reference input is used by that channel. Analog output configuration instructions are included under the *Analog Output Configuration* section earlier in this chapter.

The following ranges and ratings apply to the EXTREFX input:

Useful input voltage range:	±10 V peak with respect to RGND
Absolute maximum ratings:	±25 V peak with respect to RGND

Pins 4, 12, 20, 28, and 36 are the ground reference points for the external reference signals.

Pins 7, 8, 15, 16, 23, 24, 31, 32, and 39 are the ground reference points for the analog output channels.

Figure 2-6 shows how to make analog voltage output connections and the external reference input connection to Channel 0 and Channel 1 as an example.

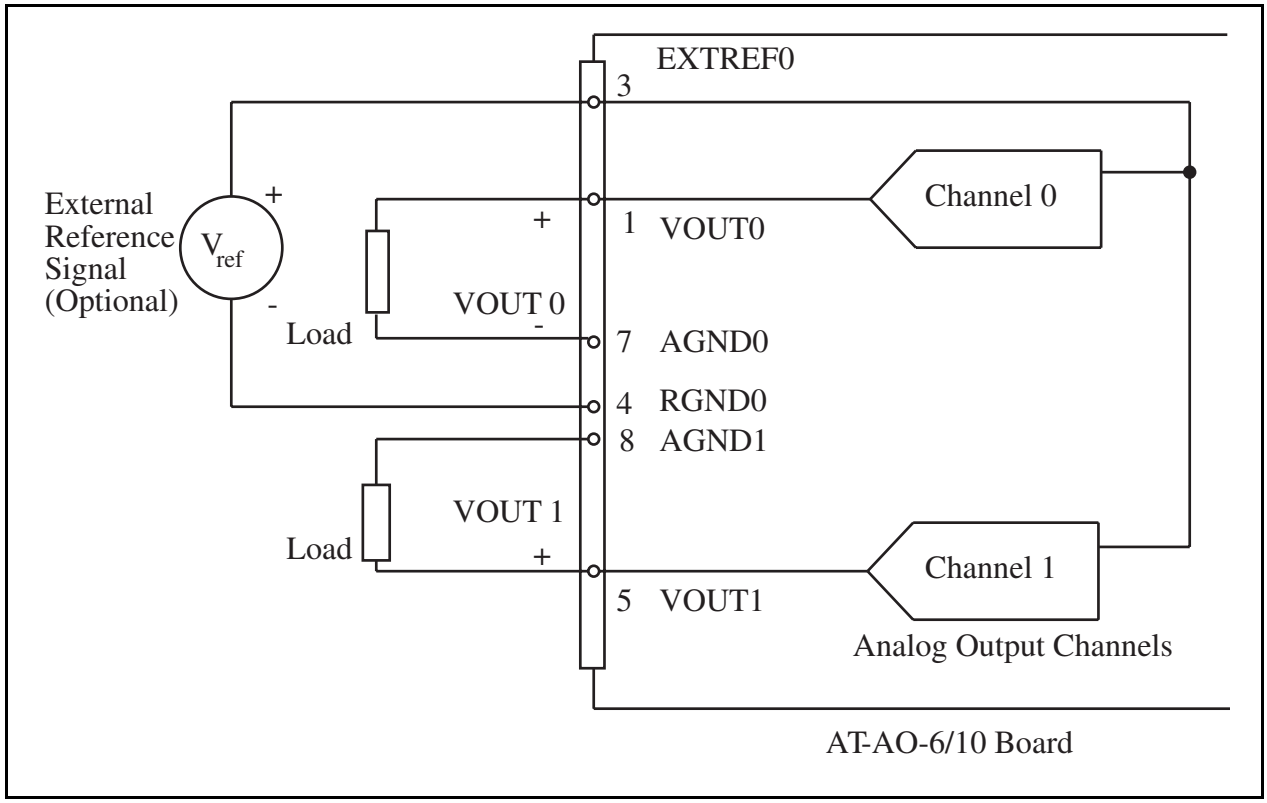


Figure 2-6. Analog Voltage Output Connections

An example of the analog current output connection is given in Chapter 3, *Theory of Operation*. The external voltage source is required to power the current loops.

The external reference signal can be either a DC or an AC signal. This reference signal is multiplied by the DAC code to generate the output voltage.

Digital I/O Signal Connections

Pins 40 through 47 of the I/O connector are digital I/O signal pins.

Pins 40, 41, 42, and 43 are connected to the digital lines ADIO<3..0> for digital I/O Port A. Pins 44, 45, 46, and 47 are connected to the digital lines BDIO<3..0> for digital I/O Port B. Pin 49 is the digital ground pin for both digital I/O ports. Ports A and B can be programmed individually to be inputs or outputs.

The following specifications and ratings apply to the digital I/O lines.

Absolute maximum voltage input rating	5.5 V with respect to DGND

Digital input specifications (referenced to DGND):

V_{IH} input logic high voltage	2 V minimum
V_{IL} input logic low voltage	0.8 V maximum
I_{IH} input current load, logic high input voltage	40 µA maximum
I_{IL} input current load, logic low input voltage	-120 µA maximum

Digital output specifications (referenced to DGND):

V_{OH} output logic high voltage	2.4 V minimum
V_{OL} output logic low voltage	0.5 V maximum
I_{OH} output source current, logic high	2.6 mA maximum
I_{OL} output sink current, logic low	24 mA maximum

With these specifications, each digital output line can drive 11 standard TTL loads and over 50 LS TTL loads.

Figure 2-7 shows signal connections for three typical digital I/O applications.

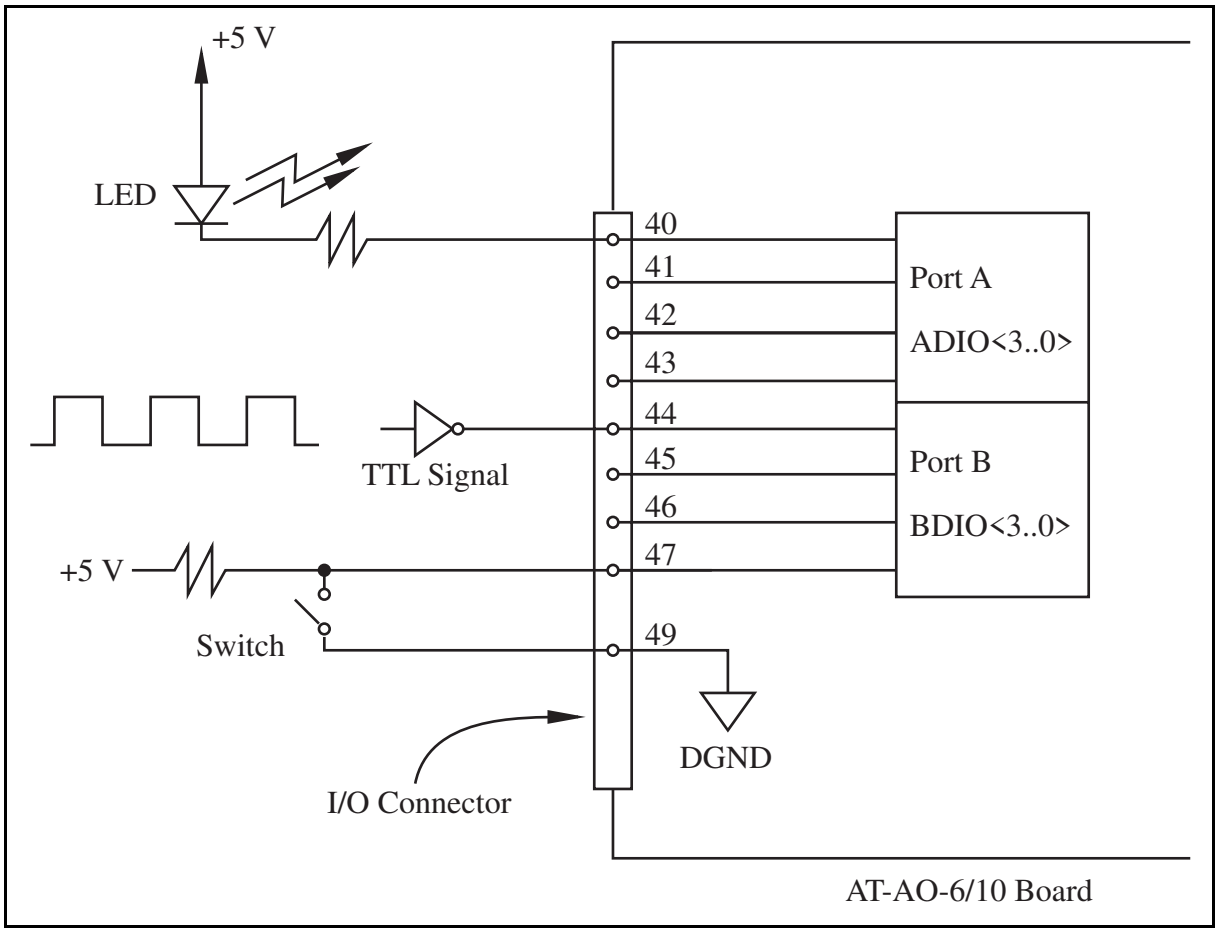


Figure 2-7. Digital I/O Connections

In Figure 2-7, Port A is configured for digital output, and Port B is configured for digital input. Digital input applications include receiving TTL signals and sensing external device states such as the state of the switch in Figure 2-7. Digital output applications include sending TTL signals and driving external devices such as the LED shown in Figure 2-7.

Power Connections

Pin 50 of the I/O connector provides +5 V from the PC power supply. This pin is referenced to DGND and can be used to power external digital circuitry.

Power Rating	1.0 A at +5 V ± 10%, fused

Warning: *Under no circumstances* should this +5 V power pin be connected directly to analog or digital ground or to any other voltage source on the AT-AO-6/10. Doing so can damage the AT-AO-6/10 and the PC. National Instruments is not liable for damage resulting from such a connection.

Update Timing Signal

The EXTUPDATE* signal on pin 48 is a TTL-compatible input signal for analog output channel updating. This signal line is pulled up to +5 V on the board, and is also connected to the RTSI switch. The external device can drive this line low. The high-to-low edge on this line triggers an internal active low pulse, EXTUPD*. The high-to-low edge of EXTUPD* initiates the update of the selected, double-buffered, analog output channels, and the rising edge of the EXTUPD* signal can generate a DataWriteEnable signal or an interrupt request to write new data to the selected output channels. Figure 2-8 shows the timing diagram of these signals.

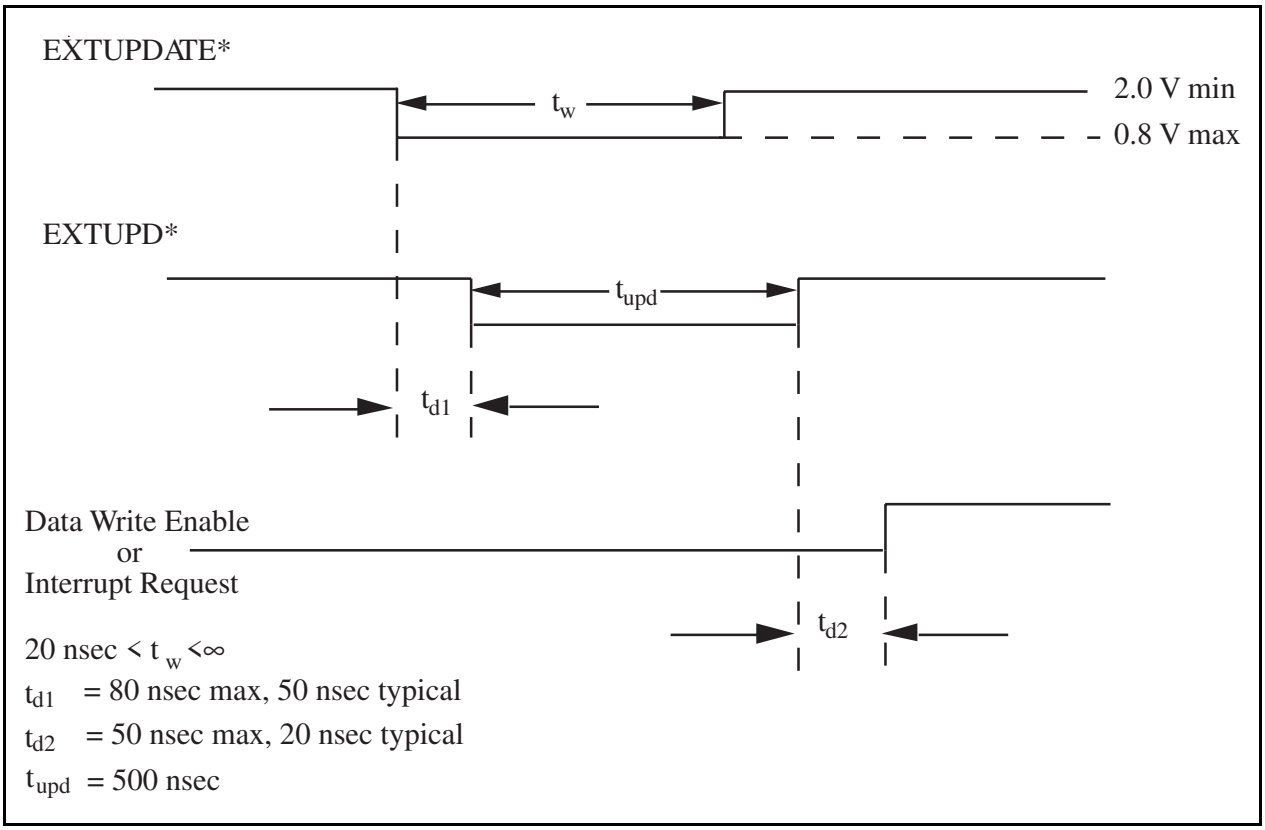


Figure 2-8. Update Timing

Field Wiring Considerations

Accuracy of signals generated by the AT-AO-6/10 can be seriously affected by environmental noise when signal wires are run to and from the AT-AO-6/10.

Noise pickup and crosstalk can be minimized and signal accuracy optimized if the following recommendations for analog signal connections are followed.

- Use individually shielded, twisted-pair connections for voltage output signals. In such cases, the voltage output and its corresponding analog ground signal wire are twisted together and the shield is connected to the analog ground at the AT-AO-6/10. The other end of the shield is left disconnected.

- Reference inputs should also be connected via shielded twisted-pair connection. The shield should be grounded at the signal source.
- Current outputs are relatively immune to line loss and noise pickup and should be used for signal transmission over long distances.
- All AT-AO-6/10 signal lines should be physically separated from high-current or high-voltage lines. These lines can induce currents into the AT-AO-6/10 signal lines if they are run in parallel paths at a close distance. Reduce the magnetic coupling by separating the lines by a reasonable distance if they run in parallel, or by running the lines at right angles to each other.
- Do not run AT-AO-6/10 signal lines through conduits that also contain power lines.
- Protect AT-AO-6/10 signal lines from magnetic fields caused by electric motors, welding equipment, breakers, or transformers by running the AT-AO-6/10 signal lines through special metal conduits if it is necessary to pass them through these areas.

Cabling Considerations

National Instruments has a cable termination accessory, the CB-50, for use with the AT-AO-6/10 board. This kit includes a terminated 50-conductor flat ribbon cable and a connector block. Signal I/O leads can be attached to screw terminals on the connector block and thereby connected to the AT-AO-6/10 I/O connector.

The CB-50 can be used for prototyping an application or in situations where AT-AO-6/10 interconnections are frequently changed. However, once a final field wiring scheme has been developed, you may want to develop your own cable.

The AT-AO-6/10 I/O connector is a 50-pin male ribbon-cable header. The manufacturer part numbers for this header are as follows:

Electronic Products Division/3M part nnmber 3596-5002
T&B/Ansley Corporation part number 609-5007

The mating connector for the AT-AO-6/10 is a 50-position ribbon socket connector, polarized, with strain relief. National Instruments uses a polarized (keyed) connector to prevent inadvertent misconnection to the AT-AO-6/10. Recommended manufacturer part numbers for this mating connector are as follows:

Electronic Products Division/3M part number 3425-7650
T&B/Ansley Corporation part number 609-5041CE

Recommended manufacturer part numbers for the standard ribbon cable (50-conductor, 28 AWG, stranded) that can be used with these connectors are:

Electronic Products Division/3M part number 3365/50
T&B/Ansley Corporation part number 171-50

Chapter 3
Theory of Operation

This chapter contains a functional overview of the AT-AO-6/10 and explains the operation of each functional unit making up the AT-AO-6/10.

Functional Overview

The block diagram in Figure 3-1 is a functional overview of the AT-AO-6/10 board.

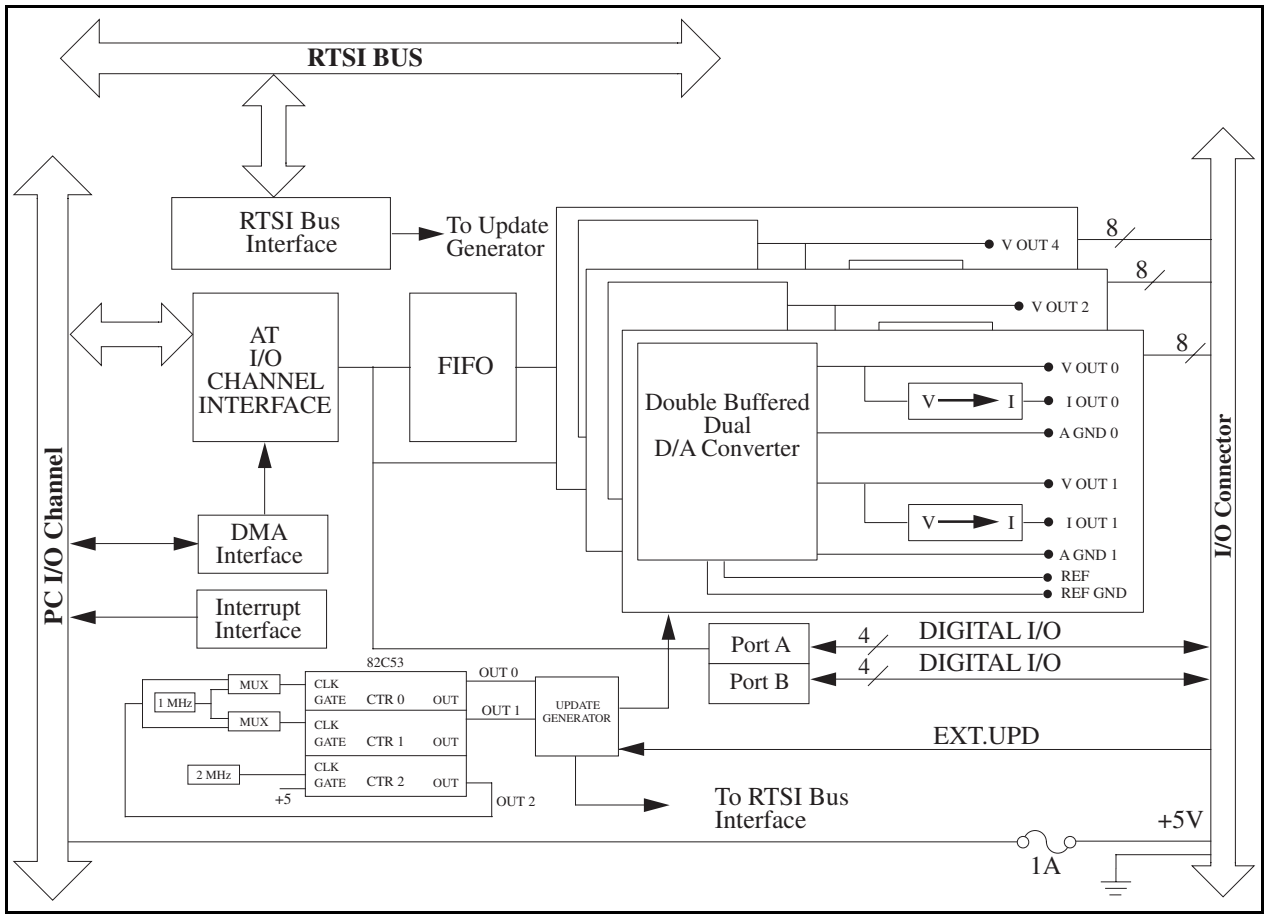


Figure 3-1. AT-AO-6/10 Block Diagram

The following are the major components making up the AT-AO-6/10 board:

- PC I/O channel interface circuitry
- Analog output circuitry
- Digital I/O circuitry
- RTSI bus interface circuitry

The internal data and control buses interconnect the components. The theory of operation of each of these components is explained in the remainder of this chapter.

PC I/O Channel Interface Circuitry

The AT-AO-6/10 board is a full-size 16-bit PC I/O channel adapter. The PC I/O channel consists of a 24-bit address bus, a 16-bit data bus, a DMA arbitration bus, interrupt lines, and several control and support signals. The components making up the AT-AO-6/10 PC I/O channel interface circuitry are shown in Figure 3-2.

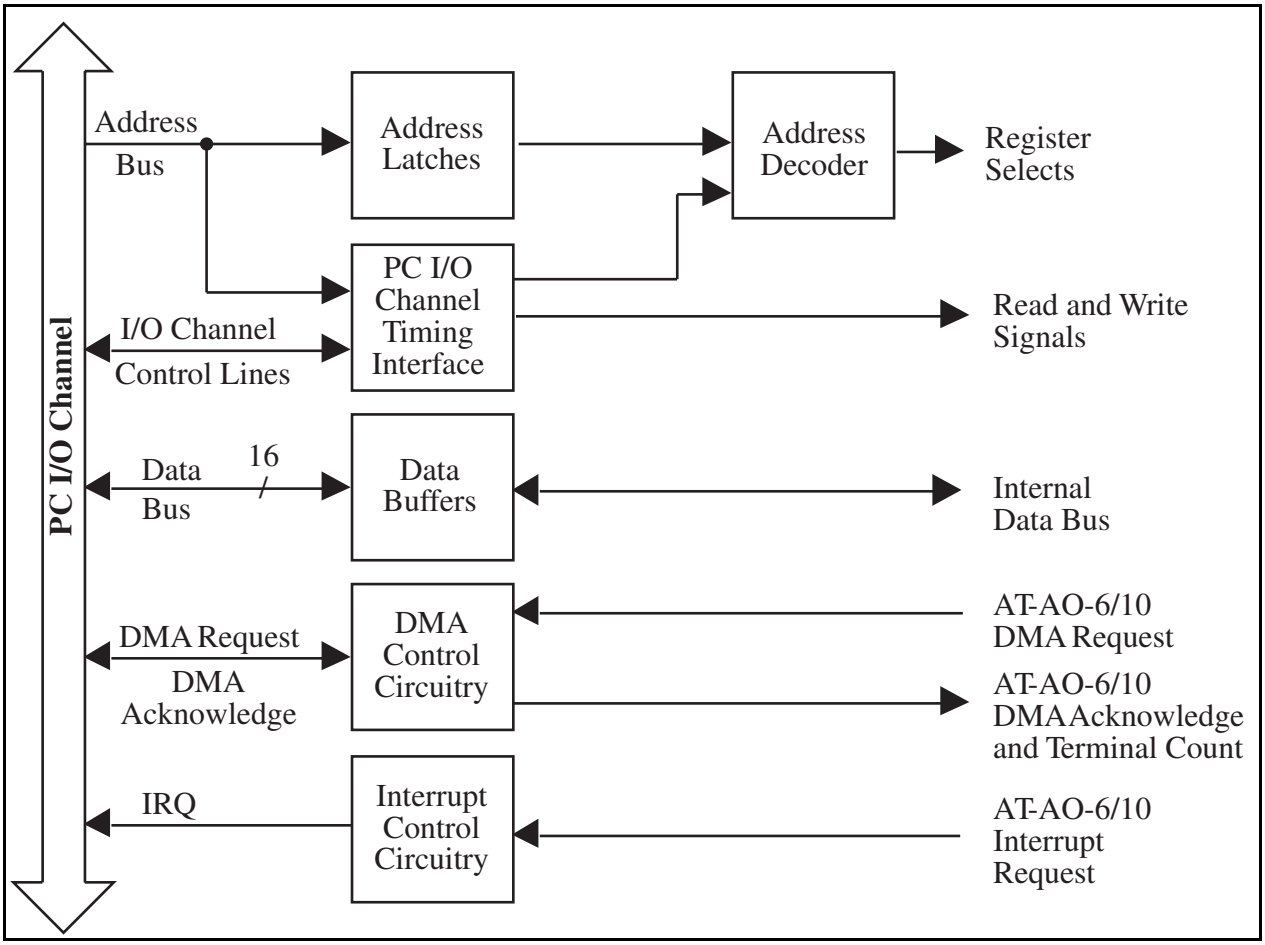


Figure 3-2. PC I/O Channel Interface Circuitry Block Diagram

The PC I/O channel interface circuitry consists of address latches, address decoder circuitry, data buffers, PC I/O channel interface timing signals, interrupt circuitry, and DMA arbitration circuitry. The PC I/O channel interface circuitry generates the signals necessary to control and monitor the operation of the AT-AO-6/10 multiple function circuitry.

The PC I/O channel has 24 address lines; the AT-AO-6/10 uses 10 of these lines to decode the board address. Therefore, the board address range is 000 to 3FF hex. SA5 through SA9 are used to generate the board enable signal. SA0 through SA4 are used to select onboard registers. These address lines are latched by the address latches at the beginning of an I/O transfer. The latched address lines send the same address to the address-decoding circuitry during the entire I/O transfer cycle. The address-decoding circuitry generates the register-select signals that identify which AT-AO-6/10 register is being accessed. The data buffers control the direction of data transfer on the bidirectional data lines based on whether the transfer is a read or write.

The PC I/O channel interface timing signals are used to generate read and write signals and to define the transfer cycle. A transfer cycle can be either an 8-bit or a 16-bit data I/O operation. The AT-AO-6/10 returns signals to the PC I/O channel to indicate when the board has been accessed, when the board is ready for another transfer, and the data bit size of the current I/O transfer.

The interrupt control circuitry routes any enabled interrupt requests to the selected interrupt request line. The AT-AO-6/10 board can share the interrupt line with other devices because the interrupt requests are tri-state output signals. Eleven interrupt request lines are available for use by the AT-AO-6/10–IRQ3, IRQ4, IRQ5, IRQ6, IRQ7, IRQ9, IRQ10, IRQ11, IRQ12, IRQ14, and IRQ15. Interrupts can be generated by the AT-AO-6/10 in the following three situations:

- When the D/A FIFO is half-full.
- When a DMA terminal count pulse is received.
- When a falling edge signal is detected on either the internal or the external DAC update signal.

Each one of these interrupts is individually enabled and cleared. See Chapter 4, *Programming*, for more information about programming with interrupts.

The DMA control circuitry generates DMA requests whenever the D/A FIFO is not full, and the DMA transfer is enabled. The DMA circuitry supports full PC I/O channel and EISA bus 16-bit DMA transfers. DMA Channels 5, 6, and 7 of the PC I/O channel, and Channels 0, 1, 2, and 3 of the EISA bus, are available for such transfers.

Analog Output Circuitry

The AT-AO-6 and AT-AO-10 have six and ten channels of 12-bit D/A output, respectively. Unipolar or bipolar output, voltage or current output, and internal or external reference voltage selections are available with each analog output channel. Figure 3-3 shows a block diagram of the analog output circuitry.

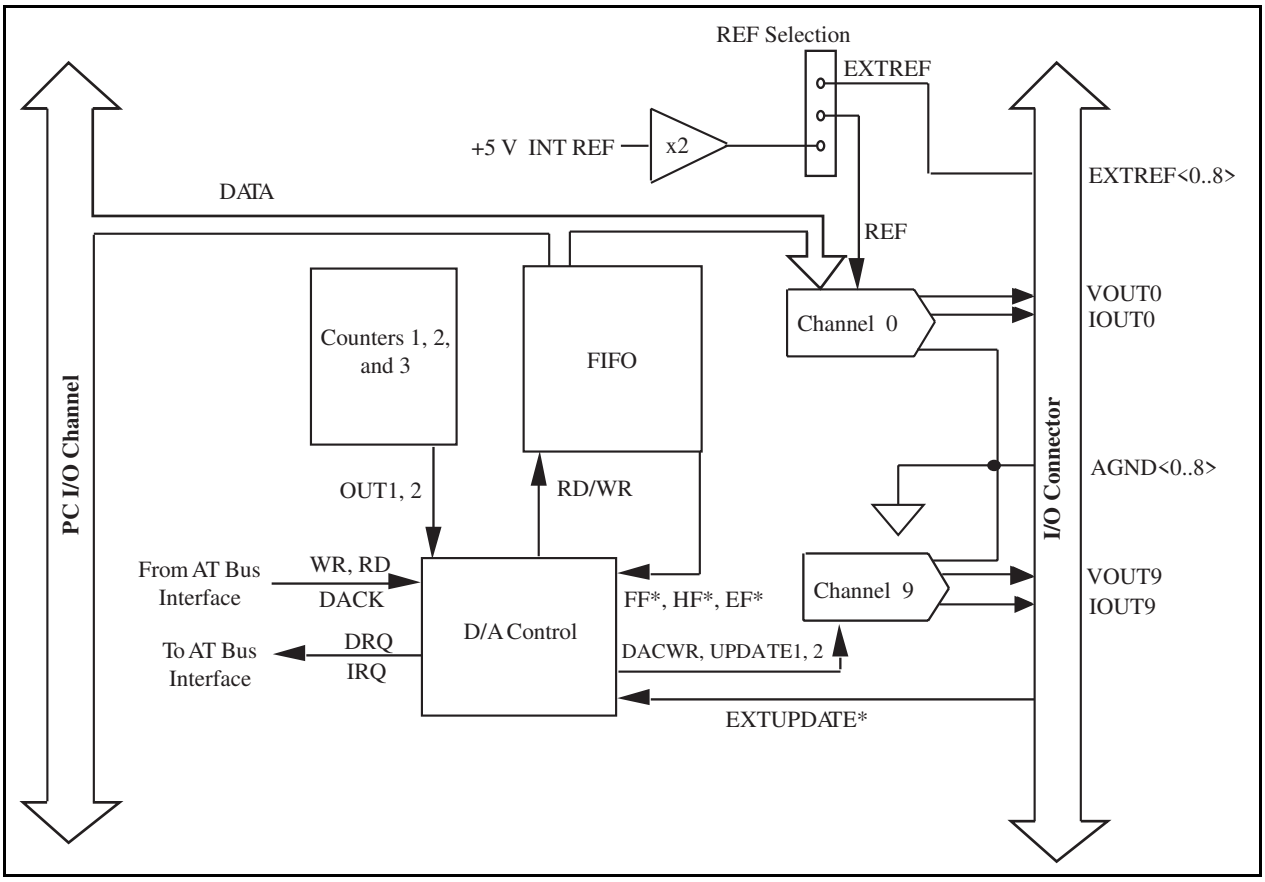


Figure 3-3. Analog Output Circuitry Block Diagram

Each analog output channel contains a 12-bit D/A converter (DAC), output operational amplifiers (op-amps), reference selection jumpers, unipolar/bipolar output selection jumpers, and a current transmitter. Each two channels share an EXTREF input line on the I/O connector.

Voltage Output

The DAC in each analog output channel generates a current proportional to the input voltage reference (Vref) multiplied by the digital code loaded into the DAC. Each DAC can be loaded with a 12-bit digital code. The output op-amps convert the DAC current output to a voltage output on the I/O connector VOUTX pins.

The DAC output op-amps can be jumper-configured to generate either a unipolar voltage output or a bipolar voltage output range. A unipolar output has an output voltage range of 0 to $+V_{ref}$ - 1 LSB V. A bipolar output has an output voltage range of $-V_{ref}$ to $+V_{ref}$ -1 LSB V. For unipolar output, 0 V output corresponds to a digital code word of 0. For bipolar output, the format of the digital code input is software-selectable from Command Register 2. If straight binary format is selected, 0 V output corresponds to a digital code word of 2,048. If two's complement format is selected, 0 V output corresponds to a digital code word of 0. One LSB is the voltage increment corresponding to an LSB change in the digital code word. For unipolar output, 1 LSB = $(V_{ref})/4,096$. For bipolar output, 1 LSB = $(V_{ref})/2,048$.

The voltage reference source for each DAC is jumper-selectable and can be supplied either externally at the EXTREF input or internally. The external reference can be either a DC or an AC signal. If an AC reference is applied, the analog output channel acts as a signal attenuator, and the AC signal appears at the output attenuated by the digital code divided by 4096 (unipolar output) or 2048 (bipolar output). The internal reference is an amplified version of the internal 5 V signal supplied in the input offset section. Using the internal reference supplies an output voltage range of 0 V to 9.9976 V in steps of 2.44 mV for unipolar output and an output voltage range of -10 V to +9.9951 V in steps of 4.88 mV for bipolar output. Gain calibration for the DACs applies only to the internal reference, not the external reference. Offset calibration can be applied to both references.

Note: Each DAC presents an impedance of 11 kΩ (unipolar mode) or 7 kΩ (bipolar mode) to ground at the EXTREF input when the external reference option is selected.

Current Output

Each channel of the AT-AO-6/10 includes a 4 to 20 mA current transmitter for use with industry-standard 4 to 20 mA current loops. An external voltage supply between 7 and 40 V must be used to power each current loop. This supply must be in series with the IOUTX connection and the load. See Figure 3-5 for a typical current output connection. The current output is available on the I/O connector between the IOUTX and AGNDX pin for each channel. Each transmitter consists of an N-channel power MOSFET current sink to ground. The output sink current is related to the output voltage by the following equation:

$$I_{sink} = \frac{(V_{out} + 2.5)}{625}$$

where I_{sink} is the output current in amperes, and V_{out} is the output voltage in volts. This equation is correct as long as the result is non-negative. The AT-AO-6/10 current outputs do not *source* current. For example, if the reference voltage is +10 V and the board is configured for unipolar output, an input digital code of zero yields an output voltage of 0 V and an output current as shown in the following equation:

$$\frac{(0 + 2.5)}{625\ \text{A}} = 4\ \text{mA}$$

With the same configuration, an input code of 4095 yields an output voltage of 9.9976 V and an output current that is shown in the following equation:

$$\frac{(9.9976 + 2.5)}{625\ \text{A}} = 19.996\ \text{mA}$$

The transfer function relating output current to output voltage is graphed in Figure 3-4.

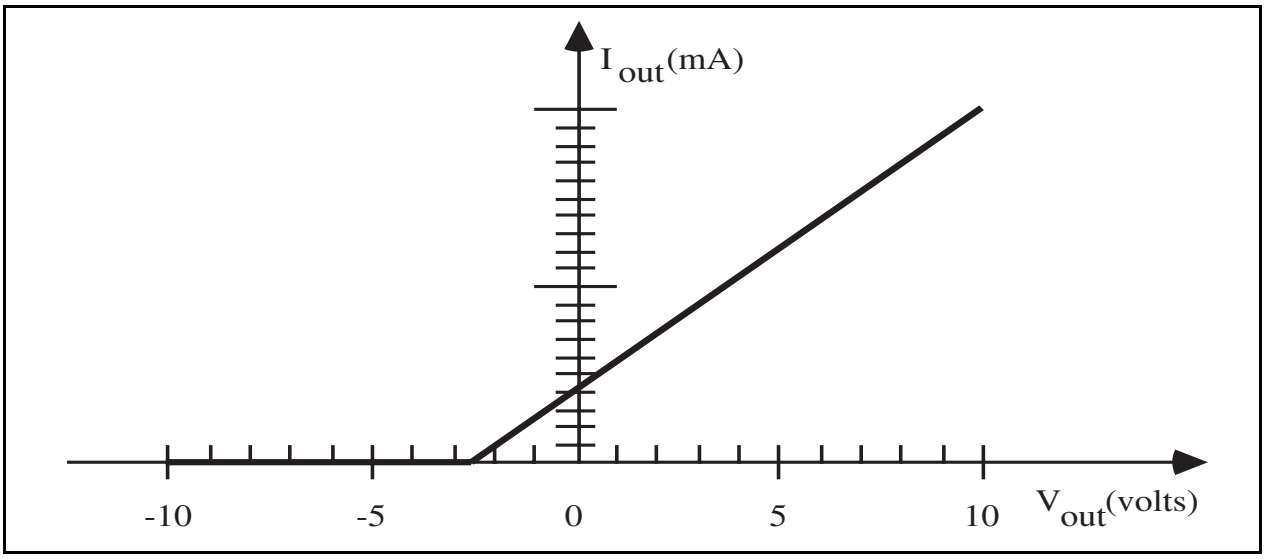


Figure 3-4. Output Sink Current Versus Output Voltage

Maintaining the voltage at the output within the specified range of 7 to 40 V is important. If the voltage is too low, the AT-AO-6/10 cannot sink the full 20 mA. If the voltage is too high, overheating can occur and the board can be damaged. Figure 3-5 shows a possible current loop connection.

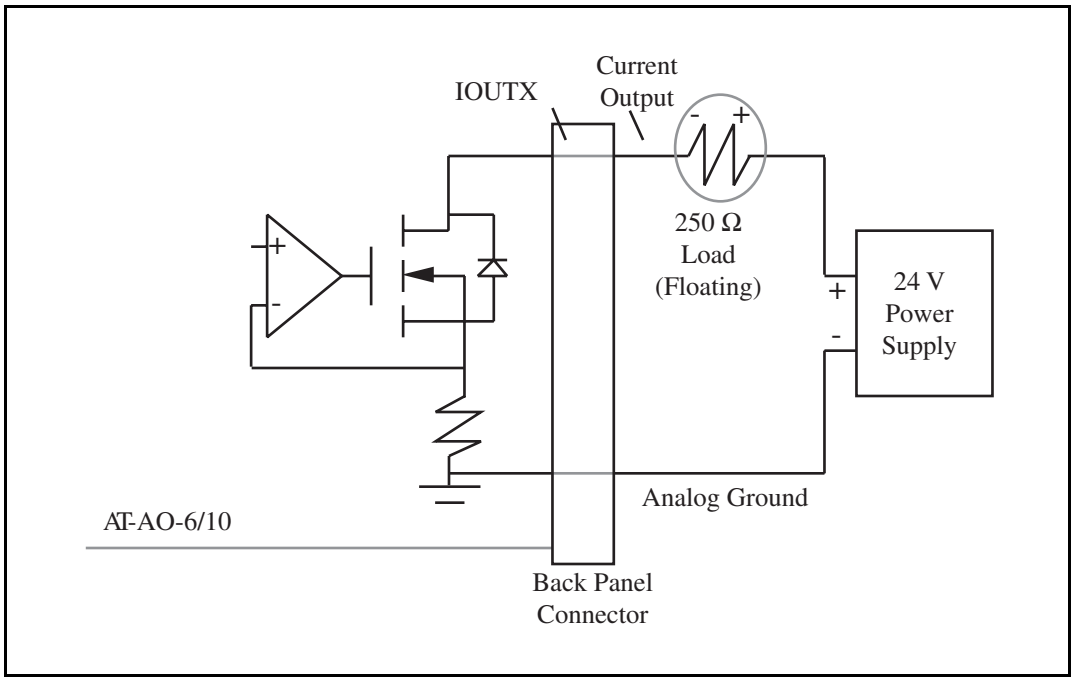


Figure 3-5. Possible Current Loop Connection

The combination of power supply voltage and load impedance used in Figure 3-5 keeps the voltage at the connector between 19 V (20 mA) and 23 V (4 mA). The voltage at the connector is always as follows:

$V_{conn} = V_{ext} - I_{out} * R_L$

where

- V_{conn} is the voltage at the connector in volts
- V_{ext} is the external power supply voltage in volts
- I_{out} is the output sink current in mA
- R_L is the resistance of the load in kΩ

Loading, Updating, and Calibrating the DACs

There are three ways to load a new value to a DAC register:

1. Write a value to the DAC register directly by the software.
2. Use the onboard 1,024-word deep FIFO as a data buffer between the host computer and the DACs. The software or the DMA transfer data to the FIFO, and concurrently, the data from the FIFO is loaded to the desired DACs upon detecting the update signals. The transfer cycle between FIFO and DAC is 500 nsec.
3. Use the FIFO retransmit feature to repeatedly load data stored in the FIFO to the desired DACs. The data is loaded into the FIFO once before the loading of the DACs begins.

The AT-AO-6/10 uses dual DAC integrated circuits. Each integrated circuit can be software configured for double-buffering mode. This feature is usually used for waveform generation. In waveform generation mode, the new value loaded to a DAC does not change the channel's output until an update signal is detected. The ten DACs on the AT-AO-10, and the six DACs on the AT-AO-6, can be divided into two groups to use different update signal sources. The following sources can be used to generate update signals:

- The onboard counter–Counter 1 output is for Group 1 of the DAC, and Counter 2 output is for Group 2 of the DAC.
- The EXTUPDATE* signal on the I/O connector–This update source can be used by either group.
- The EXTUPDATE* signal derived from the RTSI bus.
- Software controlled update.

The AT-AO-6/10 incorporates onboard calibration circuitry to individually adjust the gain and offset for each analog output channel. The startup calibration process is accomplished by retrieving constants stored in the AT-AO-6/10 EEPROM and writing them to the calibration DAC. The board is calibrated at the factory and these calibration values are stored in unmodifiable

locations in the EEPROM (see Figure 5-1). The board can also be recalibrated at the user's discretion and these new calibration constants can be stored in one of four user slots in the EEPROM. The EEPROM constants written to the calibration DAC can either be factory-calibrated values, or user-defined values to accommodate differing testing situations. A map of the EEPROM location can be found in Chapter 5, *Calibration Procedures.*

Digital I/O Circuitry

The AT-AO-6/10 has eight digital I/O lines. These lines are divided into two ports of four lines each and are located at pins ADIO<3..0> and BDIO<3..0> on the I/O connector. Figure 3-6 shows a block diagram of the digital I/O circuitry.

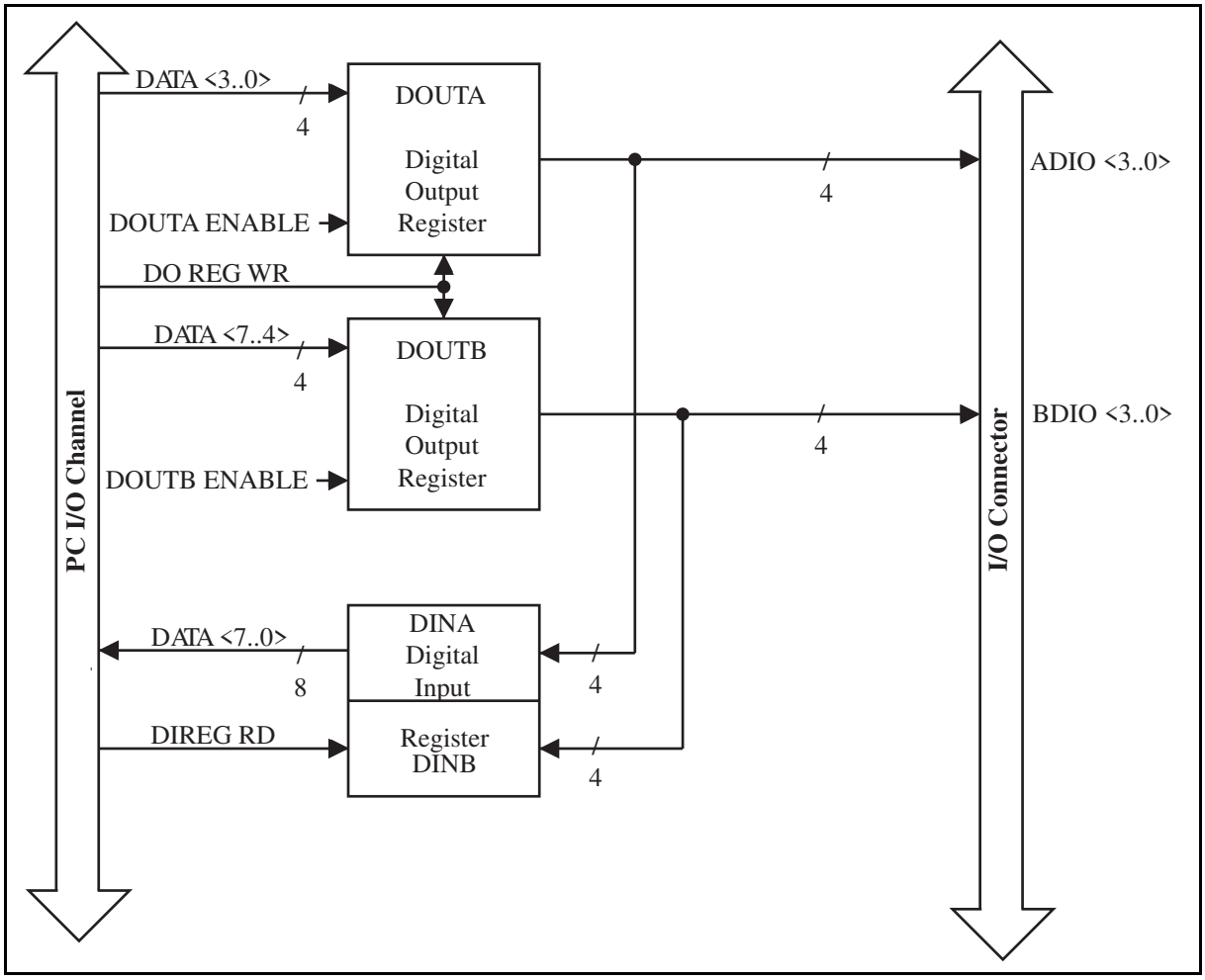


Figure 3-6. Digital I/O Circuitry Block Diagram

The digital I/O lines are controlled by the DOUT Register and monitored by the DIN Register. The DOUT Register is an 8-bit register that contains the digital output values for both Ports A and B. When Port A is enabled, bits <3..0> in the DOUT Register are driven onto digital output lines ADIO<3..0>. When Port B is enabled, bits <7..4> in the DOUT Register are driven onto digital output lines BDIO<3..0>.

Reading the DIN Register returns the state of the digital I/O lines. Digital I/O lines ADIO<3..0> are connected to bits <3..0> of the DIN Register. Digital I/O lines BDIO<3..0> are connected to bits <7..4> of the DIN Register. When a port is enabled for output, the DIN Register serves as a read-back register, returning the digital output value of the port. When a port is not enabled for output, reading the DIN Register returns the state of the digital I/O lines driven by an external device.

Both the DIN and DOUT Registers are TTL-compatible. The digital output ports, when enabled, are capable of sinking 24 mA of current and sourcing 2.6 mA of current on each digital I/O line. When the ports are not enabled for output, the digital I/O lines act as high-impedance inputs.

RTSI Bus Interface Circuitry

The AT-AO-6/10 is interfaced to the National Instrument RTSI bus. The RTSI bus has seven trigger lines and a system clock line. All National Instruments AT Series boards with RTSI bus connectors can be wired together inside the PC to share these signals. A block diagram of the RTSI bus interface circuitry is shown in Figure 3-7.

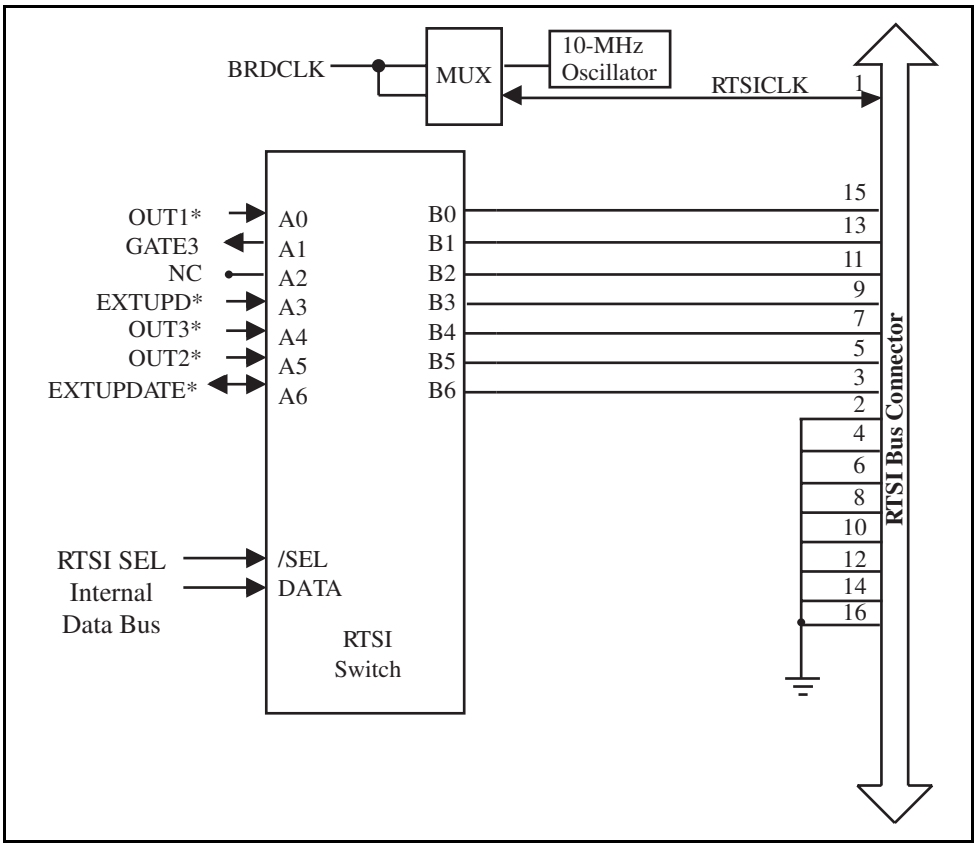


Figure 3-7. RTSI Bus Interface Circuitry Block Diagram

The RTSICLK line can be used to source a 10-MHz signal across the RTSI bus or to receive another clock signal from another AT board connected to the RTSI bus. BRDCLK is the system clock used by the AT-AO-6/10. A multiplexer selects how these clock signals are routed.

The RTSI switch is a National Instruments custom-integrated circuit that acts as a 7x7 crossbar switch. Pins B<6..0> are connected to the seven RTSI bus trigger lines. Pins A<6..0> are connected to six signals on the board. The RTSI switch can drive any of the signals at pins A<6..0> onto any one or more of the seven RTSI bus trigger lines and can drive any of the seven trigger line signals onto any one or more of the pins A<6..0>. With this capability, a signal interconnection scheme is completely flexible for any AT Series board sharing the RTSI bus. The RTSI switch is programmed via its chip select and data inputs.

On the AT-AO-6/10 board, six signals are connected to six pins of A<6..0> of the RTSI switch. The signal EXTUPDATE* is shared with the I/O connector, and is bidirectional on the RTSI switch. EXTUPD* is an active low pulse triggered by the EXTUPDATE* falling edge on the board, and can be driven to the RTSI bus. OUT1*, OUT2*, and OUT3* are onboard counter output, and can be driven to the RTSI bus. GATE3 can be an input signal connected to the Counter 3 gate. Because Counter 3 output can be selected as the source clock of Counters 1 and 2, therefore, the GATE3 signal can be used not only to control Counter 3 but also Counters 1 and 2. With these onboard interconnections, the DACs update timing can be controlled over the RTSI bus as well as externally, and the AT-AO-6/10 can send timing signals to other AT boards connected to the RTSI bus.

Chapter 4
Programming

This chapter describes in detail the address and function of each of the AT-AO-6/10 registers. This chapter also includes important information about programming the AT-AO-6/10.

Note: If you plan to use a programming software package such as NI-DAQ DOS/Windows or LabWindows with your AT-AO-6/10 board, you need not read this chapter.

Register Map

The register map for the AT-AO-6/10 is shown in Table 4-1. This table gives the register name, the register address offset from the slot base address, the register type (read only, write only, or read and write), and the size of the register in bits.

Some registers share the same address with others. The GRP2WR bit in the CFG1 Register determines which registers are being accessed at the shared address. If the GRP2WR bit is set, the registers in the parentheses are accessed. If GRP2WR is cleared, the other registers are accessed.

Table 4-1. AT-AO-6/10 Register Map

Register Name	Offset Address (Hex)	Size	Type
Configuration and Status Register Group			
CFG1 Register	0A	16-bit	Write-only
Status Register	0A	16-bit	Read-only
CFG2 Register	02	16-bit	Write-only
* (INT1CLR Register)	02	16-bit	Write-only
CFG3 Register	04	16-bit	Write-only
(INT2CLR Register)	04	16-bit	Write-only
(DMATCCLR Register)	00	16-bit	Write-only
MSM82C53 Counter/Timer Register Group			
CNTR1 Register	06	8-bit	Read-and-Write
CNTR2 Register	07	8-bit	Read-and-Write
CNTR3 Register	08	8-bit	Read-and-Write
CNTRCMD Register	09	8-bit	Read-and-Write
RTSI Bus Register Group			
(RTSISHFT Register)	06	8-bit	Write-only
(RTSISTRB Register)	07	8-bit	Write-only
Digital I/O Register Group			
DIN Register	00	16-bit	Read-only
DOUT Register	00	16-bit	Write-only

(continues)

Table 4-1. AT-AO-6/10 Register Map (continued)

Register Name	Offset Address (Hex)	Size	Type
Analog Output Register Group			
FIFO WRITE Register	0C	16-bit	Write-only
FIFO CLEAR Register	0C	16-bit	Read-only
(DAC0 Register)	0C	16-bit	Write-only
DAC1 Register	0E	16-bit	Write-only
DAC2 Register	10	16-bit	Write-only
DAC3 Register	12	16-bit	Write-only
DAC4 Register	14	16-bit	Write-only
DAC5 Register	16	16-bit	Write-only
** DAC6 Register	18	16-bit	Write-only
** DAC7 Register	1A	16-bit	Write-only
** DAC8 Register	1C	16-bit	Write-only
** DAC9 Register	1E	16-bit	Write-only

* The registers in the parentheses share the same address with other registers. If the GRP2WR bit in the CFG1 Register is set, the registers in parentheses are accessed. Otherwise the registers without parentheses are accessed when writing to these addresses.

* The DAC6 through DAC9 Registers are available on the 10-channel version of the board only.

Register Sizes

Two different transfer sizes can be used for read and write operations with the PC: byte (8-bit) and word (16-bit). Table 4-1 shows the size of each AT-AO-6/10 register. For example, reading the Status Register requires a 16-bit (word) read operation at the selected address, whereas writing to the RTSISHFT Register requires an 8-bit (byte) write operation at the selected address.

Register Description

Table 4-1 divides the AT-AO-6/10 registers into five different register groups. A bit description of each of the registers making up these groups is included later in this chapter.

The Configuration and Status Register Group controls the overall operation of the AT-AO-6/10 hardware. The configuration registers are used to program the DAC output mode, the DAC channel selection, the DAC calibration, the digital mode, and to enable DMA or interrupt requests. The status registers reflect the state of the FIFO, interrupt requests, and DMA requests. The registers in the Analog Output Register Group access the DACs or FIFO. The registers in the Digital I/O Port Group access the two 4-bit digital I/O ports. The MSM82C53 Counter/Timer Register Group selects the counting mode and initial count of the three counters. The RTSI Bus Register Group configures the RTSI bus switch.

Register Description Format

The remainder of this section discusses each of the AT-AO-6/10 registers in the order shown in Table 4-1. Each register group is introduced, followed by a detailed bit description of each register. The individual register description gives the address, type, word size, and bit map of the register, followed by a description of each bit.

The register bit map shows a diagram of the register with the MSB (bit 15 for a 16-bit register, bit 7 for an 8-bit register) shown on the left, and the LSB (bit 0) shown on the right. A square is used to represent each bit. Each bit is labeled with a name inside this square. An asterisk (*) after the bit name indicates that the bit is inverted (negative logic).

In many of the registers, one or more bits are labeled with an X, indicating *don't care* bits. When a register is read, these bits may appear set or cleared but should be ignored because they have no significance. When a register is written to, setting or clearing these bit locations has no effect on the AT-AO-6/10 hardware.

Configuration and Status Register Group

The seven registers making up the Configuration and Status Register Group can be used for general monitoring and control of the AT-AO-6/10 hardware. The three configuration registers (CFG1, CFG2, and CFG3) control the DAC output modes, DAC calibration, interrupt, and DMA operations. All the bits of these three configuration registers are cleared upon startup. The other three configuration registers (INT1CLR, INT2CLR, and DMATCCLR) clear various interrupt status bits. The Status Register reflects the DMA, interrupt, and FIFO status.

Bit descriptions of the seven registers making up the Configuration and Status Register Group are given on the following pages.

CFG1 Register

The CFG1 Register contains 16 bits that control the analog output channel selection, DMA, and interrupt operations.

Address: Base address + 0A (hex)

Type: Write-only

Word Size: 16-bit

Bit Map:

15	14	13	12	11	10	9	8
EXTINT2EN	EXTINT1EN	CNTINT2EN	CNTINT1EN	TCINTEN	CNT1SRC	CNT2SRC	FIFOEN

7	6	5	4	3	2	1	0
GRP2WR	EXTUPDEN	DMARQ	DMAEN	CH3	CH2	CH1	CH0

Bit	Name	Description
15	EXTINT2EN	External Interrupt 2 Enable Bit. When EXTINT2EN is set, a high-to-low transition on the EXTUPDATE* line triggers an active low pulse, EXTUPD*. The rising edge of the EXTUPD* pulse generates an interrupt 2 request. The interrupt 2 request is cleared by writing to the INT2CLR Register. When this bit is set, the EXTUPD* pulse also becomes the update signal for Group 2 of the DACs that have channel-numbers higher than CH<3..0>.
14	EXTINT1EN	External Interrupt 1 Enable Bit. When EXTINT1EN is set, a high-to-low transition on the EXTUPDATE* line triggers an active low pulse, EXTUPD*. The rising edge of the EXTUPD* pulse generates an interrupt 1 request. The interrupt 1 request is cleared by writing to the INT1CLR Register.
13	CNTINT2EN	Counter Interrupt 2 Enable Bit. When CNTINT2EN is set, the rising edge of OUT2* of Counter 2 generates an interrupt 2 request. The interrupt 2 request is cleared by writing to the INT2CLR Register. When this bit is set, the active low OUT2* pulse also becomes the update signal for Group 2 of the DACs that have channel-numbers higher than CH<3..0>.
12	CNTINT1EN	Counter Interrupt 1 Enable Bit. When CNTINT1EN is set, the rising edge of OUT1* of Counter 1 generates an interrupt 1 request. The interrupt 1 request is cleared by writing to the INT1CLR Register.

Bit	Name	Description (continued)
11	TCINTEN	DMA TC Interrupt or FIFO Half-Full Interrupt Enable Bit. When TCINTEN and DMAEN are set, the DMA terminal count (TC) signal generates an interrupt 1 request. If TCINTEN is set and DMAEN is cleared, the rising edge of the half-full signal HF* generated from the FIFO causes an interrupt 1 request. FH* is low when there are 512 or more words remaining in the FIFO, and FH* is high otherwise. Both interrupt requests are cleared by writing to the TCINTCLR Register.
10	CNT1SRC	Counter 1 Source Select Bit. If CNT1SRC is cleared, a 1-MHz clock is used as the counting source for Counter 1. If CNT1SRC is set, the output of Counter 3 is used as the counting source for Counter 1.
9	CNT2SRC	Counter 2 Source Select Bit. If CNT2SRC is cleared, a 1-MHz clock is used as the counting source for Counter 2. If CNT2SRC is set, the output of Counter 3 is used as the counting source for Counter 2.
8	FIFOEN	FIFO Memory Enable Bit. If FIFOEN is set, the FIFO memory is enabled. Thus, the data written to the analog output channel or channels, which form DAC Group 1 and are selected by bits CH<3..0>, are transferred through the FIFO. When the DMA transfer is used, this bit must be set because all DMA transfers are through the FIFO.
7	GRP2WR	Register Group Select Bit. Some onboard registers share the same I/O addresses. The following table shows which registers are accessed for each bit setting.

Bit Setting	Registers Accessed
GRP2WR = 0	CFG2, CFG3, Digital I/O, Counter 1, Counter 2, FIFO WRITE, FIFO CLEAR
GRP2WR = 1	INT1CLR, INT2CLR, DMATCCLR, RTSISHFT, RTSISTRB, DAC0

6	EXTUPDEN	DAC Group 1 Update Source Select Bit. If EXTUPDEN is set, internal active low pulse EXTUPD*, which is triggered by the falling edge of the EXTUPDATE* line, is the update source signal for DAC Group 1. If EXTUPDEN is cleared, the active low output of Counter 1 is the update source signal for DAC Group 1.

Bit	Name	Description (continued)
5	DMARQ	DMA Request Bit. If DMARQ and DMAEN are set, a DMA request is asserted. The DMA request can be cleared either by clearing this bit or by an active low signal, FF*, generated by the FIFO whenever the FIFO is full.
4	DMAEN	DMA Operation Enable Bit. When DMAEN is set, the DMA operation is enabled. The data transferred by the DMA operations is first stored in the FIFO and then written to DAC Group 1.
3-0	CH<3..0>	Analog Output Channel Select Bits. A value written to these four bits divides the analog output channels into two DAC groups. The channels that are equal to or lower than the value of CH<3..0> form DAC Group 1. The remaining channels form DAC Group 2. If the value of CH <3..0> is equal to zero, Channel 0 is in Group 1. The remaining channels are in Group 2. If the value of CH<3..0> is equal to nine, all 10 channels are in Group 1. If the SCANEN bit in the CFG3 Register is set, Channels 0 through Channel (CH<3..0>) make up DAC Group 1. If the SCANEN bit is cleared, Channel (CH<3..0>) is DAC Group 1. The channels in the same DAC group have the same update source. If the FIFO is enabled, the data written to the channels in Group 1 is from the FIFO.

STATUS Register

The STATUS Register contains 7 bits that reflect the status of the FIFO, the interrupts, and the output data bit of the EEPROM.

Address: Base address + 0A (hex)

Type: Read-only

Word Size: 16-bit

Bit Map:

15	14	13	12	11	10	9	8
X	X	X	X	X	X	X	X

7	6	5	4	3	2	1	0
X	FH*	FE*	FF*	INT2	INT1	TCINT	PROMOUT

Bit	Name	Description
15-7	X	Don't care bits. When read these bits return a value of 1 but should be ignored because they have no significance.
6	FH*	FIFO Half-Full Flag Bit. The FH* bit is active low when the net balance of the words written into the FIFO exceeds the number of words read out by 512 or more.
5	FE*	FIFO Empty Flag Bit. The high state of FE* indicates the FIFO is ready to output data. The low state indicates the FIFO is empty.
4	FF*	FIFO Full Flag Bit. The high state of FF* indicates the FIFO is ready to input data. The low state of FF* indicates the FIFO is full.
3	INT2	Interrupt 2 Status Bit. This bit reflects the status of interrupt 2. It is set by either the rising edge of Counter 2 output with the CNTINT2EN bit set, or the rising edge of the internal EXTUPD* signal with the EXTINT2EN bit set. It is cleared by writing to the INT2CLR Register.
2	INT1	Interrupt 1 Status Bit. This bit reflects the status of interrupt 1. It is set by either the rising edge of Counter 1 output with the CNTINT1EN bit set, or the rising edge of the internal EXTUPD* signal with the EXTINT1EN bit set. It is cleared by writing to the INT1CLR Register.

Bit	Name	Description (continued)
1	TCINT	DMA TC Interrupt or Half-Full Interrupt Status Bit. This bit reflects the status of the DMA TC or Half-Full Interrupt. It is set by either the DMA TC signal with the DMAEN bit set or the active low FH* signal with DMAEN cleared. It is cleared by writing to the DMA TC CLR Register.
0	PROMOUT	EEPROM Output Bit. This bit reflects the value of the data shifted out of the EEPROM using SCLK with the PROMEN bit set.

CFG2 Register

The CFG2 Register contains 16 bits that control the DAC calibration, the DAC input data format, and the DAC output modes.

Address: Base address + 02 (hex) (with the GRP2WR bit in the CFG1 Register cleared)

Type: Write-only

Word Size: 16-bit

Bit Map:

15	14	13	12	11	10	9	8
CALLD1	CALLD0	FFRTEN	DAC2S8*	DAC2S6*	DAC2S4*	DAC2S2*	DAC2S0*
7	6	5	4	3	2	1	0
LDAC8	LDAC6	LDAC4	LDAC2	LDAC0	PROMEN	SCLK	SDATA

Bit **Name** **Description**

15-14 CALLD<1..0>

Calibration DAC Load Bits.
Pulsing these bits loads the corresponding calibration DAC with the bits that have been clocked in by SCLK. The following table shows the pulsing pattern.

CALLD1	CALLD0	Function
0	0	no operation
0	1	load calibration DAC0
1	0	load calibration DAC1
1	1	load calibration DAC2

13 FFRTEN

FIFO Retransmit Enable Bit.
When FFRTEN is set, the retransmit function of the FIFO is enabled. The retransmit function resets the read pointer of the FIFO so the data that was previously read can be read again. This function is useful when the data for DAC waveform generation does not exceed the FIFO's depth, that is, 1,024.

12-8 DAC2S*<8..0>

DAC Input Data Format Select Bits.
When DAC2S0* is cleared, a two's complement format is used for the 16-bit data written to DAC0 and DAC1. This format is useful for the bipolar analog output mode. When DAC2S0* is set, a straight binary format is used for the 16-bit data written to DAC0 and DAC1. This format is useful for the unipolar analog output mode. Bit DAC2S2* controls the data format of DAC2 and DAC3, and in the same way bits DAC2S4* to DAC2S8* control the corresponding DACs.

Bit	Name	Description (continued)
7-3	LDAC<8..0>	Double-Buffered DAC Output Bits. When LDAC0 is cleared, DAC0 and DAC1 output are updated when they are written to. If LDAC0 is set, both DAC0 and DAC1 are updated when an active low pulse is detected on an update source line that is either an output line of a counter (either counter 1 or 2) or the EXTUPDATE* line. The LDAC2 bit controls DAC2 and DAC3, and LDAC4 through LDAC8 control DAC4 through DAC9, respectively.
2	PROMEN	EEPROM Chip Enable Bit. When PROMEN is set, the onboard EEPROM used to store the calibration constant is enabled. Before PROMEN is brought high, SCLK should be pulsed high to initialize the EEPROM circuitry.
1	SCLK	Serial Clock for EEPROM and Calibration DACs. A low-to-high transition of this bit clocks data into the EEPROM (when PROMEN is set) and the calibration DACs. If PROMEN is cleared, togging SCLK does not affect the EEPROM.
0	SDATA	Serial Data for EEPROM and Calibration DACs. This bit is used to transfer a single bit to both the EEPROM and calibration DACs.

INT1CLR Register

Writing to the INT1CLR Register clears the interrupt request asserted either by a rising edge on the Counter 1 output or by a rising edge of the EXTUPD* signal that is triggered by the falling edge of the EXTUPDATE* line.

Address: Base address + 02 (with the GRP2WR bit in the CFG1 Register set)

Type: Write-only

Word Size: 16-bit

Bit Map: Not applicable, no bits used.

CFG3 Register

The CFG3 Register contains seven bits that control digital I/O mode, analog output channel scan mode, and select the clock source on the RTSI bus.

Address: Base address + 04 (hex) (with the GRP2WR bit in the CFG1 Register cleared)

Type: Write-only

Word Size: 16-bit

Bit Map:

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0

7	6	5	4	3	2	1	0
0	DMAMODE	CLKOUT	RCLKEN	DOUTEN2	DOUTEN1	EN2.5V	SCANEN

Bit	Name	Description
15-7	0	Reserved Bits. These bits are reserved for future use and should always be cleared.
6	DMAMODE	DMA Request Mode Select Bit. When DMA is enabled, if this bit is cleared the DMA request generated by the board is a continuously high signal until the FIFO is full. If this bit is set, the DMA request signal goes to low during the active low DMA acknowledge signal period. In most PC systems, it does not make any difference when using single data DMA transfer mode.
5	CLKOUT	Onboard Clock Output Enable Bit. If this bit is set, the onboard 10-MHz clock is enabled to output to the RTSI bus. When this bit is set, the RCKLEN bit must be cleared. If this bit is cleared, the onboard clock cannot be sent to the RTSI bus.
4	RCKLEN	RTSI Bus Clock Enable Bit. When the RCKLEN bit is set, a clock signal from the RTSI bus is enabled to replace the onboard 10-MHz clock. When the RCKLEN bit is cleared, the clock from the RTSI bus is disabled.
3	DOUTEN2	Digital Output Enable 2 Bit. When this bit is set, the high nibble (bits 4 through 7) of the 8-bit digital port is enabled for output. Data written to an output port is driven to the I/O connector. An output port can be read back, and the value returned shows the current status of the I/O connector. When this bit is cleared, bits 4 through 7 of the digital I/O port are configured for input. Reading an input port returns the current status of the I/O connector.

Bit	Name	Description (continued)
2	DOUTEN1	Digital Output Enable 1 Bit. When this bit is set, the low nibble (bits 0 through 3) of the 8-bit digital port is enabled for output. Data written to an output port is driven to the I/O connector. An output port can be read back, and the value returned shows the current status of the I/O connector. When this bit is cleared, bits 0 through 3 of the digital I/O port are configured for input. Reading an input port returns the current status of the I/O connector.
1	EN2.5V	2.5-V Output Enable Bit. When EN2.5V is set, a 2.5V reference output is enabled on the IOUT9 line. If EN2.5V is cleared, the IOUT9 line is the current output of DAC Channel 9. To obtain the 2.5V output, Channel 9 current output must be shut off. To do this, the Channel 9 must be configured in bipolar mode with two's complement format, and a negative value -1000 (decimal) must be written to DAC9.
0	SCANEN	DAC Channel Scan Mode Enable Bit. When SCANEN is set, DAC Channel 0 through Channel (CH<3..0>) are scanned sequentially. In this mode, the FIFO should be enabled. A rising edge of an update signal starts a scan sequence. Data from the FIFO is written to DAC Channel 0 through Channel (CH<3..0>) sequentially. Then the next active low update signal updates the output of these channels, and the rising edge of the update signal starts another scan sequence. If the SCANEN is cleared and FIFO is enabled, the data from the FIFO is written to channel CH<3..0> only.

INT2CLR Register

Writing to the INT2CLR Register clears the interrupt request asserted either by a rising edge on the Counter 2 output or by a rising edge of the EXTUPD* signal that is triggered by the falling edge of the EXTUPDATE* line.

Address: Base address + 04 (with the GRP2WR bit in the CFG1 Register set)

Type: Write-only

Word Size: 16-bit

Bit Map: Not applicable, no bits used.

DMATCCLR Register

Writing to the DMATCCLR Register clears the interrupt request caused by either the DMA TC signal or the low-to-high transition of the Half-Full signal of the FIFO.

Address: Base address + 00 (with the GRP2WR bit in the CFG1 Register set)

Type: Write-only

Word Size: 16-bit

Bit Map: Not applicable, no bits used.

MSM82C53 Counter/Timer Register Group

The four registers making up the MSM82C53 Counter/Timer Register Group access the onboard MSM82C53 Counter/Timer.

The MSM82C53 contains three counters. Counters 1 and 2 can be used to generate update signals or interrupts for waveform generation. Counter 3 can be used to generate an alternative clock source for Counters 1 and 2.

Bit descriptions of the four registers making up the MSM82C53 Counter/Timer Register Group are given on the following pages.

CNTR1 Register

The CNTR1 Register contains eight bits that are used to load a value into Counter 1 or to read back the value of Counter 1. The CNTR1 Register can be used as an 8-bit register or as a 16-bit register by two successive write/read operations.

Address: Base address + 06 (hex) (with the GRP2WR bit cleared)

Type: Read-and-write

Word Size: 8-bit

Bit Map:

7	6	5	4	3	2	1	0
CNTR1B7	CNTR1B6	CNTR1B5	CNTR1B4	CNTR1B3	CNTR1B2	CNTR1B1	CNTR1B0

Bit	Name	Description
7-0	CNTR1B<7..0>	Counter 1 Load/Read Bits. Writing a data value to these bits loads the starting value into Counter 1. Reading these bits returns the current count of Counter 1 or latched data for Counter 1. If the Counter Latch command or the Read-Back command is used to latch the count or status of Counter 1, reading these bits returns the latched information. The latched data remains latched until it is read. If multiple Latch commands or Read-Back commands are issued before the latched data is read, only the data from the first Status Latch command and the first Counter Latch command are latched; all commands after the first are ignored. If 16-bit data is latched, the first read from this register returns the least significant byte, and the second read returns the most significant byte. If status and count information are both latched, the first read from this register returns the status byte, and the next one read for 8-bit mode, or two reads for 16-bit mode, returns the count bytes, regardless of the order in which the information was latched.

CNTR2 Register

The CNTR2 Register contains eight bits that are used to load a value into Counter 2 or to read back the value of Counter 2. The CNTR2 Register can be used as an 8-bit register or as a 16-bit register by two successive write/read operations.

Address: Base address + 07 (hex) (with the GRP2WR bit cleared)

Type: Read-and-write

Word Size: 8-bit

Bit Map:

7	6	5	4	3	2	1	0
CNTR2B7	CNTR2B6	CNTR2B5	CNTR2B4	CNTR2B3	CNTR2B2	CNTR2B1	CNTR2B0

Bit	Name	Description
7-0	CNTR2B<7..0>	Counter 2 Load/Read Bits. Writing a data value to these bits loads the starting value into Counter 2. Reading these bits returns the current count of Counter 2 or latched data for Counter 2. If the Counter Latch command or the Read-Back command is used to latch the count or status of Counter 2, reading these bits returns the latched information. The latched data remains latched until it is read. If multiple Latch commands or Read-Back commands are issued before the latched data is read, only the data from the first Status Latch command and the first Counter Latch command are latched; all commands after the first are ignored. If 16-bit data is latched, the first read from this register returns the least significant byte, and the second read returns the most significant byte. If status and count information are both latched, the first read to this register returns the status byte, and the next one read for 8-bit mode, or two reads for 16-bit mode, returns the count bytes, regardless of the order in which the information was latched.

CNTR3 Register

The CNTR3 Register contains eight bits that are used to load a value into Counter 3 or to read back the value of Counter 3. The CNTR3 Register can be used as an 8-bit register or as a 16-bit register by two successive write/read operations.

Address: Base address + 08 (hex)

Type: Read-and-write

Word Size: 8-bit

Bit Map:

7	6	5	4	3	2	1	0
CNTR3B7	CNTR3B6	CNTR3B5	CNTR3B4	CNTR3B3	CNTR3B2	CNTR3B1	CNTR3B0

Bit	Name	Description
7-0	CNTR3B<7..0>	Counter 3 Load/Read Bits. Writing a data value to these bits loads the starting value into Counter 3. Reading these bits returns the current count of Counter 3 or latched data for Counter 3. If the Counter Latch command or the Read-Back command is used to latch the count or status of Counter 3, reading these bits returns the latched information. The latched data remains latched until it is read. If multiple Latch commands or Read-Back commands are issued before the latched data is read, only the data from the first Status Latch command and the first Counter Latch command are latched; all commands after the first are ignored. If 16-bit data is latched, the first read from this register returns the least significant byte, and the second read returns the most significant byte. If status and count information are both latched, the first read to this register returns the status byte, and the next one read for 8-bit mode, or two reads for 16-bit mode, return the count bytes, regardless of the order in which the information was latched.

CNTRCMD Register

The CNTRCMD Register contains eight bits that determine the counter selection, counter size, counting format, and operation mode.

Address: Base address + 09 (hex)

Type: Write-only

Word Size: 8-bit

Bit Map:

7	6	5	4	3	2	1	0
CNTRSEL1	CNTRSEL0	RWSEL1	RWSEL0	MODESEL2	MODESEL1	MODESEL0	BCDSEL

Bit	Name	Description
7-6	CNTRSEL<1..0>	Counter Select Bits. These bits select the counter on which the command operates.

CNTRSEL1	CNTRSEL0	Operation
0	0	Select Counter 1
0	1	Select Counter 2
1	0	Select Counter 3
1	1	Read-Back command

5-4 RWSEL<1..0> Read/Write Select Bits.
These bits select data written to or read from a counter, or these bits send a Counter Latch command.

RWSEL1	RWSEL0	Operation
0	0	Counter Latch command
0	1	Read-and-write least significant byte only
1	0	Read-and-write most significant byte only
1	1	Read-and-write least significant byte then most significant byte

Bit	Name	Description (continued)
		The Counter Latch command latches the current count of the register selected by CNTRSEL1 and CNTRSEL0. The next read from the selected counter returns the latched data.
3-1	MODESEL<2..0>	Counter Mode Select Bits. These bits select the counting mode of the selected counter. The following table lists six available modes and the corresponding bit settings. Refer to Appendix C, *MSM82C53 Data Sheet*, for additional information.

MODESEL2	MODESEL1	MODESEL0	Mode
0	0	0	Mode 0 – Interrupt on Terminal Count
0	0	1	Mode 1 – Hardware Retriggerable One Shot
0	1	0	Mode 2 – Rate Generator
0	1	1	Mode 3 – Square Wave Mode
1	0	0	Mode 4 – Software Retriggerable Strobe
1	0	1	Mode 5 – Hardware Retriggerable Strobe

0	BCDSEL	Binary Coded Decimal Select Bit. If BCDSEL is set, the selected counter keeps count in BCD. If BCDSEL is cleared, the selected counter keeps count in 16-bit binary.

Read-Back Command

When bits 7 and 6 (CNTRSEL1 and CNTRSEL0) are 1, the CNTRCMD Register can be used to execute the Read-Back command. With the Read-Back command, the current totals of multiple counters can be latched in one command. The Read-Back command also can latch the status of selected counters. The control word format used for the Read-Back command is as follows:

7	6	5	4	3	2	1	0
CNTRSEL1	CNTRSEL0	COUNT*	STATUS*	CNTR3	CNTR2	CNTR1	0

Bit	**Name**	**Description**
7-6	CNTRSEL<1..0>	Counter Select Bits. Both bits *must* be one for the Read-Back command to be used.
5	COUNT*	Read-Back Count Command. If COUNT* is cleared, the current count in each of the selected counters is latched. The next read from the selected counter returns the latched data.
4	STATUS*	Read-Back Status Command. If STATUS* is cleared, the current status in each of the selected counters is latched. The next read from the selected counter returns the latched data.
3-1	CNTR<3..1>	Counter Select Bits for Read-Back Command. These bits select the counters for the Read-Back command; that is, if CNTR3 and CNTR1 are set, the Read-Back command latches data for Counter 3 and Counter 1.
0	0	Reserved Bit. This bit must be set to zero for proper operation of the AT-AO-6/10.

Status Byte

If the STATUS* bit is zero in the Read-Back command, status information for the selected counters is latched. The status byte format is as follows:

7	6	5	4	3	2	1	0
OUT	NULL	RW1	RW0	MODE2	MODE1	MODE0	BCD

Bit	**Name**	**Description**
7	OUT	Counter Output. The OUT bit reflects the current status of the counter output.
6	NULL	Last Count Written Status. If NULL is zero, the last count written to the selected counter has been loaded into the counter. If NULL is set, the last count written to the counter has not been loaded.
5-4	RW<1..0>	RWSEL1 and RWSEL0 Status. The RW1 and RW0 bits reflect the status of the RWSEL1 and RWSEL0 bits of the selected counter.
3-1	MODE<2..0>	MODE2, MODE1, and MODE0 Status. The MODE2, MODE1, and MODE0 bits reflect the state of the MODESEL2, MODESEL1, and MODESEL0 bits of the selected counter.
0	BCD	Binary Coded Decimal Select (BCDSEL) Status. The BCD bit reflects the status of the BCDSEL bit of the selected counter.

Refer to Appendix C, *MSM82C53 Data Sheet*, for more information on programming the counters.

RTSI Bus Register Group

The two registers making up the RTSI Bus Register Group program the AT-AO-6/10 RTSI switch for routing of signals on the RTSI bus trigger lines to and from several AT-AO-6/10 signal lines.

Bit descriptions of the two registers making up the RTSI Bus Register Group are given on the following pages.

RTSISHFT Register

The RTSISHFT Register contains one bit, RSI, that is a serial input to the RTSI switch. RSI must be written to 56 times to load the internal 56-bit RTSI control register.

Address: Base address + 06 (hex) (with the GRP2WR bit set)

Type: Write-only

Word Size: 8-bit

Bit Map:

7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	RSI

Bit	Name	Description
7-1	X	Don't care bits.
0	RSI	RTSI Switch Serial Input. This bit is the serial input to the RTSI switch. Each time the RSI bit is written to, the value written is shifted into the RTSI switch internal 56-bit control register. The data in the control register routes information for switching signals to and from the RTSI bus trigger lines. The RSI bit must be written to 56 times to shift the 56 bits of routing data into the internal control register. See *Programming the RTSI Switch* later in this chapter for more information.

RTSISTRB Register

Writing to the RTSISTRB Register loads the contents of the RTSI Shift Register into the RTSI Switch Control Register, thereby updating the RTSI switch routing pattern. The RTSISTRB Register is written to after shifting the 56-bit routing pattern into the RTSISHFT Register.

Address: Base address + 07 (hex) (with the GRP2WR bit set)

Type: Write-only

Word Size: 8-bit

Bit Map: Not applicable, no bits used.

Digital I/O Register Group

The two registers making up the Digital I/O Register Group monitor and control the AT-AO-6/10 digital I/O lines. The DIN Register returns the digital state of the eight digital I/O lines. A pattern written to the DOUT Register is driven onto the digital I/O lines when the digital output drivers are enabled (see the description for the CFG3 Register).

Bit descriptions for the registers making up the Digital I/O Register Group are given on the following pages.

DIN Register

Reading the DIN Register returns the logic state of the eight AT-AO-6/10 digital I/O lines.

Address: Base address + 00 (hex) (with the GRP2WR bit in the CFG1 Register cleared)

Type: Read-only

Word Size: 16-bit

Bit Map:

15	14	13	12	11	10	9	8
X	X	X	X	X	X	X	X

7	6	5	4	3	2	1	0
BDI3	BDI2	BDI1	BDI0	ADI3	ADI2	ADI1	ADI0

Bit	Name	Description
15-8	X	Don't care bits.
7-4	BDI<3..0>	These four bits represent the logic state of the digital lines BDIO<3..0>.
3-0	ADI<3..0>	These four bits represent the logic state of the digital lines ADIO<3..0>.

DOUT Register

Writing to the DOUT Register controls the eight AT-AO-6/10 digital I/O lines. The DOUT Register controls both Ports A and B. When either digital port is enabled, the pattern contained in the DOUT Register is driven onto the lines of the digital port.

Address: Base address + 00 (hex) (with the GRP2WR bit in the CFG1 Register cleared)

Type: Write-only

Word Size: 16-bit

Bit Map:

15	14	13	12	11	10	9	8
X	X	X	X	X	X	X	X

7	6	5	4	3	2	1	0
BDO3	BDO2	BDO1	BDO0	ADO3	ADO2	ADO1	ADO0

Bit	Name	Description
15-8	X	Don't care bits.
7-4	BDO<3..0>	These four bits control the digital lines BDIO<3..0>. The bit DOUTEN2 in the CFG3 Register must be set for BDO<3..0> to be driven onto the digital lines BDIO<3..0>.
3-0	ADO<3..0>	These four bits control the digital lines ADIO<3..0>. The bit DOUTEN1 in the CFG3 Register must be set for ADO<3..0> to be driven onto the digital lines ADIO<3..0>.

Analog Output Register Group

Ten of the twelve registers making up the Analog Output Register Group load the ten analog output channels. DAC0 through DAC9 control analog output Channel 0 through Channel 9, respectively. These registers can be written to individually or scanned automatically. The analog output can be updated immediately or each time an update pulse is detected on either the EXTUPDATE* line or on the output of one of the two onboard counters. The update method is selected with the LDAC bit in the CFG2 Register.

The other two registers in this group are the FIFO WRITE Register and the FIFO CLEAR Register. The FIFO WRITE Register is a write-only register. It can be written to by the programmed I/O or by the DMA transfer. The FIFO CLEAR Register is a read-only register. Reading this register clears the whole FIFO memory. The result of the reading should be ignored. Descriptions of the registers making up the Analog Output Register Group are given on the following pages.

FIFO WRITE Register

Writing to the FIFO WRITE Register loads a 16-bit value to the FIFO memory.

Address: Base address + 0C (hex) (with the GRP2WR bit in CFG1 Register cleared)

Type: Write-only

Word Size: 16-bit

Bit Map:

15	14	13	12	11	10	9	8
Sign Extension Bits				D11	D10	D9	D8

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

Bit	Name	Description
15-12	Sign Bits	Sign Extension Bits. If the two's complement format of analog output is selected, these bits are sign extension bits equal to D11. If the straight binary format is selected, these bits are zero.
11-0	D<11..0>	Data Bits The 12-bit data ranges from 0 to 4095 decimal (0000 to 0FFF hex) if straight binary format is selected, or from -2048 to +2047 decimal (F800 to 07FF hex) if two's complement format is selected. The data written to this register is loaded into the 1,024-word deep FIFO memory. This register can be accessed by either program I/O or by DMA transfer. The data stored in the FIFO memory can only be loaded to DAC Group 1. When the FIFO memory is full, the data written to the FIFO WRITE Register is lost. The status of the FIFO can be obtained by reading the STATUS Register. With DMA transfers, when the FIFO is full, the DMA request is automatically masked to stop the writing to this register.

FIFO CLEAR Register

Reading the FIFO CLEAR Register clears the entire FIFO memory.

Address: Base address + 0C (with the GRP2WR bit in the CFG1 Register cleared)

Type: Read-only

Word Size: 16-bit

Bit Map: Not applicable, no bits used.

DAC0 through DAC9 Registers

Writing to any of the DAC Registers loads the corresponding analog output channel DAC. The voltages generated by the analog output channels are updated either immediately or when an update pulse is detected. The update method is selected by the LDAC bit in the CFG2 Register. These registers are further divided into two groups by 4 bits, CH<3..0> of the CFG1 Register. The registers that have channels numbers higher than CH<3..0> make up DAC Group 2. The registers of DAC Group 2 are written by programmed I/O individually, and they are updated together if the corresponding LDAC bits are set upon the detecting of an update pulse. The source of the update pulse for this group is either OUT2 or the EXTUPDATE* signal. The rest of the DAC registers make up DAC Group 1. The data written to the DAC Group 1 registers can be either from I/O writing or from onboard FIFO directly, depending on the status of the FIFOEN bit in the CFG1 Register. If the SCANEN bit of the CFG3 Register is set, the DAC Group 1 registers are scanned sequentially from DAC0 through DAC (CH<3..0>). The data written to these registers is from the FIFO (the FIFOEN bit must be set). Between two successive update pulses each DAC is written once, and the update pulse updates them together. The update source can be either the OUT1 or the EXTUPDATE* signal. If the SCANEN bit of the CFG3 Register is cleared, only the DAC (CH<3..0>) register uses the FIFO data and is updated by the update pulse. The other registers are written individually by programmed I/O.

Address:	Base Address + 0C (with GRPWR2 set)	DAC0 Register
	Base Address + 0E (hex)	DAC1 Register
	Base Address + 10 (hex)	DAC2 Register
	Base Address + 12 (hex)	DAC3 Register
	Base Address + 14 (hex)	DAC4 Register
	Base Address + 16 (hex)	DAC5 Register
	Base Address + 18 (hex)	DAC6 Register
	Base Address + 1A (hex)	DAC7 Register
	Base Address + 1C (hex)	DAC8 Register
	Base Address + 1E (hex)	DAC9 Register

Type: Write-only

Word Size: 16-bit

Bit Map:

15	14	13	12	11	10	9	8
Sign Extension Bits					D10	D9	D8

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

Bit	Name	Description
15-12	Sign Bits	Sign Extension Bits. If the two's complement format of analog output is selected, these bits are sign extension bits equal to D11. If the straight binary format is selected, these bits are zero.

Bit	Name	Description (continued)
11-0	D<11..0>	The digital code to be loaded into the DAC. This 12-bit data ranges from 0 to 4095 decimal if straight binary format is selected, or from -2048 to +2047 decimal if two's complement format is selected.

The formula for the voltage output versus digital code for a unipolar analog output configuration is as follows:

$$V_{out} = V_{ref} * \frac{(\text{digital code})}{4,096}$$

where V_{ref} is the reference voltage applied to the analog output channel. The digital code in the above formula is a decimal value ranging from 0 to 4,095.

Table 4-2. Analog Output Voltage Versus Digital Code (Unipolar Mode)

Digital Code		**Voltage Output**	
Decimal	**Hex**	**V_{out}**	**V_{ref} = 10 V**
0	0	0	0 V
1	1	$\frac{V_{ref}}{4,096}$	2.44 mV
1,024	0400	$\frac{V_{ref}}{4}$	2.5 V
2,048	0800	$\frac{V_{ref}}{2}$	5 V
3,072	0C00	$\frac{V_{ref} * 3}{4}$ -	7.5 V
4,095	0FFF	$\frac{V_{ref} * 4,095}{4,096}$	9.9976 V

The formula for the voltage output versus digital code for a bipolar, straight binary analog output configuration is

$$V_{out} = V_{ref} * \frac{(\text{digital code} - 2,048)}{2,048}$$

where V_{ref} is the reference voltage applied to the analog output channel. The digital code in the preceding formula is a decimal value ranging from 0 to 4,095.

Table 4-3. Analog Output Voltage Versus Digital Code (Bipolar, Straight Binary Mode)

Digital Code		**Voltage Output**	
Decimal	**Hex**	$\mathbf{V_{ref}}$	$\mathbf{V_{ref}}$ **= 10 V**
0	0	$-V_{ref}$	- 10 V
1	1	$\frac{V_{ref} * (-2,047)}{2,048}$	-9.9951 V
1,024	0400	$\frac{-V_{ref}}{2}$	- 5 V
2,047	07FF	$\frac{V_{ref}}{2,048}$	- 4.88 m V
2,048	0800	0	0 V
2,049	0801	$\frac{V_{ref}}{2,048}$	4.88 m V
3,072	0C00	$\frac{V_{ref}}{2}$	5 V
4,095	0FFF	$\frac{V_{ref} * (2,047)}{2,048}$	9.9951 V

The formula for the voltage output versus digital code for a bipolar, two's complement analog output configuration is as follows:

$$V_{out} = V_{ref} * V_{ref} * \frac{\text{digital code}}{2,048}$$

where V_{ref} is the reference voltage applied to the analog output channel. The digital code in the preceding formula is a decimal value ranging from -2,048 to 2,047.

Table 4-4. Analog Output Voltage Versus Digital Code (Bipolar, Two's Complement Mode)

Digital Code		**Voltage Output**	
Decimal	**Hex**	$\mathbf{V_{ref}}$	$\mathbf{V_{ref} = 10\ V}$
-2,048	(F) 800	$-V_{ref}$	- 10 V
-2,047	(F) 801	$\frac{V_{ref} * -2,047}{2,048}$	-9.9951 V
1,024	(F) C00	$\frac{-V_{ref}}{2}$	- 5 V
-1	(F) FFF	$\frac{V_{ref}}{2,048}$	- 4.88 m V
0	0	0	0 V
1	1	$\frac{V_{ref}}{2,048}$	4.88 m V
1,024	(0) 400	$\frac{V_{ref}}{2}$	5 V
2,047	(0) 7FF	$V_{ref} * \frac{2,047}{2,048}$	9.9951 V

Programming Considerations

This section contains programming instructions for operating the circuitry on the AT-AO-6/10 board. Programming the AT-AO-6/10 involves writing and reading from the various registers on the board. The programming instructions list the sequence of steps to take. The instructions are language-independent; that is, they instruct you to write a value to a given register, to set or clear a bit in a given register, or to detect whether a given bit is set or cleared without presenting the actual code.

Register Programming Considerations

Several write-only registers on the AT-AO-6/10 contain bits that control a number of independent pieces of the onboard circuitry. In the instructions for setting or clearing these bits, specific register bits should be set or cleared without changing the current state of the remaining bits in the register. However, writing to these registers affects all register bits simultaneously. You cannot read these registers to determine which bits have been set or cleared in the past; therefore, you should maintain a software copy of the write-only registers. This software copy can then be read to determine the status of the write-only registers. To change the state of a single bit without disturbing the remaining bits, set or clear the bit in the software copy and write the software copy to the register.

Initializing the AT-AO-6/10 Board

Upon startup the AT-AO-6/10 hardware is auto-initialized. All bits in the three CFG Registers are cleared. The voltage output of each analog output channel is set to 0 V in the bipolar mode, or 5 V in the unipolar mode if the internal 10 V_{ref} is selected, or it is set to the medium value of the external reference voltage. The hardware can be also initialized by the software. To initialize the
AT-AO-6/10 hardware, complete these steps:

1. Write 0 to the CFG1 Register.
2. Write 18 to the CNTRCMD Register.
3. Write 3 to the CNTR1 Register.
4. Write 58 to the CNTRCMD Register.
5. Write 0 to the CFG2 Register.
6. Write 0 to the CFG3 Register.
7. Read the FIFO CLEAR Register. Ignore the result.
8. Write 80 to the CFG1 Register.
9. Write 0 to the INT1CLR Register.
10. Write 0 to the INT2CLR Register.
11. Write 0 to the DMATCCLR Register.

12. Write 0 to the CFG1 Register.

This sequence leaves the AT-AO-6/10 circuitry in the following state:

- FIFO is cleared.
- All interrupts are disabled.
- DMA is disabled.
- Digital I/O lines are in high-impedance state (in other words, in input mode).
- Calibration is disabled.
- Both outputs of Counter 1 and Counter 2 are in high state (Logic One).

Programming the Analog Output Circuitry

The voltage at the analog output circuitry output pins is controlled by writing to the corresponding DAC Registers and updating the analog output. The analog output can be updated in one of two ways–immediately when the DAC Register is written, or when an active low update pulse is detected.

Immediately Updating the Analog Output

The bits LDAC0 through LDAC8 in the CFG2 Register control the update method. Each LDAC bit controls two analog output channels: LDAC0 controls Channels 0 and 1, LDAC2 controls Channels 2 and 3, etc. If the LDAC*x* bit (where *x* refers to 0 through 8) is cleared, writing to the corresponding DAC Register(s) updates the channel's analog output immediately. If the LDAC*x* bit is set, writing to the DAC Register does not change the analog output until the LDAC*x* bit is cleared or an update signal is received.

Using the Update Signal for Waveform Generation

When the LDAC bit for the corresponding two DACs is set, the DACs are configured in double-buffered mode. In this mode, when a new value is written to a DAC, the output of the DAC is not changed until an update signal is received. The following sections describe how to program the analog output circuitry for waveform generation using the update signal.

Analog Output Channel Group

The analog output channels on the AT-AO-6/10 can be programmed into two groups. Writing a channel number *n* to the CH<0..3> bit field of the CFG1 Register selects Channels 0 through *n* to include in Group 1. The rest of the channels make up Group 2. Different update sources can be used for Group 1 and Group 2.

Select Update Source Signal for a Group

The available update sources for Group 1 are Counter 1 output OUT1* and EXTUPDATE*.

- Writing one to the EXTUPDEN bit of the CFG1 Register selects the EXTUPDATE* signal as the update source for Group 1.
- Writing zero to the EXTUPDEN bit of the CFG1 Register selects the OUT1* signal as the update source for Group 1.

The update sources for Group 2 are Counter 2 output OUT2* and EXTUPDATE*.

- Writing one to the EXTINT2EN bit of the CFG1 Register selects the EXTUPDATE* signal as the update source for Group 2.
- Writing one to the CNTINT2EN bit of the CFG1 Register selects the OUT2* signal as the update source for Group 2.
- The EXTINT2EN bit and the CNTINT2EN bit should not be set at the same time.

Group 1 Scan Mode Using DMA

In waveform generation operations using DMA transfers, Group 1 always uses onboard FIFO memory as a data buffer. The FIFO is 1,024 words deep. The data is read from the system memory to the FIFO by DMA operation. Then the data is written to the Group 1 DACs. In the scan mode, after detecting the update pulse, each channel in Group 1 is written once sequentially from Channel 0 to Channel *n*. The next update pulse updates the output of the channels and initializes another writing cycle. Each writing of a channel lasts 500 nsec. Therefore, a scan cycle (or update interval) must last longer than (500 nsec∗ number of channels in Group 1). The DMA continuously transfers data to the FIFO unless the FIFO is full. In addition, data is continuously written to the DACs unless the FIFO is empty. These two operations are independent and concurrent. To set up this mode, use the following programing steps:

1. Write a pattern to the CFG1 Register. The pattern should include:

   - setting the following bits–FIFOEN, DMAEN, and TCINTEN (if DMA TC interrupt is desired).

   - a proper value in the CH<0..3> bit field to select channels to be scanned clearing the EXTUPDEN bit at this time

2. Write a pattern to the CFG2 Register. The pattern should include:

   - setting the corresponding LDAC*x* bits for the channels to be scanned.

   - setting or clearing corresponding DAC2S*x** bits (where *x* refers to 0 through 8) for selecting straight binary or two's complement format.

3. Set the SCANEN bit in the CFG3 Register.

4. Program the system DMA controller; enable the corresponding DMA channel.

5. Read the FIFO Clear Register and ignore the result.

6. Set the DMARQ bit in the CFG1 Register to enable the DMA transfer.

7. Initialize the output channels by using Counter 1 to generate a single pulse to write the desired first data to the DACs. Thus the next update pulse will dump the proper output to the channels. To initialize the output channels, you must do the following:

- write 0x18 to the CNTRCMD Register.
- write 2 to the CNTR1 Register.

8. Wait for about 5 µsec.
9. Set or clear the EXTUPDEN bit in the CFG1 Register to select the update source signal.
10. If OUT1* is selected as the update signal:
    - write 0x34 to the CNTRCMD Register.
    - write the scan cycle period (low byte first, then high byte) in µsec to the CNTR1 Register.

    After writing the high byte the counter starts counting.

The DMA transfer operation may terminate on terminal count. You can also terminate it by clearing either the DMAEN bit or the DMARQ bit. After the termination of the DMA transfer, the remaining data in the FIFO is continually written to the DACs until the FIFO is empty or the FIFOEN bit is cleared.

Group 1 Scan Mode Using Interrupt

Three interrupts can be used with the Group 1 waveform generation operation–the Counter 1 Interrupt, the External Update Interrupt 1, and the FIFO Half-Full Interrupt. The FIFO Half-Full Interrupt should be used when the FIFO is used as a data buffer. The program sequence is similar to the DMA program sequence, except the DMA is disabled:

1. Write a pattern to the CFG1 Register. The pattern should include:
    - setting the FIFOEN bit.
    - a proper value in the CH<0..3> bit field to select channels to be scanned.
    - clearing the EXTUPDEN bit at this time.
2. Write a pattern to the CFG2 Register. The pattern should include:
    - setting the corresponding LDAC*x* bits for the channels to be scanned.
    - setting or clearing corresponding DAC2S*x** bits for selecting straight binary or two's complement format, respectively.
3. Set the SCANEN bit in the CFG3 Register.
4. Read the FIFO Clear Register and ignore the result.
5. Write the data to the FIFO until it is full.
6. Initialize the output channels by using Counter 1 to generate a single pulse to write the desired first data to the DACs. Thus the next update pulse will dump the proper output to the channels. To initialize the output channels, you must do the following:

- write 0x18 to the CNTRCMD Register.
- write 2 to the CNTR1 Register.

7. Set the TCINTEN bit in CFG1 Register.
8. Program the system interrupt controller and enable the proper interrupt level.
9. Set or clear the EXTUPDEN bit to select the update source signal.
10. If OUT1* is selected as the update signal:

    - write 0x34 to the CNTRCMD Register.
    - write the scan cycle period (low byte first, then high byte) in µsec to the CNTR1 Register.

    After writing the high byte the counter starts counting.

Whenever a half space or more is free in the FIFO, an interrupt is generated. The interrupt handler should write 512 words to the FIFO if there is data to be written. Each update pulse updates the DACs' output and loads the new value to each DAC. The minimum update cycle must be longer or equal to (0.5 µsec∗ the number of channels in Group 1).

If the FIFO is not used either the Counter 1 Interrupt or the External Update Interrupt can be used, depending on which update source is selected. The program steps are listed as follows:

1. Write a pattern to the CFG1 Register. The pattern should include:

    - a proper value in the CH<0..3> bit field to select channels to be written.
    - clearing or setting the EXTUPDEN bit to select the desired update source.

2. Write a pattern to the CFG2 Register. The pattern should include:

    - setting the corresponding LDAC*x* bits for the channels to be scanned.
    - setting or clearing corresponding DAC2S*x** bits for straight binary or two's complement format.

3. Set the SCANEN bit in the CFG3 Register.
4. Write the first data to the DACs.
5. Set the CNTINT1EN or the EXTUPDEN bit in the CFG1 Register depending on the update source signal selected.
6. Program the system interrupt controller and enable proper interrupt level.
7. If OUT1* is selected as the update signal:

    - write 0x34 to the CNTRCMD Register.
    - write the scan cycle period (low byte first, then high byte) in µsec to the CNTR1 Register.

    After writing the high byte the counter starts counting.

Each time an update signal updates the channels' output and causes an interrupt. The interrupt handler should write the new value to each DAC. To write a value to the DAC0, the GRP2WT bit in the CFG1 Register must be set.

Group 1 Scan Mode Using Retransmission Feature of FIFO

If the total number of words to be written to the DACs for waveform generation is less than the size of the FIFO (which is 1,024 words), the retransmission feature of the FIFO can be used to improve the performance. In this mode the data in the FIFO is written to the DACs repeatedly. In other words, when the last data in the FIFO is written out the writing pointer points to the beginning of the FIFO and the writing sequence continues. Therefore the FIFO has to load only once before the process starts. The Update signal works in the same way as other scan modes. The programming steps are listed as follows.

1. Write a pattern to the CFG1 Register. The pattern should include:
   - setting the FIFOEN bit
   - a proper value in the CH<0..3> bit field to select channels to be scanned
   - clearing the EXTUPDEN bit at this time
2. Write a pattern to the CFG2 Register. The pattern should include:
   - setting the corresponding LDAC*x* bits for the channels to be scanned.
   - setting or clearing corresponding DAC2S*x** bits for selecting straight binary or two's complement format.
3. Set the SCANEN bit in the CFG3 Register.
4. Read the FIFO Clear Register and ignore the result.
5. Write the data to the FIFO until all of the data is loaded into the FIFO.
6. Initialize the output channels by using Counter 1 to generate a single pulse to write the desired first data to the DACs. Thus the next update pulse will dump the proper output to the channels. To initialize the output channels, you must do the following:
   - write 0x18 to the CNTRCMD Register.
   - write 2 to the CNTR1 Register.
7. Set the FFRTEN bit in the CFG2 Register.
8. Set or clear the EXTUPDEN bit to select the update source signal.
9. If OUT1* is selected as the update signal:
   - write 0x34 to the CNTRCMD Register.
   - write the scan cycle period (low byte first, then high byte) in µsec to the CNTR1 Register.

After writing the high byte the counter starts counting.

Each update pulse updates the DACs' output and loads the new value to each DAC. The minimum update cycle is equal to (0.5 µsec∗ number of channels in Group 1). The process can be terminated by stopping the update signal or by clearing the FFRTEN or the FIFOEN bits.

Group 1 Single-Channel Mode Using DMA or Interrupt

If the SCANEN bit in the CFG3 Register is cleared, Group 1 is in the single-channel mode. In this mode only Channel (CH<3..0>) is used for waveform generation. If the FIFO is used, the data in the FIFO is only sent to channel (CH<3..0>), and the update signal only updates this channel (and the channel controlled by the same LDAC*x* bit). The rest of the channels in Group 1 are in the immediate update mode; that is, they are written by software and immediately updated. The programming steps are the same as those in the Scan Mode except the SCANEN bit in the CFG3 Register is cleared (that is, step 3 in the preceding programming sequence is not needed).

Group 2 Using Interrupt

The channels beyond CH<3..0>, if there are any left, make up Group 2. Group 2 does not use the FIFO and DMA operation. It can use either the Counter 2 Interrupt or the External Update Interrupt 2 to write values to the DACs and update the output channels. The Group 2 output channels are always updated together. The program steps are as follows:

1. Write a proper value to the CH<0..3> bit field of the CFG1 Register to group the DACs.

2. Write a pattern to the CFG2 Register. The pattern should include:

   • setting the corresponding LDAC*x* bits for the channels in Group 2 for waveform generation.

   • setting or clearing corresponding DAC2S*x** bits for straight binary or two's complement format.

3. Write the first data to the DACs.

4. Set the CNTINT2EN or the EXTINT2EN bit in the CFG1 Register depending on the update source signal selected.

5. Program the system interrupt controller, and enable the proper interrupt level.

6. If OUT2* is selected as the update signal:

   • write 0x74 to the CNTRCMD Register.

   • write the scan cycle period (low byte first, then high byte) in µsec to the CNTR2 Register.

   After writing the high byte the counter starts counting.

Each time an update signal updates the channel output and causes an interrupt. The interrupt handler should write the new value to each DAC.

Application Hints

If you want to use the external DAC update pin to generate an interrupt without updating the DACs, clear the EXTUPDEN bit in the CFG1 Register and set EXTINT1EN bit in the CFG1 Register. Now a falling edge at the EXTUPDATE* line will not update the DACs in Group 1, but an active low output signal from Counter 1 will. This interrupt procedure is possible only with Group 1.

Programming the Digital I/O Circuitry

The digital I/O circuitry is controlled and monitored using the DIN Register, the DOUT Register, and the two bits DOUTEN1 and DOUTEN2 in CFG3 Register. See the register bit descriptions earlier in this chapter for more information.

To enable digital output Port A, set the DOUTEN1 bit in the CFG3 Register. To enable digital output Port B, set the DOUTEN2 bit in the CFG3 Register. When a digital output port is enabled, the contents of the DOUT Register are driven onto the digital lines corresponding to that port. The digital output for both Port A and Port B is updated by writing the desired pattern to the DOUT Register.

For an external device to drive the digital I/O lines, the input ports must be enabled. Clear the DOUTEN1 bit in the CFG3 Register if an external device is driving digital I/O lines ADIO<3..0>. Clear the DOUTEN2 bit in the CFG3 Register if an external device is driving digital lines BDIO<3..0>. The DIN Register can then be read to monitor the state of the digital I/O lines as driven by the external device.

The logic state of all eight digital I/O lines can be read from the DIN Register. If the digital output ports are enabled, the DIN Register serves as a read-back register; that is, you can determine how the AT-AO-6/10 is driving the digital I/O lines by reading the DIN Register.

If any digital I/O line is not driven, it floats to an indeterminate value. If more than one device is driving any digital I/O line, the voltage at that line can also be indeterminate. In these cases, the digital line has no meaningful logic value, and reading the DIN Register can return either 1 or 0 for the state of the digital line. Upon start up both ports are enabled for input.

RTSI Bus Trigger Line Programming Considerations

The RTSI switch connects signals on the AT-AO-6/10 to the seven RTSI bus trigger lines. The RTSI switch has seven pins labeled A<6..0> connected to the AT-AO-6/10 signals and seven pins labeled B<6..0> connected to the seven RTSI bus trigger lines. Table 4-8 shows the signals connected to each pin.

Table 4-5. RTSI Switch Signal Connections

RTSI Switch Pin	Signal Name	Signal Direction	Connection on the RTSI Bus
A Side			
A0	OUT1*	Output	
A1	GATE3	Input	
A2	N/C	—	
A3	EXTUPD*	Output	
A4	OUT3*	Output	
A5	OUT2*	Output	
A6	EXTUPDATE*	Bidirectional	
B Side			
B0	TRIGGER0	Bidirectional	Pin 15
B1	TRIGGER1	Bidirectional	Pin 13
B2	TRIGGER2	Bidirectional	Pin 11
B3	TRIGGER3	Bidirectional	Pin 9
B4	TRIGGER4	Bidirectional	Pin 7
B5	TRIGGER5	Bidirectional	Pin 5
B6	TRIGGER6	Bidirectional	Pin 3

Programming the RTSI Switch

The RTSI switch can be programmed to connect any of the signals on the A side to any of the signals on the B side and vice versa. To make this connection, a 56-bit pattern is shifted into the RTSI switch by writing one bit at a time to the RTSI Switch Shift Register and then writing to the RTSI Switch Strobe Register to load the pattern into the RTSI switch.

The 56-bit pattern is made up of two 28-bit patterns, one for side A and one for side B of the RTSI switch. The low-order 28 bits select the signal sources for the B-side pins. The high-order 28 bits select the signal sources for the A-side pins. Each of the 28-bit patterns are made up of seven 4-bit fields, one for each pin. The 4-bit field selects the signal source and the output enable for the pin. Figure 4-1 shows the bit map of the RTSI switch 56-bit pattern.

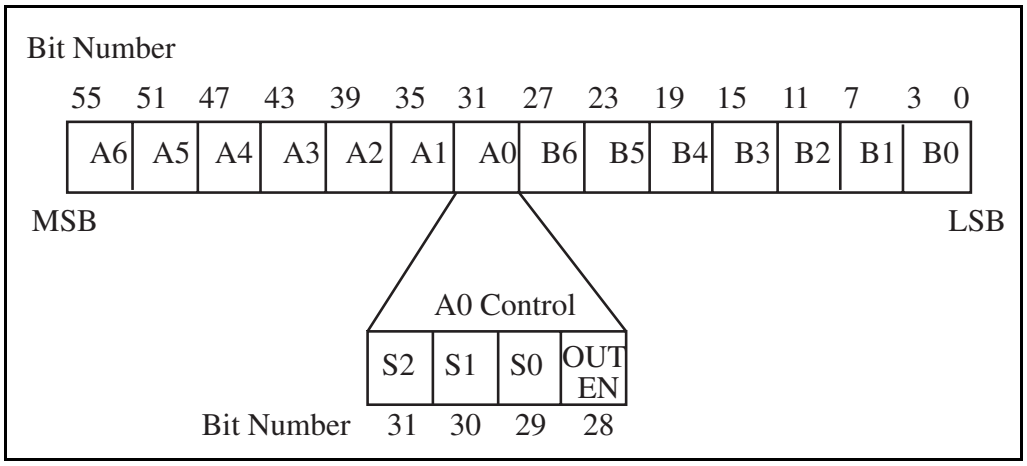


Figure 4-1. RTSI Switch Control Pattern

In Figure 4-1, the fields labeled A6 through A0 and B6 through B0 are the 4-bit control fields for each RTSI switch pin of the same name. The 4-bit control field for pin A0 is shown in Figure 4-1.

The bits labeled S2 through S0 are the signal source selection bits for the pin. One of seven source signals can be selected. Pins A6 through A0 can select any of the pins B6 through B0 as signal sources. Pins B6 through B0 select any of the pins A6 through A0 as signal sources. For example, the pattern 011 for S2 through S0 in the A1 control field selects the signal connected to pin B3 as the signal source for pin A1.

The bit labeled OUTEN is the output enable bit for that pin. If the OUTEN bit is set, the pin is driven by the selected source signal (the pin acts as an output pin). If the OUTEN bit is cleared, the pin is not driven regardless of the source signal selected; instead, the pin can be used as an input pin.

If the preceding A1 control field contains the pattern 0111, the signal connected to pin B3 (Trigger Line 3) appears at pin A1. On the AT-AO-6/10 board, this arrangement allows the GATE2* signal to be driven by Trigger Line 3. Conversely, if the B4 control field contains the pattern 1011, the signal connected to pin A5 appears at pin B4. With this arrangement, Trigger Line 4 can be driven by the AT-AO-6/10 OUT1* signal. In this way, boards connected via the RTSI bus can send signals to each other over the RTSI bus trigger lines.
To program the RTSI switch, complete these steps:

1. Calculate the 56-bit pattern based on the desired signal routing.

    a. Clear the OUTEN bit for all input pins and for all unused pins.

    b. Select the signal source pin for all output pins by setting bits S2 through S0 to the source pin number.

    c. Set the OUTEN bit for all output pins.

2. For $i = 0$ to 55, follow these steps:

   a. Copy bit i of the 56-bit pattern to bit 0 of an 8-bit temporary variable.

   b. Write the temporary variable to the RTSI Switch Shift Register (8-bit write).

3. Write 0 to the RTSI Switch Strobe Register (8-bit write). This operation loads the 56-bit pattern into the RTSI switch. At this point, the new signal routing goes into effect.

Step 2 can be completed by simply writing the low-order 8 bits of the 56-bit pattern to the RTSI Switch Shift Register, then shifting the 56-bit pattern right once, and repeating this two-step operation a total of 56 times. Only bit 0 of the word written to the RTSI Switch Shift Register is used. The higher-order bits are ignored.

Chapter 5
Calibration Procedures

This chapter discusses the calibration procedures for the AT-AO-6/10 analog output circuitry.

The AT-AO-6/10 is calibrated at the factory before shipment. An onboard EEPROM stores the calibration constants, which must be written to the 21 calibration DACs on the AT-AO-10, or 13 calibration DACs on the AT-AO-6, to be properly calibrated. To maintain the 12-bit accuracy of the AT-AO-6/10 analog output circuitry, periodic self-calibration is recommended. This self-calibration is performed under software control. Calibration constants are stored in an onboard EEPROM (see Figure 5-1). Calibration software is included with the board package as part of the utility application and utility library. Using the self-calibration feature eliminates most errors due to drift of offset and gain with time and temperature.

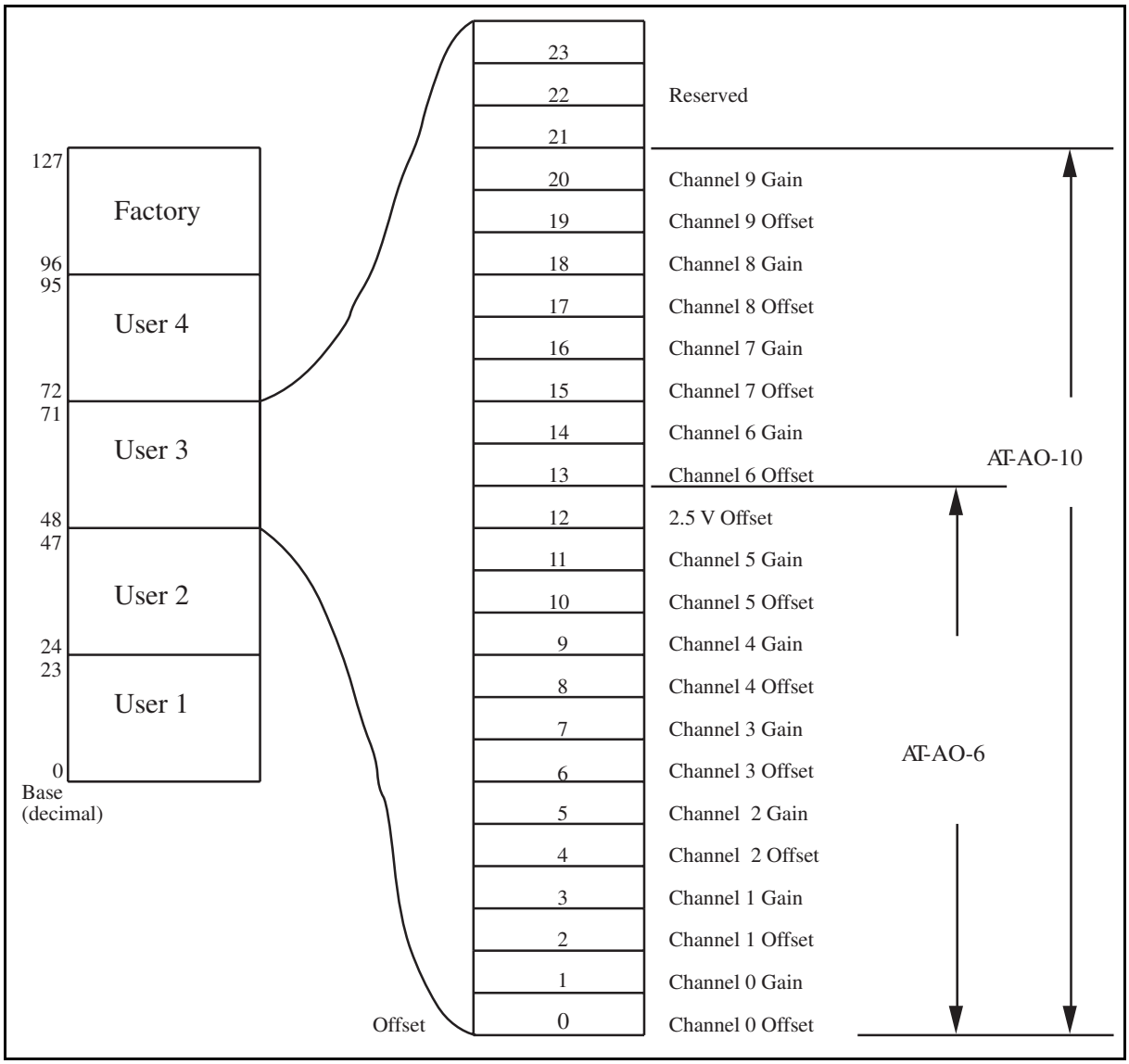


Figure 5-1. EEPROM Map

Factory calibration is valid with the analog outputs set up for a bipolar output range with the internal reference. If you want to use a different analog output configuration, it may be necessary to recalibrate the analog output offsets and gains.

Calibration DACs

There are 21 8-bit DACs on the AT-AO-10 and 13 8-bit DACs on the AT-AO-6 that are used for calibration. The AT-AO-6/10 is shipped fully calibrated. The factory-determined calibration values are stored in the location byte 96 through byte 116 of the EEPROM (see Figure 5-1), and a copy is stored the location word 0 through 20. Upon startup, the copied values are read and written to the corresponding calibration DAC by software. The user-determined calibration value can be stored in any portion of User 2 through User 4 of the EEPROM. The offset adjustment range for each channel is 200 mV in bipolar mode, and 100 mV in unipolar mode. The resolution is 8-bit, that is, the adjustment range divided by 128. The gain adjustment range is 0.5% of full

output scale for each channel. The resolution is 8-bit. Recalibration is seldom necessary. Making a recalibration every year or so is sufficient. The following sections describe the recommended calibration procedure, which requires a voltmeter with 0.005% resolution and accuracy.

Reference Calibration

The AT-AO-6/10 has built-in 5 V, 10 V, and 2.5 V references for the DACs. These references are stable with respect to time and temperature. The 5 V and 10 V references do not need to be calibrated and they are not available on the I/O connector. The 2.5 V reference is available on pin 38 when the 2.5 V OUT bit of the CFG3 Register is set. It is seldom necessary to calibrate the 2.5 V reference. Every one or two years should be sufficient.

To calibrate the 2.5 V reference signal:

1. If you have an AT-AO-10, ensure that channel 9 is in the bipolar mode.
2. Connect the positive probe of the voltmeter to the 2.5 V output on the connector (pin 38). Connect the negative probe of the voltmeter to the corresponding analog ground pin (pin 39).
3. Run the interactive calibration software for 2.5 V reference calibration. Follow the software prompt until the finishing of the calibration.

Analog Output Calibration

To null out error sources that affect the accuracy of the output voltages generated, the output calibration routine calibrates the analog output circuitry by adjusting the following potential sources of error:

- Analog output offset error
- Analog output gain error

Offset error in the analog output circuitry is the total of the voltage offsets contributed by each component in the circuitry. This error, which is independent of the DAC output voltage, appears as a voltage difference between the desired voltage and the actual output voltage generated. To correct this offset error, the routine writes a value of 0 to the 12-bit DAC under calibration and adjusts the value written to the corresponding 8-bit calibration DAC until the reading of the voltmeter is 0 volts. Then the result is stored in the proper location of the EEPROM.

Gain error in the analog output circuitry is the sum of the gain errors contributed by each component in the circuitry. This error also appears as a voltage difference between the desired voltage and the actual output voltage generated, but it is proportional to the DAC output voltage. To correct this gain error, the routine writes a full-scale positive value to the 12-bit DAC under calibration, and adjusts the value written to the corresponding 8-bit calibration DAC until the reading of full-scale voltage is reached on the voltmeter. The result is stored in the EEPROM by the routine. To perform the output calibration:

1. Connect the voltmeter to the desired DAC output between the VOUT pin and AGND pin.
2. Run the interactive calibration software. Follow the software prompt until the operation is finished.
3. Repeat steps 1 and 2 for each desired channel.

Appendix A
Specifications

This appendix lists the specifications of the AT-AO-6/10. These are typical at 25° C unless otherwise stated. The operating temperature range is 0° to 70° C.

Analog Output

Number of output channels	6 for the AT-AO-6 10 for the AT-AO-10
Type of DAC	12-bit, multiplying
Relative accuracy (nonlinearity)	0.015% of FSR maximum (±1.5 mV Unipolar, ±3 mV Bipolar) ±0.006% of FSR typical (±.6 mV Unipolar, ±1.2 mV Bipolar)
Differential nonlinearity	±1 LSB maximum (monotonic over temperature) ±0.2 LSB typical
Gain error	
Internal reference (includes adjustment range)	±1.0%, adjustable to < 0.005%
Temperature coefficient	±10 ppm/° C
External reference	±0.1%, not adjustable
Temperature coefficient	±5 ppm/° C
Voltage offset	±100 mV bipolar mode, adjustable to < ±0.5 mV
(includes adjustment range)	±50 mV unipolar mode, adjustable to < ±0.3 mV
Voltage Output	
Ranges	0 to 10 V, ±10 V 0 to V_{ref}, ±V_{ref}
*Current drive	±5 mA/ each V_{out} maximum
Output impedance	0.1 Ω maximum
Capacitive drive	500 pF maximum
Protection	Short circuit to ground
Settling time to 0.5 LSB	
20 V step	10 µsec
10 V step	5 µsec
1 V step	4 µsec
Slew rate	20 V/µsec minimum
Noise	1 mV rms, DC to 1 MHz
Current Output	
Type	4 to 20 mA sink to ground
Output resistance	1 GΩ minimum
Excitation voltage	+7 to +40 VDC (at connector pins)
Accuracy	±0.1% FSR

Slew rate	7.5 mA/µsec
Protection	Short circuit and open circuit
External reference input impedance	11 kΩ unipolar mode, 7 kΩ bipolar mode for each output channel
Transfer rate	
System memory to onboard FIFO	300 kwords to 500 kwords/sec maximum (system and software dependent)
FIFO to output channel(s)	1.6 Mwords/sec maximum

* Each channel can drive ±5 mA current maximum. But the total output power consumption is 200 mW. Thus, if all 10 channel outputs are 10 V, the maximum current output is 2 mA per channel.

Explanation of Analog Output Specifications

Relative accuracy in a D/A system is the same as nonlinearity because no uncertainty is added due to code width. Unlike an ADC, every digital code in a D/A system represents a specific analog value rather than a range of values. The relative accuracy of the system is therefore limited to the worst-case deviation from the ideal correspondence (a straight line), excepting noise. If a D/A system has been calibrated perfectly, then the relative accuracy specification reflects its worst-case absolute error.

Differential nonlinearity in a D/A system is a measure of deviation of code width from 1 LSB. In this case, code width is the difference between the analog values produced by consecutive digital codes. A specification of ±1 LSB differential nonlinearity ensures that the code width is always greater than 0 LSB (guaranteeing monotonicity) and is always less than 2 LSBs.

Digital I/O

Compatibility	TTL-compatible
Output current source capability	Can source 2.6 mA and maintain V_{OH} at 2.4 V
Output current sink capability	Can sink 24 mA and maintain V_{OL} at 0.5 V

Power Requirements (from PC AT I/O Channel)

AT-AO-6	
+5 VDC	0.6 A typical
+12 VDC	60 mA typical + load
-12 VDC	60 mA typical + load
AT-AO-10	
+5 VDC	1.6 A typical

Physical

Board dimensions	13.3 in. by 4.5 in.
I/O connector	50-pin male ribbon-cable connector

Operating Environment

Component temperature	0° to 70° C
Relative humidity	5% to 90% noncondensing

Storage Environment

Temperature	-55° to 150° C
Relative humidity	5% to 90% noncondensing

Appendix B
I/O Connector

This appendix shows the pinout and signal names for the AT-AO-6/10 50-pin I/O connector, including a description of each connection.

Figure B-1 shows the AT-AO-6/10 I/O connector.

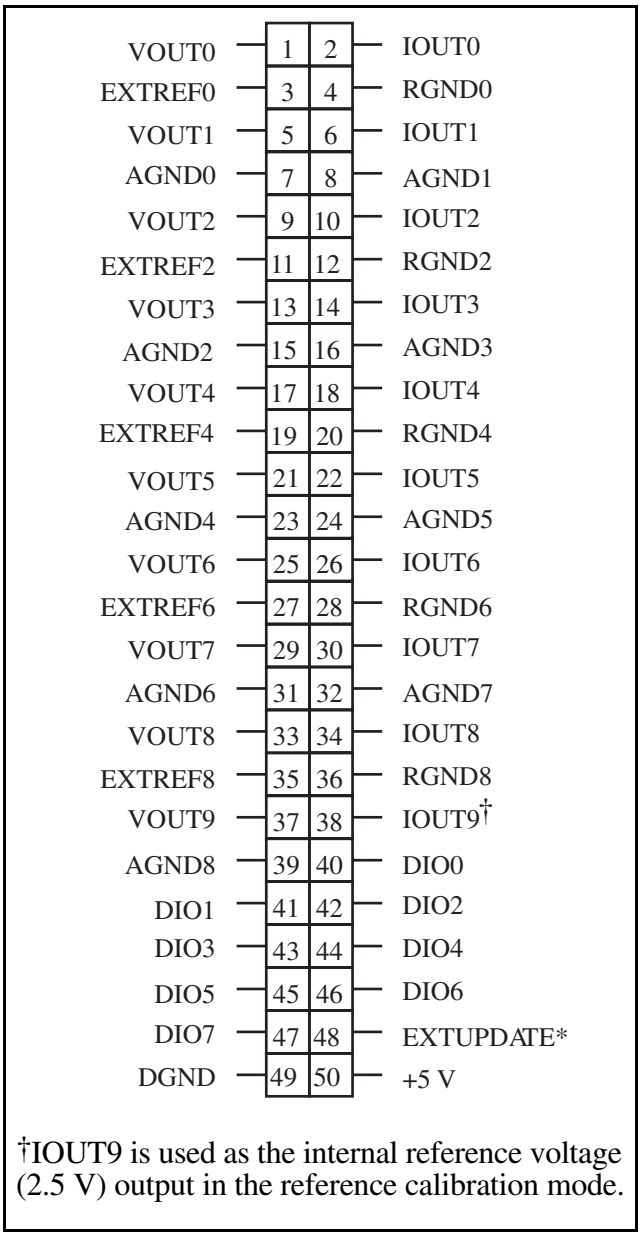


Figure B-1. AT-AO-6/10 I/O Connector

Signal Connection Descriptions

Pin	Signal Name	Description
1, 5, 9, 13, 17,21, 25, 29, 33, 37	VOUT0 through VOUT9	Analog voltage outputs of Channel 0 through Channel 9.
2, 6, 10, 14, 18, 22, 26, 30,34, 38	IOUT0 through IOUT9†	Analog current outputs of Channel 0 through Channel 9.
3, 11, 19, 27,35	EXTREF0 through EXTREF8	Analog external reference inputs for Channel 0 through Channel 9. Each external reference input signal is shared by two channels. Channel 0 and Channel 1 share EXTREF0, Channel 2 and Channel 3 share EXTREF2, etc.
4, 12, 20, 28, 36	RGND0 through RGND8	Analog external reference ground. Each of these five ground pins is the ground reference to the corresponding EXTREF*x* signal, where *x* refers to 0 through 8.
7, 8, 15, 16, 23, 24, 31, 32, 39	AGND0 through AGND8	Analog output ground for each channel. Channel 8 and Channel 9 share one ground pin, AGND8.
40, 41, 42, 43	ADIO0 through ADIO3	Digital I/O Port A signals.
44-47	BDIO0 through BDIO3	Digital I/O Port B signals.
48	EXTUPDATE*	External DAC Update. If selected, a high-to-low edge on EXTUPDATE* results in the selected outputs of DACs being updated with the value written to them.
49	DGND	Digital Ground. This pin supplies the reference for the digital signals at the I/O connector as well as the +5 VDC supply.
50	+5 V	+5 VDC Source. This pin is fused for up to 1 A of +5 V supply.

Appendix C
MSM82C53 Data Sheet*

This appendix contains the *MSM82C53 Programmable Interval Timer* (Oki Semiconductor) data sheet. This counter/timer is used on the AT-AO-6/10.

OKI semiconductor

MSM82C53-2RS/GS/JS

CMOS PROGRAMMABLE INTERVAL TIMER

GENERAL DESCRIPTION

The MSM82C53-2RS/GS/JS are programmable universal timers designed for use in microcomputer systems. Based on silicon gate CMOS technology, it requires a standby current of only 100μA (max.) when the chip is in the nonselected state. During timer operation, power consumption is still very low with only 8 mA (max.) at 8 MHz of current required.

The devices consist of three independent counters, and can count up to a maximum of 8 MHz (MSM82C53-2) The timer features six different counter modes, and binary count/BCD count functions. Count values can be set in byte or word units, and all functions are freely programmable.

FEATURES

- Maximum operating frequency of 8 MHz (MSM82C53-2)
- High speed and low power consumption achieved through silicon gate CMOS technology.
- Completely static operation
- Three independent 16-bit down-counters
- 3V to 6V single power supply
- Six counter modes available for each counter
- Binary and decimal counting possible
- 24 pin Plastic DIP (DIP24-P-600)
- 28 pin PLCC (QFJ28-P-S450)
- 32 pin-V Plastic SOP (SSOP32-P-430-VK)

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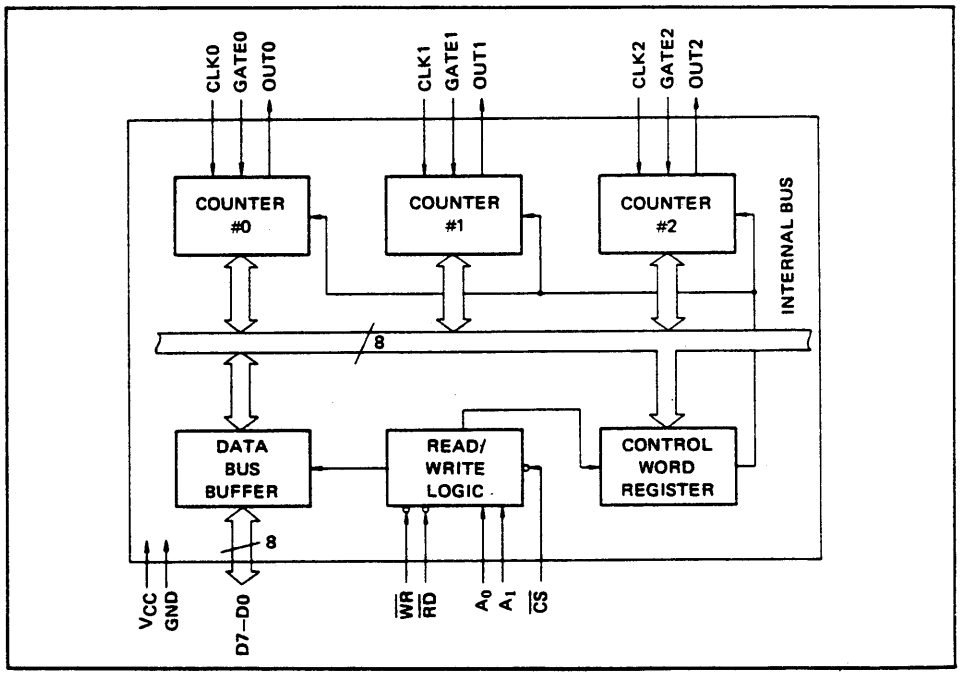
FUNCTIONAL BLOCK DIAGRAM



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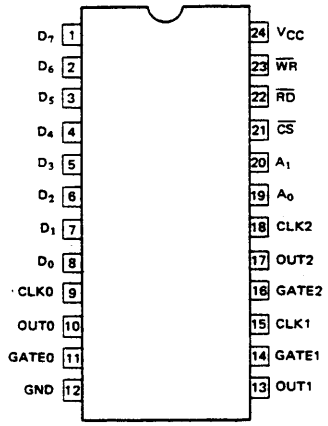
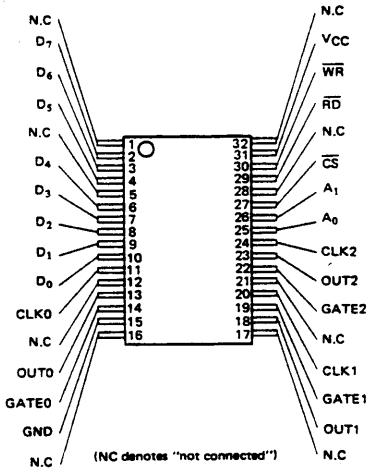
■ MSM82C53-2RS/GS/JS ■

PIN CONFIGURATION

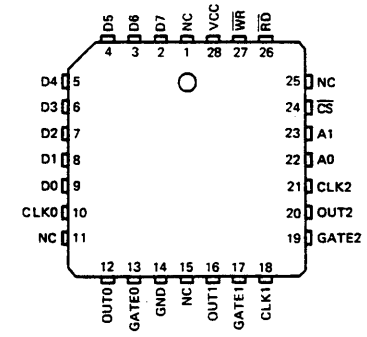
MSM82C53-2RS (Top View)
24 pin Plastic DIP



MSM82C53-2GS (Top View)
32 pin Plastic Small Outine Package



MSM82C53-2JS (Top View)
28 pin Plastic Leaded Chip Carrier



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■ I/O·MSM82C53-2RS/GS/JS ■

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Limits			Unit
			MSM82C53-2RS	MSM82C53-2GS	MSM82C53-2JS	
Ssupply Voltage	V_{CC}	Respect to GND	−0.5 to +7			V
Input Voltage	V_{IN}		−0.5 to V_{CC} + 0.5			V
Output Voltage	V_{OUT}		−0.5 to V_{CC} + 0.5			V
Storage Temperature	T_{stg}		−55 to +150			°C
Power Dissipation	P_D	Ta = 25°C	0.9	0.7	0.9	W

OPERATING RANGES

Parameter	Symbol	Limits	Conditions	Unit
Supply Voltage	V_{CC}	3 to 6	V_{IL} = 0.2V, V_{IH} = V_{CC} − 0.2V, operating frequency 2.6 MHz	V
Operating Temperature	T_{OP}	−40 to +85		°C

RECOMMENDED OPERATING CONDITIONS

5

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5	5.5	V
Operating Temperature	T_{OP}	−40	+25	+85	°C
"L" Input Voltage	V_{IL}	−0.3		+0.8	V
"H" Input Voltage	V_{IH}	2.2		V_{CC} + 0.3	V

DC CHARACTERISTICS

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
"L" Output Voltage	V_{OL}	I_{OL} = 4mA	V_{CC}=4.5V to 5.5V Ta=−40°C to +85°C			0.45	V
"H" Output Voltage	V_{OH}	I_{OH} = −1mA		3.7			V
Input Leak Current	I_{LI}	$0 \leq V_{IN} \leq V_{CC}$		−10		10	μA
Output Leak Current	I_{LO}	$0 \leq V_{OUT} \leq V_{CC}$		−10		10	μA
Standby Supply Current	I_{CCS}	$\overline{CS} \geq V_{CC}$ −0.2V $V_{IH} \geq V_{CC}$ − 0.2V $V_{IL} \leq$ 0.2V				100	μA
Operating Supply Current	I_{CC}	t_{CLK} = 125 ns C_L = 0pF				8	mA

AC CHARACTERISTICS

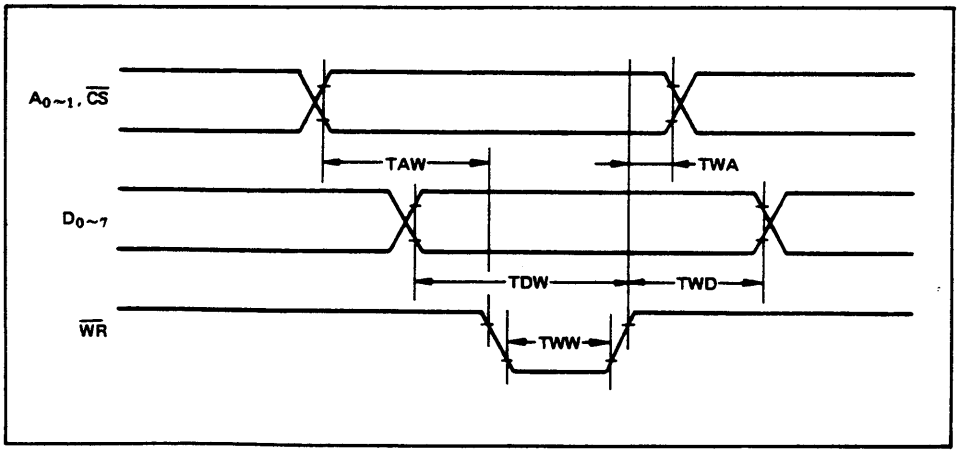
(V_{CC} = 4.5V ~ 5.5V, Ta = –40 ~ +85°C)

Parameter	Symbol	MSM82C53-2 Min.	MSM82C53-2 Max.	Unit	Conditions	
Address Set-up Time before reading	TAR	30		ns	Read cycle	C_L = 150pF
Address Hold Time after reading	TRA	0		ns		
Read Pulse Width	TRR	150		ns		
Read Recovery Time	TRVR	200		ns		
Address Set-up Time before writing	TAW	0		ns	Write cycle	
Address Hold Time after writing	TWA	20		ns		
Write Pulse Width	TWW	150		ns		
Data Input Set-up Time before writing	TDW	100		ns		
Data Input Hold Time after writing	TWD	20		ns		
Write Recovery time	TRVW	200		ns		
Clock Cycle Time	TCLK	125	D.C.	ns	Clock and gate timing	
Clock "H" Pulse Width	TPWH	60		ns		
Clock "L" Pulse Width	TPWL	60		ns		
"H" Gate Pulse Width	TGW	50		ns		
"L" Gate Pulse Width	TGL	50		ns		
Gate Input Set-up Time before clock	TGS	50		ns		
Gate Input Hold Time after clock	TGH	50		ns		
Output Delay Time after reading	TRD		120	ns	Delay time	
Output Floating Delay Time after reading	TDF	5	90	ns		
Output Delay Time after gate	TODG		120	ns		
Output Delay Time after clock	TOD		150	ns		
Output Delay Time after address	TAD		180	ns		

Note: Timing measured at V_L = 0.8V and V_H = 2.2V for both inputs and outputs.

TIME CHART

Write Timing



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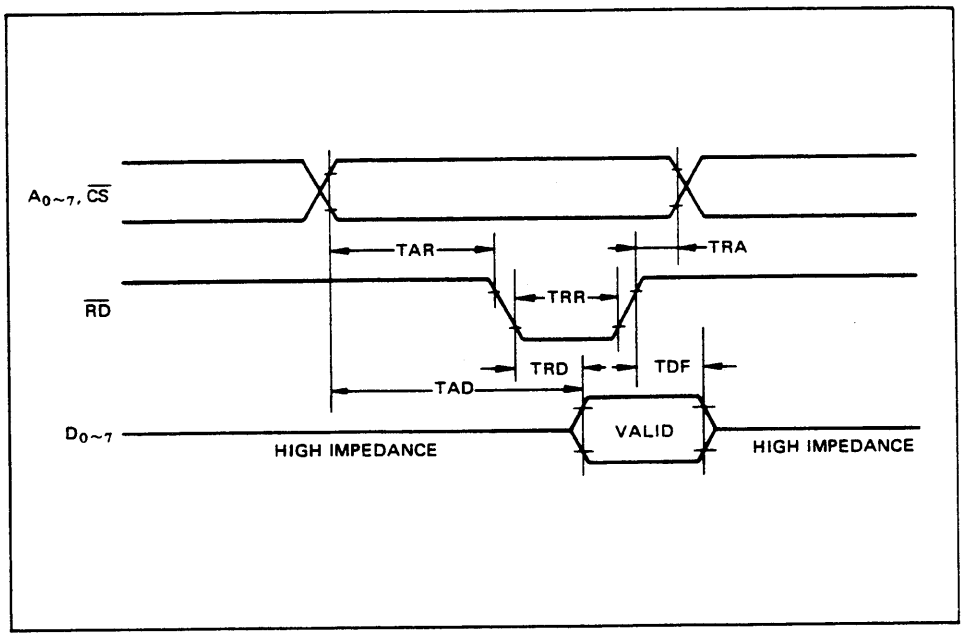
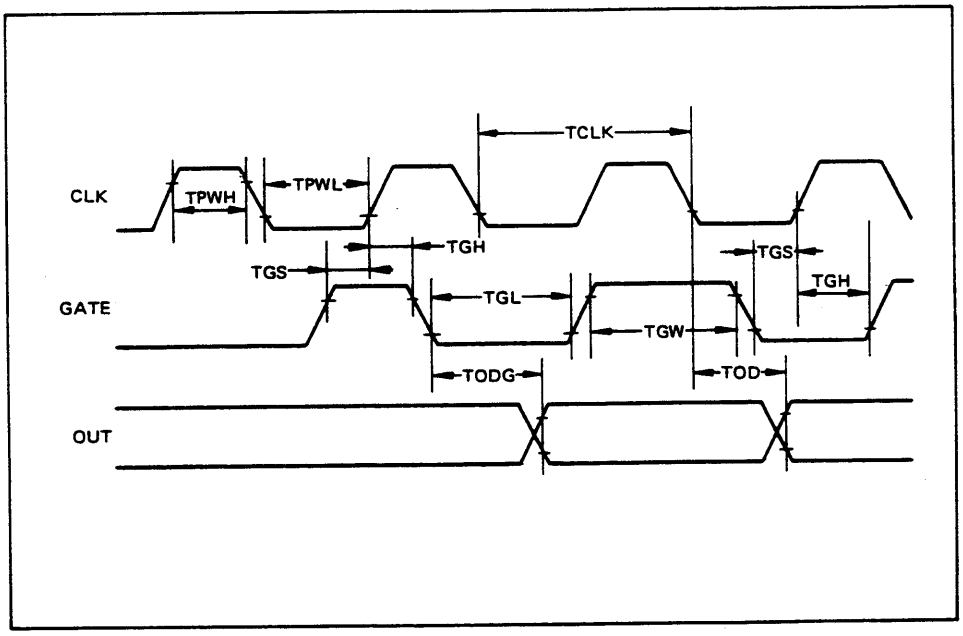
■ MSM82C53-2RS/GS/JS ■

Read Timing



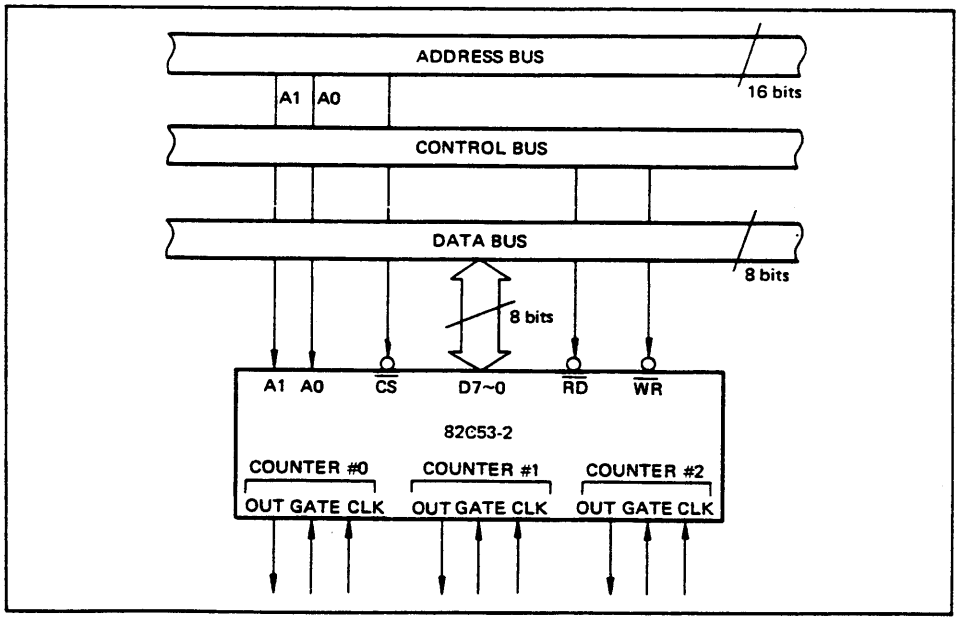
Clock & Gate Timing



DESCRIPTION OF PIN FUNCTIONS

Pin Symbol	Name	Input/output	Function
D7 ~ D0	Bidirectional data bus	Input/output	Three-state 8-bit bidirectional data bus used when writing control words and count values, and reading count values upon reception of $\overline{WR}$ and $\overline{RD}$ signals from CPU.
$\overline{CS}$	Chip select input	Input	Data transfer with the CPU is enabled when this pin is at low level. When at high level, the data bus (D_0 thru D_7) is switched to high impedance state where neither writing nor reading can be executed. Internal registers, however, remain unchanged.
$\overline{RD}$	Read input	Input	Data can be transferred from MSM82C53 to CPU when this pin is at low level.
$\overline{WR}$	Write input	Input	Data can be transferred from CPU to MSM82C53 when this pin is at low level.
A0, A1	Address input	Input	One of the three internal counters or the control word register is selected by A0/A1 combination. These two pins are normally connected to the two lower order bits of the address bus.
CLK0~2	Clock input	Input	Supply of three clock signals to the three counters incorporated in MSM82C53.
GATE0~2	Gate input	Input	Control of starting, interruption, and restarting of counting in the three respective counters in accordance to the set control word contents.
OUT0~2	Counter output	Output	Output of counter output waveform in accordance with the set mode and count value.

SYSTEM INTERFACING



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DESCRIPTION OF BASIC OPERATIONS

Data transfers between the internal registers and the external data bus is outlined in the following table.

$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	A1	A0	Function
0	1	0	0	0	Data bus to counter # 0 Writing
0	1	0	0	1	Data bus to counter # 1 Writing
0	1	0	1	0	Data bus to counter # 2 Writing
0	1	0	1	1	Data bus to control word register Writing
0	0	1	0	0	Data bus from counter # 0 Reading
0	0	1	0	1	Data bus from counter # 1 Reading
0	0	1	1	0	Data bus from counter # 2 Reading
0	0	1	1	1	Data bus in high impedance status
1	x	x	x	x	
0	1	1	x	x	

x denotes "not specified".

DESCRIPTION OF OPERATION

82C53 functions are selected by a control word from the CPU. In the required program sequence, the control word setting is followed by the count value setting and execution of the desired timer operation.

Control Word and Count Value Program

Each counter operation mode is set by control word programming. The control word format is outlined below.

D7	D6	D5	D4	D3	D2	D1	D0
SC1	SC0	RL1	RL0	M2	M1	M0	BCD
Select Counter		Read/Load		Mode			BCD

($\overline{CS}$ = 0, A0, A1 = 1,1, $\overline{RD}$ = 1, $\overline{WR}$ = 0)

- **Select Counter (SC0, SC1):** Selection of set counter

SC1	SC0	Set Contents
0	0	Counter # 0 selection
0	1	Counter # 1 selection
1	0	Counter # 2 selection
1	1	Illegal combination

- **Read/Load (RL1, RL0):** Count value Reading/Loading format setting

RL1	RL0	Set Contents
0	0	Counter Latch operation
0	1	Reading/Loading of Least Significant byte (LSB)
1	0	Reading/Loading of Most Significant byte (MSB)
1	1	Reading/Loading of LSB followed by MSB

- **Mode (M2, M1, M0):** Operation waveform mode setting

M2	M1	M0	Set Contents
0	0	0	Mode 0 (Interrupt on Terminal Count)
0	0	1	Mode 1 (Programmable One-Shot)
x	1	0	Mode 2 (Rate Generator)
x	1	1	Mode 3 (Square Wave Generator)
1	0	0	Mode 4 (Software Triggered Strobe)
1	0	1	Mode 5 (Hardware Triggered Strobe)

x denotes "not specified".

- **BCD:** Operation count mode setting

BCD	Set Contents
0	Binary Count (16-bits Binary)
1	BCD Count (4-decades Binary Coded Decimal)

After setting Read/Load, Mode, and BCD in each counter as outlined above, next set the desired count value. (In some Modes, counting is started immediately after the count value has been written). This count value setting must conform with the Read/Load format set in advance. Note that the internal counters are reset to OOOOH during control word setting. The counter value (OOOOH) can.t be read.

If the two bytes (LSB and MSB) are written at this stage (RL0 and RL1 = 1,1), take note of the following precaution.

Although the count values may be set in the three counters in any sequence after the control word has been set in each counter, count values must be set consecutively in the LSB – MSB order in any one counter.

- **Example of control word and count value setting**

  Counter # 0: Read/Load LSB only, Mode 3, Binary count, count value 3H
  Counter # 1: Read/Load MSB only, Mode 5, Binary count, count value AA00H
  Counter # 2: Read/Load LSB and MSB, Mode 0, BCD count, count value 1234

```
MVI A, 1EH
OUT n3      ] Counter #0 control word setting
MVI A, 6AH
OUT n3      ] Counter #1 control word setting
MVI A, B1H
OUT n3      ] Counter #2 control word setting
MVI A, 03H
OUT n0      ] Counter #0 count value setting
MVI A, AAH
OUT n1      ] Counter #1 count value setting
MVI A, 34H
OUT n2      ]
MVI A, 12H  ] Counter #2 count value setting
OUT n2      ] (LSB then MSB)
```

  Note: n0: Counter #0 address
  n1: Counter #1 address
  n2: Counter #2 address
  n3: Control word register address

- **The minimum and maximum count values which can be counted in each mode are listed below.**

Mode	Min.	Max.	Remarks
0	1	0	0 executes 10000H count (ditto in other modes)
1	1	0	
2	2	0	1 cannot be counted
3	2	1	1 executes 10001H count
4	1	0	
5	1	0	

Mode Definition

- **Mode 0 (terminal count)**

  The counter output is set to "L" level by the mode setting. If the count value is then written in the counter with the gate input at "H" level (that is, upon completion of writing the MSB when there are two bytes), the clock input counting is started. When the terminal count is reached, the output is switched to "H" level and is maintained in this status until the control word and count value are set again.

  Counting is interrupted if the gate input is switched to "L" level, and restarted when switched back to "H" level.

  When Count Values are written during counting, the operation is as follows:

  1 byte Read/Load.... When the new count value is written, counting is stopped immediately, and then restarted at the new count value by the next clock.

  2-byte Read/Load.... When byte 1 (LSB) of the new count value is written, counting is stopped immediately. Counting is restarted at the new count value when byte 2 (MSB) is written.

- **Mode 1 (programmable one-shot)**

  The counter output is switched to "H" level by the mode setting. Note that in this mode, counting is not started if only the count value is written. Since counting has to be started in this mode by using the leading edge of the gate input as a trigger, the counter output is switched to "L" level by the next clock after the gate input trigger. This "L" level status is maintained during the set count value, and is switched back to "H" level when the terminal count is reached.

  Once counting has been started, there is no interruption until the terminal count is reached, even if the gate input is switched to "L" level in the meantime. And although counting continues even if a new count value is written during the counting, counting is started at the new count value if another trigger is applied by the gate input.

- **Mode 2 (rate generator)**

  The counter output is switched to "H" level by the mode setting. When the gate input is at "H" level, counting is started by the next clock after the count value has been written. And if the gate input is at "L" level, counting is started by using the rising edge of the gate input as a trigger after the count value has been set.

  An "L" level output pulse appears at the counter output during a single clock duration once every n clock inputs where n is the set count value. If a new count value is written during while counting is in progress, counting is started at the new count value following output of the pulse currently being counted. And if the gate input is switched to "L" level during counting, the counter output is forced to switch to "H" level, the counting being restarted by the rising edge of the gate input.

- **Mode 3 (square waveform rate generator)**

  The counter output is switched to "H" level by the mode setting. Counting is started in the same way as described for mode 2 above.

  The repeated square wave output appearing at the counter output contains half the number of counts as the set count value. If the set count value (n) is an odd number, the repeated square wave output consists of only (n + 1)/2 clock inputs at "H" level and (n – 1)/2 clock inputs at "L" level.

  If a new count value is written during counting, the new count value is reflected immediately after the

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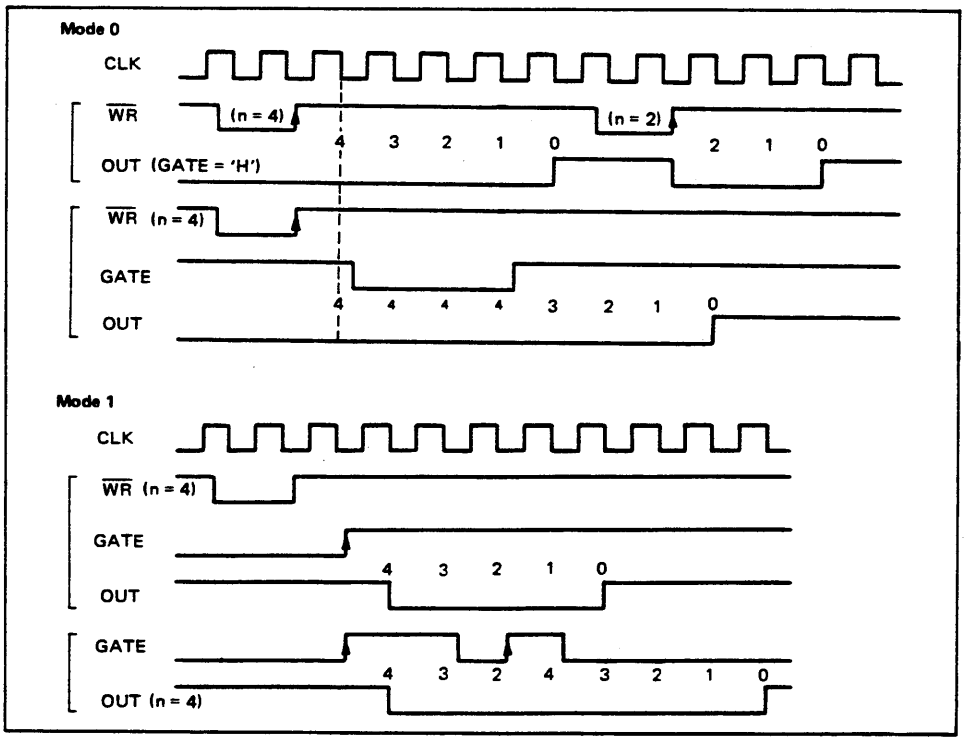
change ("H" to "L" or "L" to "H") in the next counter output to be executed. The counting operation at the gate input is done the same as in mode 2.

- **Mode 4 (software trigger strobe)**
  The counter output is switched to "H" level by the mode setting. Counting is started in the same way as described for mode 0. A single "L" pulse equivalent to one clock width is generated at the counter output when the terminal count is reached.
  This mode differs from 2 in that the "L" level output appears one clock earlier in mode 2, and that pulses are not repeated in mode 4. Counting is stopped when the gate input is switched to "L" level, and restarted from the set count value when switched back to "H" level.

- **Mode 5 (hardware trigger strobe)**
  The counter output is switched to "H" level by the mode setting. Counting is started, and the gate input used, in the same way as in mode 1.
  The counter output is identical to the mode 4 output.
  The various roles of the gate input signals in the above modes are summarized in the following table.

Mode \ Gate	"L" Level Falling Edge	Rising Edge	"H" Level
0	Counting not possible		Counting possible
1		(1) Start of counting (2) Retriggering	
2	(1) Counting not possible (2) Counter output forced to "H" level	Start of counting	Counting possible
3	(1) Counting not possible (2) Counter output forced to "H" level	Start of counting	Counting possible
4	Counting not possible		Counting possible
5		(1) Start of counting (2) Retriggering	



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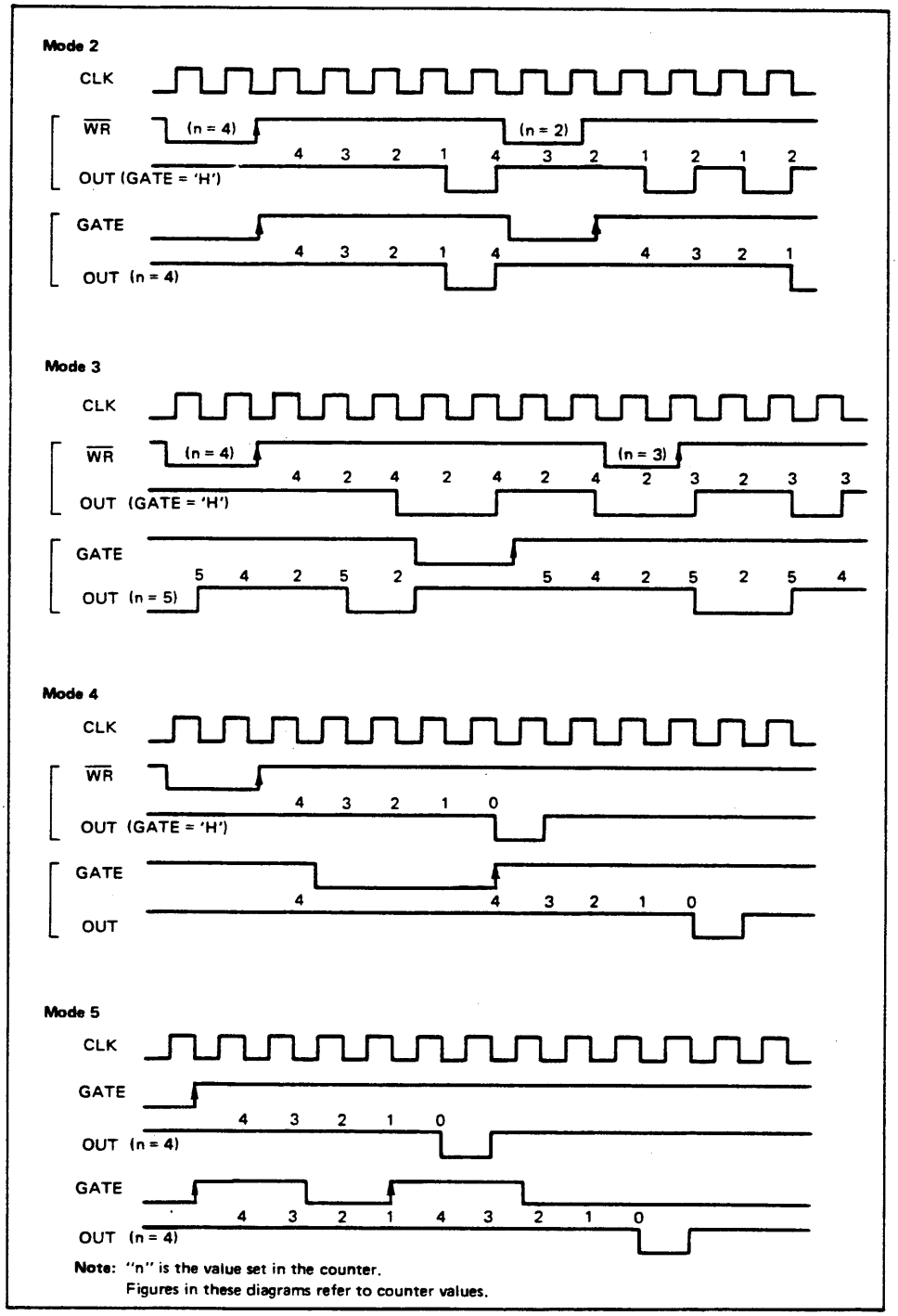

Note: "n" is the value set in the counter.
Figures in these diagrams refer to counter values.

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Reading of Counter Values

All 82C53 counting is down-counting, the counting being in steps of 2 in mode 3. Counter values can be read during counting by (1) direct reading, and (2) counter latching ("read on the fly").

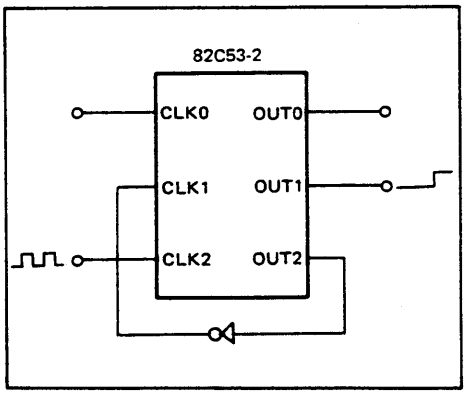
- **Direct reading**
  Counter values can be read by direct reading operations.
  Since the counter value read according to the timing of the $\overline{RD}$ and CLK signals is not guaranteed, it is necessary to stop the counting by a gate input signal, or to interrupt the clock input temporarily by an external circuit to ensure that the counter value is correctly read.

- **Counter latching**
  In this method, the counter value is latched by writing a counter latch command, thereby enabling a stable value to be read without effecting the counting in any way at all. An example of a counter latching program is given below.
  Counter latching executed for counter #1 (Read/Load 2-byte setting)

```
MVI A  01 00 x x x x
                └── Denotes counter latching
OUT n3 ──┬── Write in control word address (n3)
         └── The counter value at this point is latched
IN n1  ──┬── Reading of the LSB of the counter value latched from counter #1.
         └── n1: Counter #1 address
MOV B, A
IN n1      ── Reading of MSB from counter #1.
MOV C, A
```

Example of Practical Application

- 82C53 used as a 32-bit counter.



Use counter #1 and counter #2

Counter #1: mode 0, upper order 16-bit counter value

Counter #2: mode 2, lower order 16-bit counter value

This setting enables counting up to a maximum of 2^{32}.

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Appendix D
Customer Communication

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Computer brand _____ Model _____ Processor _____

Operating system _____

Speed _____MHz RAM _____M Display adapter _____

Mouse _____yes _____no Other adapters installed _____

Hard disk capacity _____M Brand _____

Instruments used _____

National Instruments hardware product model _____ Revision _____

Configuration _____

National Instruments software product _____ Version _____

Configuration _____

The problem is _____

_____

_____

_____

_____

List any error messages _____

_____

_____

_____

_____

The following steps will reproduce the problem _____

_____

_____

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Glossary

Prefix	Meaning	Value
p-	pico-	10^{-12}
n-	nano-	10^{-9}
µ-	micro-	10^{-6}
m-	milli-	10^{-3}
k-	kilo-	10^{3}
M-	mega-	10^{6}
G-	giga-	10^{9}

°	degrees
Ω	ohms
%	percent
A	amperes
AWG	American Wire Gauge
C	Celsius
CMOS	complementary metallic oxide semiconductor
D/A	digital-to-analog
DAC	digital-to-analog converter
DIP	dual inline package
DMA	direct memory access
EISA	Extended Industry Standard Architecture
F	farads
FIFO	first-in-first-out
FSR	Full-Scale Range
hex	hexadecimal
Hz	hertz
I/O	input/output
in.	inches
ksamples	1,000 samples
LSB	least significant bit
M	megabytes of memory
ppm	parts per million
rms	root mean square
RTSI	Real-Time System Integration
SCXI	signal conditioning eXtensions for instrumentation
sec	seconds
TTL	transistor-transistor logic
V	volts
V_{OH}	volts, output high
V_{OL}	volts, output low
V_{ref}	reference voltage
VDC	volts direct current

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