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***NI-5753***

# NI 5753

## 120 MS/s Adapter Module



**Note** Before you begin, complete the software and hardware installation instructions in the getting started guide for your FlexRIO FPGA module or Controller for FlexRIO.

The NI 5753 is a FlexRIO adapter module designed to work in conjunction with FlexRIO FPGA modules and Controllers for FlexRIO.

The NI 5753 is available in two variants, the -01 and the -02. The following table lists the key features of each variant.

NI 5753-01	NI 5753-02
Sixteen channels	Twelve channels
16-bit accuracy	16-bit accuracy
Sample rates up to 125 MS/s (default 120 MS/s)	Sample rates up to 125 MS/s (default 120 MS/s)
AC-coupled	DC-coupled
1.8 V <sub>pp</sub> (+9.1 dBm)	0.9 V <sub>pp</sub> (+3.2 dBm)

This document explains how to install and configure the NI 5753.

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# Electromagnetic Compatibility Guidelines

This product was tested and complies with the regulatory requirements and limits for electromagnetic compatibility (EMC) stated in the product specifications. These requirements and limits are designed to provide reasonable protection against harmful interference when the product is operated in the intended operational electromagnetic environment.

This product is intended for use in industrial locations. However, harmful interference may occur in some installations, when the product is connected to a peripheral device or test object, or if the product is used in residential or commercial areas. To minimize interference with radio and television reception and prevent unacceptable performance degradation, install and use this product in strict accordance with the instructions in the product documentation.

Furthermore, any modifications to the product not expressly approved by National Instruments could void your authority to operate it under your local regulatory rules.

 **Caution** To ensure the specified EMC performance, operate this product only with shielded cables and accessories.

 **Caution** To ensure the specified EMC performance, the length of all I/O cables must be no longer than 3 m (10 ft).

# FlexRIO Documentation

**Table 1.** FlexRIO Documentation Locations and Descriptions

Document	Location	Description
Getting started guide for your FlexRIO FPGA module or Controller for FlexRIO	Available from the Start menu and at <a href="https://ni.com/manuals">ni.com/manuals</a> .	Contains installation instructions for your FlexRIO system.
Specifications document for your FlexRIO FPGA module or Controller for FlexRIO	Available from the Start menu and at <a href="https://ni.com/manuals">ni.com/manuals</a> .	Contains specifications for your FlexRIO FPGA module or Controller for FlexRIO.

**Table 1. FlexRIO Documentation Locations and Descriptions (Continued)**

Document	Location	Description
Getting started guide for your adapter module	Available from the Start menu and at <a href="http://ni.com/manuals">ni.com/manuals</a> .	Contains signal information, examples, and CLIP details for your adapter module.
Specifications document for your adapter module	Available from the Start menu and at <a href="http://ni.com/manuals">ni.com/manuals</a> .	Contains specifications for your adapter module.
<i>LabVIEW FPGA Module Help</i>	Embedded in <i>LabVIEW Help</i> and at <a href="http://ni.com/manuals">ni.com/manuals</a> .	Contains information about the basic functionality of the LabVIEW FPGA Module.
<i>Real-Time Module Help</i>	Embedded in <i>LabVIEW Help</i> and at <a href="http://ni.com/manuals">ni.com/manuals</a> .	Contains information about real-time programming concepts, step-by-step instructions for using LabVIEW with the Real-Time Module, reference information about Real-Time Module VIs and functions, and information about LabVIEW features on real-time operating systems.
<i>FlexRIO Help</i>	Available from the Start menu and at <a href="http://ni.com/manuals">ni.com/manuals</a> .	Contains information about the FPGA module front panel connectors and I/O, controller for FlexRIO front panel connectors and I/O, programming instructions, and adapter module component-level IP (CLIP).
LabVIEW Examples	Available in NI Example Finder. In LabVIEW, click <b>Help»Find Examples»Hardware Input and Output»FlexRIO</b> .	Contains examples of how to run FPGA VIs and Host VIs on your device.
IPNet	Located at <a href="http://ni.com/ipnet">ni.com/ipnet</a> .	Contains LabVIEW FPGA functions and intellectual property to share.
FlexRIO product page	Located at <a href="http://ni.com/flexrio">ni.com/flexrio</a> .	Contains product information and data sheets for FlexRIO devices.

# FlexRIO Examples

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FlexRIO includes several example applications for LabVIEW. These examples serve as interactive tools, programming models, and as building blocks in your own applications.

## Accessing FlexRIO Examples

FlexRIO examples are available in LabVIEW's NI Example Finder. Complete the following steps to access the examples by task.

1. In LabVIEW, click **Help»Find Examples**.
2. In the **NI Example Finder** window that appears, click **Hardware Input and Output»FlexRIO**.

The examples are sorted by task. Click on an example and refer to the **Information** window for a description of the example. Refer the **Requirements** window for a list of hardware devices that can run the example.

You can also click the Search tab to search all installed examples by keyword. For example, search for `FlexRIO` to locate all FlexRIO examples.

Examples also are available online that demonstrate FlexRIO basics, such as using DRAM, acquiring data from adapter modules, and performing high throughput streaming. Refer to [ni.com/examples](http://ni.com/examples) for these examples and for more information.

## Verifying the System Requirements

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To use the NI 5753, your system must meet certain requirements. For more information about minimum system requirements, recommended system, and supported application development environments (ADEs), refer to the readme, which is available on the software media or online at [ni.com/updates](http://ni.com/updates).

## Unpacking

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**Caution** To prevent ESD from damaging the devices, ground yourself using a grounding strap or by holding a grounded object, such as your computer chassis.

1. Touch the antistatic package to a metal part of the computer chassis.
2. Remove each module from the package and inspect it for loose components or any other sign of damage.



**Caution** Never touch the exposed pins of connectors.



**Note** Do not install a device if it appears damaged in any way.

3. Unpack any other items and documentation from the kit.

Store the devices in the antistatic package when they are not in use.

# Preparing the Environment

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Ensure that the environment you are using the NI 5753 in meets the following specifications.

Operating temperature (IEC 60068-2-1, IEC 60068-2-2)	0 °C to 55 °C
Operating humidity (IEC 60068-2-56)	10% to 90% RH, noncondensing
Pollution Degree	2
Maximum altitude	2,000 m at 25 °C ambient temperature

Indoor use only.



**Note** Refer to the *NI 5753 Specifications* at [ni.com/manuals](http://ni.com/manuals) for complete specifications.



**Caution** Clean the hardware with a soft, nonmetallic brush. Make sure that the hardware is completely dry and free from contaminants before returning it to service.

## Installing the NI 5753

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Refer to the getting started guide for your FlexRIO FPGA module or Controller for FlexRIO for instructions about how to install your FlexRIO system, including the NI 5753.

## Confirming that Measurement & Automation Explorer (MAX) Recognizes the Device

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Use Measurement & Automation Explorer (MAX) to configure your NI hardware. MAX informs other programs about which devices reside in the system and how they are configured. MAX is automatically installed with FlexRIO Support.

1. Launch MAX by navigating to **Start»All Programs»National Instruments»NI MAX** or by clicking the NI MAX desktop icon.
2. In the Configuration pane, double-click **Devices and Interfaces** to see the list of installed devices. Installed devices appear under the name of their associated chassis.
3. (PXI and PXI Express devices only) Expand your **Chassis** tree item. MAX lists all devices installed in the chassis. Your default device names may vary.



**Note** If you do not see your hardware listed, press <F5> to refresh the list of installed devices. If the device is still not listed, power off the system, ensure the device is correctly installed, and restart.

4. (Controllers for FlexRIO only) Your device appears under the **Remote Devices** section.

# Connecting Cables to the NI 5753

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1. Use any shielded 50  $\Omega$  SMA cable to connect signals to the CLK IN connector on the front panel of your NI 5753.
2. Use the SHH19-H19-AUX cable (NI part number: 152629-01 or 152629-02) to connect to the digital I/O (DIO) and programmable function interface (PFI) signals on the AUX I/O connector. NI recommends using the SCB-19 connector block to access the DIO and PFI signals.
3. Use an MCX connector to connect signals to the analog input connector on the front panel. You can connect each channel with an individual cable, or you can use the ganged, 16-channel, male MCX to female SMA cable (part number 785244-01).

## Accessories

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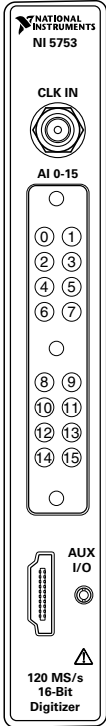
The NI 5753 can be used with the SCB-19 shielded desktop connector block.

Refer to the *SCB-19 User Guide* for information about how to connect and use the SCB-19 with the AUX I/O front panel connector on your NI 5753.

## Front Panel and Connector Pinouts

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The following figure shows the front panel connectors for the NI 5753.

Device Front Panel	Connector	Signal Description
 <p>The diagram shows the front panel of the NI 5753 module. At the top is the 'CLK IN' connector, a circular BNC-style port. Below it are 16 analog input channels labeled 'AI 0-15', arranged in two columns of eight, each with a small circular indicator. At the bottom is the 'AUX I/O' connector, a multi-pin D-sub connector. Below the connectors, there is a warning triangle icon and the text '120 MS/s 16-Bit Digitizer'.</p>	CLK IN	Sample Clock input
	AI 0-15	Analog input channels. AI 0-15 are accessible on the NI 5753-01 variant only. The NI 5753-02 variant can access AI 0-11.
	AUX I/O	Digital I/O and PFI connector



**Caution** To avoid permanent damage to the NI 5753, disconnect all signals connected to the NI 5753 before powering down the module, and connect signals only after the adapter module has been powered on by the FlexRIO FPGA module or Controller for FlexRIO.

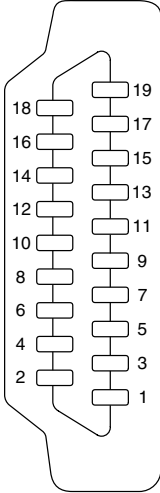


**Caution** Connections that exceed any of the maximum ratings of any connector on the NI 5753 can damage the device and the chassis. NI is not liable for any damage resulting from such connections.



# AUX I/O Connector

**Table 2.** NI 5753 AUX I/O Connector Pin Assignments

AUX I/O Connector	Pin	Signal	Signal Description
	1	DIO Port 0 (0)	Bidirectional single-ended (SE) digital I/O (DIO) data channel.
	2	GND	Ground reference for signals.
	3	DIO Port 0 (1)	Bidirectional SE DIO data channel.
	4	DIO Port 0 (2)	Bidirectional SE DIO data channel.
	5	GND	Ground reference for signals.
	6	DIO Port 0 (3)	Bidirectional SE DIO data channel.
	7	DIO Port 1 (0)	Bidirectional SE DIO data channel.
	8	GND	Ground reference for signals.
	9	DIO Port 1 (1)	Bidirectional SE DIO data channel.
	10	DIO Port 1 (2)	Bidirectional SE DIO data channel.
	11	GND	Ground reference for signals.
	12	DIO Port 1 (3)	Bidirectional SE DIO data channel.
	13	PFI 0	Bidirectional SE DIO data channel.
	14	NC	No connect.
	15	PFI 1	Bidirectional SE DIO data channel.
	16	PFI 2	Bidirectional SE DIO data channel.
	17	GND	Ground reference for signals.
	18	+5 V	+5 V power (10 mA maximum).
	19	PFI 3	Bidirectional SE DIO data channel.

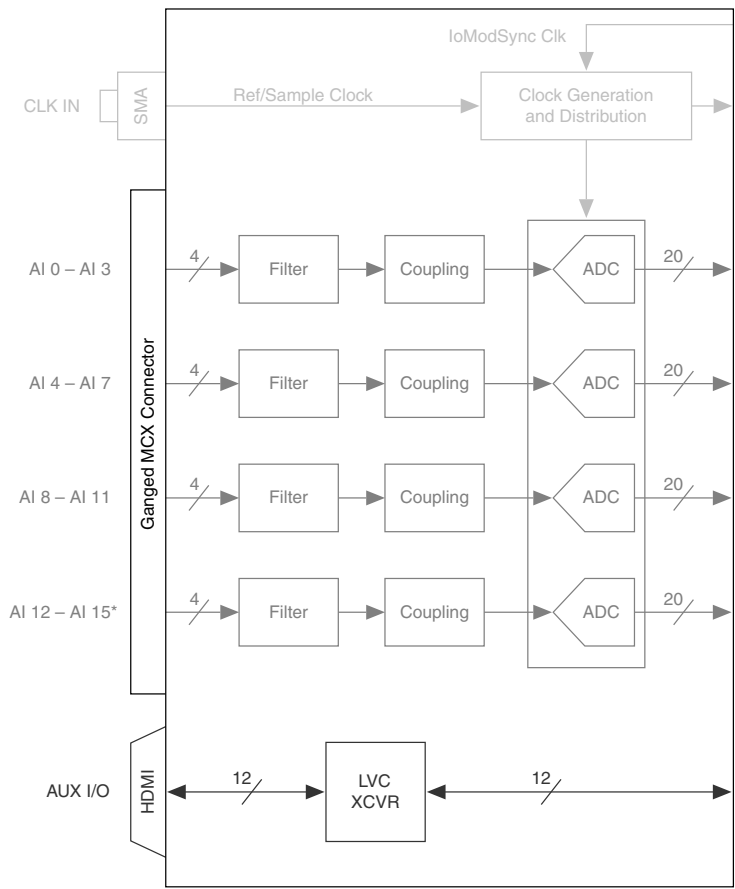


**Caution** The AUX I/O connector accepts a standard, third-party HDMI cable, but the AUX I/O port is not an HDMI interface. Do not connect the AUX I/O port on the NI 5753 to the HDMI port of another device. NI is not liable for any damage resulting from such signal connections.

# Block Diagram

The following figure shows the NI 5753 block diagram and signal flow.

**Figure 1. NI 5753 Block Diagram**



\* The AI 12 - AI 15 channels are unpopulated on the NI 5753-02 variant.

# Component-Level Intellectual Property (CLIP)

The LabVIEW FPGA Module includes component-level intellectual property (CLIP) for HDL IP integration. FlexRIO devices support two types of CLIP: user-defined and socketed.

- *User-defined CLIP* allows you to insert HDL IP into an FPGA target, enabling VHDL code to communicate directly with an FPGA VI.
- *Socketed CLIP* provides the same IP integration of the user-defined CLIP, but it also allows the CLIP to communicate directly with circuitry external to the FPGA. Adapter module socketed CLIP allows your IP to communicate directly with both the FPGA VI and the external adapter module connector interface.

The FlexRIO adapter module ships with socketed CLIP items that add module I/O to the LabVIEW project.

## NI 5753 AC-Coupled CLIP

The NI 5753 AC-coupled CLIP provides access to sixteen AC-coupled 16-bit 120 MS/s analog input channels, eight bidirectional DIO channels, and four bidirectional PFI channels. It also provides a User Command Interface to send raw SPI and I<sup>2</sup>C accesses to the adapter module for low-level configuration, and to select the clock modes:

- Internal Sample Clock (free-running)
- Internal Sample Clock locked to an external Reference Clock through the CLK/REF IN front panel connector
- Internal Sample Clock locked to an external Reference Clock through IoModSyncClock
- 70 MHz to 125 MHz external Sample Clock through the CLK/REF IN front panel connector
- 70 MHz to 125 MHz external Sample Clock through IoModSyncClock

In the LabVIEW FPGA Module, 16-bit analog input data is accessed using an I16 data type. The DIO signals are grouped into two ports of four signals each and are accessed using a U8 data type and a Boolean write enable signal. The four PFI signals are accessed individually using Boolean signals.

### Related Information

[Refer to the FlexRIO Help for more information about FlexRIO CLIP items, how to configure the NI 5753 with a socketed CLIP, and for a list of available socketed CLIP signals.](#)

## NI 5753 DC-Coupled CLIP

The NI 5753 DC-coupled CLIP provides access to twelve DC-coupled 16-bit 120 MS/s analog input channels, eight bidirectional DIO channels, and four bidirectional PFI channels. This module also contains a set of digital-to-analog converters (DACs) to trim larger DC offset errors induced by the coupling amplifier and system DC mismatch. This CLIP also provides a

User Command Interface to send raw SPI and I<sup>2</sup>C accesses to the adapter module for low-level configuration, and to select the clock modes:

- Internal Sample Clock (free-running)
- Internal Sample Clock locked to an external Reference Clock through the CLK/REF IN front panel connector
- Internal Sample Clock locked to an external Reference Clock through IoModSyncClock
- 70 MHz to 125 MHz external Sample Clock through the CLK/REF IN front panel connector
- 70 MHz to 125 MHz external Sample Clock through IoModSyncClock

In the LabVIEW FPGA Module, 16-bit analog input data is accessed using an I16 data type. The DIO signals are grouped into two ports of four signals each and are accessed using a U8 data type and a Boolean write enable signal. The four PFI signals are accessed individually using Boolean signals.

**Related Information**

*Refer to the [FlexRIO Help](#) for more information about FlexRIO CLIP items, how to configure the NI 5753 with a socketed CLIP, and for a list of available socketed CLIP signals.*

# Clocking

The NI 5753 clock source controls the sample rate and other timing functions on the device. The following table contains information about the possible NI 5753 clock sources.

Clock Source	Frequency	Description
Internal Sample Clock	120 MHz	The internal Sample Clock is free-running.
Internal Sample Clock locked to an external Reference Clock through the CLK/REF IN front panel connector	10 MHz	The internal Sample Clock can be locked to an external Reference Clock through the CLK/REF IN front panel connector.
Internal Sample Clock locked to an external Reference Clock through IoModSyncClock	10 MHz	The internal Sample Clock can be locked to an external Reference Clock through the IoModSyncClock signal.

Clock Source	Frequency	Description
External Sample Clock through the CLK/REF IN front panel connector	70 MHz to 125 MHz	An external Sample Clock can be provided from the CLK/REF IN front panel connector.
External Sample Clock through IoModSyncClock	70 MHz to 125 MHz	An external Sample Clock can be provided from the IoModSyncClock signal via the DSTARA line.

### Related Information

*Refer to the [FlexRIO Help](#) for more information about the NI 5753 clocks.*

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The NI website is your complete resource for technical support. At [ni.com/support](http://ni.com/support), you have access to everything from troubleshooting and application development self-help resources to email and phone assistance from NI Application Engineers.

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## Where to Go Next

Refer to the following figure for information about other product tasks and associated resources for those tasks.

▶ Located at [ni.com/gettingstarted](http://ni.com/gettingstarted)

🌐 Located at [ni.com/manuals](http://ni.com/manuals)

💻 Available from the Start menu

## EXPLORE

the application development environment (ADE) for your application.



🌐 Getting Started with LabVIEW

🌐 LabVIEW FPGA Module Help

## LEARN

about hardware features or review device specifications.



🌐 NI 5753 Specifications\*

💻 FlexRIO Module Development Kit User Manual

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custom applications within an application programming interface (API).



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\*This item is also installed with the driver software.

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