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NI 5761R User Guide and Specifications

The NI 5761 is a 250 MS/s analog input adapter module designed to work in conjunction with your NI FlexRIO™ FPGA module. This document contains signal information and specifications for the NI 5761R, which is comprised of an NI FlexRIO FPGA module and the NI 5761. This document also contains tutorial sections that demonstrate how to acquire data using a LabVIEW FPGA example VI and how to create and run your own LabVIEW project with the NI 5761R.

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Note Before configuring your NI 5761R, you must install the appropriate software and hardware. Refer to the *NI FlexRIO FPGA Module Installation Guide and Specifications* for installation instructions. Figure 1 shows an example of a properly connected NI FlexRIO device.

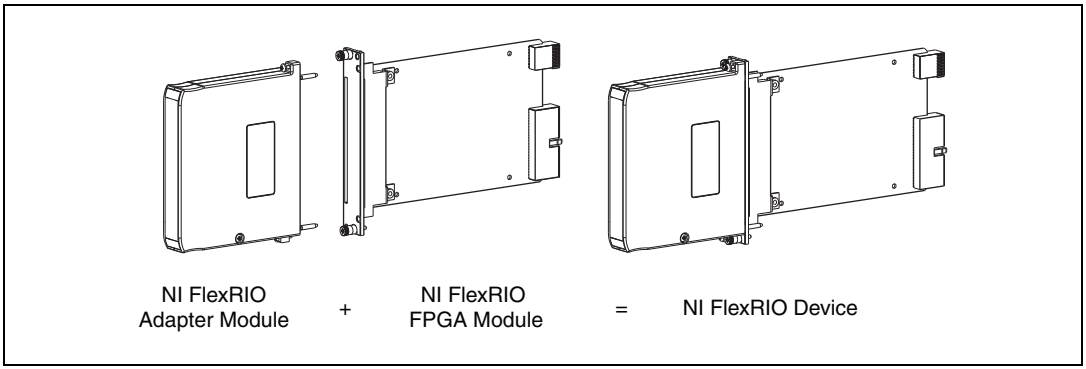


Figure 1. NI FlexRIO Device

NATIONAL INSTRUMENTS

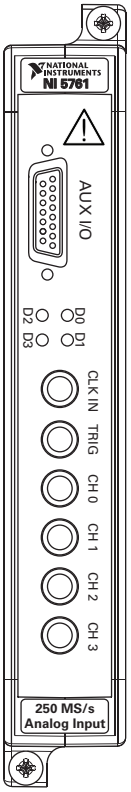
Front Panel and Connector Pinouts

Front Panel

Table 1 shows the front panel connector and signal descriptions for the NI 5761. Refer to the *Specifications* section of this document for additional signal information.

Caution To avoid permanent damage to the NI 5761, disconnect all signals connected to the NI 5761 before powering down the module, and only connect signals after the adapter module has been powered on by the NI FlexRIO FPGA module.

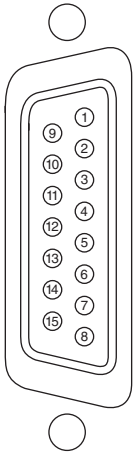
Table 1. NI 5761 Front Panel Connectors

Device Front Panel	Connector	Signal Description
	AUX I/O	Refer to Table 2 for the signal names and descriptions.
	D<0..3>	LEDs for custom configuration.
	CLK IN	Provides the NI 5761 with an external Sample clock or Reference clock.
	TRIG	Trigger input channel.
	CH 0	Analog input channels <0..3>.
	CH 1	
	CH 2	
	CH 3	

AUX I/O Connector

Table 2 shows the pins assignments for the AUX I/O connector on the NI 5761.

Table 2. NI 5761 AUX I/O Connector Pin Assignments

Micro-D Connector	Pin	Signal	Signal Description
	1	AUXIO0	General-purpose digital input or output channels.
	2	AUXIO1	
	3	AUXIO2	
	4	AUXIO3	
	5	AUXIO4	
	6	AUXIO5	
	7	AUXIO6	
	8	AUXIO7	
	9	GND	Ground.
	10	GND	
	11	GND	
	12	GND	
	13	GND	
	14	GND	
	15	GND	

Caution Connections that exceed any of the maximum ratings of any connector on the NI 5761R can damage the device and the chassis. NI is *not* liable for any damage resulting from such signal connections. For the maximum input and output ratings for each signal, refer to the *Specifications* section of this document.

Block Diagram

Figure 2 shows the NI 5761 block diagram and signal flow to and from the NI 5761 component-level intellectual property (CLIP) by way of the adapter module and the corresponding NI 5761 CLIP in LabVIEW FPGA.

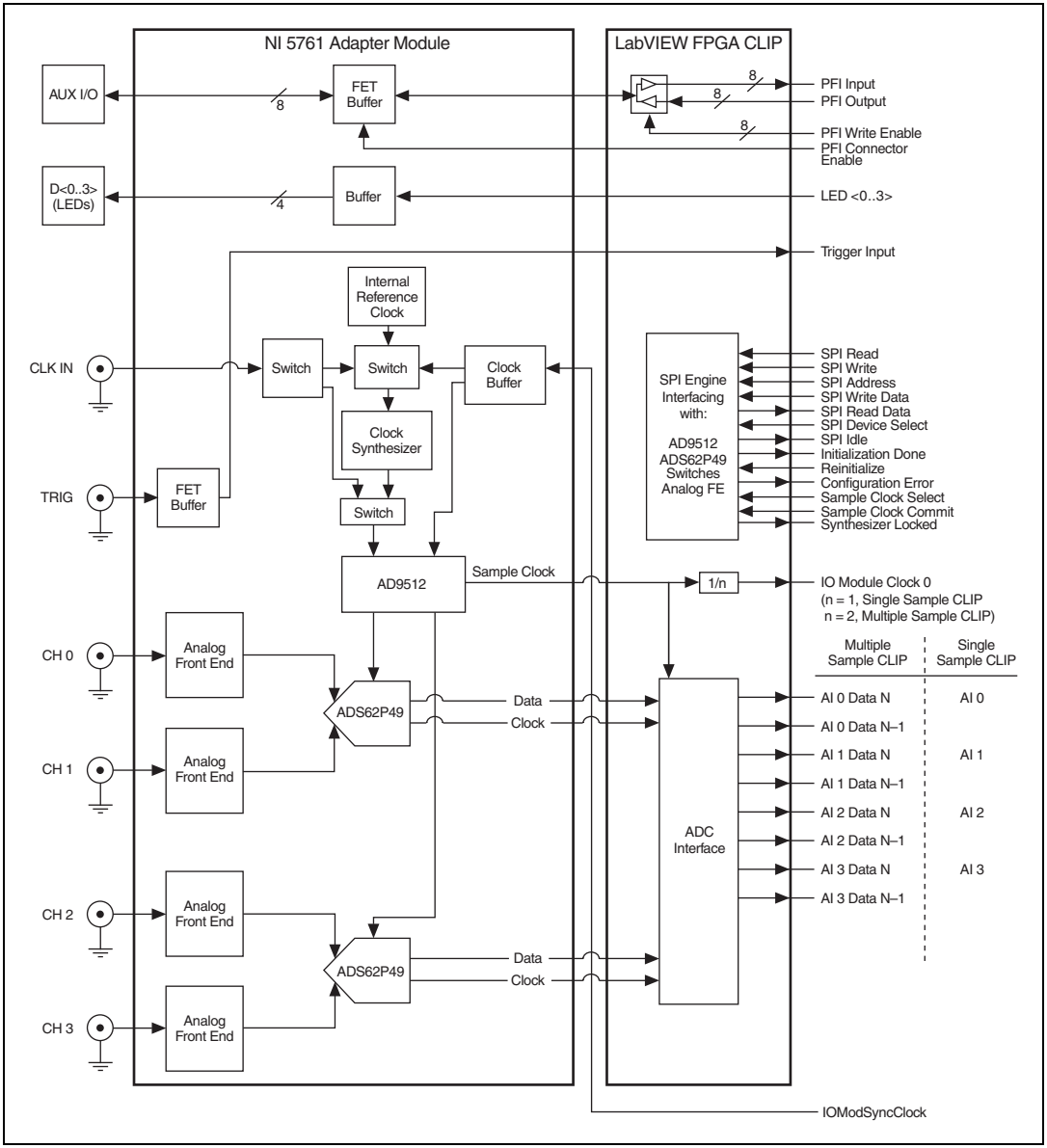


Figure 2. NI 5761 Connector Signals and NI 5761 CLIP Signal Block Diagram

NI 5761 Component-Level Intellectual Property (CLIP)

The LabVIEW FPGA Module includes a feature for HDL IP integration called CLIP. NI FlexRIO devices support two types of CLIP: user-defined and socketed.

- *User-defined CLIP* allows users to insert HDL IP into an FPGA target, enabling VHDL code to communicate directly with an FPGA VI.
- *Socketed CLIP* provides the same IP integration functionality of the user-defined CLIP, but also allows the CLIP to communicate directly with circuitry external to the FPGA. Adapter module socketed CLIP allows your IP to communicate directly with both the FPGA VI and the external adapter module connector interface.

Figure 3 shows the relationship between an FPGA VI and CLIP.

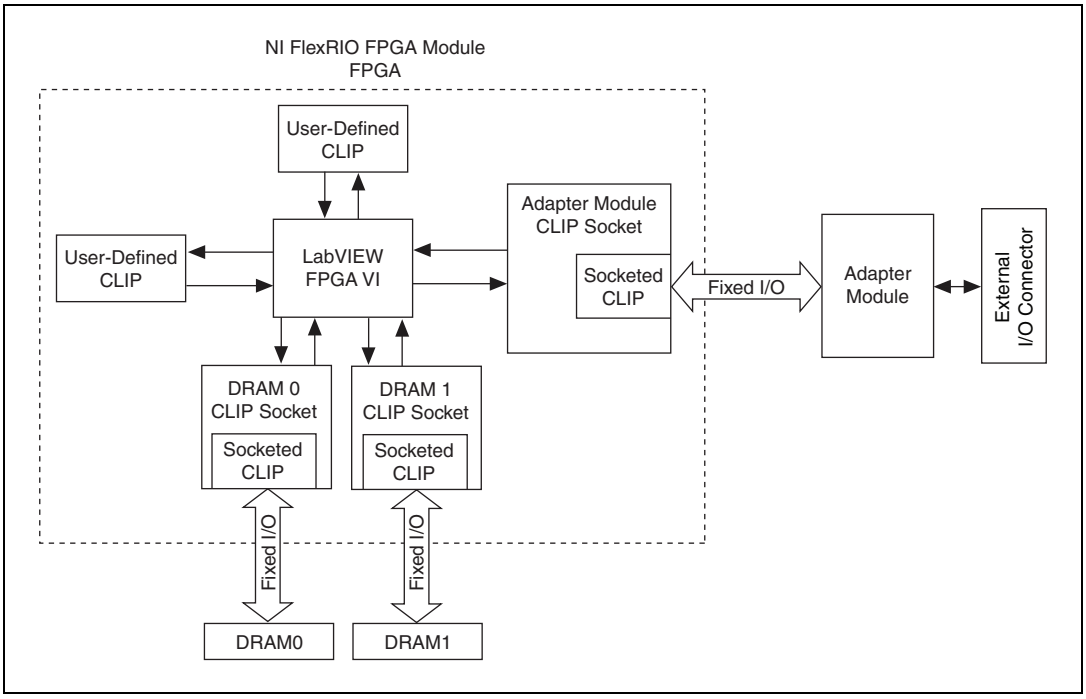


Figure 3. CLIP Relationship

The NI 5761 ships with socketed CLIP items that are used to add module I/O to the LabVIEW project. The NI 5761 ships with the following CLIP items:

- **NI 5761 Multiple Sample CLIP**—Generates two samples per clock cycle at a clock rate that is half the sample rate. The default sample rate is 250 MHz, which sets the default clock rate for this CLIP at 125 MHz. You can set a lower sample rate by using an external Sample clock. This CLIP provides access to four analog input channels, eight PFI lines, and an input clock selector that can be configured to use one of the following settings:
  - Internal Sample clock
  - Internal Sample clock locked to an external Reference clock through the CLK IN connector
  - External Sample clock through the CLK IN connector
  - Internal Sample clock locked to an external Reference clock through IoModSyncClock
  - External Sample clock through IoModSyncClock

This CLIP also contains an engine to program the CLK chip and ADCs, either through predetermined settings for an easier instrument setup or through a raw SPI address and data signals for a more advanced setup. The NI 5761 Multiple Sample CLIP is the default CLIP.

- **NI 5761 Single Sample CLIP**—Generates one sample per clock cycle at a default sample rate of 250 MHz. You can set a lower sample rate by using an external Sample clock. This CLIP provides access to four analog input channels, eight PFI lines, and an input clock selector that can be configured to use one of the following settings:
  - Internal Sample clock
  - Internal Sample clock locked to an external Reference clock through the CLK IN connector
  - External Sample clock through the CLK IN connector
  - Internal Sample clock locked to an external Reference clock through IoModSyncClock
  - External Sample clock through IoModSyncClock

This CLIP also contains an engine to program the CLK chip and ADCs, either through predetermined settings for an easier instrument setup or through a raw SPI address and data signals for a more advanced setup.

Refer to the *NI FlexRIO Help* in the *LabVIEW Help* for more information about NI FlexRIO CLIP items, configuring the NI 5761 with a socketed CLIP, and a list of available socketed CLIP and provided signals.

Cables

Use the NI CMD-to-CMD cable (NI part number 763194-01) or the NI CMD Single-ended to Pigtail cable (NI part number 763191-01) to connect signals to your AUX I/O connector. Use any 50 Ω SMA cable to connect signals to the other connectors on the front panel of your NI 5761. For more information about connecting I/O signals on your device, refer to the *Specifications* section of this document.

Clocking

The NI 5761 clocks control the sample rate and other timing functions on the device. Table 3 contains information about the possible NI 5761 clock resources.

Table 3. NI 5761 Clock Sources

Clock	Frequency	Source Options
Sample Clock	175 MHz to 250 MHz	• Internal VCO locked to a Reference clock • External through the CLK IN connector • External through IoModSyncClock
Reference Clock	10 MHz	• Internal • External through the CLK IN connector • External through IoModSyncClock

Using Your NI 5761R with a LabVIEW FPGA Example VI

The NI FlexRIO Adapter Module Support software includes a variety of example projects to help get you started creating your LabVIEW FPGA program. This section explains how to use an existing LabVIEW FPGA example project to generate and acquire samples with the NI 5761R. This example requires at least one SMA cable for connecting signals to your NI 5761R.

Note Examples available for your device are dependent on the device-specific minimum software requirements. For more information about software requirements for your device, visit `ni.com/info` and enter `rdsoftwareversion` as the Info Code to determine which minimum software versions you need for your device.

Each NI 5761R example project includes the following components:

- A LabVIEW FPGA VI that can be compiled and run embedded in FPGA hardware
- A VI that runs in LabVIEW for Windows and interacts with the LabVIEW FPGA VI

Note In NI application software, NI FlexRIO adapter modules are referred to as *IO Modules*.

Complete the following steps to run an example that acquires a waveform on CH 0 of the NI 5761.

1. Connect one end of an SMA cable to CH 0 on the front panel of the NI 5761 and the other end of the cable to your device under test (DUT).
2. Launch LabVIEW.
3. In the **Getting Started** window, click **Find Examples** to display the NI Example Finder.
4. In the **NI Example Finder** window, select **Hardware Input and Output»FlexRIO»IO Modules» NI 5761**.
5. Select **NI 5761 - Getting Started.lvproj**.
6. In the **Project Explorer** window, open **NI 5761 - Getting Started (Host).vi** under **My Computer**. The host VI opens. This VI uses the NI 7952R as the FPGA target by default. If you are using an NI FlexRIO FPGA module other than the NI 7952R, complete the following steps to change to an FPGA VI that supports your target.
   a. Select **Window»Show Block Diagram** to open the VI block diagram.
   b. On the block diagram, right-click the Open FPGA VI Reference (PXI-7952R) function and select **Configure Open FPGA VI Reference**.

c. In the **Configure Open FPGA VI Reference** dialog box, click the **Browse Project** button in the Open VI section.

d. In the **Select VI** dialog box that opens, expand the tree view for your device, select the VI under your device and click **OK**.

e. Click **OK** in the **Configure Open FPGA VI Reference** dialog box.

f. Save the VI.

7. On the front panel, in the **RIO Resource** box, select an NI 5761R resource that corresponds with the target configured in step 6.
8. Select **AI 0** in the **AI Channel** box.
9. Set the **Trigger Level (V)** and the **Record Size** controls to the desired value.
10. In the **Trigger Type** box, you can select either **Software Trigger** or **Data Edge**. If you select **Software Trigger**, the VI acquires data every time you click the **Software Trigger** button on the front panel of the VI. If you select **Data Edge**, the VI acquires data every time an edge occurs.
11. Click the **Run** button to run the VI.
12. Click the **Software Trigger** button if you selected **Software Trigger** in the **Trigger Type** box. The VI acquires data and displays the captured waveform on the **Acquired Waveform** graph as shown in Figure 4.
13. Click **STOP** to stop the VI.
14. Close the VI.

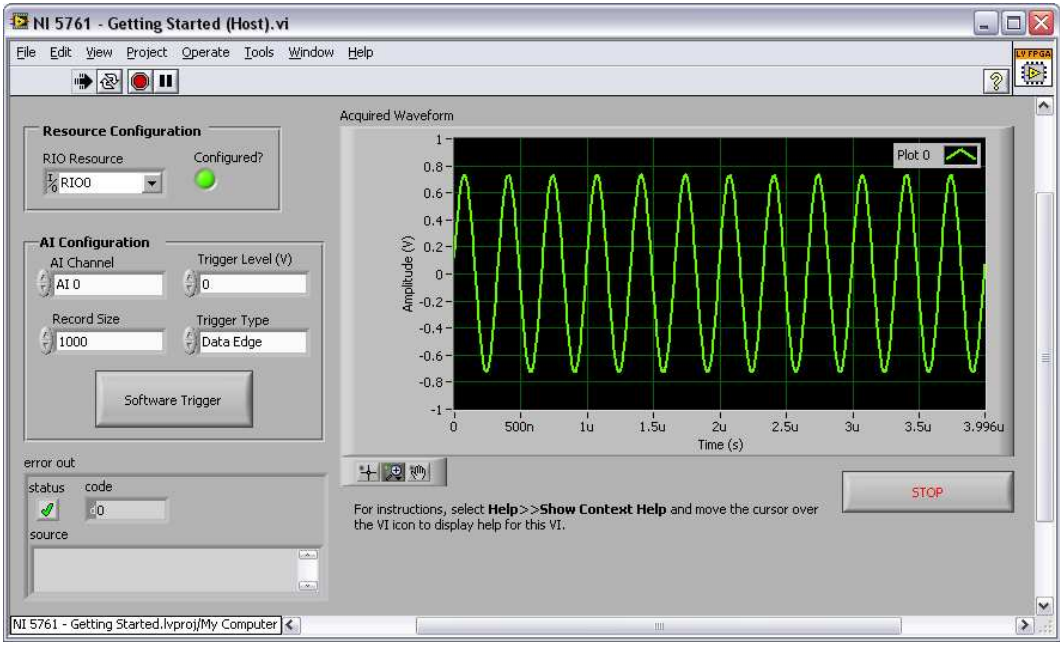


Figure 4. NI 5761 - Getting Started (Host) VI Front Panel

Creating a LabVIEW Project and Run a VI on an FPGA Target

This section explains how to setup your target and create an FPGA VI and host VI for data communication. For more detailed information about acquiring data on your NI 5761R, refer to the example VIs available on your NI FlexRIO Adapter Module Support software.

Creating a Project

1. Launch LabVIEW, or if LabVIEW is already running, select **File»New**.
2. In the **New** dialog box, select **Project»Empty Project**. Click **OK**. The new project opens in the **Project Explorer** window.
3. Save the project as `5761SampleAcq.lvproj`.

Creating an FPGA Target VI

1. In the **Project Explorer** window, right-click **My Computer** and select **New»Targets and Devices**.
2. In the **Add Targets and Devices on My Computer** dialog box, select the **Existing Target or Device** option button and expand the FPGA Target. The target is displayed.
3. Select your device and click **OK**. The target and target properties are loaded into the project tree.
4. In the **Project Explorer** window, expand **FPGA Target (RIO*x*, PXI-79*xx*R)**.
5. Right-click the FPGA target and select **New»FPGA Base Clock**.
6. In the **Resource** pull-down menu, select **IO Module Clock 0**.
7. Enter `125 MHz` in the **Compile for single frequency** control. Click **OK**.
8. Right-click the FPGA target and select **New»FPGA Base Clock** again.
9. In the **Resource** pull-down menu, select **200 MHz Clock**. Click **OK**.
10. Right-click **IO Module** and select **Properties**. In the General category, you can see the available CLIP for the NI 5761 in the Component Level IP pane. If the category information is dimmed, select the **Enable IO Module** checkbox.
11. Select **NI 5761 Multi Sample CLIP**.
12. In the Clock Selections category, select **200 MHz Clock** from the pull-down menu for **Clk200**. Leave **Clk40** configured as the **Top-Level Clock**. This step is necessary to compile the FPGA Target VI correctly. Click **OK**.

Note Configuring these clocks is required for proper CLIP operation. Refer to the NI 5761 CLIP topics in the *NI FlexRIO Help* for more information about configuring your clocks.

13. In the **Project Explorer** window, right-click the FPGA target and select **New»VI**. A blank VI opens.
14. Select **Window»Show Block Diagram** to open the VI block diagram.
15. In the **Project Explorer** window, expand the **IO Module (NI 5761 : NI 5761)** tree view.
16. Select **AI 0 Data N** and **AI 0 Data N-1** and drag them onto the block diagram.
17. Add a Timed Loop around the two nodes.
18. Wire an indicator to the output terminals of the **IO Module\AI 0 Data N** and **IO Module\AI 0 Data N-1** nodes.
19. Wire an **FPGA Clock Constant** to the input node of the Timed Loop. Set this constant to **IO Module Clock 0**.

Your block diagram should now resemble the block diagram in Figure 5.

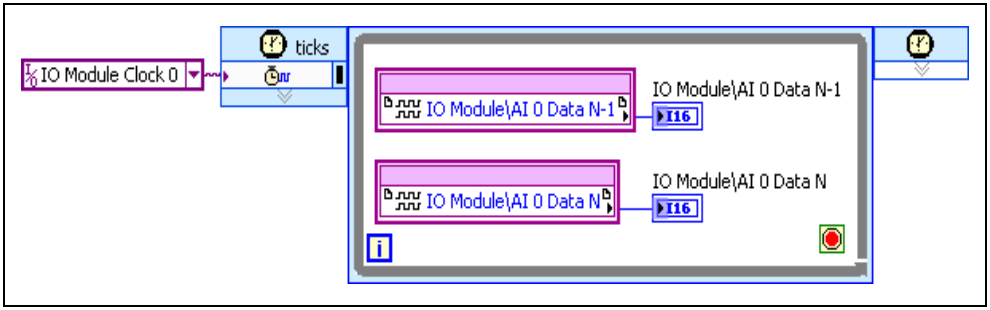


Figure 5. 5761SampleAcq (FPGA).vi Block Diagram

Tip Click the **Clean Up Diagram** button on the toolbar to cleanly organize the VI block diagrams.

20. Save the VI as `5761SampleAcq (FPGA).vi`.
21. Close the VI.
22. In the Project Explorer window under **My Computer**, expand the tree view for your device, right-click **5761SampleAcq (FPGA).vi** and select **Compile** to compile the files for your target.

    The **Generating Intermediate Files** window opens and displays the compilation progress. The **LabVIEW FPGA Compile Server** window opens and runs. The compilation takes several minutes.
23. When the compilation completes, click the **Stop Server** button.
24. Click **Close** in the **Successful Compile Report** window.
25. Save and close the VI.
26. Save the project.

Creating a Host VI

1. In the **Project Explorer** window, right-click **My Computer** and select **New»VI**. A blank VI opens. Select **Window»Show Block Diagram** to open the VI block diagram.
2. Add the Open FPGA VI Reference function, located on the **FPGA Interface** palette, to the block diagram.
3. Right-click the Open FPGA VI Reference function, labeled `No Target`, and select **Configure Open FPGA VI Reference**.
4. In the **Configure Open FPGA VI Reference** dialog box, select the **VI** option button.
5. In the **Select VI** window that opens, select **5761SampleAcq (FPGA).vi** under your device, and click **OK**.
6. Click **OK** in the **Configure Open FPGA VI Reference** dialog box. The new target name appears under the Open FPGA VI Reference function in the block diagram.
7. Add a While Loop to the block diagram.
8. Right-click the stop condition inside the While Loop and select **Create Control** to create a STOP control on the VI front panel.
9. Add the Read/Write Control function, located on the **FPGA Interface** palette, inside the While Loop.
10. Wire the **FPGA VI Reference Out** indicator of the Open FPGA VI Reference function to the **FPGA VI Reference In** control on the Read/Write Control function.

11. Wire the **error out** indicator of the Open FPGA VI Reference function to the **error in** control of the Read/Write Control function.
12. Configure the Read/Write Control function by clicking the terminal section labeled `Unselected`, and selecting **IO Module/AI 0 Data N**.
13. Add the **IO Module/AI 0 Data N-1** I/O item to the Read/Write Control function by clicking the lower edge of the control node with the Positioning tool and dragging the edge down.
14. Wire an indicator to the output terminal of the IO Module\AI 0 Data N node.
15. Wire an Indicator from the output terminal of the IO Module\AI 0 Data N-1 node.
16. Add the Close FPGA VI Reference function, located on the **FPGA Interface** palette, to the right of the While Loop on the block diagram.
17. Wire the **FPGA VI Reference Out** indicator of the Read/Write Control function to the **FPGA VI Reference In** control of the Close FPGA VI Reference function.
18. Wire the **error out** indicator of the Read/Write Control function to the **error in** control of the Close FPGA VI Reference function.

    Your block diagram should now resemble the block diagram in Figure 6.

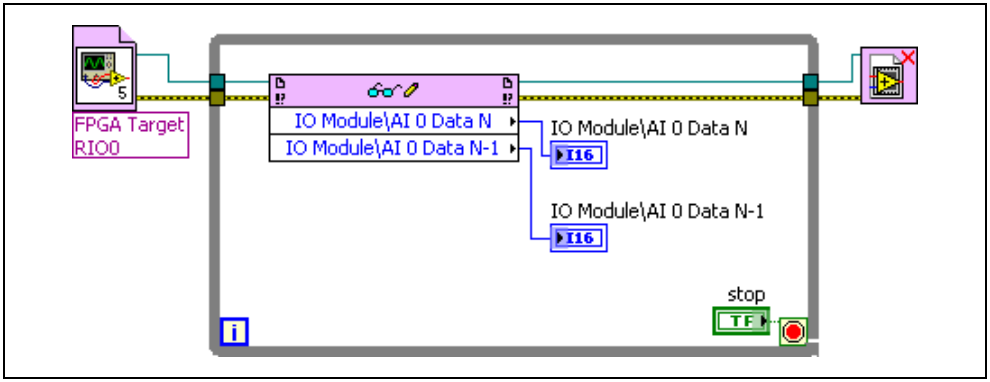


Figure 6. 5761SampleAcq(Host).vi Block Diagram

19. Save the VI as `5761SampleAcq(Host).vi`.

Running the Host VI

1. Connect one end of an SMA cable to CH 0 on the front panel of the NI 5761 and the other end of the cable to your DUT.
2. Open the front panel of `5761SampleAcq(Host).vi`.
3. Click the **Run** button to run the VI.
4. The VI acquires data from the DUT on AI 0 Data N and AI 0 Data N-1.
5. Click the **STOP** button on the front panel and close the VI.

How to Use Your NI FlexRIO Documentation Set

Refer to the Figure 7 and Table 4 for information about how to use your NI FlexRIO documentation set.

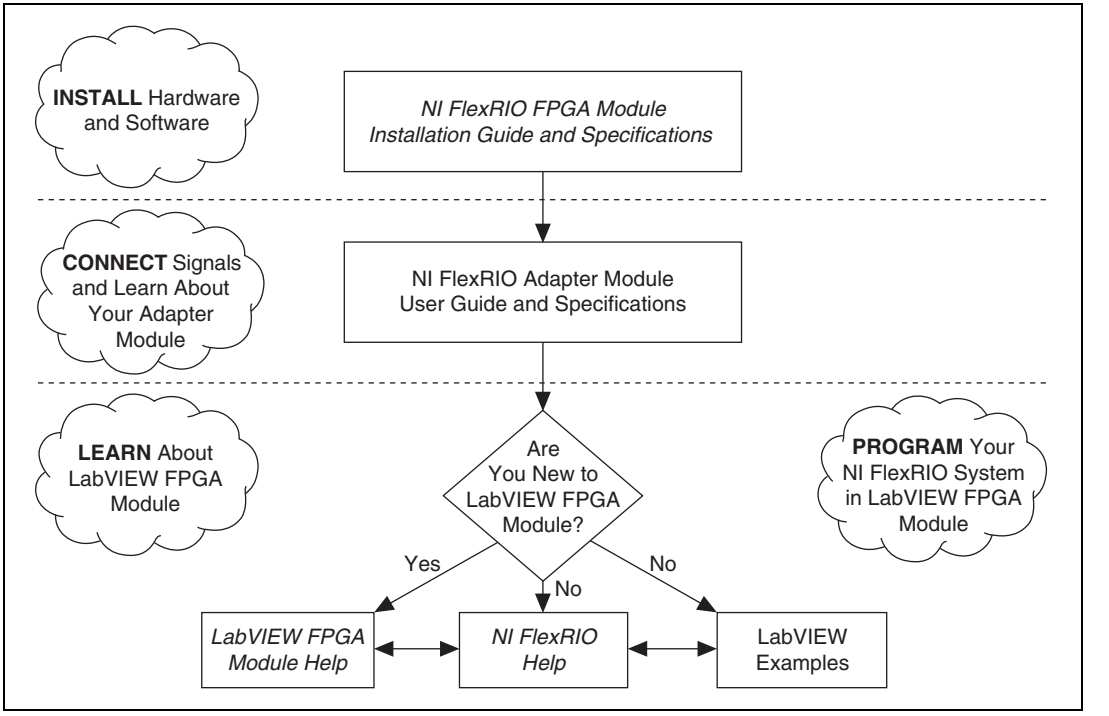


Figure 7. How to Use Your NI FlexRIO Documentation Set

Table 4. NI FlexRIO Documentation Locations and Descriptions

Document	Location	Description
NI FlexRIO FPGA Module Installation Guide and Specifications[*]	Available in your FPGA module hardware kit and from the Start Menu.	Contains installation instructions for your NI FlexRIO system and specifications for your FPGA module.
NI Adapter Module User Guide and Specifications[*]	Available in your adapter module hardware kit and from the Start Menu.	Contains signal information, examples, and specifications for your adapter module.
LabVIEW FPGA Module Help[*]	Embedded in *LabVIEW Help*.	Contains information about the basic functionality of LabVIEW FPGA Module.
NI FlexRIO Help[*]	Embedded in *LabVIEW FPGA Module Help*.	Contains FPGA module, adapter module, and CLIP configuration information.
LabVIEW Examples	Available in LabVIEW Example Finder.	Contains examples of how to run FPGA VIs and Host VIs on your device.
Other Useful Information on `ni.com`		
`ni.com/ipnet`	Contains LabVIEW FPGA functions and intellectual property to share.	
`ni.com/flexrio`	Contains product information and data sheets for NI FlexRIO devices.	
[*] These documents are also available at `ni.com/manuals`.		

Specifications

This section lists the specifications of the NI FlexRIO adapter module (NI 5761). Pair these specifications with the specifications listed in the *NI FlexRIO FPGA Module Installation Guide and Specifications*. For more information about safety and electromagnetic compatibility refer to the *Read Me First: Safety and Electromagnetic Compatibility* document included in your hardware kit or available at `ni.com/manuals`.

Caution To avoid permanent damage to the NI 5761, disconnect all signals connected to the NI 5761 before powering down the module, and only connect signals after the module has been powered on by the NI FlexRIO FPGA module.

Note All numeric specifications are typical unless otherwise noted. All graphs illustrate the performance of a representative module.

Typical values describe useful product performance that are not covered by warranty. Typical values cover the expected performance of units over ambient temperature ranges of 23 ±5 °C with a 90% confidence level, based on measurements taken during development or production.

Analog Input (AI CH 0 through AI CH 3)

General Characteristics

Number of channels.....Four, single-ended, simultaneously sampled

Connector.....SMA

Input impedance.....50 Ω, per connector

Sample rate

Internal Sample clock .....250 MHz

External Sample clock .....175 MHz to 250 MHz

Digital data range.....±8,191

ADC part number.....ADS62P49[1]; 14-bit resolution, dual ADC

AC-Coupled Specifications

Input range (normal operating conditions) .....2.07 V_{pk-pk}

Absolute maximum input.....±10 V DC, 5 V_{pk-pk} AC

Bandwidth (–3 dB).....0.1 MHz to 500 MHz

Bandwidth (–1 dB).....1 MHz to 250 MHz

[1] For additional information on the ADS62P49, refer to the Texas Instruments device data sheet at `www.ti.com`.

Table 5 lists the AC-coupled spectral performance measurements. All values are measured with a 250 MHz external Sample clock.

Table 5. AC-Coupled Spectral Performance

Measurement	20.17 MHz	70.17 MHz*	123.17 MHz*
SNR	72.5 dB	71.4 dB	70.5 dB
SINAD	72.3 dB	71.2 dB	70.3 dB
SFDR	88 dB	84 dB	80 dB
* These measurements were extrapolated from a –4 dBFS plot.			

Channel to channel isolation

1 MHz .....>90 dB
100.1 MHz .....90 dB
501 MHz .....80 dB

AC-Coupled Measurements

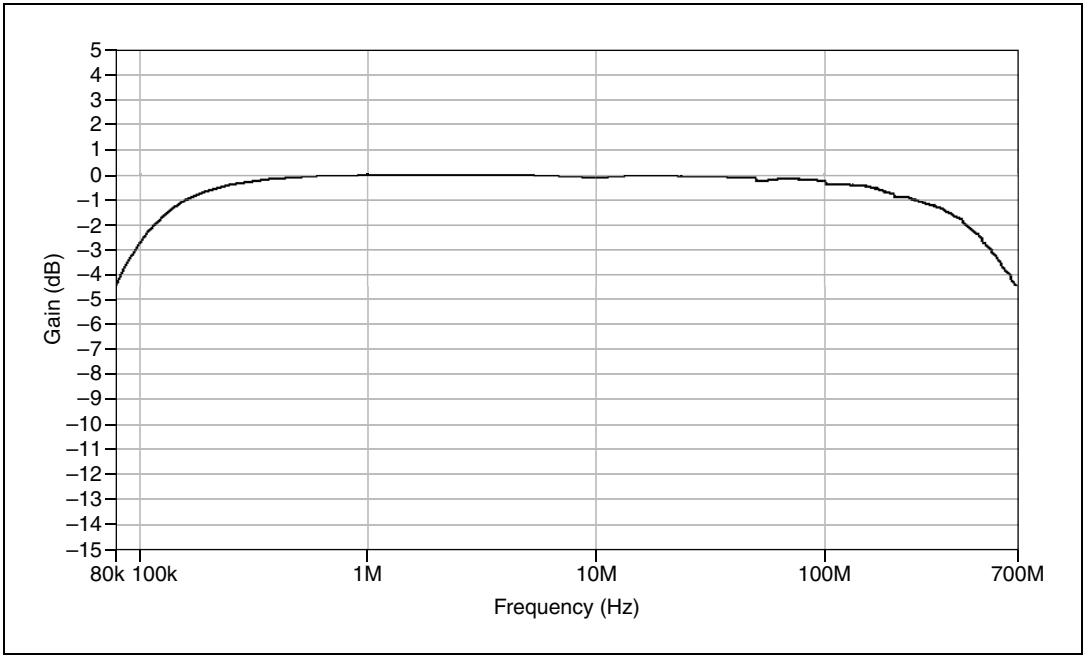


Figure 8. AC-Coupled Bandwidth (Passband)

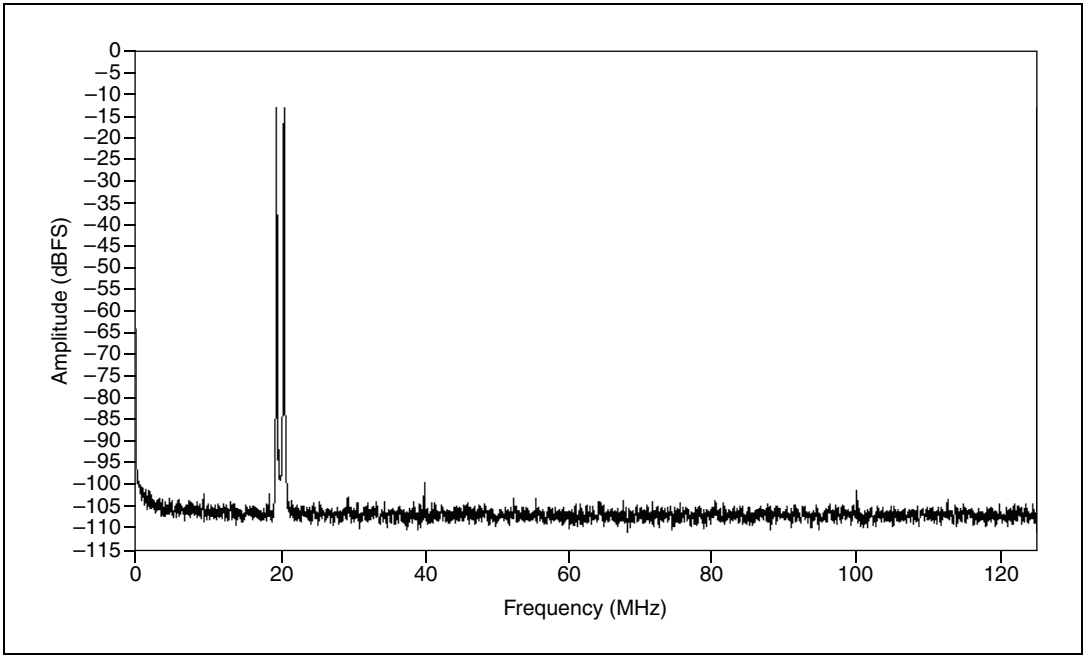


Figure 9. AC-Coupled Spectral Measurements: 19.5 MHz and 20.5 MHz, –13 dBFS, 8,192 Point FFT, 10 RMS Average

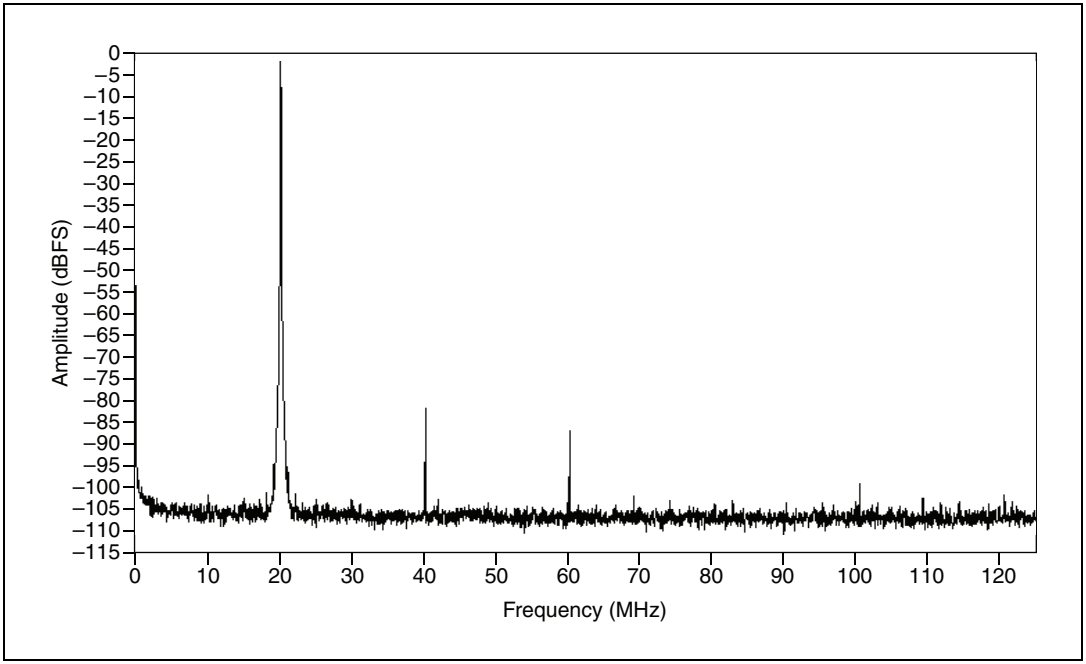


Figure 10. AC-Coupled Spectral Measurements: 20.1 MHz, –1 dBFS, 8,192 Point FFT, 10 RMS Average

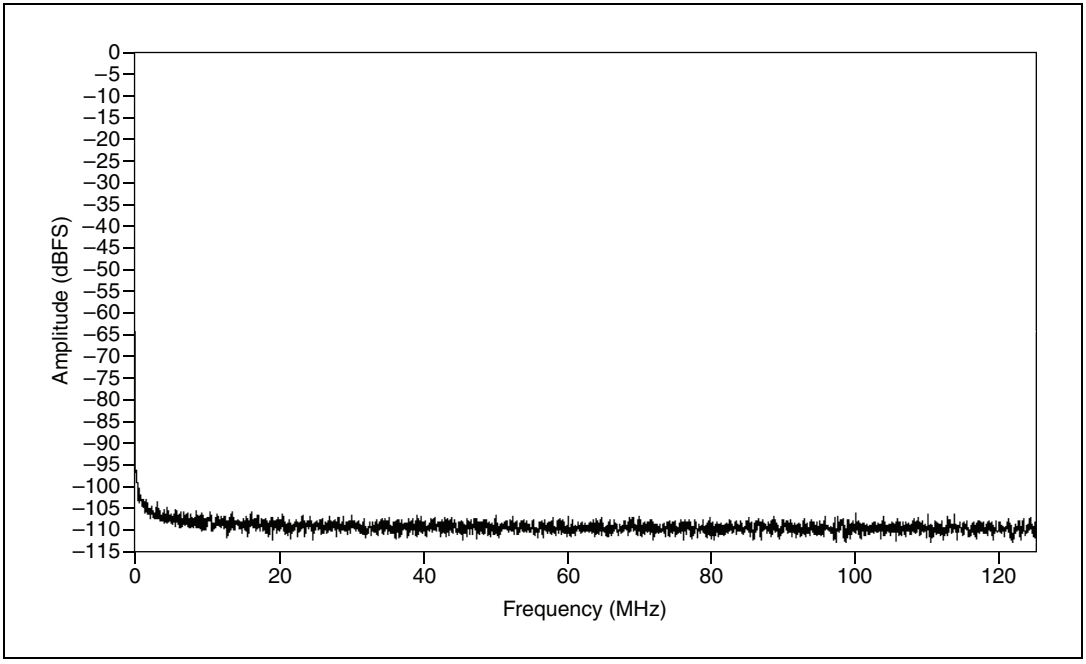


Figure 11. AC-Coupled Spectral Measurements: Terminated, 8,192 Point FFT, 10 RMS Average

DC-Coupled Specifications

Input range (normal operating conditions) .....1.23 V_{pk-pk}

Absolute maximum input.....±4.5 V DC

Bandwidth (–3 dB).....DC to 500 MHz

Bandwidth (–1 dB).....DC to 250 MHz

Table 6 lists the DC-coupled spectral performance measurements. All values are measured with a 250 MHz external Sample clock.

Table 6. DC-Coupled Spectral Performance

Measurement	20.1 MHz	70.1 MHz	122.1 MHz
SNR	65.7 dB	64.3 dB	63 dB
SINAD	65.2 dB	61.8 dB	56.6 dB
SFDR	76 dB	65 dB	58 dB

Channel to channel isolation

1 MHz .....>90 dB

100.1 MHz .....80 dB

501 MHz .....70 dB

Note To ensure proper device operation, DC-coupled channels on the NI 5761 must see 50 Ω at DC looking back at their source. If you are connecting a to source with an output impedance less than 50 Ω, you can add series resistance close to the source to properly bias the NI 5761 input terminals. You can also use the NI 5761 input channel bias DACs to remove DC offset present in the system. For more information about programming the bias DACs, refer to the NI 5761 CLIP topics in the *NI FlexRIO Help*.

DC-Coupled Measurements

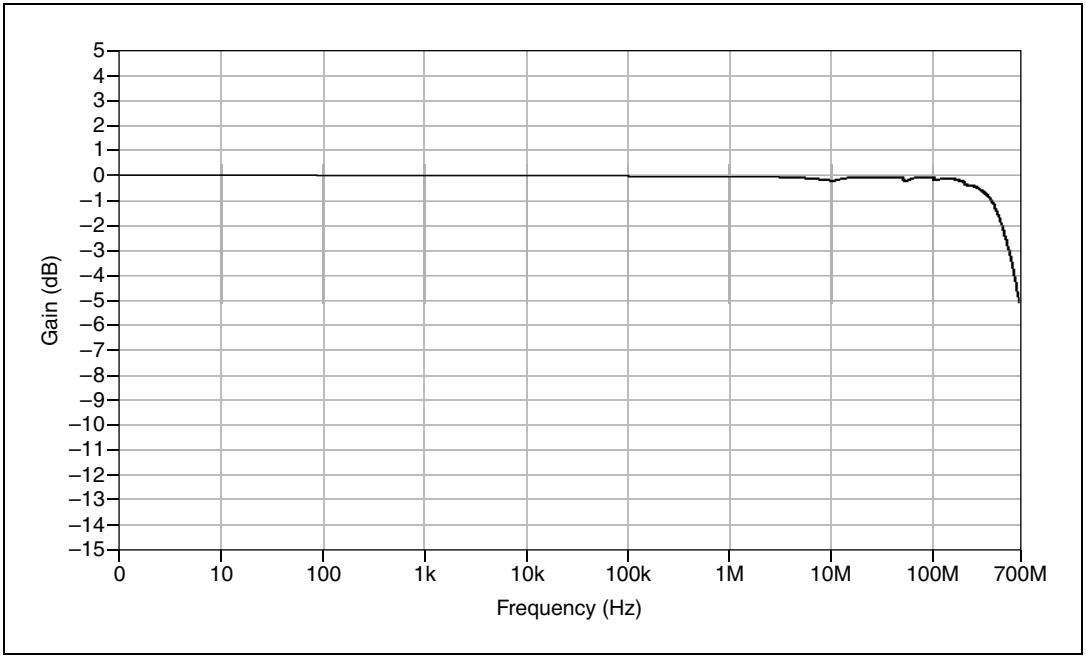


Figure 12. DC-Coupled Bandwidth (Passband)

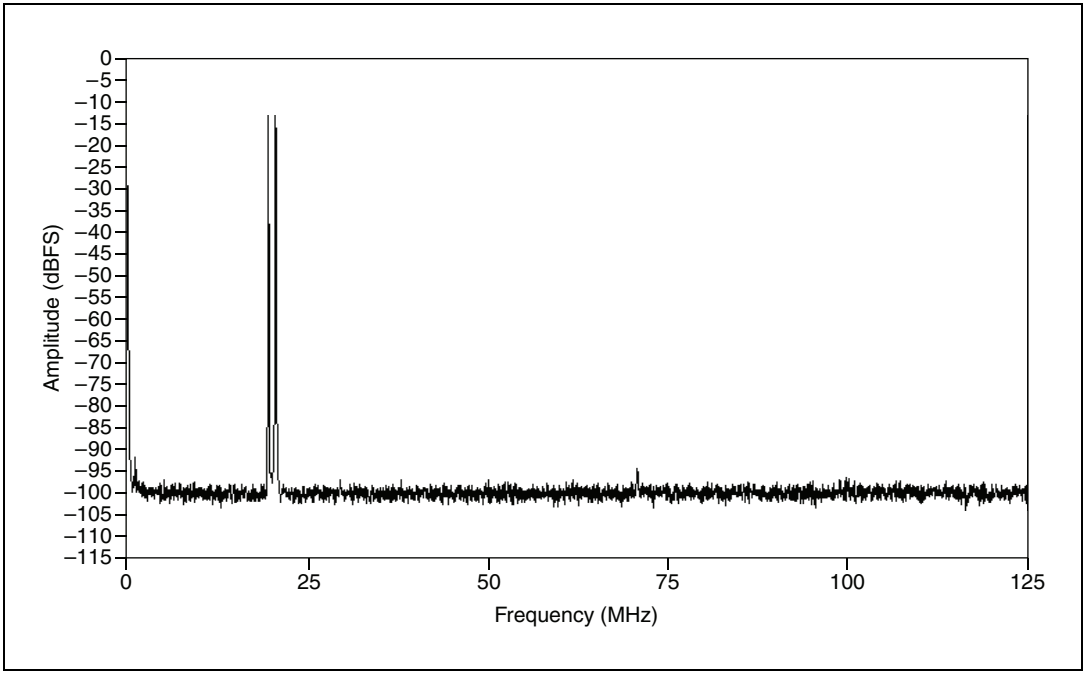


Figure 13. DC-Coupled Spectral Measurements: 19.5 MHz and 20.5 MHz, –13 dBFS, 8,192 Point FFT, 10 RMS Average

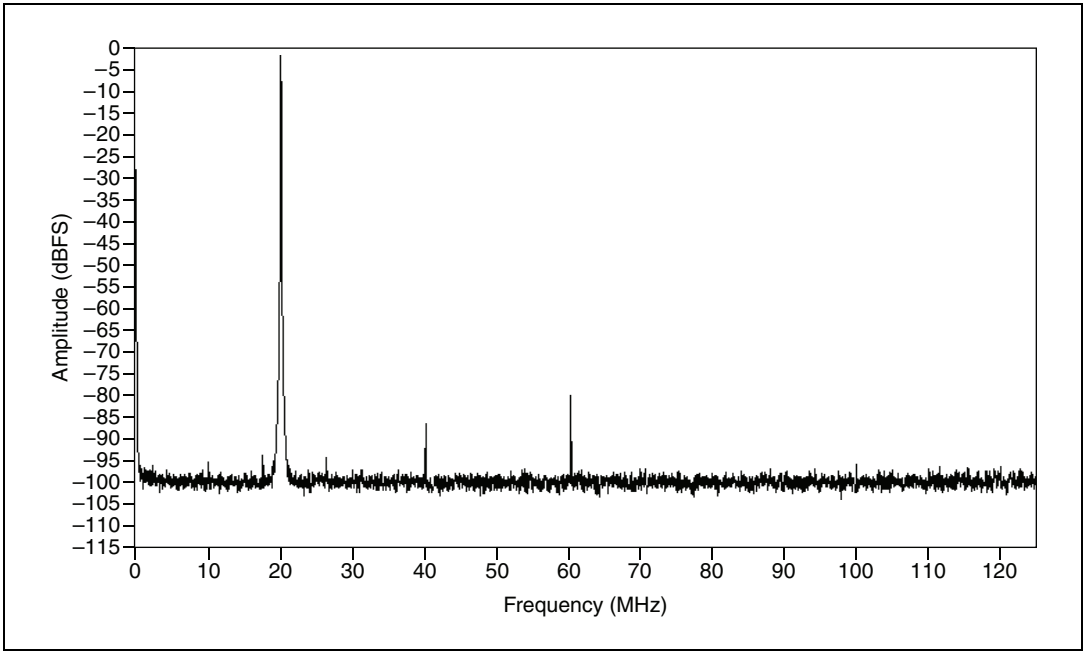


Figure 14. DC-Coupled Spectral Measurements: 20.1 MHz, –1 dBFS, 8,192 Point FFT, 10 RMS Average

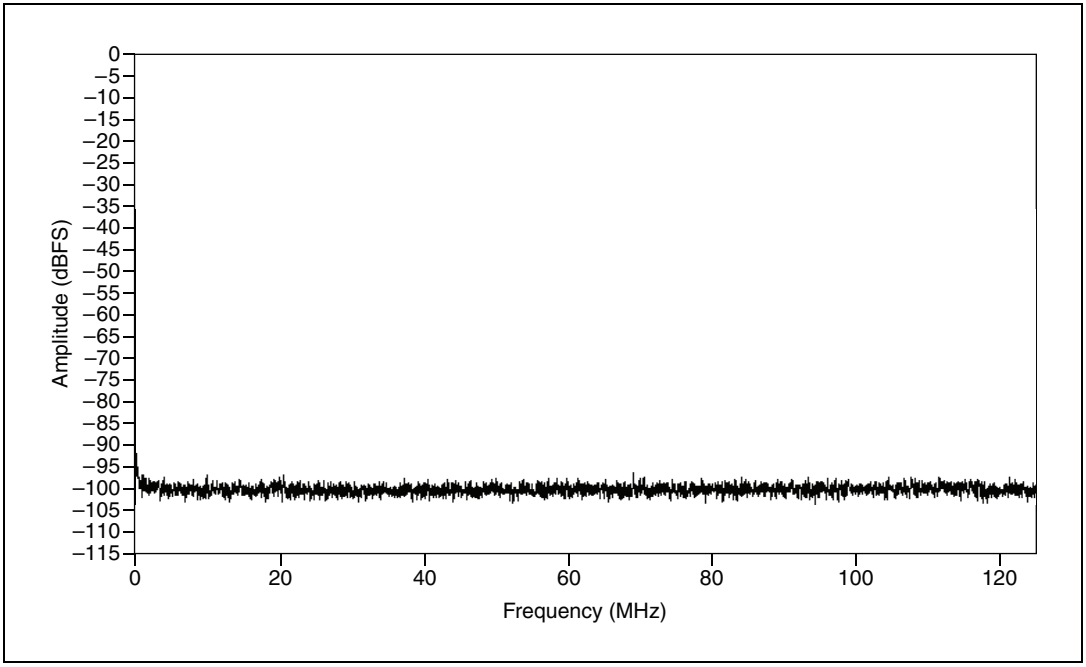


Figure 15. DC-Coupled Spectral Measurements: Terminated, 8,192 Point FFT, 10 RMS Average

Analog Input Phase Noise

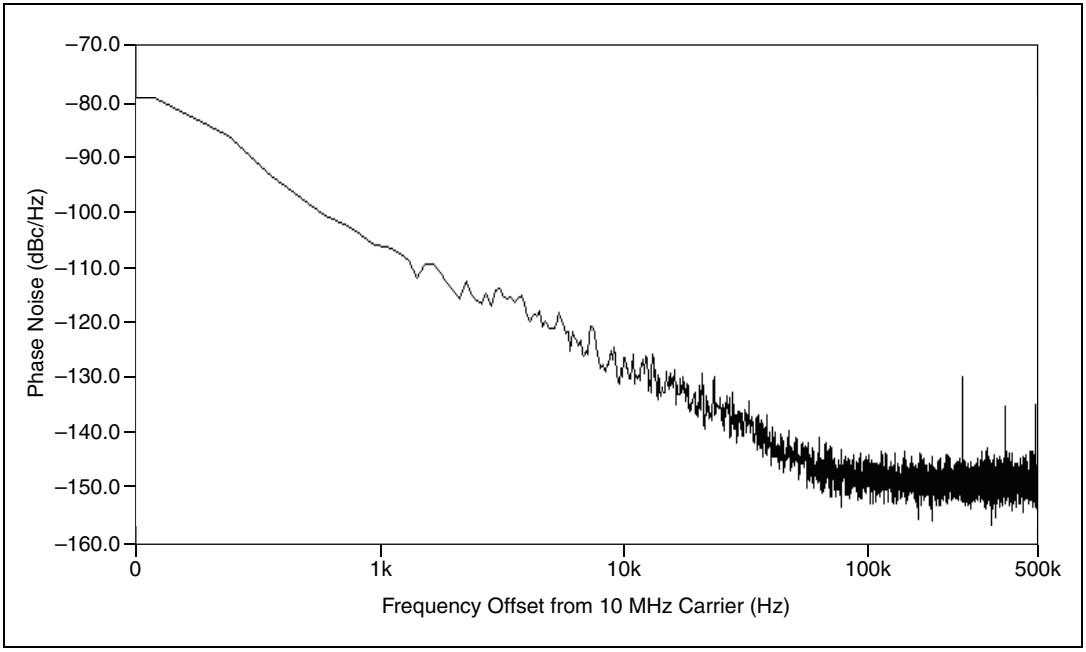


Figure 16. Analog Input Phase Noise

Internal Sample Clock

General Characteristics

Oscillator type ..... Fixed frequency synthesizer

Frequency ..... 250 MHz

Reference spurs ..... <70 dBc

Phase noise

- 10 kHz offset ..... –100 dBc/Hz
- 100 kHz offset ..... –120 dBc/Hz

Clock distribution part number ..... AD9512[1]; clock distribution

Reference clock sources ..... Internal, External through the CLK IN connector, or IoModSyncClk[2]

Internal reference type ..... TCXO

Internal reference stability ..... ±1 ppm

Internal reference frequency ..... 10 MHz

CLK IN

General Characteristics

Number of channels ..... 1, single-ended

Connector ..... SMA

Input impedance ..... 50 Ω

Input coupling ..... AC

External Sample Clock

Input voltage range ..... 0.63 V_{pk-pk} to 2.5 V_{pk-pk}

Input frequency range ..... 175 MHz to 250 MHz

Absolute maximum input ..... ±10 V DC, 3.1 V_{pk-pk} AC

External Reference Clock

Input voltage range ..... 1.4 V_{pk-pk} to 4.4 V_{pk-pk}

Input frequency range ..... 10 MHz

Absolute maximum input ..... ±10 V DC, 5 V_{pk-pk} AC

External Trigger

General Characteristics

Number of channels ..... 1, single-ended

Connector ..... SMA

Input impedance ..... 50 Ω

Input coupling ..... DC

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[1] For additional information about the AD9512, refer to the Analog Devices device data sheet at `www.analog.com`.

[2] IoModSyncClk is available only on the NI PXIe-796*x*R FPGA modules.

Input levels

Voltage Level	Minimum	Maximum
V_{IL}	0 V	0.7 V
V_{IH}	1.7 V	5.5 V

Absolute maximum input.....–0.5 V to 7 V

PFI<0..7>

General Characteristics

Number of channels.....8 bidirectional

Connector type.....Micro–D

Interface standard.....2.5 V LVCMOS

Interface logic

Voltage Level	Minimum	Maximum
V_{IL}	0 V	0.7 V
V_{IH}	1.7 V	5.5 V
V_{OL}	0 V	0.4 V
V_{OH}	1.9 V	2.5 V

Z_{in}.....17.5 kΩ
Z_{out}.....50 Ω
I_{out}.....2 mA

Maximum toggle frequency.....500 kHz

Absolute maximum input.....–0.5 V to 7 V

EEPROM Map

Byte Address	Size (Bytes)	Field Name
0x0	2	Vendor ID
0x2	2	Product ID
0x4	4	Serial Number
0x8	116	Reserved
0x7C	132	User Space

Caution *Only* write to *User Space*. Writing to any other offset may cause the NI 5761 to stop functioning.

Power

Total power, typical operation.....5.3 W

Physical

Dimensions .....12.9 × 2.0 × 12.1 cm
(5.1 × 0.8 × 4.7 in.)

Weight.....312 g (11 oz)

Front panel connectors.....6 SMA and one Micro-D connector

Environmental

The NI 5761 is intended for indoor use only.

Operating environment[1] .....0 °C to 55 °C,
tested in accordance with IEC-60068-2-1 and IEC-60068-2-2.

Relative humidity range.....10% to 90%, noncondensing,
tested in accordance with IEC-60068-2-56.

Altitude .....2,000 m at 25 °C ambient temperature.

Pollution Degree 2

Storage environment

Ambient temperature range .....–20 °C to 70 °C,
tested in accordance with IEC-60068-2-1 and IEC-60068-2-2.

Relative humidity range.....5% to 95%, noncondensing,
tested in accordance with IEC-60068-2-56.

Note Clean the device with a soft, non-metallic brush. Make sure that the device is completely dry and free from contaminants before returning it to service.

Safety

This product meets the requirements of the following standards of safety for electrical equipment for measurement, control, and laboratory use:

- IEC 61010-1, EN 61010-1
- UL 61010-1, CSA 61010-1

Note For UL and other safety certifications, refer to the product label or the *Online Product Certification* section.

[1] For PXI/PXI Express chassis configurations that group NI FlexRIO adapter modules in three or more contiguous slots, National Instruments recommends limiting the ambient operating temperature to less than 50 °C.

Electromagnetic Compatibility

This product meets the requirements of the following EMC standards for electrical equipment for measurement, control, and laboratory use:

- EN 61326-1 (IEC 61326-1): Class A emissions; Basic immunity
- EN 55011 (CISPR 11): Group 1, Class A emissions
- AS/NZS CISPR 11: Group 1, Class A emissions
- FCC 47 CFR Part 15B: Class A emissions
- ICES-001: Class A emissions

Note For EMC declarations and certifications, refer to the *Online Product Certification* section of this document.

Caution For EMC compliance, operate this device with shielded cables and accessories.

CE Compliance CE

This product meets the essential requirements of applicable European Directives as follows:

- 2006/95/EC; Low-Voltage Directive (safety)
- 2004/108/EC; Electromagnetic Compatibility Directive (EMC)

Online Product Certification

To obtain product certifications and the Declaration of Conformity for this product, visit `ni.com/certification`, search by model number or product line, and click the appropriate link in the Certification column.

Environmental Management

National Instruments is committed to designing and manufacturing products in an environmentally responsible manner. NI recognizes that eliminating certain hazardous substances from our products is beneficial not only to the environment but also to NI customers.

For additional environmental information, refer to the *NI and the Environment* Web page at `ni.com/environment`. This page contains the environmental regulations and directives with which NI complies, as well as other environmental information not included in this document.

Waste Electrical and Electronic Equipment (WEEE)

EU Customers At the end of the product life cycle, all products *must* be sent to a WEEE recycling center. For more information about WEEE recycling centers, National Instruments WEEE initiatives, and compliance with WEEE Directive 2002/96/EC on Waste and Electronic Equipment, visit `ni.com/environment/weee`.

电子信息产品污染控制管理办法 （中国 RoHS）

中国客户 National Instruments 符合中国电子信息产品中限制使用某些有害物质指令 (RoHS)。关于 National Instruments 中国 RoHS 合规性信息，请登录 `ni.com/environment/rohs_china`。(For information about China RoHS compliance, go to `ni.com/environment/rohs_china`.)

Where to Go for Support

The National Instruments Web site is your complete resource for technical support. At ni.com/support you have access to everything from troubleshooting and application development self-help resources to email and phone assistance from NI Application Engineers.

National Instruments corporate headquarters is located at 11500 North Mopac Expressway, Austin, Texas, 78759-3504. National Instruments also has offices located around the world to help address your support needs. For telephone support in the United States, create your service request at ni.com/support and follow the calling instructions or dial 512 795 8248. For telephone support outside the United States, contact your local branch office:

Australia 1800 300 800, Austria 43 662 457990-0, Belgium 32 (0) 2 757 0020,
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Czech Republic 420 224 235 774, Denmark 45 45 76 26 00,
Finland 358 (0) 9 725 72511, France 01 57 66 24 24, Germany 49 89 7413130,
India 91 80 41190000, Israel 972 3 6393737, Italy 39 02 41309277,
Japan 0120-527196, Korea 82 02 3451 3400, Lebanon 961 (0) 1 33 28 28,
Malaysia 1800 887710, Mexico 01 800 010 0793,
Netherlands 31 (0) 348 433 466, New Zealand 0800 553 322,
Norway 47 (0) 66 90 76 60, Poland 48 22 328 90 10, Portugal 351 210 311 210,
Russia 7 495 783 6851, Singapore 1800 226 5886, Slovenia 386 3 425 42 00,
South Africa 27 0 11 805 8197, Spain 34 91 640 0085,
Sweden 46 (0) 8 587 895 00, Switzerland 41 56 2005151,
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375509A-01 May10