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NI 5762R User Guide and Specifications

The NI 5762 is a two-channel, 250 MS/s, 16-bit high-speed digitizer adapter module designed to work in conjunction with your NI FlexRIO™ FPGA module. The NI 5762 is available in these two versions:

- NI 5762 (-01): Single-ended, AC-coupled with a 100 MHz elliptic filter
- NI 5762 (-02): Single-ended, AC-coupled, ideal for undersampling applications

Read the white labels on the side of your device to determine which version of the NI 5762 you are using. This document contains signal information and specifications for the NI 5762R, which is composed of an NI FlexRIO FPGA module and the NI 5762. This document also contains tutorial sections that demonstrate how to acquire data using a LabVIEW FPGA example VI and how to create and run your own LabVIEW project with the NI 5762R.

Contents

Note Before configuring your NI 5762R, you must install the appropriate software and hardware. Refer to the *NI FlexRIO FPGA Module Installation Guide and Specifications* for installation instructions. Figure 1 shows an example of a properly connected NI FlexRIO device.

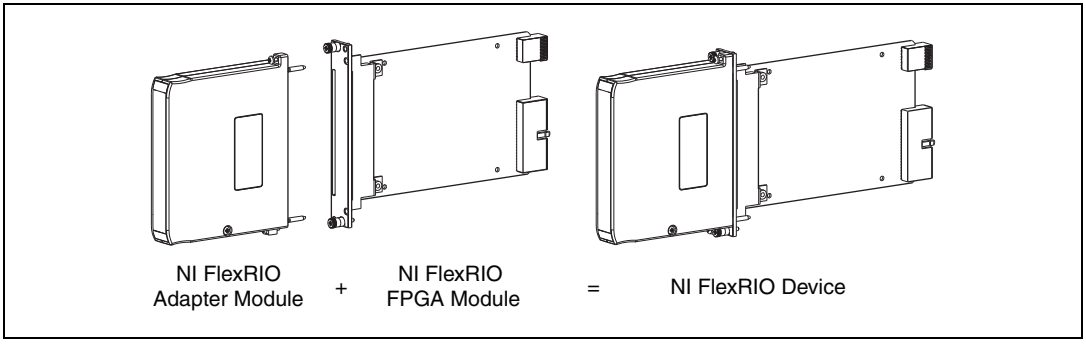


Figure 1. NI FlexRIO Device

Note *NI 5762R* refers to the combination of your NI 5762 adapter module and your NI FlexRIO FPGA module. *NI 5762* refers to your NI 5762 adapter module only.

NATIONAL INSTRUMENTS

Electromagnetic Compatibility Guidelines

This product was tested and complies with the regulatory requirements and limits for electromagnetic compatibility (EMC) as stated in the product specifications. These requirements and limits are designed to provide reasonable protection against harmful interference when the product is operated in its intended operational electromagnetic environment.

This product is intended for use in industrial locations. There is no guarantee that harmful interference will not occur in a particular installation, when the product is connected to a test object, or if the product is used in residential areas. To minimize the potential for the product to cause interference to radio and television reception or to experience unacceptable performance degradation, install and use this product in strict accordance with instructions in the product documentation.

Furthermore, any changes or modifications to the product not expressly approved by National Instruments could void your authority to operate it under your local regulatory rules.

Caution To ensure the specified EMC performance, you must install PXI EMC Filler Panels (National Instruments part number 778700-01) in adjacent chassis slots. For more information about installing PXI EMC filler panels on your NI 5762R, refer to the *Appendix: Installing EMI Controls* section of this document.

Caution To ensure the specified EMC performance, operate this product only with shielded cables and accessories.

Caution To ensure the specified EMC performance, install the included snap-on ferrites (National Instruments part number 711856-01) on any cable attached to the AUX I/O connector in accordance with the instructions listed in the *Appendix: Installing EMI Controls* section.

Caution This product is sensitive to electrostatic discharge (ESD). To ensure the specified EMC performance, follow the programming instructions listed at the end of the *Using Your NI 5762R with a LabVIEW FPGA Example VI* and *Creating a LabVIEW Project and Running a VI on an FPGA Target* sections of this document.

How to Use Your NI FlexRIO Documentation Set

Refer to Figure 2 and Table 1 for information about how to use your NI FlexRIO documentation set.

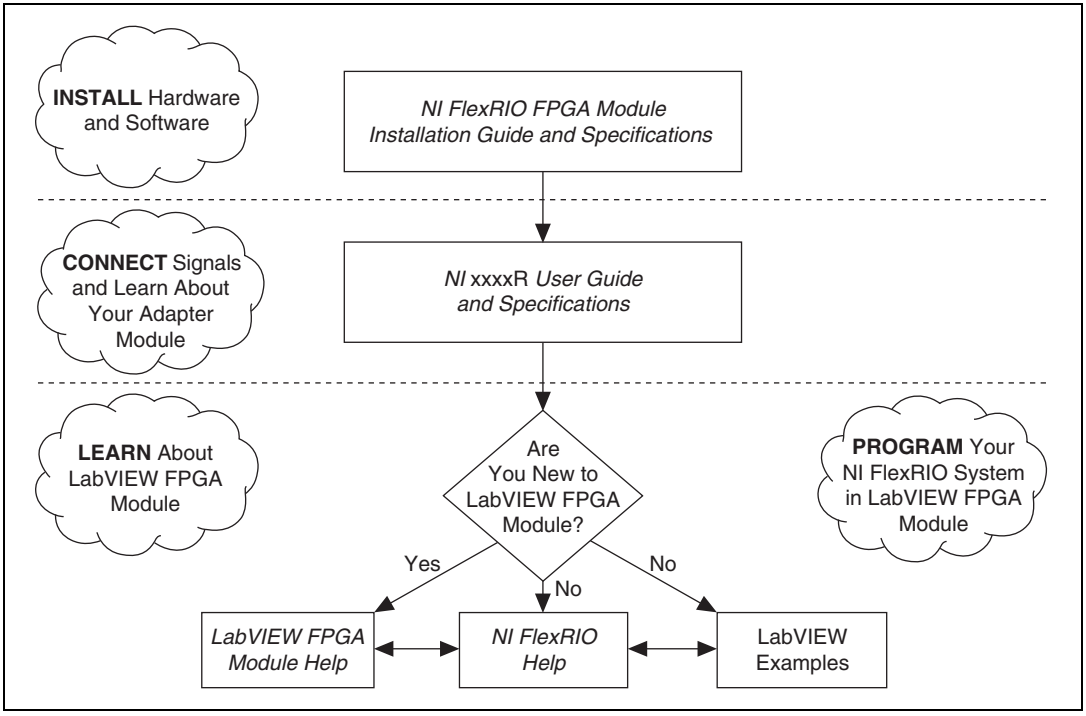


Figure 2. How to Use Your NI FlexRIO Documentation Set

Table 1. NI FlexRIO Documentation Locations and Descriptions

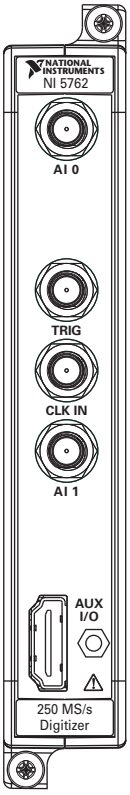
Document	Location	Description
NI FlexRIO FPGA Module Installation Guide and Specifications[*]	Available in your FPGA module hardware kit and from the Start Menu.	Contains installation instructions for your NI FlexRIO system and specifications for your FPGA module.
NI Adapter Module User Guide and Specifications[*]	Available in your adapter module hardware kit and from the Start Menu.	Contains signal information, examples, and specifications for your adapter module.
LabVIEW FPGA Module Help[*]	Embedded in *LabVIEW Help*.	Contains information about the basic functionality of LabVIEW FPGA Module.
NI FlexRIO Help[*]	Embedded in *LabVIEW FPGA Module Help*.	Contains FPGA module, adapter module, and CLIP configuration information.
LabVIEW Examples	Available in NI Example Finder.	Contains examples of how to run FPGA VIs and Host VIs on your device.
Other Useful Information on `ni.com`		
`ni.com/ipnet`	Contains LabVIEW FPGA functions and intellectual property to share.	
`ni.com/flexrio`	Contains product information and data sheets for NI FlexRIO devices.	
[*] These documents are also available at `ni.com/manuals`.		

Front Panel and Connector Pinouts

Table 2 shows the front panel connectors and signal descriptions for both versions of the NI 5762. Refer to the *Specifications* section of this document for additional signal information.

Caution To avoid permanent damage to the NI 5762, disconnect all signals connected to the NI 5762 before powering down the module, and connect signals only after the adapter module has been powered on by the NI FlexRIO FPGA module.

Table 2. NI 5762 Front Panel Connectors

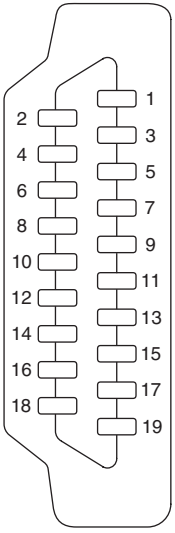
Device Front Panel	Connector	Signal Description
	AI 0	Single-ended analog input channel 0.
	TRIG	External trigger input.
	CLK IN*	Reference or external clock input.
	AI 1	Single-ended analog input channel 1.
	AUX I/O	Refer to Table 3 for the signal list and descriptions.
* When not using an external Sample clock or the Reference clock, terminate the CLK IN input connector with a 50 Ω terminator. Failing to terminate the CLK IN connector may negatively impact the jitter performance of the NI 5762.		

Caution Connections that exceed any of the maximum ratings of any connector on the NI 5762R can damage the device and the chassis. NI is *not* liable for any damage resulting from such signal connections. For the maximum input and output ratings for each signal, refer to the *Specifications* section of this document.

AUX I/O Connector

Table 3 shows the pin assignments for the AUX I/O connector on the NI 5762.

Table 3. NI 5762 AUX I/O Connector Pin Assignments

AUX I/O Connector	Pin	Signal	Signal Description
	1	DIO Port 0 (0)	Bidirectional single-ended digital I/O data channel.
	2	GND	Ground reference for signals.
	3	DIO Port 0 (1)	Bidirectional single-ended digital I/O data channel.
	4	DIO Port 0 (2)	Bidirectional single-ended digital I/O data channel.
	5	GND	Ground reference for signals.
	6	DIO Port 0 (3)	Bidirectional single-ended digital I/O data channel.
	7	DIO Port 1 (0)	Bidirectional single-ended digital I/O data channel.
	8	GND	Ground reference for signals.
	9	DIO Port 1 (1)	Bidirectional single-ended digital I/O data channel.
	10	DIO Port 1 (2)	Bidirectional single-ended digital I/O data channel.
	11	GND	Ground reference for signals.
	12	DIO Port 1 (3)	Bidirectional single-ended digital I/O data channel.
	13	PFI 0	Bidirectional single-ended digital I/O data channel.
	14	NC	No connect.
	15	PFI 1	Bidirectional single-ended digital I/O data channel.
	16	PFI 2	Bidirectional single-ended digital I/O data channel.
	17	GND	Ground reference for signals.
	18	+5V	+5 V power (10 mA, maximum).
	19	PFI 3	Bidirectional single-ended digital I/O data channel.

Caution The AUX I/O connector accepts a standard, third-party HDMI cable, but the AUX I/O port is not an HDMI interface. Do *not* connect the AUX I/O port on the NI 5762 into the HDMI port of another device. NI is *not* liable for any damage resulting from such signal connections.

Block Diagram

Figure 3 shows a block diagram image of the signal flow to and from the NI 5762 adapter module and the NI 5762 component-level intellectual property (CLIP) in LabVIEW FPGA.

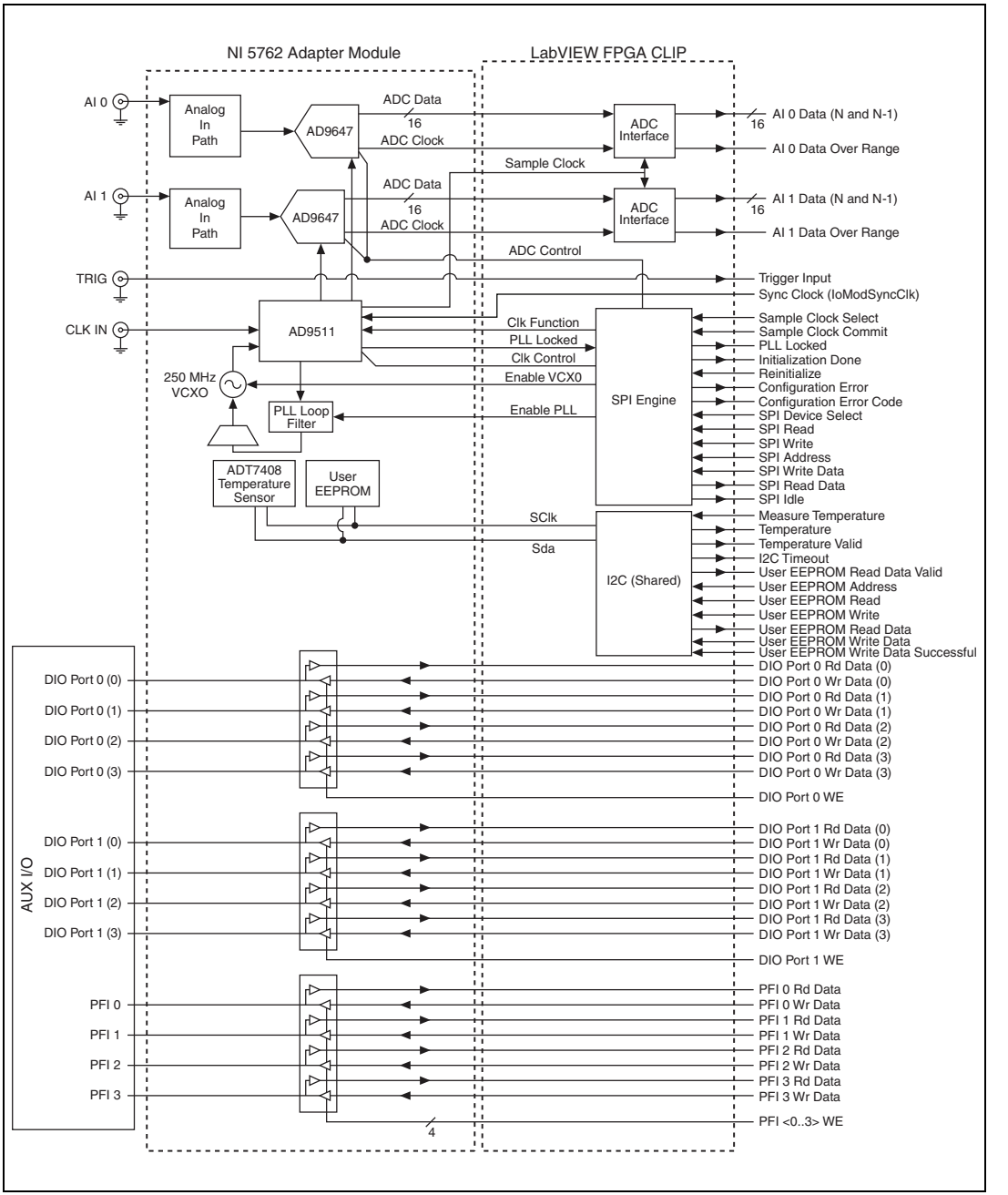


Figure 3. NI 5762 Connector Signals and NI 5762 CLIP Signal Block Diagram

NI 5762 Component-Level Intellectual Property (CLIP)

The LabVIEW FPGA Module includes a feature for HDL IP integration called CLIP. NI FlexRIO devices support two types of CLIP: user-defined and socketed.

- *User-defined CLIP* allows users to insert HDL IP into an FPGA target, enabling VHDL code to communicate directly with an FPGA VI.
- *Socketed CLIP* provides the same IP integration functionality of the user-defined CLIP, but it also allows the CLIP to communicate directly with circuitry external to the FPGA. Adapter module socketed CLIP allows your IP to communicate directly with both the FPGA VI and the external adapter module connector interface.

Figure 4 shows the relationship between an FPGA VI and CLIP.

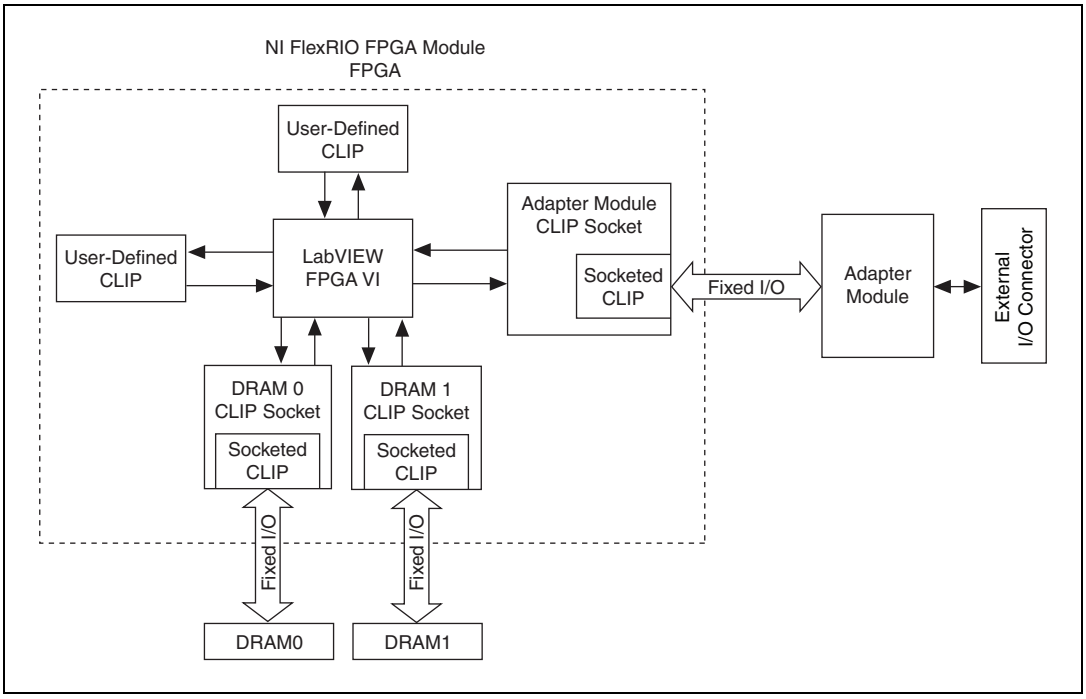


Figure 4. CLIP Relationship

The NI 5762 ships with socketed CLIP items that are used to add module I/O to the LabVIEW project. The NI 5762 ships with the following CLIP items:

- **NI 5762 Multiple Sample CLIP**—This CLIP generates two samples per clock cycle at a clock rate that is half the sample rate. The default sample rate is 250 MHz, which sets the default clock rate for this CLIP at 125 MHz. You can set a lower sample rate by using an external Sample clock. This CLIP provides access to two analog input channels, eight DIO lines, four PFI lines, and an input clock selector that can be configured to use one of the following settings:
  - Internal Sample clock
  - Internal Sample clock locked to an external Reference clock through Sync Clock (IoModSyncClk)
  - Internal Sample clock locked to an external Reference clock through the CLK IN connector
  - External Sample clock through the CLK IN connector

This CLIP also contains an engine to program the clock chip and ADCs, either through predetermined settings for an easier instrument setup or through a raw SPI address and data signals for a more advanced setup. Additionally, this CLIP provides an I2C interface to access a user EEPROM and a temperature sensor. In the LabVIEW FPGA Module, each analog signal uses a signed I16 data type. The DIO signals are grouped into two ports of four signals each and are accessed using a U8 data type and Boolean write enable signal. The four PFI signals are accessed individually using Boolean controls.

The NI 5762 Multiple Sample CLIP is the default CLIP.

- **NI 5762 Single Sample CLIP**—This CLIP generates one sample per clock cycle at a default sample rate of 250 MHz. You can set a lower sample rate by using an external Sample clock. This CLIP provides access to two analog input channels, eight digital input/output lines, four PFI lines, and an input clock selector that can be configured to use one of the following settings:
  - Internal Sample clock
  - Internal Sample clock locked to an external Reference clock through Sync Clock (IoModSyncClk)
  - Internal Sample clock locked to an external Reference clock through the CLK IN connector
  - External Sample clock through the CLK IN connector

This CLIP also contains an engine to program the clock chip and ADCs, either through predetermined settings for an easier instrument setup or through a raw SPI address and data signals for a more advanced setup. Additionally, this CLIP provides an I2C interface to access a user EEPROM and a temperature sensor. The DIO signals are grouped into two ports of four signals each and are accessed using a U8 data type and Boolean write enable signal. The four PFI signals are accessed individually using Boolean controls.

Refer to the *NI FlexRIO Help* for more information about NI FlexRIO CLIP items, configuring the NI 5762 with a socketed CLIP, and a list of available socketed CLIP signals.

Cables

Use any shielded 50 Ω coaxial cable with an SMA plug end to connect to the AI 0, AI 1, EXT TRIG, and CLK IN connectors on the NI 5762 front panel.

Use any HDMI cable with the two provided cable ferrites to connect to the digital I/O and PFI signals on the AUX I/O connector. Refer to the *Appendix: Installing EMI Controls* section for more information about attaching cable ferrites.

For more information about connecting I/O signals on your device, refer to the *Specifications* section of this document.

Clocking

The NI 5762 clocks control the sample rate and other timing functions on the device. Table 4 contains information about the possible NI 5762 clock resources. For more clocking information, refer to the *CLK IN* section of the specifications.

Table 4. NI 5762 Clock Sources

Clock	Frequency	Description
Internal Clock PLL Off	250 MHz	The internal VCXO acts as a free-running clock.
Internal Clock PLL On (IoModSyncClk)	250 MHz	The internal VCXO locks to PXI_CLK10 through Sync Clock (IoModSyncClk), which is provided only through the backplane of NI PXIe-796*x*R devices.
Internal Clock PLL On (CLK IN)	250 MHz	The internal VCXO locks to an external Reference clock (10 MHz), which is provided through the CLK IN front panel connector.
External Clock (CLK IN)	150 MHz to 250 MHz	An external Sample clock can be provided through the CLK IN front panel connector.

Using Your NI 5762R with a LabVIEW FPGA Example VI

Note You must install the software before running this example. Refer to the *NI FlexRIO FPGA Module Installation Guide and Specifications* for more information about installing your software.

The NI FlexRIO Adapter Module Support software includes a variety of example projects to help get you started creating your LabVIEW FPGA application. This section explains how to use an existing LabVIEW FPGA example project to generate and acquire samples with the NI 5762R. This example requires at least one SMA cable for connecting signals to your NI 5762R.

Note The examples available for your device are dependent on the version of the software and driver you are using. For more information about which software versions are compatible with your device, visit `ni.com/info` and enter `rdsoftwareversion` as the Info Code.

Each NI 5762R example project includes the following components:

- A LabVIEW FPGA VI that can be compiled and run on the FPGA embedded in the hardware. This VI is referred to as the FPGA Target VI.
- A VI that runs on Windows that interacts with the LabVIEW FPGA VI. This VI is referred to as the Host VI.

Note In the LabVIEW FPGA Module software, NI FlexRIO adapter modules are referred to as *IO Modules*.

Complete the following steps to run an example that acquires a waveform on AI 0 of the NI 5762.

1. Connect one end of an SMA cable to AI 0 on the front panel of the NI 5762 and the other end of the cable to your device under test (DUT).
2. Launch LabVIEW.
3. In the **Getting Started** window, click **Find Examples** to display the NI Example Finder.
4. In the **NI Example Finder** window, select **Hardware Input and Output»FlexRIO» IO Modules»NI 5762 (-0*x*)**. (Where *x* corresponds with the hardware version of the NI 5762 you are using.)
5. Select **NI 5762 (-0*x*) - Getting Started.lvproj**.
6. In the **Project Explorer** window, open **NI 5762 - Getting Started (Host).vi** under **My Computer**. The host VI opens. The Open FPGA VI Reference function in this VI uses the NI 7952R as the FPGA target by default. If you are using an NI FlexRIO FPGA module other than the NI 7952R, complete the following steps to change to the FPGA VI to support your target.
   a. Select **Window»Show Block Diagram** to open the VI block diagram.
   b. On the block diagram, right-click the **Open FPGA VI Reference** (PXI-7952R) function and select **Configure Open FPGA VI Reference**.
   c. In the **Configure Open FPGA VI Reference** dialog box, click the **Browse** button next to the **Bitfile** button.
   d. In the **Select Bitfile** dialog box that opens, select the bitfile for your desired target. The bitfile name is based on the adapter module, example type, and FPGA module.
   e. Click the **Select** button.
   f. Click **OK** in the **Configure Open FPGA VI Reference** dialog box.
   g. Save the VI.
7. On the front panel, in the **RIO Resource** pull-down menu, select an NI 5762R resource that corresponds with the target configured in step 6.
8. Select **AI 0** in the **AI Channel control**.
9. Set the **Trigger Level (V)**, **Record Size**, **Sample Rate**, and **Range (V)** controls to the desired value.
10. In the **Trigger Type** control, you can select either **Software Trigger** or **Data Edge**. If you select **Software Trigger**, the VI acquires data every time you click the **Software Trigger** button on the front panel of the VI. If you select **Data Edge**, the VI acquires data every time an edge occurs.
11. Click the **Run** button to run the VI.
12. Click the **Software Trigger** button if you selected **Software Trigger** in the **Trigger Type** control. The VI acquires data and displays the captured waveform on the **Acquired Waveform** graph as shown in Figure 5.
13. Click the **STOP** button to stop the VI.
14. Close the VI.

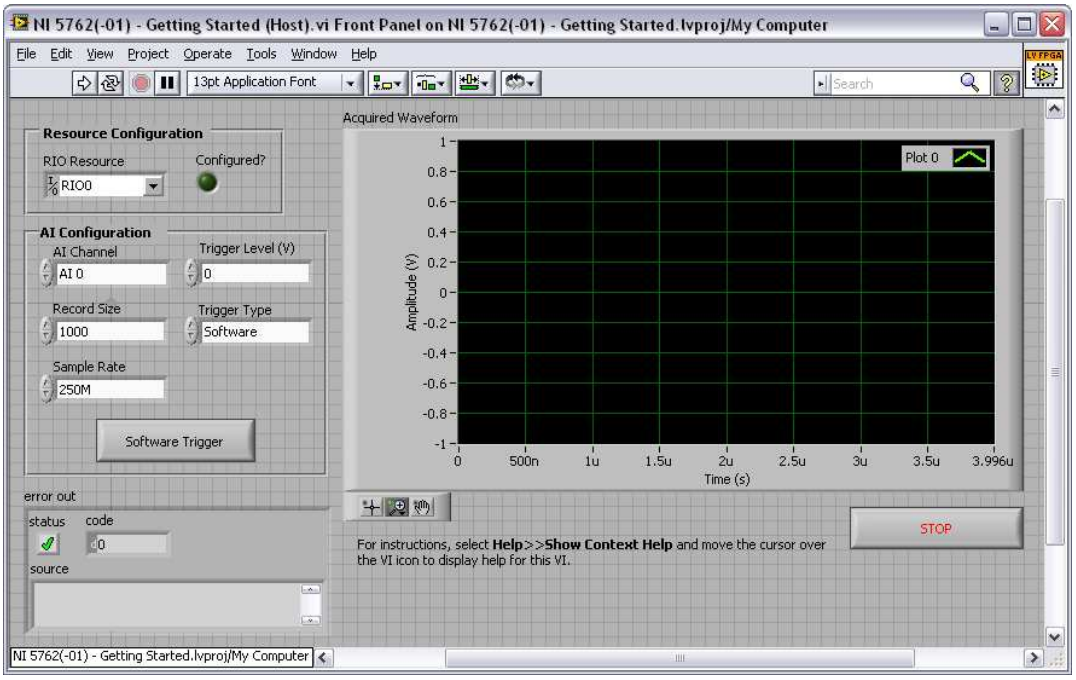


Figure 5. NI 5762 - Getting Started (Host) VI Front Panel

Creating a LabVIEW Project and Running a VI on an FPGA Target

This section explains how to set up your target and create an FPGA VI and host VI for data communication. For more detailed information about acquiring data on your NI 5762R, refer to the device-specific examples available in NI Example Finder.

Creating a Project

1. Launch LabVIEW, or if LabVIEW is already running, select **File»New**.
2. In the **New** dialog box, select **Project»Empty Project** and click **OK**. The new project opens in the **Project Explorer** window.
3. Save the project as `5762SampleAcq.lvproj`.

Creating an FPGA Target VI

1. In the **Project Explorer** window, right-click **My Computer** and select **New»Targets and Devices**.
2. In the **Add Targets and Devices on My Computer** dialog box, select the **Existing Target or Device** option button and expand **FPGA Target**. The target is displayed.
3. Select your device and click **OK**. The target and target properties are loaded into the **Project Explorer** window.
4. In the **Project Explorer** window, expand **FPGA Target (RIO*x*, PXI-79*xx*R)**.
5. Right-click **FPGA Target (RIO*x*, PXI-79*xx*R)** and select **New»FPGA Base Clock**.
6. In the **Resource** pull-down menu, select **IO Module Clock 0**.
7. Enter `125 MHz` in the **Compile for single frequency** control and click **OK**.

8. Right-click **FPGA Target (RIO*x*, PXI-79*xx*R)** and select **New»FPGA Base Clock again**.
9. In the **Resource** pull-down menu, select **200 MHz Clock** and click **OK**.
10. Right-click **IO Module** in the **Project Explorer** window and select **Properties**.
11. Select the **NI 5762 (-0*x*)** (where *x* corresponds with the NI part number of your device) from the IO Module list. The available CLIP for the NI 5762 is displayed in the **General** category of the Component Level IP pane. If the information in the **General** category is dimmed, select the **Enable IO Module** checkbox.
12. Select **NI 5762 Multiple Sample CLIP** in the Name list of the Component Level IP section.
13. In the **Clock Selections** category, select **200 MHz Clock** from the pull-down menu for **Clock 200 MHz**. Leave **Clock 40 MHz** configured as the **Top-Level Clock**. This step is necessary to compile the FPGA VI correctly.
14. Click **OK**.

Note Configuring these clocks is required for proper CLIP operation. Refer to the NI 5762 CLIP topics in the *NI FlexRIO Help* for more information about configuring your clocks.

15. In the **Project Explorer** window, right-click the FPGA target and select **New»VI**. A blank VI opens.
16. Select **Window»Show Block Diagram** to open the VI block diagram.
17. In the **Project Explorer** window, expand the **IO Module (NI 5762 : NI 5762)** tree view.
18. Drag **AI 0 Data N and AI 0 Data N-1** to the block diagram.
19. Add a Timed Loop structure around the two nodes.
20. Wire indicators to the output terminals of the **IO Module\AI 0 Data N** and **IO Module\AI 0 Data N-1** nodes.
21. Wire an **FPGA Clock Constant** to the input node of the Timed Loop. Set this constant to **IO Module Clock 0**.

Your block diagram should now resemble the block diagram in Figure 6.

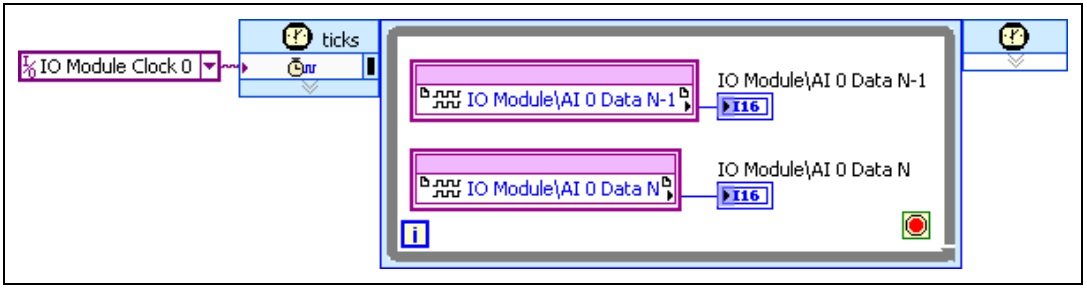


Figure 6. 5762SampleAcq (FPGA).vi Block Diagram

Tip Click the **Clean Up Diagram** button on the toolbar to cleanly organize the VI block diagrams.

22. Save the VI as `5762SampleAcq (FPGA).vi`.
23. Click the **Run** button. LabVIEW creates a default build specification and begins compiling the VI. The **Generating Intermediate Files** window opens and displays the code generation progress. Next, the **Compilation Status** window opens and displays the progress of the compilation. The compilation takes several minutes.
24. Click **Close** in the **Compilation Status** window.

25. Save and close the VI.
26. Save the project.

Creating a Host VI

1. In the **Project Explorer** window, right-click **My Computer** and select **New»VI**. A blank VI opens.
2. Select **Window»Show Block Diagram** to open the VI block diagram.
3. Place the **Open FPGA VI Reference function**, located on the **FPGA Interface** palette, on the block diagram.
4. Right-click the **Open FPGA VI Reference function** and select **Configure Open FPGA VI Reference**.
5. In the **Configure Open FPGA VI Reference** dialog box, select **VI** in the **Open** section.
6. In the **Select VI** dialog box that opens, select **5762SampleAcq (FPGA).vi** under your device and click **OK**.
7. Click **OK** in the **Configure Open FPGA VI Reference** dialog box. The target name appears under the **Open FPGA VI Reference** function in the block diagram.
8. Add a While Loop to the block diagram. Place it to the right of the **Open FPGA VI Reference** function.
9. Right-click the conditional terminal inside the While Loop, and select **Create Control** to create a STOP button on the VI front panel window.
10. Add the **Read/Write Control function**, located on the **FPGA Interface** palette, inside the While Loop.
11. Wire the **FPGA VI Reference Out** output terminal of the **Open FPGA VI Reference function** to the **FPGA VI Reference In input terminal on the** Read/Write Control **function**.
12. Wire the **error out** terminal of the **Open FPGA VI Reference function** to the **error in** control of the **Read/Write Control function**.
13. Configure the Read/Write Control function by clicking the terminal section labeled **Unselected**, and selecting **IO Module/AI 0 Data N**.
14. Add the **IO Module/AI 0 Data N-1** I/O item to the Read/Write Control function by clicking the handle on the bottom of the control node with the Positioning tool and dragging the edge down.
15. Wire indicators to the output terminals of the IO Module**AI 0 Data N** and IO Module**AI 0 Data N-1** nodes.
16. Add the **Close FPGA VI Reference function**, located on the **FPGA Interface** palette, to the right of the While Loop on the block diagram.
17. Wire the **FPGA VI Reference Out** terminal of the Read/Write Control **function** to the **FPGA VI Reference In terminal of the Close FPGA VI Reference function**.

18. Wire the **error out** terminal of the **Read/Write Control function** to the **error in** terminal of the **Close FPGA VI Reference function**.

    Your block diagram should now resemble the block diagram in Figure 7.

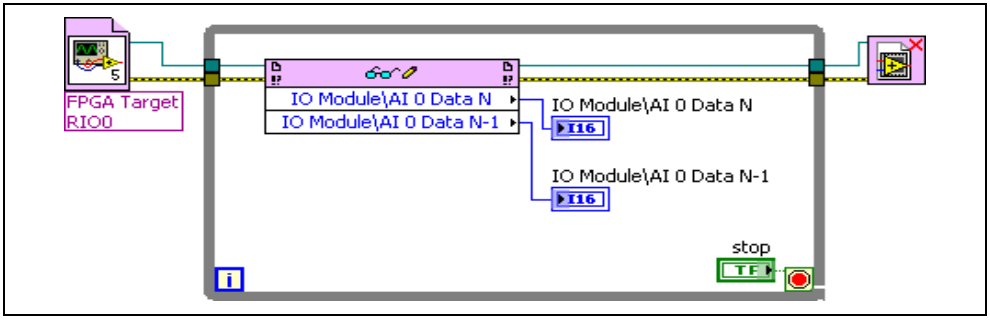


Figure 7. 5762SampleAcq(Host).vi Block Diagram

19. Save the VI as `5762SampleAcq(Host).vi`.

Running the Host VI

1. Connect one end of an SMA cable to AI 0 on the front panel of the NI 5762 and the other end of the cable to your DUT.
2. Open the front panel of `5762SampleAcq(Host).vi`.
3. Click the **Run** button to run the VI.
4. The VI acquires data from the DUT on **AI 0 Data N and AI 0 Data N-1**.
5. Click the **STOP** button on the front panel and close the VI.

Specifications

This section lists the specifications for both the NI 5762 (-01) and NI 5762 (-02) adapter modules. Pair these specifications with the specifications listed in the *NI FlexRIO FPGA Module Installation Guide and Specifications*. For more information about safety and electromagnetic compatibility refer to the *Read Me First: Safety and Electromagnetic Compatibility* document included in your hardware kit or available at `ni.com/manuals`.

Caution To avoid permanent damage to the NI 5762, disconnect all signals connected to the NI 5762 before powering down the module, and only connect signals after the module has been powered on by the NI FlexRIO FPGA module.

Note All numeric specifications are typical unless otherwise noted. All graphs illustrate the average performance of an NI 5762.

Typical values describe useful product performance that are not covered by warranty. Typical values cover the expected performance of units over ambient temperature ranges of 23 ±5 °C with an 85% confidence level, based on measurements taken during development or production.

Note For additional specifications and information about the ADCs (AD9467), refer to the Analog Devices data sheet at `www.analog.com`.

Analog Input (AI CH 0 and AI CH 1)

General Characteristics

Number of channels ..... 2, single-ended, simultaneously sampled

Connector type ..... SMA

Input impedance ..... 50 Ω, per connector

Input coupling ..... AC

Sample rate

- Internal Sample clock ..... 250 MHz
- External Sample clock ..... 150 MHz to 250 MHz

Digital data range ..... ±32,767

ADC part number ..... AD9467[1]; 16-bit resolution

Typical Specifications

Input range (normal operating conditions at 10 MHz)

- NI 5762 (-01) ..... 2.0 V_{pk-pk} (10 dBm)
- NI 5762 (-02) ..... 1.9 V_{pk-pk} (9.6 dBm)

Gain accuracy ..... ±0.035 dB

DC offset

- NI 5762 (-01) ..... ±1 mV
- NI 5762 (-02) ..... –5 mV ± 0.6 mV

[1] For additional information about the AD9467, refer to the Analog Devices data sheet at `www.analog.com`.

Crosstalk .....Better than –110 dBFS
(10 dBm signal at 70.1 MHz on the adjacent channel)

Absolute maximum voltage .....±3 V DC, 5 V_{pk-pk} AC

Table 5. Bandwidth (3 dB)

Device	Lower 3 dB Frequency	Upper 3 dB Frequency
NI 5762 (-01)	61.7 kHz	102 MHz
NI 5762 (-02)	61.7 kHz	Refer to Figures 8 and 10.

Measurements

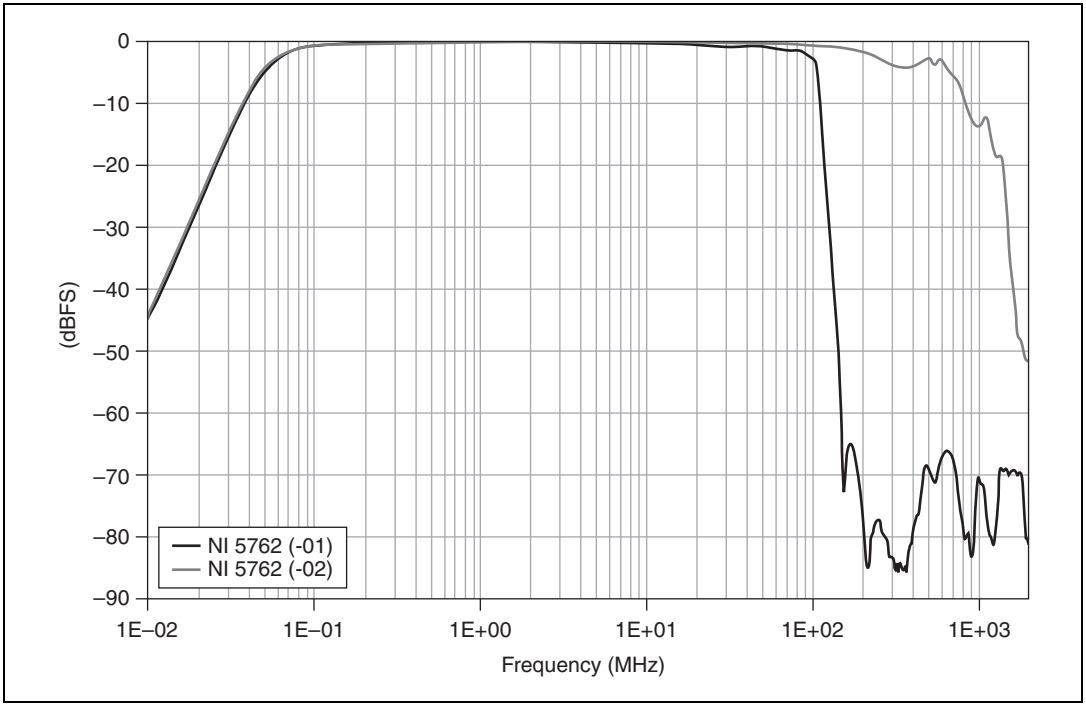


Figure 8. Frequency Response (Logarithmic Scale)

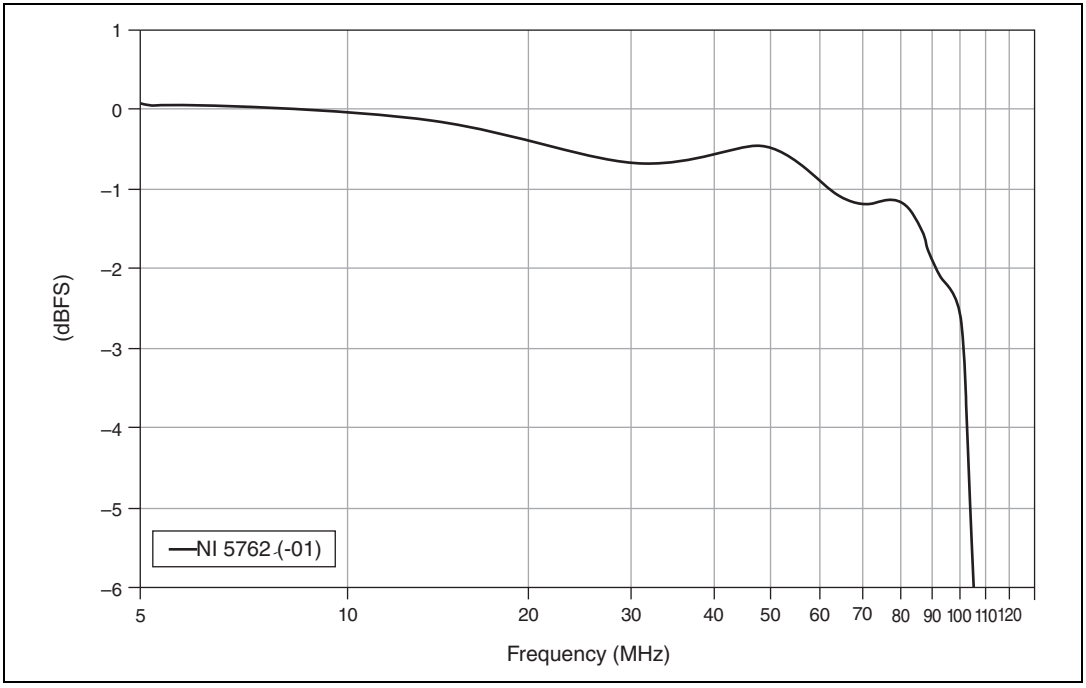


Figure 9. Frequency Response, NI 5762 (-01) only (Logarithmic Scale)

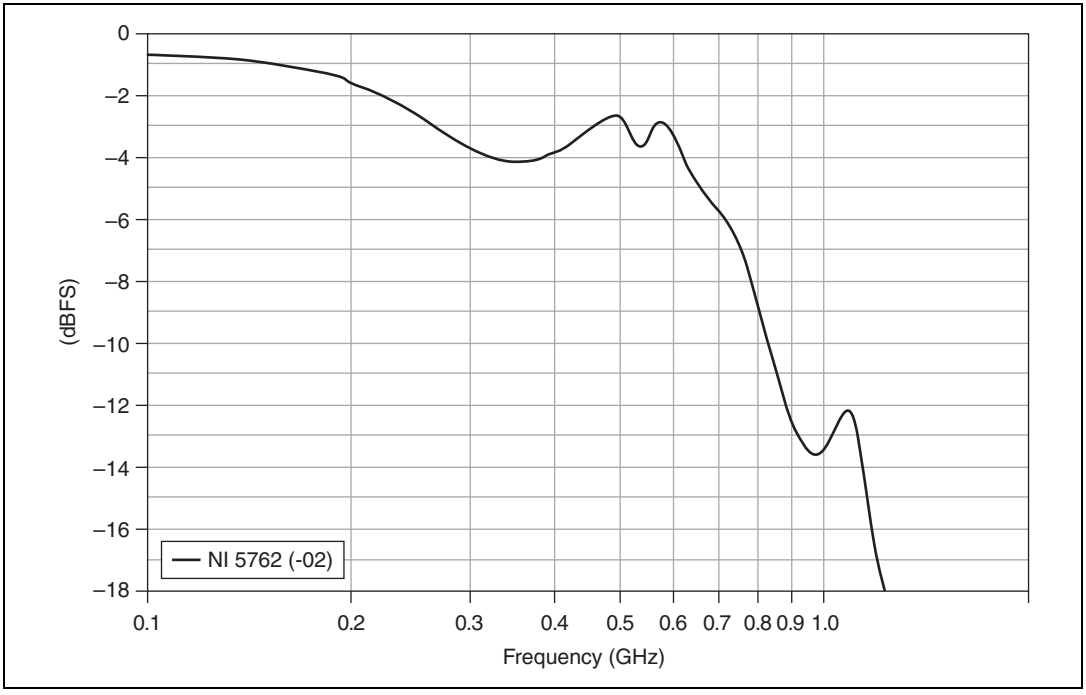


Figure 10. Frequency Response, NI 5762 (-02) only (Logarithmic Scale)

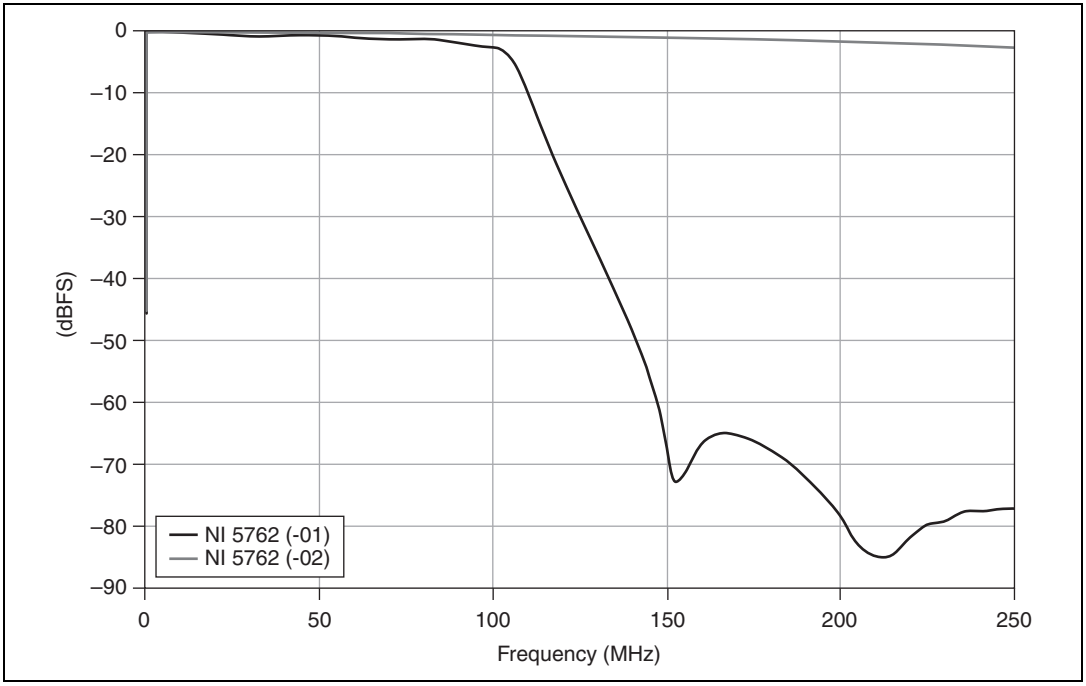


Figure 11. Frequency Response (Linear Scale)

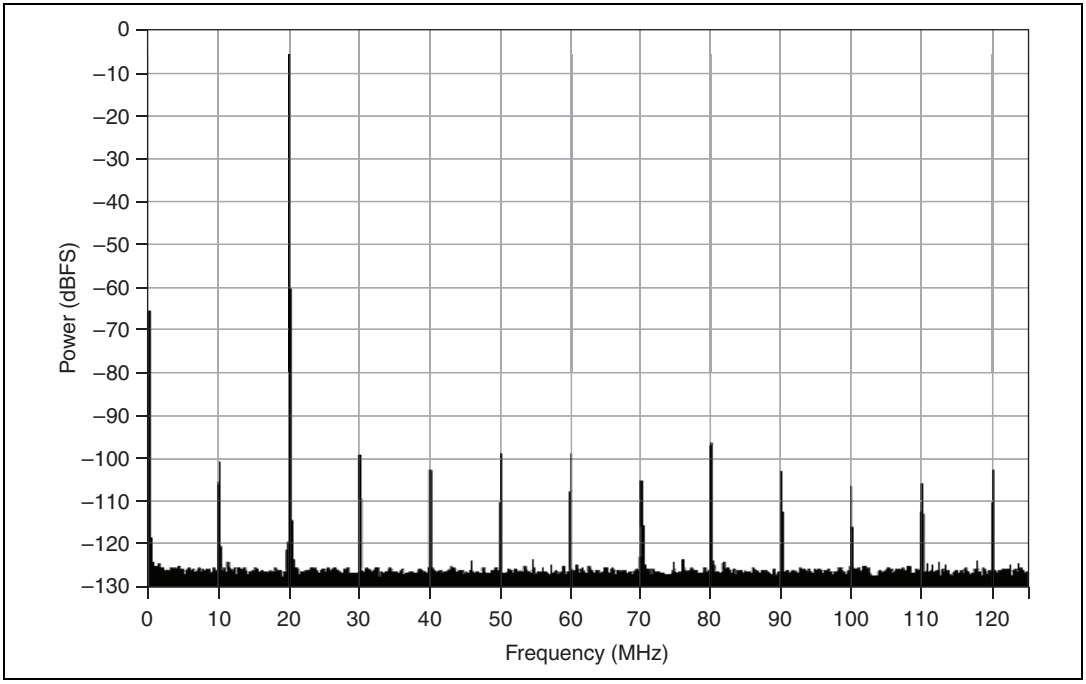


Figure 12. Single-Tone Spectrum at 20 MHz, –3.1 dBFS, SFDR –90.8 dBc, NI 5762 (-01) and NI 5762 (-02)

Table 6. Spectral Performance

Measurement	NI 5762 (-01)		NI 5762 (-02)	
	Power	**Result**	**Power**	**Result**
SNR at 10.1 MHz	–1 dBFS	74.6 dBc	–1 dBFS	75.8 dBc
SINAD at 10.1 MHz	–1 dBFS	73.3 dBc	–1 dBFS	75.2 dBc
SFDR at 10.1 MHz (with harmonics)	–6 dBFS	–88.2 dBc	–3 dBFS	–88.4 dBc
SFDR at 10.1 MHz (without harmonics)	–6 dBFS	–116 dBc	–6 dBFS	–117 dBc
IMD3 (Two Tones at 20.0 MHz and 20.1 MHz)	–7 dBFS	–97 dBFS	–7 dBFS	–97 dBFS

Analog Input Phase Noise

Average noise density .....–147 dBm/Hz or 9.98 nV/√Hz

RMS noise

PLL off.....572×10^{-15} seconds

PLL on[1].....313×10^{-15} seconds

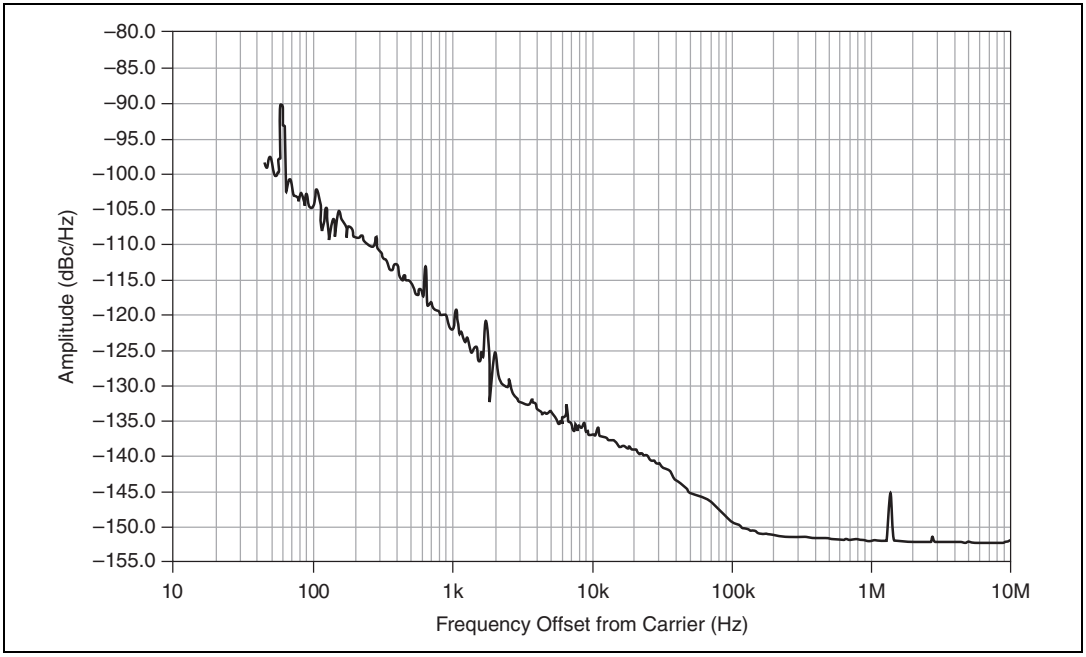


Figure 13. Analog Input Phase Noise with 100 MHz Input Signal, PLL On

[1] Measured using PXI_CLK10 as the source for the Sync Clock (IoModSyncClk) from the PXI Express backplane.

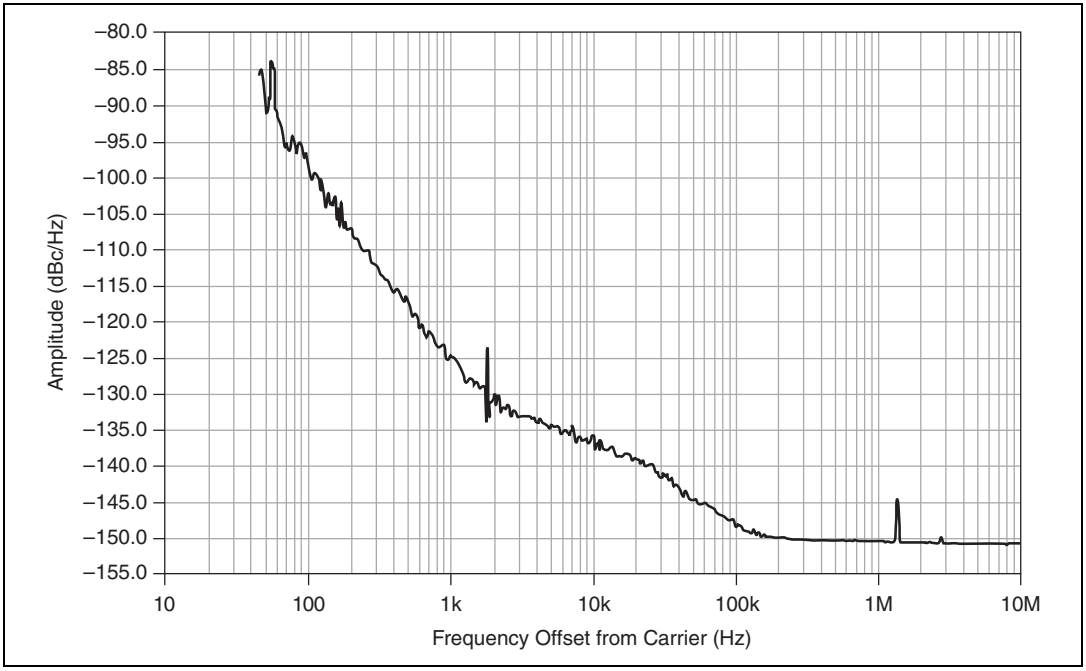


Figure 14. Analog Input Phase Noise with 100 MHz Input Signal, PLL Off

Internal Sample Clock

Clock distribution part number .....AD9511[1]

Oscillator type .....VCXO

Frequency .....250 MHz

Phase noise

10 kHz offset .....–137 dBc/Hz

100 kHz offset .....–151 dBc/Hz

Internal stability .....±1 ppm

CLK IN

Number of channels .....1, single-ended

Connector type .....SMA

Input impedance .....50 Ω

Input coupling .....AC

Input voltage range .....0.63 V_{pk-pk} to 2.0 V_{pk-pk}

Absolute maximum voltage .....±3.0 V DC, 3.0 V_{pk-pk} AC

[1] For additional information about the AD9511, refer to the Analog Devices data sheet at `www.analog.com`.

External Sample clock

Input frequency range ..... 150 MHz to 250 MHz

External Reference clock

Input frequency ..... 10 MHz

Default Settings

All specifications are measured with a default ADC reference setting of 2.5 V unless otherwise specified. The ADC reference can be configured to values from 2.0 V to 2.5 V. You can optimize the SNR and SFDR over various input frequencies and bandwidths by adjusting the ADC reference and buffer current settings.

Note For more information about the supported analog input ranges and buffer currents, refer to pages 19 and 23 of the AD9467 data sheet available at `www.analog.com`.

TRIG

General Characteristics

Number of channels ..... 1, single-ended

Connector ..... SMA

Input impedance ..... 50 Ω

Input coupling ..... DC

Input levels

Maximum V_{IL} ..... 0.9 V

Minimum V_{IH} ..... 2.0 V

Absolute maximum voltage ..... –0.5 V to 5 V

AUX I/O (Port 0 DIO <0..3>, Port 1 DIO <0..3>, and PFI <0..3>)

General Characteristics

Number of channels ..... 12 bidirectional (8 DIO and 4 PFI)

Connector type ..... HDMI

Interface standard ..... 3.3 V LVCMOS

Interface logic

Maximum V_{IL} ..... 0.8 V

Minimum V_{IH} ..... 2.0 V

Maximum V_{OL} ..... 0.4 V

Minimum V_{OH} ..... 2.7 V

Maximum V_{OH} ..... 3.6 V

Z_{out} ..... 50 Ω ± 20%

I_{out} (DC) ..... ±2 mA

Pull-down resistor ..... 150 kΩ

Recommended operating voltage ..... –0.3 V to 3.6 V

Overvoltage protection ..... ±10 V

Maximum toggle frequency.....6.6 MHz

+5 V maximum power.....10 mA

+5 V voltage tolerance.....4.2 V to 5 V

Configuration EEPROM Map

Byte Address	Size (Bytes)	Field Name
0x0	2	Vendor ID
0x2	2	Product ID
0x4	4	Serial Number
0x8	116	Reserved
0x7C	132	User Space

Caution *Only* write to *User Space*. Writing to any other offset may cause the NI 5762 to stop functioning.

Power

Total power, typical operation.....5.3 W

Physical

Dimensions.....12.9 × 2.0 × 12.1 cm
(5.1 × 0.8 × 4.7 in.)

Weight.....332 g (11.7 oz)

Front panel connectors.....SMA and HDMI

Environmental

The NI 5762 is intended for indoor use only.

Operating environment[1].....0 °C to 55 °C,
tested in accordance with IEC-60068-2-1 and IEC-60068-2-2.

Relative humidity range.....10% to 90%, noncondensing,
tested in accordance with IEC-60068-2-56.

Altitude.....2,000 m at 25 °C ambient temperature.

Pollution Degree.....2

Storage environment

Ambient temperature range.....–20 °C to 70 °C,
tested in accordance with IEC-60068-2-1 and IEC-60068-2-2.

Relative humidity range.....5% to 95%, noncondensing,
tested in accordance with IEC-60068-2-56.

[1] For PXI/PXI Express chassis configurations that group NI FlexRIO adapter modules in three or more contiguous slots, National Instruments recommends limiting the ambient operating temperature to less than 50 °C.

Note Clean the device with a soft, non-metallic brush. Make sure that the device is completely dry and free from contaminants before returning it to service.

Shock and Vibration

Operational shock .....30 g peak, half-sine, 11 ms pulse, tested in accordance with IEC-60068-2-27. Test profile developed in accordance with MIL-PRF-28800F.

Random vibration

Operating .....5 Hz to 500 Hz, 0.3 g_{rms}

Nonoperating .....5 Hz to 500 Hz, 2.4 g_{rms}, tested in accordance with IEC-60068-2-64. Nonoperating test profile exceeds the requirements of MIL-PRF-28800F, Class 3.

Safety

This product meets the requirements of the following standards of safety for electrical equipment for measurement, control, and laboratory use:

- IEC 61010-1, EN 61010-1
- UL 61010-1, CSA 61010-1

Note For UL and other safety certifications, refer to the product label or the *Online Product Certification* section.

Electromagnetic Compatibility

This product meets the requirements of the following EMC standards for electrical equipment for measurement, control, and laboratory use:

- EN 61326-1 (IEC 61326-1): Class A emissions; Basic immunity
- EN 55011 (CISPR 11): Group 1, Class A emissions
- AS/NZS CISPR 11: Group 1, Class A emissions
- FCC 47 CFR Part 15B: Class A emissions
- ICES-001: Class A emissions

Note For EMC declarations and certifications, refer to the *Online Product Certification* section of this document.

CE Compliance CE

This product meets the essential requirements of applicable European Directives as follows:

- 2006/95/EC; Low-Voltage Directive (safety)
- 2004/108/EC; Electromagnetic Compatibility Directive (EMC)

Online Product Certification

To obtain product certifications and the Declaration of Conformity for this product, visit `ni.com/certification`, search by model number or product line, and click the appropriate link in the Certification column.

Environmental Management

NI is committed to designing and manufacturing products in an environmentally responsible manner. NI recognizes that eliminating certain hazardous substances from our products is beneficial to the environment and to NI customers.

For additional environmental information, refer to the *NI and the Environment* Web page at `ni.com/environment`. This page contains the environmental regulations and directives with which NI complies, as well as other environmental information not included in this document.

Waste Electrical and Electronic Equipment (WEEE)

EU Customers At the end of the product life cycle, all products *must* be sent to a WEEE recycling center. For more information about WEEE recycling centers, National Instruments WEEE initiatives, and compliance with WEEE Directive 2002/96/EC on Waste and Electronic Equipment, visit `ni.com/environment/weee`.

电子信息产品污染控制管理办法 （中国 RoHS）

中国客户 National Instruments 符合中国电子信息产品中限制使用某些有害物质指令 (RoHS)。关于 National Instruments 中国 RoHS 合规性信息，请登录 `ni.com/environment/rohs_china`。(For information about China RoHS compliance, go to `ni.com/environment/rohs_china`.)

Where to Go for Support

The National Instruments Web site is your complete resource for technical support. At `ni.com/support` you have access to everything from troubleshooting and application development self-help resources to email and phone assistance from NI Application Engineers.

National Instruments corporate headquarters is located at 11500 North Mopac Expressway, Austin, Texas, 78759-3504. National Instruments also has offices located around the world to help address your support needs. For telephone support in the United States, create your service request at `ni.com/support` and follow the calling instructions or dial 512 795 8248. For telephone support outside the United States, visit the Worldwide Offices section of `ni.com/niglobal` to access the branch office Web sites, which provide up-to-date contact information, support phone numbers, email addresses, and current events.

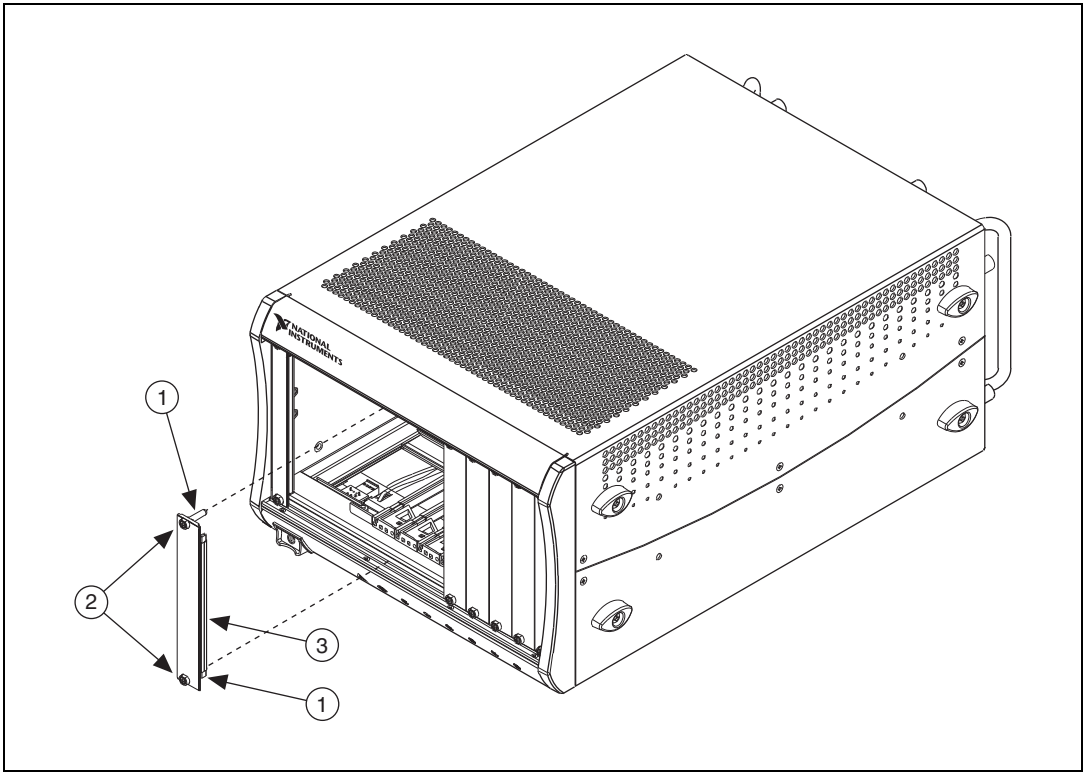
Appendix: Installing EMI Controls

To ensure specified EMC performance, HDMI cable ferrites and PXI EMC filler panels must be properly installed on your NI 5762R system. Your kit includes two HDMI cable ferrites, but PXI EMC filler panels (National Instruments part number 778700-01) must be purchased separately. For more installation information, refer to the *NI FlexRIO FPGA Module Installation Guide and Specifications*.

Installing PXI EMC Filler Panels

Complete the following instructions to install PXI EMC filler panels (National Instruments part number 778700-01) in your PXI chassis:

1. Remove the captive screw covers.
2. Install the PXI EMC filler panels by securing the captive mounting screws to the chassis, as shown in Figure 15. Make sure that the EMC gasket is on the right side of the PXI EMC filler panel.



1	Captive Screw Covers	2	Captive Mounting Screws	3	EMC Gasket

Figure 15. PXI EMC Filler Panels and Chassis

Note You must populate all slots with a module or a PXI EMC filler panel to ensure proper module cooling. Do not over tighten screws (2.5 lb · in. maximum). For additional information about the use of PXI EMC filler panels in your PXI system, visit `ni.com/info` and enter `emcpanels`.

Attaching HDMI Cable Ferrites

Complete the following instructions to attach the snap-on cable ferrites included with your kit to your HDMI cable. Install one ferrite at each end of the HDMI cable.

1. Open the ferrite by unsnapping the clasp.
2. Place the HDMI cable inside the ferrite.
3. Close the ferrite around the cable until it snaps into place.

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