C Series Reference and Procedures

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Contents

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Use this book as a reference for information about using C Series modules with NI CompactRIO Device Drivers in LabVIEW. This book contains information about the FPGA I/O functions, I/O resources, arbitration options, methods, and properties each C Series module supports in FPGA Programming mode; and information about the I/O variables and properties each C Series module supports in Scan Interface mode.

To view related topics, click the **Locate** button, shown at left, in the toolbar at the top of this window. The **LabVIEW Help** highlights this topic in the **Contents** tab so you can navigate the related topics.

C Series Module IDs

You can use the Module ID property with the FPGA I/O Property Node to read the IDs associated with C Series modules. You also can wire a reference to a module in Scan Interface mode to a generic-class property node in a VI block diagram, and select the **ProductID** property to read the ID programmatically. Note that the **ProductID** output will be displayed in decimal by default, and the following IDs are in hexadecimal.

By ID

ID	Module
0x709C	NI 9435
0x709D	NI 9411
0x709E	NI 9423
0x709F	NI 9421 with screw terminal
0x70A0	NI 9474
0x70A1	NI 9472 with screw terminal
0x70A2	NI 9481

0x70A3	NI 9211
0x70A4	NI 9201
0x70A5	NI 9221
0x70A6	NI 9215 with screw terminal
0x70A7	NI 9263
0x7129	NI 9203
0x712A	NI 9205 with DSUB
0x712B	NI 9217
0x712C	NI 9265
0x712E	NI 9421 with DSUB
0x712F	NI 9425
0x7130	NI 9401
0x7131	NI 9403
0x7132	NI 9472 with DSUB
0x7133	NI 9476
0x7135	NI 9215 with BNC
0x714F	NI 9853
0x71A1	NI 9201 with DSUB
0x71A2	NI 9221 with DSUB
0x71C2	NI 9239
0x71C3	NI 9237 with RJ-50
0x71CA	NI 9422
0x71CB	NI 9477
0x71EA	NI 9205 with spring terminal
0x71EB	NI 9206
0x71ED	NI 9505
0x71F3	NI 9852
0x71F6	NI 9485
0x72B5	NI 9234
0x72F6	NI 9264
0x72FD	NI 9229 with screw terminal
0x7304	NI 9375

0x7305	NI 9870
0x7306	NI 9871
0x730C	NI 9219
0x731A	NI 9478
0x7328	NI 9402
0x732A	NI 9235
0x732B	NI 9236
0x736A	NI 9426
0x7367	NI 9239 with BNC
0x7368	NI 9229 with BNC
0x7377	NI 9475
0x7383	NI 9225
0x73A4	NI 9237 with DSUB
0x73E0	NI 9220 with spring terminal
0x7408	NI 9225E
0x7409	NI 9481E
0x740A	NI 9211E
0x740B	NI 9203E
0x740C	NI 9403E
0x740D	NI 9215E
0x7415	NI 9269
0x7416	NI 9227
0x741C	NI 9239E
0x741D	NI 9229E
0x741E	NI 9263E
0x741F	NI 9237E
0x743A	NI 9213E
0x743B	NI 9478E
0x743F	NI 9870E
0x7440	NI 9871E
0x7441	NI 9219E
0x7442	NI 9265E

0x7445	NI 9222
0x7446	NI 9222E
0x7447	NI 9264E
0x7449	NI 9213
0x744B	NI 9205E
0x744C	NI 9227E
0x744D	NI 9269E
0x745D	NI 9215E with BNC
0x747A	NI 9375 with DSUB
0x749B	NI 9201E with screw terminal
0x749C	NI 9221E with screw terminal
0x749D	NI 9201E with DSUB
0x749E	NI 9221E with DSUB
0x74A1	NI 9505E
0x74AA	NI 9207E with DSUB
0x74AB	NI 9208E with DSUB
0x74AC	NI 9208 with DSUB
0x74AD	NI 9207 with DSUB
0x74EC	NI 9223
0x74ED	NI 9223E
0x74EE	NI 9214
0x753F	NI 9232
0x7615	NI 9220 with DSUB
0x7642	NI 9381
0x76E3	NI 9482
0x76E8	NI 9244
0x77EA	NI 9250
0x77B8	NI 9247
0x77C5	NI 9344
0x77CC	NI 9230
0x77E3	NI 9246
0x77E9	NI 9251

0x777E	NI 9361
0x7786	NI 9260 with BNC
0x778C	NI 9260 with mini XLR
0x780D	NI 9224
0x780E	NI 9228
0x7827	NI 9770
0x7889	NI 9775
0x788A	NI 9202 with DSUB
0x788C	NI 9202 with spring terminal
0x788F	NI 9266
0x78B1	NI 9210
0x78B6	NI 9262 with DSUB
0x7900	NI 9476 with spring terminal
0x7930	NI 9231
0x79C4	NI 9253
0x79C8	NI 9252 with screw terminal
0x79CA	NI 9252 with DSUB
0x7A59	NI 9470
0x7A5E	NI 9326

By Module

Module	ID
NI 9201	0x70A4
NI 9201 with DSUB	0x71A1
NI 9201E with DSUB	0x749D
NI 9201E with screw terminal	0x749B
NI 9202 with DSUB	0x788A
NI 9202 with spring terminal	0x788C
NI 9203	0x7129
NI 9203E	0x740B
NI 9205 with DSUB	0x712A
NI 9205 with spring terminal	0x71EA

NI 9205E	0x744B
NI 9206	0x71EB
NI 9207 with DSUB	0x74AD
NI 9207E with DSUB	0x74AA
NI 9208 with DSUB	0x74AC
NI 9208E with DSUB	0x74AB
NI 9210	0x78B1
NI 9211	0x70A3
NI 9211E	0x740A
NI 9213	0x7449
NI 9213E	0x743A
NI 9214	0x74EE
NI 9215 with BNC	0x7135
NI 9215 with screw terminal	0x70A6
NI 9215E with BNC	0x745D
NI 9215E with screw terminal	0x740D
NI 9217	0x712B
NI 9219	0x730C
NI 9219E	0x7441
NI 9220 with spring terminal	0x73E0
NI 9220 with DSUB	0x7615
NI 9221	0x70A5
NI 9221 with DSUB	0x71A2
NI 9221E with DSUB	0x749E
NI 9221E with screw terminal	0x749C
NI 9222	0x7445
NI 9222E	0x7446
NI 9223	0x74EC
NI 9223E	0x74ED
NI 9224	0x780D
NI 9225	0x7383
NI 9225E	0x7408

NI 9227	0x7416
NI 9227E	0x744C
NI 9228	0x780E
NI 9229 with screw terminal	0x72FD
NI 9229E	0x741D
NI 9229 with BNC	0x7368
NI 9230	0x77CC
NI 9231	0x7930
NI 9232	0x753F
NI 9234	0x72B5
NI 9235	0x732A
NI 9236	0x732B
NI 9237 with DSUB	0x73A4
NI 9237 with RJ-50	0x71C3
NI 9237E	0x741F
NI 9239	0x71C2
NI 9239E	0x741C
NI 9239 with BNC	0x7367
NI 9244	0x76E8
NI 9246	0x77E3
NI 9247	0x77B8
NI 9250	0x77EA
NI 9251	0x77E9
NI 9252 with screw terminal	0x79C8
NI 9252 with DSUB	0x79CA
NI 9253	0x79C4
NI 9260 with BNC	0x7786
NI 9260 with mini XLR	0x778C
NI 9262 with DSUB	0x78B6
NI 9263	0x70A7
NI 9263E	0x741E
NI 9264	0x72F6

NI 9264E	0x7447
NI 9265	0x712C
NI 9265E	0x7442
NI 9266	0x788F
NI 9269	0x7415
NI 9269E	0x744D
NI 9326	0x7A5E
NI 9344	0x77C5
NI 9361	0x777E
NI 9375	0x7304
NI 9375 with DSUB	0x747A
NI 9381	0x7642
NI 9401	0x7130
NI 9402	0x7328
NI 9403	0x7131
NI 9403E	0x740C
NI 9411	0x709D
NI 9421 with DSUB	0x712E
NI 9421 with screw terminal	0x709F
NI 9422	0x71CA
NI 9423	0x709E
NI 9425	0x712F
NI 9426	0x736A
NI 9435	0x709C
NI 9470	0x7A59
NI 9472 with DSUB	0x7132
NI 9472 with screw terminal	0x70A1
NI 9474	0x70A0
NI 9475	0x7377
NI 9476	0x7133
NI 9476 with spring terminal	0x7900
NI 9477	0x71CB

NI 9478	0x731A
NI 9478E	0x743B
NI 9481	0x70A2
NI 9481E	0x7409
NI 9482	0x76E3
NI 9485	0x71F6
NI 9505	0x71ED
NI 9505E	0x74A1
NI 9770	0x7827
NI 9775	0x7889
NI 9852	0x71F3
NI 9853	0x714F
NI 9870	0x7305
NI 9870E	0x743F
NI 9871	0x7306
NI 9871E	0x7440

Analog Input Modules

Use this book as a reference for the following information:

- FPGA I/O functions, I/O resources, arbitration options, methods, and properties each C Series analog input module supports in FPGA Interface mode
- I/O variables and properties each C Series analog input module supports in Scan Interface mode
- Instructions for using LabVIEW with CompactRIO analog input devices

To view related topics, click the **Locate** button, shown at left, in the toolbar at the top of this window. The **LabVIEW Help** highlights this topic in the **Contents** tab so you can navigate the related topics.

Converting and Calibrating CompactRIO Analog Input Values (FPGA Interface)

Set the **Calibration Mode** to **Calibrated** in the **C Series Module Properties** dialog box for an analog input module if you want the FPGA I/O Node to return calibrated, fixed-point data for the module. If you set the **Calibration Mode** to **Raw**, the FPGA I/O Node returns uncalibrated, binary values for the following analog input modules:

- NI 9201
- NI 9202
- NI 9203
- NI 9205
- NI 9206
- NI 9215
- NI 9216
- NI 9217
- NI 9218
- NI 9220
- NI 9221
- NI 9222
- NI 9223
- NI 9224
- NI 9225
- NI 9226
- NI 9227
- NI 9228
- NI 9229
- NI 9230
- NI 9231
- NI 9232
- NI 9234
- NI 9235
- NI 9236
- NI 9237
- NI 9238
- NI 9239
- NI 9246
- NI 9247
- NI 9250
- NI 9251
- NI 9252
- NI 9253
- NI 9381

If you set the **Calibration Mode** to **Raw**, you must convert the binary values into meaningful engineering units and apply calibration constants to achieve more accurate results. You must convert and calibrate these values in the host VI.

Note After you convert the binary values to engineering units for the NI 9217, you can also convert the nominal resistance values into temperature values.

Note The binary data returned by some modules is already calibrated. Refer to the topics listed in the following table for information about converting values into engineering units:

Module	Link for More Information
NI 9202	Converting NI 9202 Data
NI 9207	Converting NI 9207 Data
NI 9208	Converting NI 9208 Data
NI 9211	Converting NI 9211 Data
NI 9212	Converting NI 9212 Data
NI 9213	Converting NI 9213 Data
NI 9214	Converting NI 9214 Data
NI 9219	Converting NI 9219 Data
NI 9224	Converting NI 9224 Data
NI 9228	Converting NI 9228 Data
NI 9231	Converting NI 9231 Data
NI 9242	Converting NI 9242 and NI 9244 Data
NI 9244	Converting NI 9242 and NI 9244 Data
NI 9250	Converting NI 9250 Data
NI 9251	Converting NI 9251 Data
NI 9252	Converting NI 9252 Data
NI 9253	Converting NI 9253 Data

Using a VI to Convert and Calibrate Values

For the NI 9205, you can also refer to the Binary to Nominal Polynomial (Host) VI in the `labview\examples\CompactRIO\Module Specific\NI 9205\NI 9205 Linearization Coefficients\NI 9205 Linearization Coefficients.lvproj` for an example of using the straight-line conversion algorithm along with the NI-MCal linearization correction to convert binary analog input values to calibrated engineering units. You can use the Binary to Nominal Polynomial (Host) VI as a subVI in the host VI.

Open example (NI 9205)

For the NI 9206, you can also refer to the Binary to Nominal Polynomial (Host) VI in the `labview\examples\CompactRIO\Module Specific\NI 9206\NI 9206 Linearization Coefficients\NI 9206 Linearization Coefficients.lvproj` for an example of using the straight-line conversion algorithm along with the NI-MCal linearization correction to convert binary analog input values to calibrated engineering units. You can use the Binary to Nominal Polynomial (Host) VI as a subVI in the host VI.

Open example (NI 9206)

Using an Equation to Convert and Calibrate Values

You can use the following equation in the host VI to convert binary analog input values to calibrated engineering units:

Input Engineering Units = (**Binary Value** × **LSB Weight** – **Offset**)*

where

Binary Value is the signed or unsigned value returned by the FPGA I/O Node

LSB Weight is the value returned by the LSB Weight property

Offset is the value returned by the Offset property.

The units of **LSB Weight** and **Offset** differ per module. Refer to the reference topic for the module you are using for the **LSB Weight** and **Offset** units. You can find the reference topic for the module by navigating on the **Contents** tab to **FPGA**

Module»CompactRIO Reference and Procedures»Analog Input Modules»NI 9xxx.

To convert to calibrated engineering units, use the FPGA I/O Property Node to read the LSB Weight and Offset properties. If you do not want to read the LSB Weight and Offset values from the module, you can convert to uncalibrated engineering units by using the following values for **Offset** and **LSB Weight**:

Offset = 0†

LSB Weight = **Typical Input Span** ÷ $2^{\textbf{ADC Resolution}}$

where

Typical Input Span is the value for the module in the table below

ADC Resolution is the ADC resolution value in the hardware documentation for the module

Module	Typical Input Span
NI 9201	21.06 V
NI 9203	21.56 mA (unipolar), 43.12 mA (bipolar)
NI 9205	20.8 V
NI 9206	21.5 V
NI 9215	20.8 V
NI 9216	100 Ω RTD
NI 9217	100 Ω RTD
NI 9218	Varies by mode
NI 9220	20.8 V
NI 9221	125 V
NI 9222	21.2 V
NI 9223	21.2 V
NI 9225	850 V
NI 9226	1000 Ω RTD
NI 9227	29.954 A
NI 9229	125.28 V
NI 9230	63 V
NI 9232	63 V

NI 9234	10.2 V
NI 9235	52.6 mV/V
NI 9236	52.6 mV/V
NI 9237	50 mV/V
NI 9238	1.25 V
NI 9239	21.04 V
NI 9246	62.5 A
NI 9247	294 A
NI 9381	5 V

*When converting and calibrating data acquired from the NI 9203 in ±20 mA range, the equation is:

Input Engineering Units = ((**Binary Value** – 32768) × **LSB Weight** – **Offset**)

†When calculating engineering units for the NI 9203 in ±20 mA range, **Offset** = 20 mA.

Detecting Out-of-Range Channels for CompactRIO Analog Input Channels (FPGA Interface)

You can detect an out-of-range CompactRIO analog input channel when you read the channel. If you set the **Calibration Mode** to **Calibrated** in the **C Series Module Properties** dialog box and the FPGA I/O Node returns a value greater than the minimum operating range value, the channel might be out of range. Refer to the hardware documentation for the module for more information about module specifications.

If you set the **Calibration Mode** to **Raw** in the **C Series Module Properties** dialog box and a channel is out of range, the FPGA I/O Node returns the full-scale binary value, as shown in the table below.

Module	Full-Scale Binary Value
NI 9201	–2,048 (0xF800) or 2,047 (0x7FF)
NI 9202*	–8,388,608 (0xFF800000) or 8,388,607 (0x7FFFFF)
NI 9203	0 (0x0000) or 65,535 (0xFFFF)

NI 9205*	–32,768 (0x8000) or 32,767 (0x7FFF)
NI 9206*	–32,768 (0x8000) or 32,767 (0x7FFF)
NI 9207	–8,388,608 (0xFF800000) or 8,388,607 (0x7FFFFF)
NI 9208	–8,388,608 (0xFF800000) or 8,388,607 (0x7FFFFF)
NI 9209	–8,388,608 (0xFF800000) or 8,388,607 (0x7FFFFF)
NI 9210	–8,388,608 (0xFF800000) or 8,388,607 (0x7FFFFF)
NI 9211	–8,388,608 (0xFF800000) or 8,388,607 (0x7FFFFF)
NI 9212	–8,388,608 (0xFF800000) or 8,388,607 (0x7FFFFF)
NI 9213	–8,388,608 (0xFF800000) or 8,388,607 (0x7FFFFF)
NI 9214	–8,388,608 (0xFF800000) or 8,388,607 (0x7FFFFF)
NI 9215	–32,768 (0x8000) or 32,767 (0x7FFF)
NI 9217	–8,388,608 (0xFF800000) or 8,388,607 (0x7FFFFF)
NI 9218	–8,388,608 (0xFF800000) or 8,388,607 (0x7FFFFF)
NI 9219	–8,388,608 (0xFF800000) or 8,388,607 (0x7FFFFF)
NI 9220	–32,768 (0x8000) or 32,767 (0x7FFF)
NI 9221	–2,048 (0xF800) or 2,047 (0x7FF)
NI 9222	–32,768 (0x8000) or 32,767 (0x7FFF)
NI 9223	–32,768 (0x8000) or 32,767 (0x7FFF)
NI 9224*	–8,388,608 (0xFF800000) or 8,388,607 (0x7FFFFF)
NI 9225	–8,388,608 (0xFF800000) or 8,388,607 (0x7FFFFF)
NI 9227	–8,388,608 (0xFF800000) or 8,388,607 (0x7FFFFF)

NI 9228*	–8,388,608 (0xFF800000) or 8,388,607 (0x7FFFFF)
NI 9229	–8,388,608 (0xFF800000) or 8,388,607 (0x7FFFFF)
NI 9230	–8,388,608 (0xFF800000) or 8,388,607 (0x7FFFFF)
NI 9231*	–8,388,608 (0xFF800000) or 8,388,607 (0x7FFFFF)
NI 9232	–8,388,608 (0xFF800000) or 8,388,607 (0x7FFFFF)
NI 9234	–8,388,608 (0xFF800000) or 8,388,607 (0x7FFFFF)
NI 9235	–8,388,608 (0xFF800000) or 8,388,607 (0x7FFFFF)
NI 9236	–8,388,608 (0xFF800000) or 8,388,607 (0x7FFFFF)
NI 9237	–8,388,608 (0xFF800000) or 8,388,607 (0x7FFFFF)
NI 9238	–8,388,608 (0xFF800000) or 8,388,607 (0x7FFFFF)
NI 9239	–8,388,608 (0xFF800000) or 8,388,607 (0x7FFFFF)
NI 9242*	–8,388,608 (0xFF800000) or 8,388,607 (0x7FFFFF)
NI 9244*	–8,388,608 (0xFF800000) or 8,388,607 (0x7FFFFF)
NI 9246	–8,388,608 (0xFF800000) or 8,388,607 (0x7FFFFF)
NI 9247	–8,388,608 (0xFF800000) or 8,388,607 (0x7FFFFF)
NI 9250*	–8,388,608 (0xFF800000) or 8,388,607 (0x7FFFFF)
NI 9251*	–8,388,608 (0xFF800000) or 8,388,607 (0x7FFFFF)
NI 9252*	–8,388,608 (0xFF800000) or 8,388,607 (0x7FFFFF)

NI 9253*	–8,388,608 (0xFF800000) or 8,388,607 (0x7FFFFF)
NI 9381	0 (0x0000) or 4,095 (0x0FFF)

*For the NI 9202/9205/9206/9224/9228/9231/9242/9244/9250/9251/9252/9253, a channel might be out of range before the FPGA I/O Node reaches the minimum or maximum full-scale binary value.

Synchronizing Multiple Modules (FPGA Interface)

You can synchronize multiple modules that are connected to the same FPGA device if your application meets the following requirements:

- The modules must use the same master timebase source
- The modules must start acquisition mode at the same time
- A single FPGA I/O Node function must read the synchronous data

You must create FPGA I/O items for the module before you can configure the items using the FPGA I/O Node. Develop the FPGA VI to meet the guidelines described in the following table.

For delta-sigma modules, you will need to synchronize multiple sample rates.

Guideline	Details
Share a master timebase source	Configure the modules to share master timebase source.
Start the synchronized acquisition	▪ Configure an FPGA I/O Node with **Start** channels for the module you want to synchronize. ▪ Wire a Boolean constant set to TRUE to each **Start** channel. ▪ Ensure that all I/O channels are in the same FPGA I/O Node. Otherwise, the FPGA I/O Node will not return synchronized data.

Acquire data from synchronized modules with the same data rate	▪ Configure an FPGA I/O Node with all of the channels from which you want to synchronously sample. ▪ Ensure that all I/O channels are in the same FPGA I/O Node. Otherwise, the FPGA I/O Node will not return synchronized data. ▪ Refer to the Synchronizing NI 923x Modules (FPGA) VI in `labview\examples\CompactRIO\Module Specific\NI 923x\Synchronizing NI 923x Modules\Synchronizing NI 923x Modules.lvproj` for an example of synchronizing multiple modules with the same data rate.
Acquire data from synchronized modules with different data rates	▪ If you synchronize modules that are configured for different data rates, create a separate loop for each data rate in the FPGA VI. ▪ In each loop, configure an FPGA I/O Node with all of the channels that are configured for the data rate of that loop. If you place channels that are configured for different rates in the same loop, LabVIEW returns an overrun warning, error 65539, from the FPGA I/O Node when you run the VI. ▪ A delay occurs before the FPGA I/O Node returns the first data point. The length of the delay depends on the data rate and model number of the module. The equation for the delay is provided in the following table.
Understand the maximum sample rate when synchronizing multiple modules	—

Equation for synchronizing multiple samples rates

Module	Decimation Rate, **m**	Clock Divider, **n**	Time to First Sample (s)

NI 9231, NI 9250, NI 9251	32	n = 1	(281.625 * **m** * **n** + 5.5) * **Master_Timebase_Period** ± 1 **Master_Timebase_Period**
	64	n = 1	(281.625 * **m** * **n** + 8.5) * **Master_Timebase_Period** ± 1 **Master_Timebase_Period**
	128, ..., 1,024	n = 1	(281.625 * **m** * **n** + 6.5) * **Master_Timebase_Period** ± 1 **Master_Timebase_Period**
	32, ..., 1,024	n = 2, ..., 12	(281.625 * **m** * **n** + 5.5) * **Master_Timebase_Period** ± 1 **Master_Timebase_Period**
NI 9218, NI 9225, NI 9227, NI 9229, NI 9234, NI 9237, NI 9238, NI 9239, NI 9242, NI 9244, NI 9246, NI 9247	256	n = 1	(8.5 + **n** * 34,152) * **Master_Timebase_Period**
		n = 2, ..., 31	(5.5 + **n** * 34,152) * **Master_Timebase_Period**
NI 9230, NI 9232	64	n = 1, ..., 31	77/**Fs** + 4-5 **Master_Timebase_Period**
	128	n = 1, ..., 31	72/**Fs** + 4-5 **Master_Timebase_Period**
	256	n = 1, ..., 31	68/**Fs** + 4-5 **Master_Timebase_Period**
NI 9235, NI 9236	512	n = 1, ..., 31	39/**Fs** + 110.5 MClk + 1 OClk + **Analog Delay**

Notes:

Master_Timebase_Period = period of the internal or external clock that the module uses (1/13.1072 MHz, 1/12.8 MHz, or 1/10 MHz).

Fs = sample rate.

The divider and decimation rate depend on which sample rate you select. The datasheet for each modules provides an equation to help you determine the clock divider and decimation rate and/or lists the clock divider and decimation rate for each sample rate.

- For example, the NI 9232 Datasheet lists the decimation rate as 64 and clock divider as 1 when sampling at 102.4 kHz.

- Using the equation in the NI 9218 Datasheet, we can determine that the clock divider is 1 when the sample rate is 51.2 kHz. **n** = Master_Timebase_Frequency/256/**fs** (this is the equation provided in the NI 9218 Datasheet reorganized to solve for **n**).

Equation for synchronizing multiple samples rates

Module	Clock Divider, **b**	Time to First Sample (s)
NI 9202	1	((5.40625 + **e**) * **a** * **b** * **c** * **d** + 4.5) * **Master_Timebase_Period** ± 1 **Master_Timebase_Period**
	2, ..., 11	((5.40625 + **e**) * **a** * **b** * **c** * **d** + 5.5) * **Master_Timebase_Period** ± 1 **Master_Timebase_Period**

Notes:
Master_Timebase_Period = period of the internal or external clock that the module uses (1/13.1072 MHz, 1/12.8 MHz, or 1/10 MHz).
a = ADC Decimation Rate
b = Timebase Clock Divider
c = ADC Clock Divider
d = Filter Decimation Rate
e = Filter Frequency

- 0 for notch at Fs
- 1 for notch at Fs/2
- 3 for notch at Fs/4
- 7 for notch at Fs/8
- 15 for notch at Fs/16

Refer to the NI 9202 Datasheet on ni.com for the values of **a**, **b**, **c**, and **d** for each sample rate.

Equation for synchronizing multiple samples rates

Module	Filter	Clock Divider, **b**	Time to First Sample (s)
NI 9252, NI 9253	Comb	2	((5.40625 + **b**) * **128** * **a** + 8.5) * **Master_Timebase_Period** ± 1 **Master_Timebase_Period**
		Others	((5.40625 + **b**) * **128** * **a** + **5**.5) * **Master_Timeb**

			ase_Period ± 1 **Master_Timebase_Period**
	Butterworth	2	(5.40625 * **128** * **a** + 8.5) * **Master_Timebase_Period** ± 1 **Master_Timebase_Period**
		Others	(5.40625 * **128** * **a** + 5.5) * **Master_Timebase_Period** ± 1 **Master_Timebase_Period**

Notes:
Master_Timebase_Period = period of the internal or external clock that the module uses (1/13.1072 MHz, 1/12.8 MHz, or 1/10 MHz).
a = Decimation Rate
b = Filter Frequency

- 0 for Filter Frequency—1 (notch at Fs)
- 1 for Filter Frequency—2 (notch at Fs/2)
- 3 for Filter Frequency—3 (notch at Fs/4)
- 7 for Filter Frequency—4 (notch at Fs/8)
- 15 for Filter Frequency—5 and 6 (notch at Fs/16)

Refer to the NI 9252 or NI 9253 Datasheet on ni.com for the values of **a** for each sample rate.

Related Topics

Configuring the Master Timebase Source for a Module

Understanding the Maximum Sample Rate when Synchronizing Multiple Modules (FPGA Interface)

Configuring the Master Timebase Source for a Module (FPGA Interface)

The information in this topic applies to the following modules:

- NI 9202
- NI 9218
- NI 9225
- NI 9232
- NI 9234
- NI 9235
- NI 9242
- NI 9244
- NI 9246
- NI 9253
- NI 9260
- NI 9469

- NI 9227
- NI 9229
- NI 9230
- NI 9231
- NI 9236
- NI 9237
- NI 9238
- NI 9239
- NI 9247
- NI 9250
- NI 9251
- NI 9252
- NI 9770
- NI 9775
- NI 9470

In a system that contains more than one of these modules, you can configure one module as the master timebase source (**master**) and configure the other modules to use that master timebase source (**slaves**). Sharing the same master timebase source allows you to synchronize multiple modules. The master timebase source is divided to acquire data at the data rate you configure.

Note The NI 9151 R Series Expansion chassis does not support synchronizing multiple modules.

Note The NI 9770 does not support synchronization with other non-NI 9770 modules.

Note You can only use another NI 9775 or the NI 9469 as the master timebase source for the NI 9775. If you select the NI 9469, you can only use the 12.8 MHz clock as the exported clock frequency.

Configuring the Onboard Clock of a Module as the Master Timebase Source

Complete the following steps to configure the internal Onboard Clock of one module as the master timebase source.

1. Configure the CompactRIO system, and add a module.
2. Right-click the module in the **Project Explorer** window and select **Properties** to launch the **C Series Module Properties** dialog box.
3. Select **<Onboard Clock>** from the **Master Timebase Source** pull-down menu.
4. Click the **OK** button.
5. Select **File»Save All** in the **Project Explorer** window.

Configuring a Master Module to Share the Master Timebase Source with Slaves

Complete the following steps to configure the master timebase source for a master module and share that timebase with slave modules.

1. Configure the CompactRIO system, and add the module you want to use as the master.
2. Right-click the module in the **Project Explorer** window and select **Properties** to launch the **C Series Module Properties** dialog box.
3. Select **<Onboard Clock>** from the **Master Timebase Source** pull-down menu.
4. Place a checkmark in the **Export Onboard Clock** checkbox.
5. Add a module you want to use as a slave.
6. Right-click the slave module in the **Project Explorer** window and select **Properties** to display the **C Series Module Properties** dialog box.
7. Select the name of the master module from the **Master Timebase Source** pull-down menu.
8. Repeat steps 5 through 7 for each slave module you want to configure.
9. Click the **OK** button.
10. Select **File»Save All** in the **Project Explorer** window.

Related Topics

Synchronizing Multiple Modules (FPGA Interface)

Understanding the Maximum Sample Rate when Synchronizing Multiple Modules (FPGA Interface)

Modules with a Selectable Timebase Source

To synchronize multiple modules, you must configure the modules to share the same master timebase source. You can select the timebase source for the following modules, which allows you to configure them to share the same master timebase source:

- NI 9202
- NI 9218
- NI 9225
- NI 9227
- NI 9229
- NI 9230
- NI 9231
- NI 9232
- NI 9234
- NI 9235
- NI 9236
- NI 9237
- NI 9238
- NI 9239
- NI 9242
- NI 9244
- NI 9246
- NI 9247
- NI 9250
- NI 9251
- NI 9252
- NI 9253
- NI 9260
- NI 9469
- NI 9770
- NI 9775

Note The NI 9151 R series Expansion chassis does not support synchronizing multiple modules.

Note The NI 9770 does not support synchronization with other non-NI 9770 modules.

Note The NI 9775 can only be a slave to an NI 9469 module with a 12.8 MHz timebase. Otherwise, it can only be a master.

Related Topics

Configuring the Master Timebase Source for a Module

Understanding the Maximum Sample Rate when Synchronizing Multiple Modules (FPGA Interface)

Synchronizing Multiple Modules (FPGA Interface)

Understanding the Maximum Sample Rate when Synchronizing Multiple Modules (FPGA Interface)

The modules listed below derive their sampling rate from the internal master timebase.

Select a module to show more information about the internal master timebase and maximum sample rate for each module.

Show information for:

- Select a module -
number

Internal master timebase		value
Maximum sample rate		
	when module uses internal master timebase[1]	value
	when module is a slave[2] to - Select a master module -	value

1	The maximum sample rate for a module using the internal master timebase and is not sourcing the timebase to different model types.
2	When synchronizing multiple modules, the maximum sample rate of a slave module depends on the frequency of the master module internal master timebase. The maximum sample rate of the system is the lowest sample rate of all the modules being synchronized.

Related Topics

Configuring the Master Timebase Source for a Module (FPGA Interface)

Synchronizing Multiple Modules (FPGA Interface)

Acquiring Data from a Module (FPGA Interface)

The information in this topic applies to the following modules:

- NI 9202
- NI 9218
- NI 9225
- NI 9227
- NI 9229
- NI 9234
- NI 9235
- NI 9236
- NI 9237
- NI 9238
- NI 9246
- NI 9247
- NI 9250
- NI 9251
- NI 9252

- NI 9230
- NI 9231
- NI 9232
- NI 9239
- NI 9242
- NI 9244
- NI 9253
- NI 9770
- NI 9775

The module has input channels that are sampled simultaneously at the data rate for which you have configured the module. Use the **Start** and **Stop** channels to put the module in and out of acquisition mode, in which the module can only acquire data. Use the FPGA I/O Node to read the data from the module. While the module is in acquisition mode, you cannot perform other operations with the module, such as accessing properties or, for some modules, TEDS information.

Note You must create FPGA I/O items for the module before you can configure the items using the FPGA I/O Node.

Putting the Module in Acquisition Mode

Complete the following steps to put the module in acquisition mode.

1. Configure an FPGA I/O Node with the **Start** channel of the module.
2. Wire a Boolean constant set to TRUE to the **Start** input of the FPGA I/O Node to send a synchronization pulse to the module. The module starts acquiring data at the data rate you configure.

Reading Data from the Module

When the module starts acquiring data, you can use an FPGA I/O Node to read data from the module. You can connect the AI output of the FPGA I/O Node (or, for the NI 9770, the RF In/I or RF In/Q items) to various types of functions, including an FPGA Memory function or an FPGA FIFO function. If you read from multiple channels on the module, place the channels in the same FPGA I/O Node to ensure that the VI reads the data synchronously.

Because the module internally acquires data at a specified rate, the FPGA I/O Node does not return data until new data has been acquired by the module. If the module did not start acquiring data or stops acquiring data while an FPGA I/O Node is waiting for data from the module, the FPGA I/O Node returns I/O Not Start error 65582.

Exiting Acquisition Mode

Complete the following steps to exit acquisition mode.

1. Configure an FPGA I/O Node with the **Stop** channel of the module.
2. Write a TRUE to the **Stop** input. The module is no longer in acquisition mode and you can now access its properties or, for some modules, TEDS information.

Example

Refer to the module Getting Started (FPGA) VI at `labview\examples\CompactRIO\Module Specific\<module>\<module> Getting Started` for an example of reading from the module.

Configuring the Data Rate for a Module (FPGA Interface)

The information in this topic applies to the following modules:

- NI 9202
- NI 9218
- NI 9225
- NI 9227
- NI 9229
- NI 9230
- NI 9231
- NI 9232
- NI 9234
- NI 9235
- NI 9236
- NI 9237
- NI 9238
- NI 9239
- NI 9242
- NI 9244
- NI 9246
- NI 9247
- NI 9250
- NI 9251
- NI 9252
- NI 9253
- NI 9260
- NI 9770
- NI 9775

You can configure the rate at which the module acquires and returns data at edit time using the **C Series Module Properties** dialog box. You can programmatically change the data rate at run time using the FPGA I/O Property Node. The execution of an I/O Property Node that is configured with a **Data Rate** property overwrites the value you configured in the **C Series Module Properties** dialog box.

Configuring the Data Rate Using the C Series Module Properties Dialog Box

Complete the following steps to configure the data rate for the module using the **C Series Module Properties** dialog box.

1. Configure the CompactRIO system, and add the module.
2. Right-click the module in the **Project Explorer** window and select **Properties** to launch the **C Series Module Properties** dialog box.
3. Select the rate from the **Data Rate** pull-down menu.
4. Click the **OK** button.
5. Select **File»Save All** in the **Project Explorer** window.

Configuring the Data Rate Using the FPGA I/O Property Node

Complete the following steps to configure the data rate for the module using the FPGA I/O Property Node.

1. Place an FPGA I/O Property Node on the block diagram and configure it for the module.
2. Click the **Property** section and select **Data Rate** from the shortcut menu.
3. Right-click the **Data Rate** input and select **Create»Control** from the shortcut menu.
4. On the front panel of the VI, select a rate from the **Data Rate** pull-down menu.

You can change the data rate at run time by writing to the control from the host VI. Refer to the module Getting Started (FPGA) VI at `labview\examples\CompactRIO\Module Specific\<module>\<module> Getting Started` for an example of configuring the data rate using the FPGA I/O Property Node.

Troubleshooting

The **Data Rate** property might return error 65538 if the module is acquiring data. You must use the **Stop** channel to stop acquiring data before you can write properties to the module.

Accessing TEDS Information from a Module (FPGA Interface)

The information in this topic applies to the following modules:

- NI 9218
- NI 9219
- NI 9230
- NI 9231
- NI 9232
- NI 9234
- NI 9237
- NI 9250

You can access Transducer Electronic Data Sheet (TEDS) information from TEDS-compatible transducers connected to the channels of the module. You must enable TEDS support for the module before you can read TEDS information. You can access TEDS information only from the host VI.

Enabling TEDS Support

Complete the following steps to enable TEDS support for the module.

1. Configure the CompactRIO system, and add the module.
2. Right-click the module in the **Project Explorer** window and select **Properties** to launch the **C Series Module Properties** dialog box.
3. Place a checkmark in the **Enable TEDS Support** checkbox.
4. Click the **OK** button.

The FPGA VI must have an FPGA I/O Node or an FPGA I/O Property Node that communicates with the module. If it does not, the LabVIEW FPGA Compile Server optimizes the VI when you compile it, and the host VI cannot communicate with the module.

Reading TEDS Information in the Host VI

After you develop the FPGA VI and open a reference to it in the host VI, complete the following steps to read TEDS information from the module.

Note The host VI cannot access TEDS information while the module is in acquisition mode. The module must exit acquisition mode before the host VI can access TEDS information.

1. Place an Invoke Method function on the block diagram.
2. Wire the **FPGA VI Reference Out** output of the Open FPGA VI Reference function to the **FPGA VI Reference In** input of the Invoke Method function.
3. Click **Method** on the Invoke Method function and select Read TEDS from the shortcut menu.
4. Right-click the **Slot** or **Connector** input of the Invoke Method function and select **Create»Constant** or **Create»Control** from the shortcut menu. Configure the constant or control for the slot of the module. Valid slot values are 1 through **N**, where **N** is the number of slots in the chassis.
5. Right-click the **Channel** input of the Invoke Method function and select **Create»Constant** from the shortcut menu. Configure the constant for the channel on the module for which you want to read TEDS information.

Modules	Valid Channel Values
NI 9218	0 through 1
NI 9219	0 through 3
NI 9230	0 through 2
NI 9231	0 through 7
NI 9232	0 through 2
NI 9234	0 through 3
NI 9237	0 through 3
NI 9250	0 through 1

6. Add a TEDS_Parse Binary TEDS VI, available on the **TEDS** palette, to the block diagram.

   Add Find

7. Add a TEDS_Data to Table VI, available on the **TEDS** palette, to the block diagram.

   Add Find

8. Wire the **TEDS Binary** output of the Invoke Method function to the **binary TEDS array** input of the TEDS_Parse Binary TEDS VI.

9. Wire the **v0.9 (TEDS)** output of the Invoke Method function to the **v0.9 TEDS (F)** input of the TEDS_Data to Table VI.
10. Wire the **TEDS data out** output of the TEDS_Parse Binary VI to the **TEDS data in** input of the TEDS_Data to Table VI.

When you run the VI, LabVIEW reads the TEDS from the sensor, and the LabVIEW TEDS Toolkit parses the TEDS information and outputs it as a table.

Note You must enable error handling in the FPGA VI to receive consistent error messages in the host VI.

Example

Refer to the module Getting Started (FPGA) VI at `labview\examples\CompactRIO\Module Specific\<module>\<module> Getting Started` for an example of how to access TEDS information.

Understanding Loop Timing (FPGA Interface)

The following modules have an internal master timebase and are internally timed:

- NI 9202
- NI 9225
- NI 9227
- NI 9229
- NI 9230
- NI 9231
- NI 9232
- NI 9234
- NI 9235
- NI 9236
- NI 9237
- NI 9238
- NI 9239
- NI 9242
- NI 9244
- NI 9246
- NI 9247
- NI 9250
- NI 9251
- NI 9252
- NI 9253
- NI 9260
- NI 9770
- NI 9775

Do not use the Loop Timer or Wait functions in a loop with an FPGA I/O Node that acquires data from one of these modules.

When you create a loop that reads data from one of these modules, make sure the loop does not execute slower than the data rate of the module. If the loop execution time is slower than the data rate, the FPGA I/O Node returns an overrun warning and

continues to read data. The overrun warning means that the data the FPGA I/O Node returns is valid, but the function missed one or more data points since the last time it read data from the module. The function returns the overrun warning when all of the following conditions are true:

- The module is in acquisition mode.
- An FPGA I/O Node that is acquiring data from the module executes at least once after you put the module in acquisition mode.
- The FPGA I/O Node did not read one or more data points since the previous time the function executed.

If the application acquires multiple buffers of data from the module and the timing relationship between them is not important, you can ignore the overrun warning returned with the first point of each buffer.

Avoiding Overrun Warnings

To avoid overrun warnings, develop the FPGA VI to meet the following guidelines:

Conditions	Guidelines
Your application acquires multiple buffers of data from a module with an internal master timebase.	If the timing relationship between the buffers is not important, you can ignore the overrun warning returned with the first point of each buffer.
You are reading from multiple modules with an internal master timebase in the same loop.	▪ Use one FPGA I/O Node to read the channels. ▪ Configure the modules to share a master timebase source and have the same data rate.
You are reading from a module with an internal master timebase and another analog input module in the same loop.	▪ If the rate at which you can acquire data from the other module is as fast or faster than the data rate configured for the module with an internal master timebase, you can read from both modules in the same loop. ▪ If you use the same FPGA I/O Node to read data from all modules, the FPGA I/O Node does not return data for the other mod

	ule until the module with an internal master timebase acquires data. ▪ If the other module has a slower data rate than the module with an internal master timebase and you read from both modules in the same loop, the FPGA I/O Node for the module with an internal master timebase returns an overrun warning and continues reading data. To avoid missing data, you can either change the data rate of the module with an internal master timebase or read from each module in a different loop.

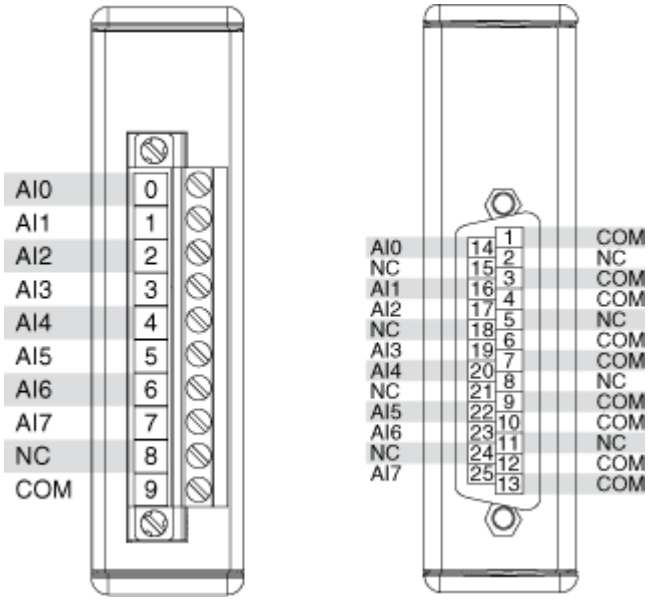
NI 9201

CompactRIO 8-Channel, ±10 V, 12-Bit Analog Input Module

Software Reference (?)

FPGA Interface | Scan Interface

NI 9201 Pinout



Related Topics

Converting and Calibrating CompactRIO Analog Input Values

NI 9201 (FPGA Interface)

CompactRIO 8-Channel, ±10 V, 12-Bit Analog Input Module

FPGA I/O Node

You can use an FPGA I/O Node, configured for reading, with this device.

Terminals in Software

Use the FPGA I/O Node to access the following terminals for this device.

Terminal	Description
AI**x**	Analog input channel **x**, where **x** is the number of the channel. The NI 9201 has AI channels 0 to 7.

You can configure the minimum time between conversions and understand scanning for these channels.

Arbitration

This device supports only the Arbitrate if Multiple Requestors Only option for arbitration. You cannot configure arbitration settings for this device.

Methods

This device does not support any methods.

I/O Properties

Use the FPGA I/O Property Node to access the following I/O properties for this device.

Property	Description

LSB Weight	Returns the LSB weight in nV/LSB for the channel. Use this value to convert and calibrate NI 9201 data if you set the **Calibration Mode** to **Raw** in the C Series Module Properties dialog box.
Offset	Returns the calibration offset in nV for the channel. Use this value to convert and calibrate NI 9201 data if you set the **Calibration Mode** to **Raw** in the **C Series Module Properties** dialog box.

Module Properties

Use the FPGA I/O Property Node to access the following module properties for this device.

Property	Description
Module ID	Returns the module ID, 0x70A4.
Serial Number	Returns the unique serial number of the module.
Vendor ID	Returns the NI vendor ID, 0x1093.

Single-Cycle Timed Loop

This device does not support the single-cycle Timed Loop.

C Series Module Properties Dialog Box for the NI 9201/9221 (FPGA Interface)

Right-click an NI 9201 or NI 9221 C Series module in the **Project Explorer** window and select **Properties** from the shortcut menu to display this dialog box.

Use this dialog box to configure a C Series module.

This dialog box includes the following components:

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.

- **Module Type**—Specifies the type of C Series module. You cannot change this option.
- **Location**—Specifies a slot in the chassis for the C Series module.
- **Calibration Mode**—Sets the calibration mode for the C Series module. Select **Calibrated** if you want the FPGA I/O Node to return calibrated, fixed-point data from the module in units of volts. The fixed-point data is signed, with a word length of 16 bits and an integer word length of 5 bits for the NI 9201 and 7 bits for the NI 9221. Select **Raw** if you want the FPGA I/O Node to return uncalibrated, binary data from the module. If you select **Raw**, you must convert and calibrate the analog input values in the host VI. The default is **Calibrated**.
- **Minimum Time Between Conversions**—Specifies the minimum time between conversions in µs.

Configuring the Minimum Time Between Conversions for the NI 9201/9221 (FPGA Interface)

You can configure the minimum time between conversions for the NI 9201/9221 in the C Series Module Properties dialog box.

Complete the following steps to configure the minimum time between conversions for the NI 9201/9221.

1. Configure the CompactRIO system, and add an NI 9201/9221.
2. Right-click the NI 9201/9221 in the **Project Explorer** window and select **Properties** from the shortcut menu to display the **C Series Module Properties** dialog box.
3. Enter a value between 0 and 10 µs in increments of 25 ns in the **Minimum Time Between Conversions** text box.
4. Click the **OK** button.
5. Select **File»Save All** in the **Project Explorer** window.

Note The default minimum time between conversions for the NI 9201 is 2 µs, and the default minimum time between conversions for

the NI 9221 is 1.25 µs. The accuracy specifications in the NI 9201 and NI 9221 hardware documentation on ni.com/manuals are based on these default values. Refer to the following tables for examples of how the value you enter in the **Minimum Time Between Conversions** text box affects the actual time between conversions and the accuracy of the module.

Refer to the following table if you are using a chassis other than the NI 9151 R Series Expansion chassis.

Module	Sampling Data from a Single or Multiple Channels?	Minimum Time Between Conversions*	Able to Achieve Specified Time Between Conversions?**	Module Accuracy
NI 9201	Single	≥ 1.25 µs	Yes	Module accuracy not affected
		< 1.25 µs	No	Module accuracy not affected
	Multiple	≥ 2 µs	Yes	Module accuracy not affected
		< 2 µs	No	Module accuracy degrades
NI 9221	Single	≥ 1.25 µs	Yes	Module accuracy not affected
		< 1.25 µs	No	Module accuracy not affected
	Multiple	≥ 1.25 µs	Yes	Module accuracy not affected
		< 1.25 µs	No	Module accuracy degrades

Refer to the following table if you are using the NI 9151 R Series Expansion chassis.

Module	Sampling Data from a Single	Minimum Time Between Conversions*	Able to Achieve Specified Time	Module Accuracy

	or Multiple Channels?		Between Conversions?**	
NI 9201	Single	≥ 2.1 µs	Yes	Module accuracy not affected
		< 2.1 µs	No	Module accuracy not affected
	Multiple	≥ 2.1 µs	Yes	Module accuracy not affected
		< 2.1 µs and ≥ 2 µs	No	Module accuracy not affected
		< 2 µs	No	Module accuracy degrades
NI 9221	Single	≥ 2.1 µs	Yes	Module accuracy not affected
		< 2.1 µs	No	Module accuracy not affected
	Multiple	≥ 2.1 µs	Yes	Module accuracy not affected
		< 2.1 µs and ≥ 1.25 µs	No	Module accuracy not affected
		< 1.25 µs	No	Module accuracy degrades

* The value you set in the **C Series Module Properties** dialog box.

** The actual time between conversions depends on how you develop the FPGA VI. Yes indicates that it is possible to write an FPGA VI that can sustain the minimum time between conversions specified in the **C Series Module Properties** dialog box. No indicates that the minimum time between conversions specified in the **C Series Module Properties** dialog box is too low and you may not be able to write an FPGA VI that can sustain the specified time.

Understanding NI 9201/9221 Scanning (FPGA Interface)

To scan the channels of the NI 9201/9221, configure an FPGA I/O Node with the channels you want to acquire from the module. The module implements a pipeline that is automatically managed by the FPGA I/O Node. Channels within the FPGA I/O

Node are sampled in numerical order regardless of the order they appear in the node.

The first time an FPGA I/O Node configured with channels on an NI 9201/9221 module executes, the module performs two setup conversions before converting the first channel. The two setup conversions prime the pipeline for subsequent FPGA I/O Node reads. The module does not repeat the setup conversions unless the FPGA I/O Node channel configuration changes and the pipeline needs to be primed again.

NI 9201 (Scan Interface)

CompactRIO 8-Channel, ±10 V, 12-Bit Analog Input Module


Open example

Module I/O Variables

To use I/O from this module in a VI, drag and drop I/O variables from the **Project Explorer** window to the block diagram of the VI. The I/O variables for the channels return calibrated floating-point data in volts.

Module Channels

The NI 9201 has the following channels.

Channel	Description
AI**x**	Analog input channel **x**, where **x** is the number of the channel. For the NI 9201, **x** is 0 to 7.

C Series Module Properties Dialog Box

Use this dialog box to configure the NI 9201. Right-click the NI 9201 in the **Project Explorer** window and select **Properties** to display this dialog box. You can configure the following options.

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module

based on the slot number. You can use this field to give the module a descriptive name.

- **Module Type**—Specifies the type of C Series module. You cannot change this value.
- **Location**—Specifies a slot in the chassis for the C Series module.

NI 9202

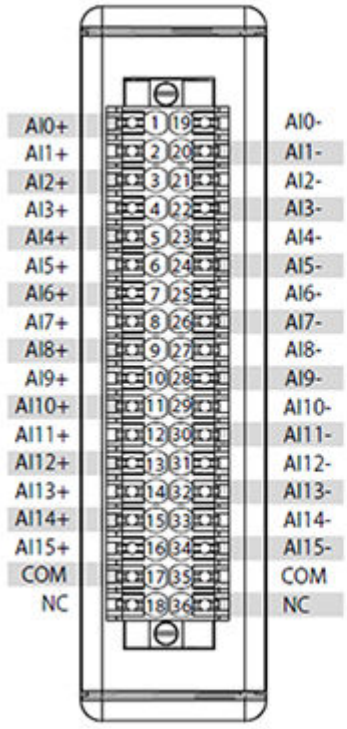
CompactRIO 16-Channel, 24-Bit Differential Analog Input Module

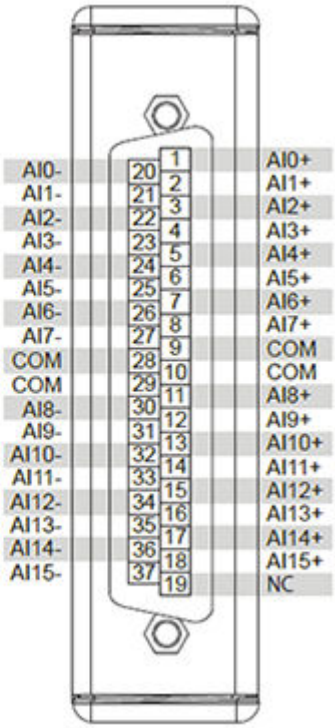
Software Reference (?)

FPGA Interface |

NI 9202

NI 9202 Pinout





Related Topics

FPGA Interface
C Series Module Properties Dialog Box
Converting and Calibrating CompactRIO Analog Input Values
Detecting Out-of-Range Channels for CompactRIO Analog Input Channels
Acquiring Data from a Module
Configuring the Data Rate for a Module (FPGA Interface)
Converting NI 9202 Data
Synchronizing Multiple NI 9225/9227/9229/923x/924x/9202/9260 Modules
Understanding Loop Timing (FPGA Interface)

NI 9202 (FPGA Interface)

CompactRIO 16-Channel, 24-Bit Differential Analog Input Module

 Open example

 Find related examples

FPGA I/O Node

You can use an FPGA I/O Node, configured for reading, with this device.

Terminals in Software

Use the FPGA I/O Node to access the following terminals for this device.

Terminal	Description
AI**x**	Analog input channel **x**, where **x** is the number of the channel. The NI 9202 has channels 0 to 15.
Onboard Clock	Gives access to the onboard clock in the LabVIEW block diagram. The onboard clock frequency is 12.8 MHz. Use the FPGA I/O Node in a single-cycle timed loop to access this channel. You must export the onboard clock of the NI 9202 to access this channel.

Start	Channel that controls when the NI 9202 starts acquiring data. If TRUE is written to the **Start** channel, the NI 9202 starts acquiring data. When the NI 9202 is acquiring data, you must write TRUE to the **Stop** channel before you can access properties for the module. If FALSE is written to the **Start** channel, no operation is performed.
Stop	Channel that controls when the NI 9202 stops acquiring data. If TRUE is written to the **Stop** channel, the NI 9202 stops acquiring data. When the NI 9202 is acquiring data, you must write TRUE to the **Stop** channel before you can access properties for the module. If FALSE is written to the **Stop** channel, no operation is performed.

Arbitration

This device supports only the Arbitrate if Multiple Requestors Only option for arbitration. You cannot configure arbitration settings for this device.

Module Properties

Use the FPGA I/O Property Node to access the following module properties for this device.

Property	Description
Data Rate	Sets the rate at which the NI 9202 acquires data.
Module ID	Returns the module ID, 0x788C for the spring terminal and 0x788A for the DSUB variant.
Serial Number	Returns the unique serial number of the module.
Vendor ID	Returns the NI vendor ID, 0x1093.
Input Delay	Returns the filter delay based on the data rate and filter setting.
Filter Frequency Config	Sets the frequency of the first notch in the filter response.

Note Changes to the filter settings apply to all channels.

Single-Cycle Timed Loop

This device does not support the single-cycle Timed Loop.

C Series Module Properties Dialog Box for the NI 9202 (FPGA Interface)

Right-click an NI 9202 C Series module in the **Project Explorer** window and select **Properties** from the shortcut menu to display this dialog box.

Use this dialog box to configure a C Series module.

This dialog box includes the following components:

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Type**—Specifies the type of C Series module. You cannot change this option.
- **Location**—Specifies a slot in the chassis for the C Series module.
- **Calibration Mode**—Sets the calibration mode for the C Series module. Select **Calibrated** if you want the FPGA I/O Node to return calibrated, fixed-point data from the module. The fixed-point data is signed, with 24-bits word length and 4-bits integer word length. Select **Raw** if you want the FPGA I/O Node to return calibrated, binary data from the module. If you select **Raw**, you must convert the binary data to the actual analog input values in the host VI. In **Raw** mode, you also need to apply some gain correction constants for some data rates. The default is **Calibrated**.
- **Master Timebase Source**—Specifies the master timebase source that the module uses.
- **Export Onboard Clock**—Place a checkmark in this checkbox if you want to make this module accessible as a master timebase source to other modules.

- **Data Rate**—Specifies the rate at which the module acquires data.
- **Filter Frequency Config**—Sets the frequency of the first notch in the filter response. Setting changes apply to all channels. Available values:
  - Data Rate/1
  - Data Rate/2
  - Data Rate/4
  - Data Rate/8
  - Data Rate/16

Converting NI 9202 Data (FPGA Interface)

Set the **Calibration Mode** to **Calibrated** in the C Series Module Properties dialog box for the NI 9202 if you want the FPGA I/O Node to return calibrated, fixed-point data from the module.

Set the **Calibration Mode** to **Raw** if you want the FPGA I/O Node to return calibrated, binary data from the module. If you set the **Calibration Mode** to **Raw**, you must convert the binary values to engineering units. You must convert these values in the host VI as demonstrated in the `labview\examples\CompactRIO\Module Specific\NI 9202\NI 9202 Scaling\NI 9202 Raw To Scaled.lvproj`.

The binary values are not uniform across data rates. Therefore, to get the **Corrected Raw**, multiply the binary value with the **Gain Correction** with respect to the data rate used as demonstrated in the `labview\examples\CompactRIO\Module Specific\NI 9202\NI 9202 Raw Correction\NI 9202 Raw Correction.lvproj`.

Open example (NI 9202 Raw To Scaled) Open example (NI 9202 Raw Correction)

Data Rates[1]	Scaling	Gain Correction
10 kS/s, 5 kS/s	**Volts** = **Binary Value** × 2018176 pV/LSB	**Corrected Binary Value** = **Binary Value** × 1.6
60 S/s[2]	**Volts** = **Binary Value** × 1356704 pV/LSB	**Corrected Binary Value** = **Binary Value** × 1.07563

400 S/s, 200 S/s, 100 S/s, 10 S/s[2]	**Volts** = **Binary Value** × 1291512 pV/LSB	**Corrected Binary Value** = **Binary Value** × 1.024
2 kS/s, 1 kS/s, 500 S/s, 250 S/s, 125 S/s, 50 S/s[2]	**Volts** = **Binary Value** × 1614448 pV/LSB	**Corrected Binary Value** = **Binary Value** × 1.28
60 S/s[3]	**Volts** = **Binary Value** × 2274057 pV/LSB	**Corrected Binary Value** = **Binary Value** × 1.802817
10 S/s[3], 50 S/s[3], Others	**Volts** = **Binary Value** × 1261244 pV/LSB	**Corrected Binary Value** = **Binary Value** × 1

where **Binary Value** is the value returned by the FPGA I/O Node.

[1] The actual data rate changes with the master timebase when using an external master timebase. In order to provide power line frequency rejection when using master timebase frequencies of both 12.8 MHz and 13.1072 MHz, there are two sets of settings for the data rates of 10 S/s, 50 S/s and 60 S/s. Refer to the following footnotes for the correct scaling constants and gain corrections, depending on your master timebase frequency.

[2] Data rates setting when using internal master timebase or an external master timebase of 12.8 MHz.

[3] Data rates setting when using an external master timebase of 13.1072 MHz.

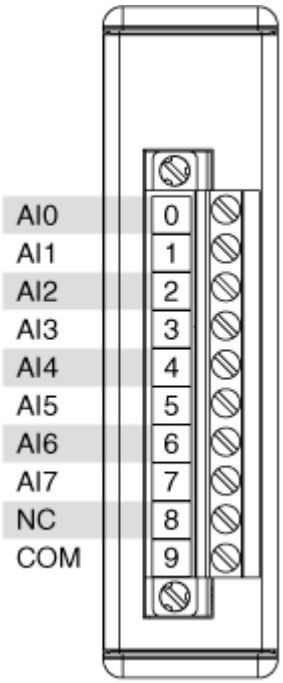
NI 9203

CompactRIO 8-Channel, ±20 mA, 16-Bit Analog Input Module

Software Reference (?)

FPGA Interface | Scan Interface

NI 9203 Pinout



Related Topics

Converting and Calibrating CompactRIO Analog Input Values

NI 9203 (FPGA Interface)

CompactRIO 8-Channel, ±20 mA, 16-Bit Analog Input Module

Open example Find related examples

FPGA I/O Node

You can use an FPGA I/O Node, configured for reading, with this device.

Terminals in Software

Use the FPGA I/O Node to access the following terminals for this device.

Terminal	Description

AI**x**	Analog input channel **x**, where **x** is the number of the channel. The NI 9203 has AI channels 0 to 7.

Arbitration

This device supports only the Arbitrate if Multiple Requestors Only option for arbitration. You cannot configure arbitration settings for this device.

I/O Methods

This device does not support any I/O methods.

Module Methods

Use the FPGA I/O Method Node to access the following module method for this device.

Method	Description
Set Input Range	Sets the input range for a channel as either 0–20 mA or ±20 mA. This method overwrites the valu e you configure in the C Series Module Propertie s dialog box.

I/O Properties

Use the FPGA I/O Property Node to access the following I/O properties for this device.

Property	Description
LSB Weight (±20 mA range)	Returns the LSB weight in pA/LSB for the chann el. Use this value to convert and calibrate NI 920 3 data if you set the **Calibration Mode** to **Raw** in the C Series Module Properties dialog box, an d you set the input range to ±20 mA.
LSB Weight (4–20 mA range)	Returns the LSB weight in pA/LSB for the chann el. Use this value to convert and calibrate NI 920 3 data if you set the **Calibration Mode** to **Raw** in the **C Series Module Properties** dialog box , and you set the input range to 0–20 mA.

Module Properties

Use the FPGA I/O Property Node to access the following module properties for this device.

Property	Description
Module ID	Returns the module ID, 0x7129.
Offset (±20 mA range)	Returns the calibration offset in pA for the channel. Use this value to convert and calibrate NI 9203 data if you set the **Calibration Mode** to **Raw** in the C Series Module Properties dialog box, and you set the input range to ±20 mA.
Offset (4–20 mA range)	Returns the calibration offset in pA for the channel. Use this value to convert and calibrate NI 9203 data if you set the **Calibration Mode** to **Raw** in the **C Series Module Properties** dialog box, and you set the input range to 0–20 mA.
Serial Number	Returns the unique serial number of the module.
Vendor ID	Returns the NI vendor ID, 0x1093.

Single-Cycle Timed Loop

This device does not support the single-cycle Timed Loop.

C Series Module Properties Dialog Box for the NI 9203 (FPGA Interface)

Right-click an NI 9203 C Series module in the **Project Explorer** window and select **Properties** from the shortcut menu to display this dialog box.

Use this dialog box to configure a C Series module.

This dialog box includes the following components:

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.

- **Module Type**—Specifies the type of C Series module. You cannot change this option.
- **Location**—Specifies a slot in the chassis for the C Series module.
- **Calibration Mode**—Sets the calibration mode for the C Series module. Select **Calibrated** if you want the FPGA I/O Node to return calibrated, fixed-point data from the module in units of amps. The fixed-point data is signed, with a word length of 21 bits and an integer word length of –4 bits. Select **Raw** if you want the FPGA I/O Node to return uncalibrated, binary data from the module. If you select **Raw**, you must convert and calibrate the analog input values in the host VI. The default is **Calibrated**.
- **Minimum Time Between Conversions**—Specifies the minimum time between conversions in µs.
- **Channel Configuration**—Specifies the input range for each channel.
  - **Channels**—Specifies the channel(s) for which you want to select the input range.
  - **Input Range**—Specifies the input range for the selected channel(s) as either 0–20 mA or ±20 mA.

NI 9203 (Scan Interface)

CompactRIO 8-Channel, ±20 mA, 16-Bit Analog Input Module


Open example

Module I/O Variables

To use I/O from this module in a VI, drag and drop I/O variables from the **Project Explorer** window to the block diagram of the VI. The I/O variables for the channels return calibrated floating-point data in amps.

Module Channels

The NI 9203 has the following channels.

Channel	Description

AI**x**	Analog input channel **x**, where **x** is the number of the channel. For the NI 9203, **x** is 0 to 7.

C Series Module Properties Dialog Box

Use this dialog box to configure the NI 9203. Right-click the NI 9203 in the **Project Explorer** window and select **Properties** to display this dialog box. You can configure the following options.

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this value.
- **Location**—Specifies a slot in the chassis for the C Series module.
- **Channel Configuration**—You can specify the input range for each channel.
  - **Channels**—Specifies the channel(s) for which you want to select the input range.
  - **Input Range**—Specifies the input range for the selected channel(s) as either 0–20 mA or ±20 mA.

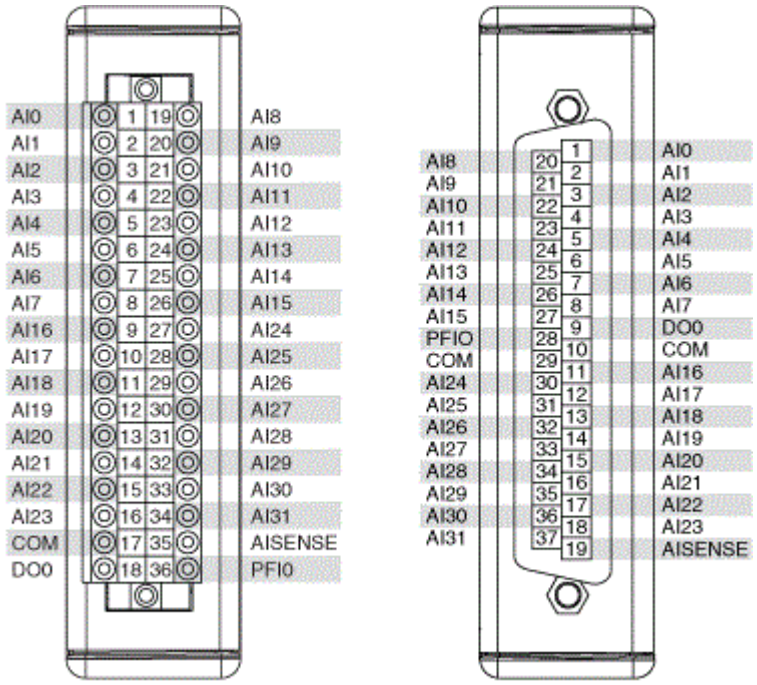
NI 9205

CompactRIO 32-Channel Single-Ended/16-Channel Differential, ±200 mV to ±10 V, 16-Bit Analog Input Module

Software Reference (?)

FPGA Interface | Scan Interface

NI 9205 Pinout



Related Topics

FPGA Interface
Converting and Calibrating CompactRIO Analog Input Values
Detecting Out-of-Range Channels
IO Sample Method
Set Terminal Mode Method
Set Triggers Method
Set Voltage Range Method
Conversion Timing for the NI 9205/9206
Self-Calibration for the NI 9205/9206

NI 9205 (FPGA Interface)

CompactRIO 32-Channel Single-Ended/16-Channel Differential, ±200 mV to ±10 V, 16-Bit Analog Input Module

Open example

Find related examples

FPGA I/O Node

You can use an FPGA I/O Node, configured for reading, with this device.

Terminals in Software

Use the FPGA I/O Node to access the following terminals for this device.

Terminal	Description
AI**x**	Analog input channel **x**, where **x** is the number of the channel. The NI 9205 has AI channels 0 to 31. The channel is sampled using the currently configured terminal mode and voltage range. You can configure these settings at edit time using the C Series Module Properties dialog box or at run time using the Set Terminal Mode or Set Voltage Range methods.
DI0	Digital input channel used to access the module digital line, which is labeled PFI0. This terminal is not available for an onboard NI 9205 on a Single-Board RIO (sbRIO) device.
Trig	Returns the output of the module trigger circuitry. Use the Set Triggers method to configure the trigger circuit.
DO0	Digital output channel 0. This terminal is not available for an onboard NI 9205 on an sbRIO device.

Refer to the Conversion Timing topic for information about the order and timing of conversions for these I/O channels.

Arbitration

This device supports only the Arbitrate if Multiple Requestors Only option for arbitration. You cannot configure arbitration settings for this device.

I/O Methods

This device does not support any I/O methods.

Module Methods

Use the FPGA I/O Method Node to access the following module methods for this device.

Method	Description
IO Sample	Acquires a single sample from the module. The channel number, terminal mode, and voltage ra nge are all configurable at run time. **Note** NI suggests that you do not configure th e VI to run an IO Sampl e method and another FPGA I/O Method Node in parallel when both a re targeted to the same C Series module. Simil arly, NI suggests that y ou do not configure th e VI to run multiple IO Sample methods in par allel when the IO Samp le methods are targete d to the same C Series module. Refer to the NI 9205 Basic IO VI and the NI 9205 Advanced IO VI in the `labview\examples\CompactRIO\Module Specific\NI 9205\NI 9205 Basic IO\NI 9205 Basic IO.lvproj` and `labview\examples\CompactRIO\Module Specific\NI 9205\NI 9205 Advanced IO\NI 9205 Advanced IO.lvproj` for examples related to this method. Open example (NI 9205 Basic IO) Open example (NI 9205 Advanced IO)

Restore Last External Calibration Constants	Restores the calibration constants of the module to the factory values. You must enable self-calibration on the C Series Module Properties dialog box to use this method.  **Caution** The Restore Last External Calibration Constants method node must be used with the example VI to prevent damaging the module. Refer to the NI 9205 Self-Calibration VI in the `labview\examples\CompactRIO\Module Specific\NI 9205\NI 9205 Self Calibration\NI 9205 Self Calibration.lvproj` for an example of using this method.
Set Terminal Mode	Sets the terminal mode for a channel as RSE (referenced single-ended), NRSE (non-referenced single-ended), or DIFF (differential). This method overwrites the value you configure in the **C Series Module Properties** dialog box.
Set Triggers	Sets the trigger output to one of the following values: ▪ None ▪ AI Below Low ▪ AI Above High ▪ AI Inside Region ▪ AI Below Low with Hysteresis ▪ AI Above High with Hysteresis ▪ DI Trigger  **Note** The onboard NI 9205 on sbRIO devices

	does not support DI triggering. Refer to the NI 9205 Basic Triggering VI and the NI 9205 Advanced Triggering VI in the `labview\examples\CompactRIO\Module Specific\NI 9205\NI 9205 Basic Triggering\NI 9205 Basic Triggering.lvproj` and `labview\examples\CompactRIO\Module Specific\NI 9205\NI 9205 Advanced Triggering\NI 9205 Advanced Triggering.lvproj` for examples related to this method.  Open example (NI 9205 Basic Triggering)  Open example (NI 9205 Advanced Triggering)
Set Voltage Range	Sets the input range for a channel as ±10 V, ±5 V, ±1 V, or ±200 mV. This method overwrites the value you configure in the **C Series Module Properties** dialog box.
Write Self-Calibration Constants	Replaces the calibration constants of the module with new values. You must enable self-calibration on the C Series Module Properties dialog box to use this method. ▪ **Self-Calibration Constants**—Contains offset and gain constants for the analog input ranges of the module.  **Caution** The Write Self-Calibration Constants method node must be used with the example VI to prevent damaging the module. Refer to the NI 9205 Self-Calibration VI in the `labview\examples\CompactRIO\Module Specific\NI 9205\NI 9205 Self Calibration\NI 9205 Self Calibratio`

	n.lvproj for an example of using this method .

I/O Properties

This device does not support any I/O properties.

Module Properties

Use the FPGA I/O Property Node to access the following module properties for this device.

Property	Description
Linearization Coefficient x	(Optional) NI-MCal linearization coefficient x, where **x** is the number of the linearization coefficient. The NI 9205 has linearization coefficients 3 to 0. You can use these coefficients in calibration to compensate for some types of measurement nonlinearity inherent in this device. When returning calibrated data from the FPGA I/O Node, the Linearization Coefficients are not used to calculate the calibrated data. This means that calibrated data returned in FPGA does not compensate for the measurement nonlinearities in the device. Refer to the NI 9205 Advanced IO VI in the labview\examples\CompactRIO\Module Specific\NI 9205\NI 9205 Advanced IO\NI 9205 Advanced IO.lvproj for an example of this concept. Open example
LSB Weight (±10 V range)	Returns the LSB weight in pV/LSB for the ±10 V range. Use this value to convert and calibrate NI 9205 data if you set the **Calibration Mode** to **Raw** in the C Series Module Properties dialog box .

LSB Weight (±1 V range)	Returns the LSB weight in pV/LSB for the ±1 V range. Use this value to convert and calibrate NI 9205 data if you set the **Calibration Mode** to **Raw** in the **C Series Module Properties** dialog box.
LSB Weight (±200 mV range)	Returns the LSB weight in pV/LSB for the ±200 mV range. Use this value to convert and calibrate NI 9205 data if you set the **Calibration Mode** to **Raw** in the **C Series Module Properties** dialog box.
LSB Weight (±5 V range)	Returns the LSB weight in pV/LSB for the ±5 V range. Use this value to convert and calibrate NI 9205 data if you set the **Calibration Mode** to **Raw** in the **C Series Module Properties** dialog box.
Module ID	Returns the module ID, 0x712A (NI 9205 with DSUB) or 0x71EA (NI 9205 with spring terminal).
Offset (±10 V range)	Returns the calibration offset in nV for the ±10 V range. Use this value to convert and calibrate NI 9205 data if you set the **Calibration Mode** to **Raw** in the C Series Module Properties dialog box.
Offset (±1 V range)	Returns the calibration offset in nV for the ±1 V range. Use this value to convert and calibrate NI 9205 data if you set the **Calibration Mode** to **Raw** in the **C Series Module Properties** dialog box.
Offset (±200 mV range)	Returns the calibration offset in nV for the ±200 mV range. Use this value to convert and calibrate NI 9205 data if you set the **Calibration Mode** to **Raw** in the **C Series Module Properties** dialog box.
Offset (±5 V range)	Returns the calibration offset in nV for the ±5 V range. Use this value to convert and calibrate NI 9205 data if you set the **Calibration Mode** to **Raw** in the **C Series Module Properties** dialog box.

Serial Number	Returns the unique serial number of the module .
Vendor ID	Returns the NI vendor ID, 0x1093.

Single-Cycle Timed Loop

This device does not support the single-cycle Timed Loop.

C Series Module Properties Dialog Box for the NI 9205/9206 (FPGA Interface)

Right-click an NI 9205 or NI 9206 C Series module in the **Project Explorer** window and select **Properties** from the shortcut menu to display this dialog box.

Use this dialog box to configure a C Series module.

This dialog box includes the following components:

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this option.
- **Location**—Specifies a slot in the chassis for the C Series module.
- **Calibration Mode**—Sets the calibration mode for the C Series module. Select **Calibrated** if you want the FPGA I/O Node to return calibrated, fixed-point data from the module in units of volts. The fixed-point data is signed, with a word length of 26 bits and an integer word length of 5 bits. Select **Raw** if you want the FPGA I/O Node to return uncalibrated, binary data from the module. If you select **Raw**, you must convert and calibrate the analog input values in the host VI. The default is **Calibrated**.
- **Channel Configuration**—Specifies the input range for each channel.
  - **Channels**—Specifies the channel(s) for which you want to select the input range.

- **Input Range**—Specifies the input range for the selected channel(s) as ±10 V, ±5 V, ±1 V, or ±200 mV.
- **Terminal Mode**—Specifies the terminal mode for the selected channel(s) as RSE (referenced single-ended), NRSE (non-referenced single-ended), or DIFF (differential).

- **Minimum Time Between Conversions**—Specifies the minimum time between conversions in µs.
- **Enable Advanced Self-Calibration Nodes**—Place a checkmark in this checkbox if you want to enable Self-Calibration support in the FPGA for this module.

IO Sample Method (FPGA Interface)

This module method acquires a single sample from the module. The channel number, terminal mode, and voltage range are all configurable at run time. You use this module method by selecting it in an FPGA I/O Method Node that is configured for the appropriate device and/or channel. Details Examples

Note NI suggests that you do not configure the VI to run an IO Sample method and another FPGA I/O Method Node in parallel when both are targeted to the same C Series module. Similarly, NI suggests that you do not configure the VI to run multiple IO Sample methods in parallel when the IO Sample methods are targeted to the same C Series module.

Configuration [i+2] contains encoded configuration information that gets loaded into the module conversion pipeline. This configuration information controls the data to be sampled two iterations into the future. Refer to the Conversion Timing topic for more information. Refer to the Configuration Encoding table below for an example of how the configuration information is encoded.

Data [i] Returns the data from the current sample.

error in describes error conditions that occur before this VI or function runs. The default is no `error`. If an error occurred before this VI or function runs, the VI or function passes the **error in** value to **error out**. This VI or function runs normally only if no error occurred before this VI or function runs. If an error occurs while this VI or function runs, it runs normally and sets its own error status in **error out**. Use **error in** and **error out** to check errors and to specify execution order by wiring **error out** from one node to **error in** of the next node.

status is TRUE (X) if an error occurred before this VI or function ran or FALSE (checkmark) to indicate a warning or that no error occurred before this VI or function ran. The default is FALSE.

code is the error code number identifying an error. The default is 0. If status is TRUE, code is a nonzero error code. If status is FALSE, code is 0 or a warning code.

source always contains an empty string because strings are not supported in LabVIEW FPGA.

error out contains error information. If **error in** indicates that an error occurred before this VI or function ran, **error out** contains the

same error information. Otherwise, it describes the error status that this VI or function produces. Right-click the **error out** indicator on the front panel and select **Explain Error** from the shortcut menu for more information about the error.

status is TRUE (X) if an error occurred or FALSE (checkmark) to indicate a warning or that no error occurred.

code is the error code number identifying an error. The default is 0. If status is TRUE, code is a nonzero error code. If status is FALSE, code is 0 or a warning code.

source always contains an empty string because strings are not supported in LabVIEW FPGA.

Configuration Encoding Table

The following table describes how to construct the Configuration [i+2] value to write to the IO Sample method to perform a particular operation. The **Operation** column lists the types of operations that can be performed using the IO Sample method. The **Configuration Bit Fields** column lists the bit positions within the **Configuration** [i+2] number that need to be set. The **Values** column specifies the binary value to apply to the specified **Configuration Bit Fields**.

Operation	Configuration Bit Fields	Values
AI Read	15:13	001b

	12:11	01b for channels 0-15 10b for channels 16-31
	10:8	000b for channels 0, 8, 16, or 24 001b for channels 1, 9, 17, or 25 … 110b for channels 6, 14, 22, or 30 111b for channels 7, 15, 23, or 31
	7:6	00b
	5:4	00b for NRSE mode 11b for RSE or DIFF modes
	3:2	11b for channels 8-15 or 24-31 01b for DIFF mode on channels 0-7 or 16-23 10b for RSE or NRSE mode on channels 0-7 or 16-23
	1:0	00b for ±10 V 01b for ±5 V 10b for ±1 V 11b for ±200 mV
DI0 Read	15:0	0000000000000000b
DO0 Write	15:1	010000000000000b
	0	Binary value to write to DO0

Using This Method

The IO Sample method provides an efficient and flexible interface to the module. You can use this method to acquire a single sample from any of the channels on the module, at any range, and with any available input mode.

When this method is executed, the module performs a single conversion on the next channel present in the conversion pipeline on the module. The data from this conversion is returned via the **Data** [i] method output. At the same time that the conversion data is read from the module, the new configuration information specified by the **Configuration** [i+2] input is loaded into the configuration pipeline on the module. The pipeline is two samples deep. So, the configuration information specified on one execution of the IO Sample method determines which channel will

be sampled by the IO Sample method two iterations into the future. Refer to the Conversion Timing topic for more details.

Examples

Refer to the NI 9205 Basic IO VI and the NI 9205 Advanced IO VI in the `labview\examples\CompactRIO\Module Specific\NI 9205\NI 9205 Basic IO\NI 9205 Basic IO.lvproj` and `labview\examples\CompactRIO\Module Specific\NI 9205\NI 9205 Advanced IO\NI 9205 Advanced IO.lvproj` for examples of the IO concepts discussed above.

Open example (NI 9205 Basic IO)

Open example (NI 9205 Advanced IO)

Set Terminal Mode Method (FPGA Interface)

Overrides the default setting provided in the C Series Module Properties dialog box. You use this module method by selecting it in an FPGA I/O Method Node that is configured for the appropriate device and/or channel.

AI Channel is the channel you want to set the terminal mode for.

Terminal Mode is an enumeration of the following trigger modes:

- **RSE** is a single-ended measurement between any of the 32 individual channels and the module ground.
- **NRSE** is a single-ended measurement between any of the 32 individual channels and the AISENSE line into the module.
- **DIFF** is a differential measurement between two of the 32 individual channels, with the name of the differential channel matching the channel tied to the positive side of the differential measurement. Channels AI0 to AI7, and

AI16 to AI23 may be set to DIFF configuration.

error in describes error conditions that occur before this VI or function runs. The default is no `error`. If an error occurred before this VI or function runs, the VI or function passes the **error in** value to **error out**. This VI or function runs normally only if no error occurred before this VI or function runs. If an error occurs while this VI or function runs, it runs normally and sets its own error status in **error out**. Use **error in** and **error out** to check errors and to specify execution order by wiring **error out** from one node to **error in** of the next node.

status is TRUE (X) if an error occurred before this VI or function ran or FALSE (checkmark) to indicate a warning or that no error occurred before this VI or function ran. The default is FALSE.

code is the error or warning code. The default is `0`. If **status** is TRUE, **code** is a nonzero error code. If **status** is FALSE, **code** is `0` or a warning code.

source always contains an empty string because strings are not supported in LabVIEW FPGA.

error out contains error information. If **error in** indicates that an error occurred before this VI or function ran, **error out** contains the same error information. Otherwise, it describes the error status that this VI or function produces. Right-click the **error out** indicator on the front panel and select **Explain Error** from the shortcut menu for more information about the error.

status is TRUE (X) if an error occurred or FALSE (checkmark) to indicate a warning or that no error occurred.

code is the error or warning code. If **status** is TRUE, **code** is a nonzero error code. If **status** is FALSE, **code** is 0 or a warning code.

source always contains an empty string because strings are not supported in LabVIEW FPGA.

Set Triggers Method (FPGA Interface)

This module method controls the data returned by the trigger digital input line. You use this module method by selecting it in an FPGA I/O Method Node that is configured for the appropriate device and/or channel. Details Examples

Trigger Mode is an enumeration of the following trigger mode options:

- **None** disables the trigger function.

- **AI Below Low** detects when the analog signal is below the low threshold you specify.
- **AI Above High** detects when the analog signal is above the high threshold you specify.
- **AI Inside Region** detects when the analog signal is between the high and low thresholds you specify.
- **AI Below Low with Hysteresis** asserts the trigger when the signal starts above the high threshold you specify and then crosses below the low threshold you specify. The trigger deasserts when the signal crosses above the high threshold you specify.
- **AI Above High with Hysteresis** asserts the trigger when the signal starts below the low threshold you specify and then crosses above the high threshold you specify. The trigger deasserts when the signal crosses below the low threshold you specify.
- **DI Trigger** detects when the digital signal on PFI0 is logic high.

Note The onboard NI 9205 on Single-Board RIO (sbRIO) devices does not support DI triggering.

AI High Threshold defines the upper threshold for the analog trigger circuit.

AI Low Threshold defines the lower threshold for the analog trigger circuit.

error in describes error conditions that occur before this VI or function runs. The default is no `error`. If an error occurred before this VI or function runs, the VI or function passes the **error in** value to **error out**. This VI or function runs normally only if no error occurred before this VI or function runs. If an error occurs while this VI or function runs, it runs normally and sets its own error status in **error out**. Use **error in** and **error out** to check errors and to specify execution order by wiring **error out** from one node to **error in** of the next node.

status is TRUE if an error occurred. If **status** is TRUE, the VI does not perform any operations.

code is the error code number identifying an error. The default is `0`. If status is TRUE, code is a nonzero error code. If status is FALSE, code is `0` or a warning code.

source always contains an empty string because strings are not supported in LabVIEW FPGA.

error out contains error information. If **error in** indicates that an error occurred before this VI or function ran, **error out** contains the same error information. Otherwise, it describes the error status that this VI or function produces. Right-click the **error out** indicator on

the front panel and select **Explain Error** from the shortcut menu for more information about the error.

status is TRUE if an error occurred. If **status** is TRUE, the VI does not perform any operations.

code is the error code number identifying an error. The default is 0. If status is TRUE, code is a nonzero error code. If status is FALSE, code is 0 or a warning code.

source always contains an empty string because strings are not supported in LabVIEW FPGA.

Using This Method

Use the Set Triggers Method to configure the trigger circuit on the module. Once the trigger circuit is configured, use an FPGA I/O Node configured to access the Trig channel to monitor the output of the trigger circuit. The trigger circuit does not automatically initiate any conversions on the module. It is up to the FPGA VI to monitor the Trig line, and then initiate a conversion using an FPGA I/O Node or the IO Sample method when the appropriate trigger event occurs.

Perform the following steps to trigger an acquisition using the Set Triggers Method:

1. Ensure that the module pipeline is primed with the next two channels that you want to sample after the trigger event. This step will minimize the delay between the trigger event and the AI channels getting sampled. For analog triggering modes, this step also configures the analog trigger circuitry to monitor the desired channel. The AI trigger circuit monitors the channel

waiting in the module pipeline for the next conversion.

If you are using FPGA I/O Nodes to perform the acquisition, this step can be accomplished by executing an FPGA I/O Node configured to match the FPGA I/O Node that you will be executing after the trigger event. If you are using one of the analog triggering modes along with the FPGA I/O Nodes, the AI trigger circuit will operate on the lowest numbered channel present in the FPGA I/O Node.

Refer to the IO Sample method and Conversion Timing topics for more information on managing the module pipeline using the IO Sample method. If you are using one of the analog trigger modes along with the IO Sample method, the AI trigger circuit will operate on the channel waiting in the pipeline to be converted by the next IO Sample method.

2. Execute the Set Triggers method with the appropriate trigger mode selected. The trigger mode circuitry is implemented in the hardware as you specify in this method. Refer to the NI 9205 and NI 9206 hardware documentation on ni.com/manuals for more information about the trigger modes.
3. Monitor the Trig channel in a loop until you see the appropriate trigger condition occur.
4. Execute an FPGA I/O Node or IO Sample method function to acquire data in response to the trigger event.

Examples

Refer to the NI 9205 Basic Triggering VI and the NI 9205 Advanced Triggering VI in the `labview\examples\CompactRIO\Module Specific\NI 9205\NI 9205 Basic Triggering\NI 9205 Basic Triggering.lvproj` and `labview\examples\CompactRIO\Module Specific\NI 9205\NI 9205 Advanced Triggering\NI 9205 Advanced Triggering.lvproj` for examples of the triggering concepts discussed above.

Open example (NI 9205 Basic Triggering)

Open example (NI 9205 Advanced Triggering)

Set Voltage Range Method (FPGA Interface)

This module method overrides the default setting provided in the C Series Module Properties dialog box. You use this module method by selecting it in an FPGA I/O Method Node that is configured for the appropriate device and/or channel.

AI Channel is the channel you want to set the voltage range for.

Voltage Range is an enumeration of the following voltage ranges:

- ±10 V
- ±5 V
- ±1 V
- ±200 mV

error in describes error conditions that occur before this VI or function runs. The default is no `error`. If an error occurred before this VI or function runs, the VI or function passes the **error in** value to **error out**. This VI or function runs normally only if no error occurred before this VI or function runs. If an error occurs while this VI or function runs, it runs normally and sets its own error status in **error out**. Use **error in** and **error out** to check errors and to specify execution order by wiring **error out** from one node to **error in** of the next node.

status is TRUE if an error occurred. If **status** is TRUE, the VI does not perform any operations.

code is the error code number identifying an error. The default is `0`. If status is TRUE, code is a nonzero error

code. If status is FALSE, code is 0 or a warning code.

source always contains an empty string because strings are not supported in LabVIEW FPGA.

error out contains error information. If **error in** indicates that an error occurred before this VI or function ran, **error out** contains the same error information. Otherwise, it describes the error status that this VI or function produces. Right-click the **error out** indicator on the front panel and select **Explain Error** from the shortcut menu for more information about the error.

status is TRUE if an error occurred. If **status** is TRUE, the VI does not perform any operations.

code is the error code number identifying an error. The default is 0. If status is TRUE, code is a nonzero error code. If status is FALSE, code is 0 or a warning code.

source always contains an empty string because strings are not supported in LabVIEW FPGA.

Conversion Timing for the NI 9205/9206 (FPGA Interface)

Example

The NI 9205 and NI 9206 modules implement a two-element deep pipeline for access to the AI, DI0, and DO0 channels. This pipeline results in maximum sample rate and maximum sample quality. The Trig channel has a parallel data path that bypasses the pipeline.

When using the FPGA I/O Node to sample channels, the pipeline is automatically managed by the FPGA I/O Node, and the channels within the FPGA I/O Node are sampled in numerical order regardless of the order they appear in the node.

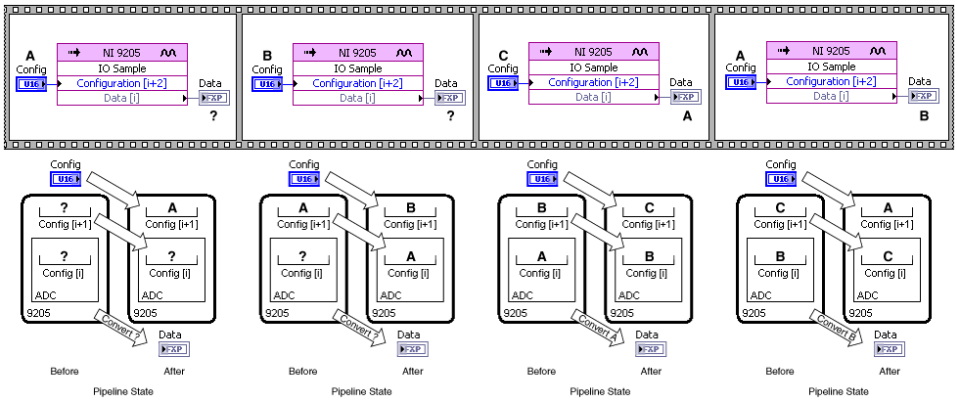
If the first two channel requests in the FPGA I/O Node do not match the two channel requests stored in the module pipeline, there will be a delay before the first channel sample occurs. This delay is caused by the FPGA I/O Node automatically updating the module channel sample pipeline, which takes two channel sample cycles.

To minimize the need for the pipeline updates, each FPGA I/O Node leaves the module pipeline primed to repeat itself. If you use only one FPGA I/O Node in a looping structure, only the first iteration of the loop will incur the two-cycle time delay. All subsequent iterations operate with no delay.

When using the IO Sample method, you must take steps to manage this pipeline in the VIs.

To read one channel, that channel configuration must be requested two cycles before the time it is to be sampled. The U16 configuration value for an AI channel sample contains the channel number, channel input range, and terminal mode. The U16 configuration value also can represent an access to the DIO or DOO channels, which is treated the same as an AI operation.

The following diagram illustrates how the pipeline works within a sequence structure. A typical application would use a loop structure to iterate through a scan list, which is a predefined list of configurations, continuously. The sequence structure and art elements show how data moves into the NI 9205/9206 pipeline and then is converted. Note that the IO Sample method first converts the configuration that is in the ADC, and then shifts the configuration values through the pipeline to prepare for the next time LabVIEW calls the IO Sample method.



The simplest form of pipeline management is to force the pipeline on every set of samples. This assumes that the pipeline is always wrong at the first sample, and sends all IO Sample requests in order. The last two data points need some configuration to be requested, but it does not matter, in this use case, what configuration that is.

A better form of pipeline management emulates the behavior of the FPGA I/O Node. Instead of always assuming that the pipeline is wrong, you choose the last two configuration values based on the first two samples you want to include in the next iteration. This pipeline management system can be accomplished in two parts: initialization and sample iteration.

Tip

NI recommends you use the IO Sample method for the following reasons:

- Smaller on FPGA—With large channel count, the IO Sample method is more efficient with FPGA resources, and thus requires less space on the FPGA for the same application.
- Sample flexibility—The IO Sample method gives you more flexibility to change channel range, terminal mode, and

channel order at run time and at full sample rate.

- Application timing flexibility—The IO Sample method returns all sample data as soon as it is available. The FPGA I/O Node will gather data for all requested samples and then return all at once.

The **Minimum Time Between Conversions** control you can set in the C Series Module Properties dialog box determines the shortest possible time between any two conversions. For channels sampled within the same FPGA I/O Node, the time you set determines the exact time between conversions. For channels sampled within separate FPGA I/O Nodes or for conversions caused by looping on an FPGA I/O Node, the time you set may be less than the actual time between conversions. However, the minimum time you set is never greater than the time between conversions. If the application tries to execute an FPGA I/O Node or IO Sample method faster than the specified minimum time between conversions, the conversion is delayed until the minimum time you set is satisfied.

The default minimum time between conversions for the NI 9205/9206 is 8 µs. The accuracy specifications in the NI 9205 and NI 9206 hardware documentation on ni.com/manuals are based on this default value. If you set the minimum time between conversions to at least 8 µs, the accuracy of the module is not affected. If you set the minimum time between conversions to less than 8 µs, the accuracy of the module degrades if you sample data from multiple channels.

Example

Refer to the NI 9205 Advanced IO VI in the `labview\examples\CompactRIO\Module Specific\NI 9205\NI 9205 Advanced IO\NI 9205 Advanced IO.lvproj` for an example of conversion timing on the NI 9205 and NI 9206 C Series Modules.

Self-Calibration for the NI 9205/9206 (FPGA Interface)

Self-Calibration adjusts the calibration constants stored onboard the module. You can perform a self-calibration at any time to account for changes in environmental conditions. You can enable self-calibration on the C Series Module Properties dialog box.

Enabling Self-Calibration on the NI 9205 or NI 9206 allows access to the Write Self-Calibration Constants and Restore Last External Calibration Constants module methods.

Caution The Write Self-Calibration Constants and Restore Last External Calibration Constants method nodes must be used with the example VI to prevent damaging the module.

Refer to the NI 9205 Self-Calibration VI in the `labview\examples\CompactRIO\Module Specific\NI 9205\NI 9205 Self Calibration\NI 9205 Self Calibration.lvproj` for an example of self-calibration.

NI 9205 (Scan Interface)

CompactRIO 32-Channel Single-Ended/16-Channel Differential, ±200 mV to ±10 V, 16-Bit Analog Input Module


Open example

Module I/O Variables

To use I/O from this module in a VI, drag and drop I/O variables from the **Project Explorer** window to the block diagram of the VI. The I/O variables for the channels return calibrated floating-point data in volts.

Module Channels

The NI 9205 has the following channels.

Channel	Description
AI**x**	Analog input channel **x**, where **x** is the number of the channel. For the NI 9205, **x** is 0 to 31.

C Series Module Properties Dialog Box

Use this dialog box to configure the NI 9205. Right-click the NI 9205 in the **Project Explorer** window and select **Properties** to display this dialog box. You can configure the following options.

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this value.
- **Location**—Specifies a slot in the chassis for the C Series module.
- **Channel Configuration**—You can specify the input range for each channel.
  - **Channels**—Specifies the channel(s) for which you want to select the input range.
  - **Input Range**—Specifies the input range for the selected channel(s) as ±10 V, ±5 V, ±1 V, or ±200 mV.
  - **Terminal Mode**—Specifies the terminal mode for the selected channel(s) as RSE (referenced single-ended), NRSE (non-referenced single-ended), or DIFF (differential).
  - **Minimum Time between Conversions**—Specifies the time (in uSec) between channel samples. The Scan Engine samples all channels of the module sequentially. The default time between sampling one channel and the next is 8 µs. If you connect all unused channels to ground, you should not have to increase this setting. If for some reason you cannot connect unused channels to ground, you can reduce noise by increasing the minimum time between conversions.

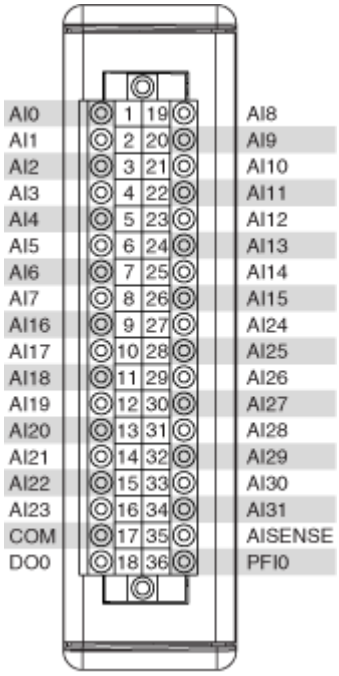
NI 9206

CompactRIO 32-Channel Single-Ended/16-Channel Differential, ±200 mV to ±10 V, 16-Bit Analog Input Module

Software Reference (?)

FPGA Interface | Scan Interface

NI 9206 Pinout



Related Topics

FPGA Interface
Converting and Calibrating CompactRIO Analog Input Values
Detecting Out-of-Range Channels
IO Sample Method
Set Terminal Mode Method
Set Triggers Method
Set Voltage Range Method
Conversion Timing for the NI 9205/9206
Self-Calibration for the NI 9205/9206

NI 9206 (FPGA Interface)

CompactRIO 32-Channel Single-Ended/16-Channel Differential, ±200 mV to ±10 V, 16-Bit Analog Input Module

Open example Find related examples

FPGA I/O Node

You can use an FPGA I/O Node, configured for reading, with this device.

Terminals in Software

Use the FPGA I/O Node to access the following terminals for this device.

Terminal	Description
AI**x**	Analog input channel **x**, where **x** is the number of the channel. The NI 9206 has AI channels 0 to 31. The channel is sampled using the currently configured terminal mode and voltage range. You can configure these settings at edit time using the C Series Module Properties dialog box or at run time using the Set Terminal Mode or Set Voltage Range methods.
DI0	Digital input channel used to access the module digital line, which is labeled PFI0.
Trig	Returns the output of the module trigger circuitry. Use the Set Triggers method to configure the trigger circuit.
DO0	Digital output channel 0.

Refer to the Conversion Timing topic for information about the order and timing of conversions for these I/O channels.

Arbitration

This device supports only the Arbitrate if Multiple Requestors Only option for arbitration. You cannot configure arbitration settings for this device.

I/O Methods

This device does not support any I/O methods.

Module Methods

Use the FPGA I/O Method Node to access the following module methods for this device.

Method	Description
IO Sample	Acquires a single sample from the module. The channel number, terminal mode, and voltage ra nge are all configurable at run time. **Note** NI suggests that you do not configure th e VI to run an IO Sampl e method and another FPGA I/O Method Node in parallel when both a re targeted to the same C Series module. Simil arly, NI suggests that y ou do not configure th e VI to run multiple IO Sample methods in par allel when the IO Samp le methods are targete d to the same C Series module. Refer to the NI 9206 Basic IO VI and the NI 9206 Advanced IO VI in the `labview\examples\CompactRIO\Module Specific\NI 9206\NI 9206 Basic IO\NI 9206 Basic IO.lvproj` and `labview\examples\CompactRIO\Module Specific\NI 9206\NI 9206 Advanced IO\NI 9206 Advanced IO.lvproj` for examples related to this method. Open example (NI 9206 Basic IO) Open example (NI 9206 Advanced IO)

Set Terminal Mode	Sets the terminal mode for a channel as RSE (referenced single-ended), NRSE (non-referenced single-ended), or DIFF (differential). This method overwrites the value you configure in the **C Series Module Properties** dialog box.
Set Triggers	Sets the trigger output to one of the following values: ▪ None ▪ AI Below Low ▪ AI Above High ▪ AI Inside Region ▪ AI Below Low with Hysteresis ▪ AI Above High with Hysteresis ▪ DI Trigger Refer to the NI 9206 Basic Triggering VI and the NI 9206 Advanced Triggering VI in the `labview\examples\CompactRIO\Module Specific\NI 9206\NI 9206 Basic Triggering\NI 9206 Basic Triggering.lvproj` and `labview\examples\CompactRIO\Module Specific\NI 9206\NI 9206 Advanced Triggering\NI 9206 Advanced Triggering.lvproj` for examples related to this method.  Open example (NI 9206 Basic Triggering)  Open example (NI 9206 Advanced Triggering)
Set Voltage Range	Sets the input range for a channel as ±10 V, ±5 V, ±1 V, or ±200 mV. This method overwrites the value you configure in the **C Series Module Properties** dialog box.

I/O Properties

This device does not support any I/O properties.

Module Properties

Use the FPGA I/O Property Node to access the following module properties for this device.

Property	Description
Linearization Coefficient x	(Optional) NI-MCal linearization coefficient x, where **x** is the number of the linearization coefficient. The NI 9206 has linearization coefficients 3 to 0. You can use these coefficients in calibration to compensate for some types of measurement nonlinearity inherent in this device. When returning calibrated data from the FPGA I/O Node, the Linearization Coefficients are not used to calculate the calibrated data. This means that calibrated data returned in FPGA does not compensate for the measurement nonlinearities in the device. Refer to the NI 9206 Advanced IO VI in the `labview\examples\CompactRIO\Module Specific\NI 9206\NI 9206 Advanced IO\NI 9206 Advanced IO.lvproj` for an example of this concept.  Open example
LSB Weight (±10 V range)	Returns the LSB weight in pV/LSB for the ±10 V range. Use this value to convert and calibrate NI 9206 data if you set the **Calibration Mode** to **Raw** in the C Series Module Properties dialog box.
LSB Weight (±1 V range)	Returns the LSB weight in pV/LSB for the ±1 V range. Use this value to convert and calibrate NI 9206 data if you set the **Calibration Mode** to **Ra**

	w in the **C Series Module Properties** dialog box.
LSB Weight (±200 mV range)	Returns the LSB weight in pV/LSB for the ±200 mV range. Use this value to convert and calibrate NI 9206 data if you set the **Calibration Mode** to **Raw** in the **C Series Module Properties** dialog box.
LSB Weight (±5 V range)	Returns the LSB weight in pV/LSB for the ±5 V range. Use this value to convert and calibrate NI 9206 data if you set the **Calibration Mode** to **Raw** in the **C Series Module Properties** dialog box.
Module ID	Returns the module ID, 0x71EB.
Offset (±10 V range)	Returns the calibration offset in nV for the ±10 V range. Use this value to convert and calibrate NI 9206 data if you set the **Calibration Mode** to **Raw** in the C Series Module Properties dialog box.
Offset (±1 V range)	Returns the calibration offset in nV for the ±1 V range. Use this value to convert and calibrate NI 9206 data if you set the **Calibration Mode** to **Raw** in the **C Series Module Properties** dialog box.
Offset (±200 mV range)	Returns the calibration offset in nV for the ±200 mV range. Use this value to convert and calibrate NI 9206 data if you set the **Calibration Mode** to **Raw** in the **C Series Module Properties** dialog box.
Offset (±5 V range)	Returns the calibration offset in nV for the ±5 V range. Use this value to convert and calibrate NI 9206 data if you set the **Calibration Mode** to **Raw** in the **C Series Module Properties** dialog box.
Serial Number	Returns the unique serial number of the module.
Vendor ID	Returns the NI vendor ID, 0x1093.

Single-Cycle Timed Loop

This device does not support the single-cycle Timed Loop.

C Series Module Properties Dialog Box for the NI 9205/9206 (FPGA Interface)

Right-click an NI 9205 or NI 9206 C Series module in the **Project Explorer** window and select **Properties** from the shortcut menu to display this dialog box.

Use this dialog box to configure a C Series module.

This dialog box includes the following components:

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this option.
- **Location**—Specifies a slot in the chassis for the C Series module.
- **Calibration Mode**—Sets the calibration mode for the C Series module. Select **Calibrated** if you want the FPGA I/O Node to return calibrated, fixed-point data from the module in units of volts. The fixed-point data is signed, with a word length of 26 bits and an integer word length of 5 bits. Select **Raw** if you want the FPGA I/O Node to return uncalibrated, binary data from the module. If you select **Raw**, you must convert and calibrate the analog input values in the host VI. The default is **Calibrated**.
- **Channel Configuration**—Specifies the input range for each channel.
  - **Channels**—Specifies the channel(s) for which you want to select the input range.
  - **Input Range**—Specifies the input range for the selected channel(s) as ±10 V, ±5 V, ±1 V, or ±200 mV.
  - **Terminal Mode**—Specifies the terminal mode for the selected channel(s) as RSE (referenced single-ended), NRSE (non-referenced single-ended), or DIFF (differential).

- **Minimum Time Between Conversions**—Specifies the minimum time between conversions in µs.
- **Enable Advanced Self-Calibration Nodes**—Place a checkmark in this checkbox if you want to enable Self-Calibration support in the FPGA for this module.

IO Sample Method (FPGA Interface)

This module method acquires a single sample from the module. The channel number, terminal mode, and voltage range are all configurable at run time. You use this module method by selecting it in an FPGA I/O Method Node that is configured for the appropriate device and/or channel. Details Examples

Note NI suggests that you do not configure the VI to run an IO Sample method and another FPGA I/O Method Node in parallel when both are targeted to the same C Series module. Similarly, NI suggests that you do not configure the VI to run multiple IO Sample methods in parallel when the IO Sample methods are targeted to the same C Series module.

Configuration [i+2] contains encoded configuration information that gets loaded into the module conversion pipeline. This configuration information controls the data to be sampled two iterations into the future. Refer to the Conversion Timing topic for more information. Refer to the Configuration Encoding table below for an example of how the configuration information is encoded.

Data [i] Returns the data from the current sample.

error in describes error conditions that occur before this VI or function runs. The default is no `error`. If an error occurred before this VI or function runs, the VI or function passes the **error in** value to **error out**. This VI or function runs normally only if no error occurred before

this VI or function runs. If an error occurs while this VI or function runs, it runs normally and sets its own error status in **error out**. Use **error in** and **error out** to check errors and to specify execution order by wiring **error out** from one node to **error in** of the next node.

status is TRUE (X) if an error occurred before this VI or function ran or FALSE (checkmark) to indicate a warning or that no error occurred before this VI or function ran. The default is FALSE.

code is the error code number identifying an error. The default is 0. If status is TRUE, code is a nonzero error code. If status is FALSE, code is 0 or a warning code.

source always contains an empty string because strings are not supported in LabVIEW FPGA.

error out contains error information. If **error in** indicates that an error occurred before this VI or function ran, **error out** contains the same error information. Otherwise, it describes the error status that this VI or function produces. Right-click the **error out** indicator on the front panel and select **Explain Error** from the shortcut menu for more information about the error.

status is TRUE (X) if an error occurred or FALSE (checkmark) to indicate a warning or that no error occurred.

code is the error code number identifying an error. The default is 0. If status is TRUE, code is a nonzero error code. If status is FALSE, code is 0 or a warning code.

source always contains an empty string because strings are not supported in LabVIEW FPGA.

Configuration Encoding Table

The following table describes how to construct the Configuration [i+2] value to write to the IO Sample method to perform a particular operation. The **Operation** column lists the types of operations that can be performed using the IO Sample method. The **Configuration Bit Fields** column lists the bit positions within the **Configuration** [i+2] number that need to be set. The **Values** column specifies the binary value to apply to the specified **Configuration Bit Fields**.

Operation	Configuration Bit Fields	Values
AI Read	15:13	001b
	12:11	01b for channels 0-15 10b for channels 16-31
	10:8	000b for channels 0, 8, 16, or 24 001b for channels 1, 9, 17, or 25 … 110b for channels 6, 14, 22, or 30

		111b for channels 7, 15, 23, or 31
	7:6	00b
	5:4	00b for NRSE mode 11b for RSE or DIFF modes
	3:2	11b for channels 8-15 or 24-31 01b for DIFF mode on channels 0-7 or 16-23 10b for RSE or NRSE mode on channels 0-7 or 16-23
	1:0	00b for ±10 V 01b for ±5 V 10b for ±1 V 11b for ±200 mV
DI0 Read	15:0	0000000000000000b
DO0 Write	15:1	010000000000000b
	0	Binary value to write to DO0

Using This Method

The IO Sample method provides an efficient and flexible interface to the module. You can use this method to acquire a single sample from any of the channels on the module, at any range, and with any available input mode.

When this method is executed, the module performs a single conversion on the next channel present in the conversion pipeline on the module. The data from this conversion is returned via the **Data [i]** method output. At the same time that the conversion data is read from the module, the new configuration information specified by the **Configuration [i+2]** input is loaded into the configuration pipeline on the module. The pipeline is two samples deep. So, the configuration information specified on one execution of the IO Sample method determines which channel will be sampled by the IO Sample method two iterations into the future. Refer to the Conversion Timing topic for more details.

Examples

Refer to the NI 9205 Basic IO VI and the NI 9205 Advanced IO VI in the `labview\examples\CompactRIO\Module Specific\NI 9205\NI 9205 Basic IO`

\NI 9205 Basic IO.lvproj and labview\examples\CompactRIO\Module Specific\NI 9205\NI 9205 Advanced IO\NI 9205 Advanced IO.lvproj for examples of the IO concepts discussed above.

Open example (NI 9205 Basic IO)

Open example (NI 9205 Advanced IO)

Set Terminal Mode Method (FPGA Interface)

Overrides the default setting provided in the C Series Module Properties dialog box. You use this module method by selecting it in an FPGA I/O Method Node that is configured for the appropriate device and/or channel.

AI Channel is the channel you want to set the terminal mode for.

Terminal Mode is an enumeration of the following trigger modes:

- **RSE** is a single-ended measurement between any of the 32 individual channels and the module ground.
- **NRSE** is a single-ended measurement between any of the 32 individual channels and the AISENSE line into the module.
- **DIFF** is a differential measurement between two of the 32 individual channels, with the name of the differential channel matching the channel tied to the positive side of the differential measurement. Channels AI0 to AI7, and AI16 to AI23 may be set to DIFF configuration.

error in describes error conditions that occur before this VI or function runs. The default is no `error`. If an error occurred before this VI or function runs, the VI or function passes the **error in** value to **error out**. This VI or function

runs normally only if no error occurred before this VI or function runs. If an error occurs while this VI or function runs, it runs normally and sets its own error status in **error out**. Use **error in** and **error out** to check errors and to specify execution order by wiring **error out** from one node to **error in** of the next node.

status is TRUE (X) if an error occurred before this VI or function ran or FALSE (checkmark) to indicate a warning or that no error occurred before this VI or function ran. The default is FALSE.

code is the error or warning code. The default is 0. If **status** is TRUE, **code** is a nonzero error code. If **status** is FALSE, **code** is 0 or a warning code.

source always contains an empty string because strings are not supported in LabVIEW FPGA.

error out contains error information. If **error in** indicates that an error occurred before this VI or function ran, **error out** contains the same error information. Otherwise, it describes the error status that this VI or function produces. Right-click the **error out** indicator on the front panel and select **Explain Error** from

the shortcut menu for more information about the error.

status is TRUE (X) if an error occurred or FALSE (checkmark) to indicate a warning or that no error occurred.

code is the error or warning code. If **status** is TRUE, **code** is a nonzero error code. If **status** is FALSE, **code** is 0 or a warning code.

source always contains an empty string because strings are not supported in LabVIEW FPGA.

Set Triggers Method (FPGA Interface)

This module method controls the data returned by the trigger digital input line. You use this module method by selecting it in an FPGA I/O Method Node that is configured for the appropriate device and/or channel. Details Examples

Trigger Mode is an enumeration of the following trigger mode options:

- **None** disables the trigger function.
- **AI Below Low** detects when the analog signal is below the low threshold you specify.
- **AI Above High** detects when the analog signal is above the high threshold you specify.

- **AI Inside Region** detects when the analog signal is between the high and low thresholds you specify.
- **AI Below Low with Hysteresis** asserts the trigger when the signal starts above the high threshold you specify and then crosses below the low threshold you specify. The trigger deasserts when the signal crosses above the high threshold you specify.
- **AI Above High with Hysteresis** asserts the trigger when the signal starts below the low threshold you specify and then crosses above the high threshold you specify. The trigger deasserts when the signal crosses below the low threshold you specify.
- **DI Trigger** detects when the digital signal on PFI0 is logic high.

Note The onboard NI 9205 on Single-Board RIO (sbRIO) devices does not support DI triggering.

AI High Threshold defines the upper threshold for the analog trigger circuit.

AI Low Threshold defines the lower threshold for the analog trigger circuit.

error in describes error conditions that occur before this VI or function runs. The default is no `error`. If an error occurred before this VI or function runs, the VI or function passes the **error in** value to **error out**. This VI or function runs normally only if no error occurred before this VI or function runs. If an error occurs while this VI or function runs, it runs normally and

sets its own error status in **error out**. Use **error in** and **error out** to check errors and to specify execution order by wiring **error out** from one node to **error in** of the next node.

status is TRUE if an error occurred. If **status** is TRUE, the VI does not perform any operations.

code is the error code number identifying an error. The default is 0. If status is TRUE, code is a nonzero error code. If status is FALSE, code is 0 or a warning code.

source always contains an empty string because strings are not supported in LabVIEW FPGA.

error out contains error information. If **error in** indicates that an error occurred before this VI or function ran, **error out** contains the same error information. Otherwise, it describes the error status that this VI or function produces. Right-click the **error out** indicator on the front panel and select **Explain Error** from the shortcut menu for more information about the error.

status is TRUE if an error occurred. If **status** is TRUE, the VI does not perform any operations.

code is the error code number identifying an error. The default is 0. If status is TRUE, code is a nonzero error code. If status is FALSE, code is 0 or a warning code.

source always contains an empty string because strings are not supported in LabVIEW FPGA.

Using This Method

Use the Set Triggers Method to configure the trigger circuit on the module. Once the trigger circuit is configured, use an FPGA I/O Node configured to access the Trig channel to monitor the output of the trigger circuit. The trigger circuit does not automatically initiate any conversions on the module. It is up to the FPGA VI to monitor the Trig line, and then initiate a conversion using an FPGA I/O Node or the IO Sample method when the appropriate trigger event occurs.

Perform the following steps to trigger an acquisition using the Set Triggers Method:

1. Ensure that the module pipeline is primed with the next two channels that you want to sample after the trigger event. This step will minimize the delay between the trigger event and the AI channels getting sampled. For analog triggering modes, this step also configures the analog trigger circuitry to monitor the desired channel. The AI trigger circuit monitors the channel waiting in the module pipeline for the next conversion.

   If you are using FPGA I/O Nodes to perform the acquisition, this step can be accomplished by executing an FPGA I/O Node configured to match the FPGA I/O Node that you will be executing after the trigger event. If you are using one of the analog triggering modes along with the FPGA I/O Nodes, the AI trigger circuit will operate on the lowest numbered channel present in the FPGA I/O Node.

Refer to the IO Sample method and Conversion Timing topics for more information on managing the module pipeline using the IO Sample method. If you are using one of the analog trigger modes along with the IO Sample method, the AI trigger circuit will operate on the channel waiting in the pipeline to be converted by the next IO Sample method.

2. Execute the Set Triggers method with the appropriate trigger mode selected. The trigger mode circuitry is implemented in the hardware as you specify in this method. Refer to the NI 9205 and NI 9206 hardware documentation on ni.com/manuals for more information about the trigger modes.
3. Monitor the Trig channel in a loop until you see the appropriate trigger condition occur.
4. Execute an FPGA I/O Node or IO Sample method function to acquire data in response to the trigger event.

Examples

Refer to the NI 9205 Basic Triggering VI and the NI 9205 Advanced Triggering VI in the `labview\examples\CompactRIO\Module Specific\NI 9205\NI 9205 Basic Triggering\NI 9205 Basic Triggering.lvproj` and `labview\examples\CompactRIO\Module Specific\NI 9205\NI 9205 Advanced Triggering\NI 9205 Advanced Triggering.lvproj` for examples of the triggering concepts discussed above.

Open example (NI 9205 Basic Triggering)

Open example (NI 9205 Advanced Triggering)

Set Voltage Range Method (FPGA Interface)

This module method overrides the default setting provided in the C Series Module Properties dialog box. You use this module method by selecting it in an FPGA I/O Method Node that is configured for the appropriate device and/or channel.

AI Channel is the channel you want to set the voltage range for.

Voltage Range is an enumeration of the following voltage ranges:

- ±10 V
- ±5 V
- ±1 V
- ±200 mV

error in describes error conditions that occur before this VI or function runs. The default is no `error`. If an error occurred before this VI or function runs, the VI or function passes the **error in** value to **error out**. This VI or function runs normally only if no error occurred before this VI or function runs. If an error occurs while this VI or function runs, it runs normally and sets its own error status in **error out**. Use **error in** and **error out** to check errors and to specify execution order by wiring **error out** from one node to **error in** of the next node.

status is TRUE if an error occurred. If **status** is TRUE, the VI does not perform any operations.

code is the error code number identifying an error. The default is 0. If status is TRUE, code is a nonzero error code. If status is FALSE, code is 0 or a warning code.

source always contains an empty string because strings are not supported in LabVIEW FPGA.

error out contains error information. If **error in** indicates that an error occurred before this VI or function ran, **error out** contains the same error information. Otherwise, it describes the error status that this VI or function produces. Right-click the **error out** indicator on the front panel and select **Explain Error** from the shortcut menu for more information about the error.

status is TRUE if an error occurred. If **status** is TRUE, the VI does not perform any operations.

code is the error code number identifying an error. The default is 0. If status is TRUE, code is a nonzero error code. If status is FALSE, code is 0 or a warning code.

source always contains an empty string because strings are not supported in LabVIEW FPGA.

Conversion Timing for the NI 9205/9206 (FPGA Interface)

Example

The NI 9205 and NI 9206 modules implement a two-element deep pipeline for access to the AI, DI0, and DO0 channels. This pipeline results in maximum sample rate and maximum sample quality. The Trig channel has a parallel data path that bypasses the pipeline.

When using the FPGA I/O Node to sample channels, the pipeline is automatically managed by the FPGA I/O Node, and the channels within the FPGA I/O Node are sampled in numerical order regardless of the order they appear in the node.

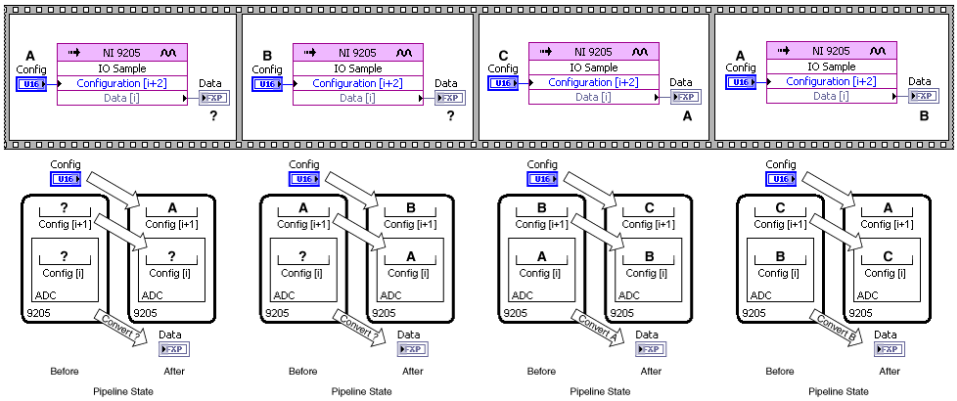
If the first two channel requests in the FPGA I/O Node do not match the two channel requests stored in the module pipeline, there will be a delay before the first channel sample occurs. This delay is caused by the FPGA I/O Node automatically updating the module channel sample pipeline, which takes two channel sample cycles.

To minimize the need for the pipeline updates, each FPGA I/O Node leaves the module pipeline primed to repeat itself. If you use only one FPGA I/O Node in a looping structure, only the first iteration of the loop will incur the two-cycle time delay. All subsequent iterations operate with no delay.

When using the IO Sample method, you must take steps to manage this pipeline in the VIs.

To read one channel, that channel configuration must be requested two cycles before the time it is to be sampled. The U16 configuration value for an AI channel sample contains the channel number, channel input range, and terminal mode. The U16 configuration value also can represent an access to the DIO or DOO channels, which is treated the same as an AI operation.

The following diagram illustrates how the pipeline works within a sequence structure. A typical application would use a loop structure to iterate through a scan list, which is a predefined list of configurations, continuously. The sequence structure and art elements show how data moves into the NI 9205/9206 pipeline and then is converted. Note that the IO Sample method first converts the configuration that is in the ADC, and then shifts the configuration values through the pipeline to prepare for the next time LabVIEW calls the IO Sample method.



The simplest form of pipeline management is to force the pipeline on every set of samples. This assumes that the pipeline is always wrong at the first sample, and sends all IO Sample requests in order. The last two data points need some configuration to be requested, but it does not matter, in this use case, what configuration that is.

A better form of pipeline management emulates the behavior of the FPGA I/O Node. Instead of always assuming that the pipeline is wrong, you choose the last two configuration values based on the first two samples you want to include in the next iteration. This pipeline management system can be accomplished in two parts: initialization and sample iteration.

Tip

NI recommends you use the IO Sample method for the following reasons:

- Smaller on FPGA—With large channel count, the IO Sample method is more efficient with FPGA resources, and thus requires less space on the FPGA for the same application.
- Sample flexibility—The IO Sample method gives you more flexibility to change channel range, terminal mode, and

channel order at run time and at full sample rate.

- Application timing flexibility—The IO Sample method returns all sample data as soon as it is available. The FPGA I/O Node will gather data for all requested samples and then return all at once.

The **Minimum Time Between Conversions** control you can set in the C Series Module Properties dialog box determines the shortest possible time between any two conversions. For channels sampled within the same FPGA I/O Node, the time you set determines the exact time between conversions. For channels sampled within separate FPGA I/O Nodes or for conversions caused by looping on an FPGA I/O Node, the time you set may be less than the actual time between conversions. However, the minimum time you set is never greater than the time between conversions. If the application tries to execute an FPGA I/O Node or IO Sample method faster than the specified minimum time between conversions, the conversion is delayed until the minimum time you set is satisfied.

The default minimum time between conversions for the NI 9205/9206 is 8 µs. The accuracy specifications in the NI 9205 and NI 9206 hardware documentation on ni.com/manuals are based on this default value. If you set the minimum time between conversions to at least 8 µs, the accuracy of the module is not affected. If you set the minimum time between conversions to less than 8 µs, the accuracy of the module degrades if you sample data from multiple channels.

Example

Refer to the NI 9205 Advanced IO VI in the `labview\examples\CompactRIO\Module Specific\NI 9205\NI 9205 Advanced IO\NI 9205 Advanced IO.lvproj` for an example of conversion timing on the NI 9205 and NI 9206 C Series Modules.

Self-Calibration for the NI 9205/9206 (FPGA Interface)

Self-Calibration adjusts the calibration constants stored onboard the module. You can perform a self-calibration at any time to account for changes in environmental conditions. You can enable self-calibration on the C Series Module Properties dialog box.

Enabling Self-Calibration on the NI 9205 or NI 9206 allows access to the Write Self-Calibration Constants and Restore Last External Calibration Constants module methods.

Caution The Write Self-Calibration Constants and Restore Last External Calibration Constants method nodes must be used with the example VI to prevent damaging the module.

Refer to the NI 9205 Self-Calibration VI in the `labview\examples\CompactRIO\Module Specific\NI 9205\NI 9205 Self Calibration\NI 9205 Self Calibration.lvproj` for an example of self-calibration.

NI 9206 (Scan Interface)

CompactRIO 32-Channel Single-Ended/16-Channel Differential, ±200 mV to ±10 V, 16-Bit Analog Input Module


Open example

Module I/O Variables

To use I/O from this module in a VI, drag and drop I/O variables from the **Project Explorer** window to the block diagram of the VI. The I/O variables for the channels return calibrated floating-point data in volts.

Module Channels

The NI 9206 has the following channels.

Channel	Description
AI**x**	Analog input channel **x**, where **x** is the number of the channel. For the NI 9206, **x** is 0 to 31.

C Series Module Properties Dialog Box

Use this dialog box to configure the NI 9206. Right-click the NI 9206 in the **Project Explorer** window and select **Properties** to display this dialog box. You can configure the following options.

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this value.
- **Location**—Specifies a slot in the chassis for the C Series module.
- **Channel Configuration**—You can specify the input range for each channel.
  - **Channels**—Specifies the channel(s) for which you want to select the input range.
  - **Input Range**—Specifies the input range for the selected channel(s) as ±10 V, ±5 V, ±1 V, or ±200 mV.
  - **Terminal Mode**—Specifies the terminal mode for the selected channel(s) as RSE (referenced single-ended), NRSE (non-referenced single-ended), or DIFF (differential).
  - **Minimum Time between Conversions**—Specifies the time between channel samples. The Scan Engine samples all channels of the module sequentially. The default time between sampling one channel and the next is 8 µs. If you connect all unused channels to ground, you should not have to increase this setting. If for some reason you cannot connect unused channels to ground, you can reduce noise by increasing the minimum time between conversions.

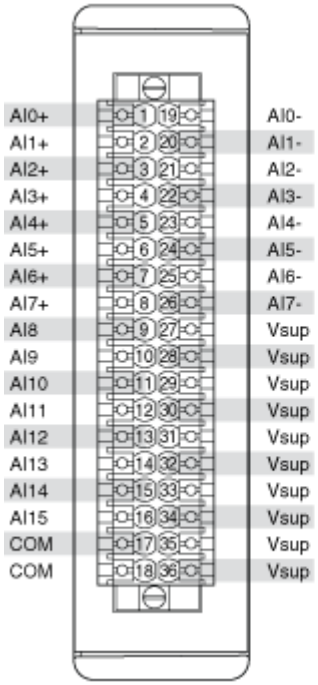
NI 9207

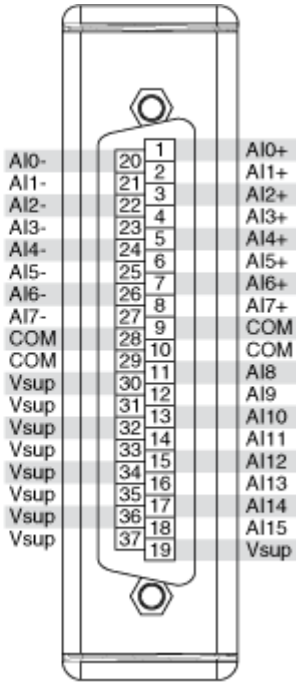
CompactRIO 16-Channel, ±20 mA/±10 V, 24-Bit Isolated Analog Input Module

Software Reference (?)

FPGA Interface | Scan Interface

NI 9207 Pinout





Related Topics

FPGA Interface
Detecting Out-of-Range Channels
Converting NI 9207 Data

NI 9207 (FPGA Interface)

CompactRIO 16-Channel, ±20 mA/±10 V, 24-Bit Isolated Analog Input Module

Open example Find related examples

FPGA I/O Node

You can use an FPGA I/O Node, configured for reading, with this device.

Terminals in Software

Use the FPGA I/O Node to access the following terminals for this device.

Terminal	Description
AI**x**	Analog input channel **x**, where **x** is the number of the channel. The NI 9207 has AI channels 0 to 15.

Arbitration

This device supports only the Arbitrate if Multiple Requestors Only option for arbitration. You cannot configure arbitration settings for this device.

I/O Methods

This device does not support any I/O methods.

Module Methods

This device does not support any module methods.

I/O Properties

This device does not support any I/O properties.

Module Properties

Use the FPGA I/O Property Node to access the following module properties for this device.

Property	Description
Conversion Time	Sets the time it takes to acquire one point of data from one or more channels in a single FPGA I/O Node. You can select **High Speed** or **High Resolution**. Refer to the NI 9207 hardware documentation on ni.com/manuals for more information about the **High Speed** and **High Resolution** conversion times. This property overwrites the value you configure in the C Series Module Pro

	perties dialog box. Returns the conversion time setting when confi gured to read.
Module ID	Returns the module ID, 0x74AD.
Serial Number	Returns the unique serial number of the module .
Vendor ID	Returns the NI vendor ID, 0x1093.

Single-Cycle Timed Loop

This device does not support the single-cycle Timed Loop.

C Series Module Properties Dialog Box for the NI 9207 (FPGA Interface)

Right-click an NI 9207 C Series module in the **Project Explorer** window and select **Properties** from the shortcut menu to display this dialog box.

Use this dialog box to configure a C Series module.

This dialog box includes the following components:

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this option.
- **Location**—Specifies a slot in the chassis for the C Series module.
- **Calibration Mode**—Sets the calibration mode for the C Series module. Select **Calibrated** if you want the FPGA I/O Node to return calibrated, fixed-point data from the module. Refer to the table below for information about the units and encoding of the fixed-point data depending on the channel type. Select **Raw** if you want the FPGA I/O Node to return calibrated, binary data from the module. If you select **Raw**, you must convert the binary values to engineering units. The default is **Calibrated**.

Channel Type	Units of Fixed-Point Data	Integer Type	Word Length	Integer Word Length
Voltage	Volts	Signed	24 bits	5 bits
Current	Amps	Signed	24 bits	–4 bits

- **Conversion Time**—Specifies the time it takes to acquire one point of data from one or more channels in a single FPGA I/O Node. You can select **High Speed** or **High Resolution**. The default is **High Resolution**. Refer to the NI 9207 hardware documentation on ni.com/manuals for more information about the **High Speed** and **High Resolution** conversion times.

Converting NI 9207 Data (FPGA Interface)

Set the **Calibration Mode** to **Calibrated** in the C Series Module Properties dialog box for the NI 9207 if you want the FPGA I/O Node to return calibrated, fixed-point data from the module. Set the **Calibration Mode** to **Raw** if you want the FPGA I/O Node to return calibrated, binary data from the module. If you set the **Calibration Mode** to **Raw**, you must convert the binary values to engineering units. You must convert these values in the host VI.

Using an Equation to Convert Binary Current Values to Amperes

You can use the following equation in the host VI to convert binary current values to amperes:

Amps = **Binary Value** × 0.022 A ÷ 8,388,607

where **Binary Value** is the value returned by the FPGA I/O Node.

Using an Equation to Convert Binary Voltage Values to Volts

You can use the following equation in the host VI to convert binary voltage values to volts:

Volts = **Binary Value** × 10.4 V ÷ 8,388,607

where **Binary Value** is the value returned by the FPGA I/O Node.

NI 9207 (Scan Interface)

CompactRIO 8-Channel ±10 V, 8-Channel ±20 mA, 24-Bit Isolated Analog Input Module

Open example

Module I/O Variables

To use I/O from this module in a VI, drag and drop I/O variables from the **Project Explorer** window to the block diagram of the VI. The I/O variables for channels AI0–AI7 return calibrated floating-point data in volts, and the I/O variables for channels AI8–AI15 return calibrated floating-point data in amps.

Module Channels

The NI 9207 has the following channels.

Channel	Description
AI**x**	Analog input channel **x**, where **x** is the number of the channel. For the NI 9207, **x** is 0 to 15.

C Series Module Properties Dialog Box

Use this dialog box to configure the NI 9207. Right-click the NI 9207 in the **Project Explorer** window and select **Properties** to display this dialog box. You can configure the following options.

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this value.
- **Location**—Specifies a slot in the chassis for the C Series module.
- **Conversion Time**—Determines the time it takes to acquire one point of data from one or more channels. You can select **High Speed** or **High**

Resolution. Refer to the NI 9207 hardware documentation on ni.com/manuals for more information about the **High Speed** and **High Resolution** conversion times.

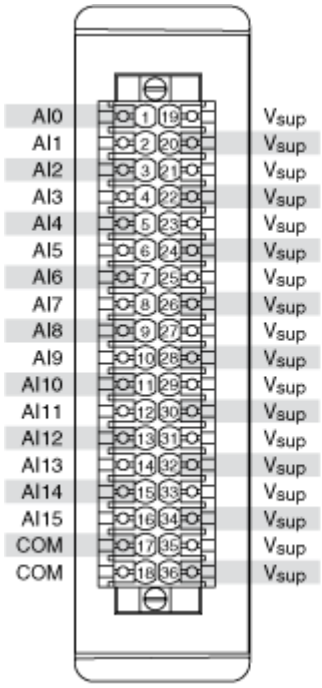
NI 9208

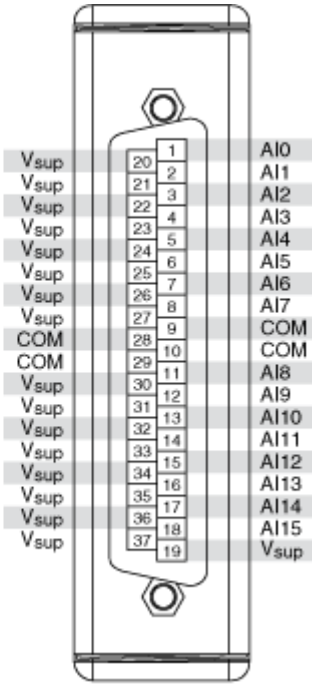
CompactRIO 16-Channel, ±20 mA, 24-Bit Isolated Analog Input Module

Software Reference (?)

FPGA Interface | Scan Interface

NI 9208 Pinout





Related Topics

FPGA Interface
Detecting Out-of-Range Channels
Converting NI 9208 Data

NI 9208 (FPGA Interface)

CompactRIO 16-Channel, ±20 mA, 24-Bit Isolated Analog Input Module

 Open example

 Find related examples

FPGA I/O Node

You can use an FPGA I/O Node, configured for reading, with this device.

Terminals in Software

Use the FPGA I/O Node to access the following terminals for this device.

Terminal	Description
AI**x**	Analog input channel **x**, where **x** is the number of the channel. The NI 9208 has AI channels 0 to 15.

Arbitration

This device supports only the Arbitrate if Multiple Requestors Only option for arbitration. You cannot configure arbitration settings for this device.

I/O Methods

This device does not support any I/O methods.

Module Methods

This device does not support any module methods.

I/O Properties

This device does not support any I/O properties.

Module Properties

Use the FPGA I/O Property Node to access the following module properties for this device.

Property	Description
Conversion Time	Sets the time it takes to acquire one point of data from one or more channels in a single FPGA I/O Node. You can select **High Speed** or **High Resolution**. Refer to the NI 9208 hardware documentation on ni.com/manuals for more information about the **High Speed** and **High Resolution** conversion times. This property overwrites the value you configure in the C Series Module Properties dialog box. Returns the conversion time setting when configured to read.
Module ID	Returns the module ID, 0x74AC.
Serial Number	Returns the unique serial number of the module.
Vendor ID	Returns the NI vendor ID, 0x1093.

Single-Cycle Timed Loop

This device does not support the single-cycle Timed Loop.

C Series Module Properties Dialog Box for the NI 9208 (FPGA Interface)

Right-click an NI 9208 C Series module in the **Project Explorer** window and select **Properties** from the shortcut menu to display this dialog box.

Use this dialog box to configure a C Series module.

This dialog box includes the following components:

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this option.
- **Location**—Specifies a slot in the chassis for the C Series module.

- **Calibration Mode**—Sets the calibration mode for the C Series module. Select **Calibrated** if you want the FPGA I/O Node to return calibrated, fixed-point data from the module in units of amps. The fixed-point data is signed, with a word length of 24 bits and an integer word length of –4 bits. Select **Raw** if you want the FPGA I/O Node to return calibrated, binary data from the module. If you select **Raw**, you must convert the binary current values to amps. The default is **Calibrated**.
- **Conversion Time**—Specifies the time it takes to acquire one point of data from one or more channels in a single FPGA I/O Node. You can select **High Speed** or **High Resolution**. The default is **High Resolution**. Refer to the NI 9208 hardware documentation on ni.com/manuals for more information about the **High Speed** and **High Resolution** conversion times.

Converting NI 9208 Data (FPGA Interface)

Set the **Calibration Mode** to **Calibrated** in the C Series Module Properties dialog box for the NI 9208 if you want the FPGA I/O Node to return calibrated, fixed-point data from the module in units of amps. Set the **Calibration Mode** to **Raw** if you want the FPGA I/O Node to return calibrated, binary data from the module. If you set the **Calibration Mode** to **Raw**, you must convert the binary current values to amps. You must convert these values in the host VI.

You can use the following equation in the host VI to convert binary current values to amperes:

Amps = **Binary Value** × 0.022 A ÷ 8,388,607

where	**Binary Value** is the value returned by the FPGA I/O Node.

NI 9208 (Scan Interface)

CompactRIO 16-Channel, ±20 mA, 24-Bit Isolated Analog Input Module

Open example

Module I/O Variables

To use I/O from this module in a VI, drag and drop I/O variables from the **Project Explorer** window to the block diagram of the VI. The I/O variables for the channels return calibrated floating-point data in amps.

Module Channels

The NI 9208 has the following channels.

Channel	Description
AI**x**	Analog input channel **x**, where **x** is the number of the channel. For the NI 9208, **x** is 0 to 15.

C Series Module Properties Dialog Box

Use this dialog box to configure the NI 9208. Right-click the NI 9208 in the **Project Explorer** window and select **Properties** to display this dialog box. You can configure the following options.

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this value.
- **Location**—Specifies a slot in the chassis for the C Series module.
- **Conversion Time**—Determines the time it takes to acquire one point of data from one or more channels. You can select **High Speed** or **High Resolution**. Refer to the NI 9208 hardware documentation on ni.com/manuals for more information about the **High Speed** and **High Resolution** conversion times.

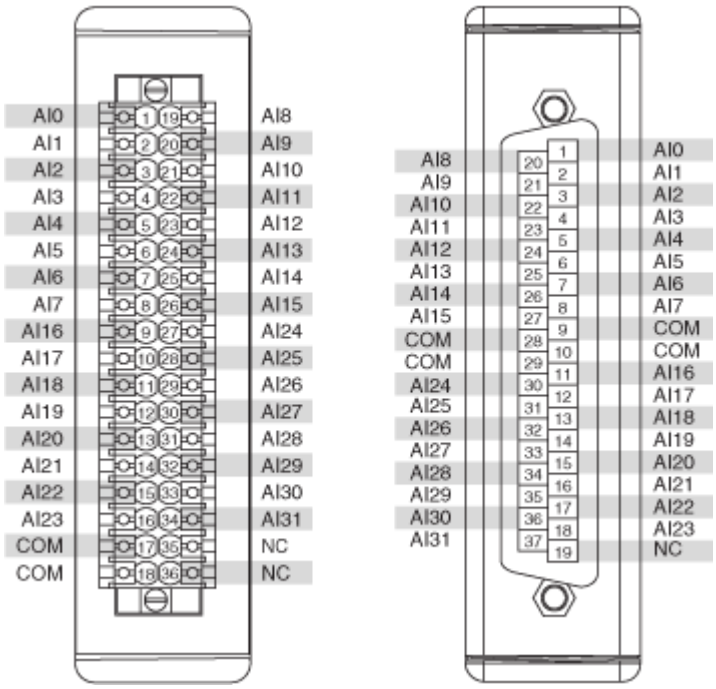
NI 9209

CompactRIO 16-Channel Differential, 32-Channel Single-Ended, ±10 V, 24-Bit Analog Input Module

Software Reference (?)

FPGA Interface

NI 9209 Pinout



Related Topics

FPGA Interface
Detecting Out-of-Range Channels
Converting NI 9209 Data

NI 9209 (FPGA Interface)

CompactRIO 16-Channel Differential, 32-Channel Single-Ended, ±10 V, 24-Bit Analog Input Module

 Open example

 Find related examples

FPGA I/O Node

You can use an FPGA I/O Node, configured for reading, with this device.

Terminals in Software

Use the FPGA I/O Node to access the following terminals for this device.

Terminal	Description
AI**x**	Analog input channel **x**, where **x** is the number of the channel. The NI 9209 has AI channels 0 to 31.

Arbitration

This device supports only the Arbitrate if Multiple Requestors Only option for arbitration. You cannot configure arbitration settings for this device.

I/O Methods

This device does not support any I/O methods.

Module Methods

Use the FPGA I/O Method Node to access the following module methods for this device.

Method	Description
Set Terminal Mode	Sets the terminal mode for a channel as RSE (referenced single-ended) or DIFF (differential). This method overwrites the value you configure in the **C Series Module Properties** dialog box.

I/O Properties

This device does not support any I/O properties.

Module Properties

Use the FPGA I/O Property Node to access the following module properties for this device.

Property	Description
Conversion Time	Sets the time it takes to acquire one point of data from one or more channels in a single FPGA I/O Node. You can select **High Speed** or **High Resolution**. Refer to the NI 9209 hardware documentation on ni.com/manuals for more information about the **High Speed** and **High Resolution** conversion times. This property overwrites the value you configure in the C Series Module Properties dialog box. Returns the conversion time setting when configured to read.
Module ID	Returns the module ID, 0x77F3.
Serial Number	Returns the unique serial number of the module.
Vendor ID	Returns the NI vendor ID, 0x1093.

Single-Cycle Timed Loop

This device does not support the single-cycle Timed Loop.

C Series Module Properties Dialog Box for the NI 9209 (FPGA Interface)

Right-click an NI 9209 C Series module in the **Project Explorer** window and select **Properties** from the shortcut menu to display this dialog box.

Use this dialog box to configure a C Series module.

This dialog box includes the following components:

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module

based on the slot number. You can use this field to give the module a descriptive name.

- **Module Type**—Specifies the type of C Series module. You cannot change this option.
- **Location**—Specifies a slot in the chassis for the C Series module.
- **Calibration Mode**—Sets the calibration mode for the C Series module. Select **Calibrated** if you want the FPGA I/O Node to return calibrated fixed-point data from the module in units of volts. The fixed-point data is signed, with a word length of 24 bits and an integer word length of 5 bits. Select **Raw** if you want the FPGA I/O Node to return calibrated, binary data from the module. If you select **Raw**, you must convert the binary current values to amps. The default is **Calibrated**.
- **Conversion Time**—Specifies the time it takes to acquire one point of data from one or more channels in a single FPGA I/O Node. You can select **High Speed** or **High Resolution**. The default is **High Resolution**. Refer to the NI 9209 hardware documentation on ni.com/manuals for more information about the **High Speed** and **High Resolution** conversion times.
- **Channels**—Specifies which channels you want to configure settings for.
- **Terminal Mode**—Specifies the terminal mode for the selected channels as RSE (referenced single-ended) or DIFF (differential).

Converting NI 9209 Data (FPGA Interface)

Set the **Calibration Mode** to **Calibrated** in the C Series Module Properties dialog box for the NI 9209 if you want the FPGA I/O Node to return calibrated, fixed-point data from the module. Set the **Calibration Mode** to **Raw** if you want the FPGA I/O Node to return calibrated, binary data from the module. If you set the **Calibration Mode** to **Raw**, you must convert the binary values to engineering units. You must convert these values in the host VI.

Using an Equation to Convert Binary Voltage Values to Volts

You can use the following equation in the host VI to convert binary voltage values to volts:

Volts = **Binary Value** × 10.4 V ÷ 8,388,607

where	**Binary Value** is the value returned by the FPGA I/O Node.

NI 9209 (Scan Interface)

CompactRIO 16-Channel Differential, 32-Channel Single-Ended, ±10 V, 24-Bit Analog Input Module

Open example

Module I/O Variables

To use I/O from this module in a VI, drag and drop I/O variables from the **Project Explorer** window to the block diagram of the VI. The I/O variables for the channels return calibrated floating-point data in volts.

Module Channels

The NI 9209 has the following channels.

Channel	Description
AI**x**	Analog input channel **x**, where **x** is the number of the channel. For the NI 9209, **x** is 0 to 31.

C Series Module Properties Dialog Box

Use this dialog box to configure the NI 9209. Right-click the NI 9209 in the **Project Explorer** window and select **Properties** to display this dialog box. You can configure the following options.

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this value.

- **Location**—Specifies a slot in the chassis for the C Series module.
- **Conversion Time**—Determines the time it takes to acquire one point of data from one or more channels. You can select **High Speed** or **High Resolution**.
- **Terminal Mode**—Specifies the terminal mode for one or more selected channels as referenced, single-ended (RSE) or differential (DIFF).

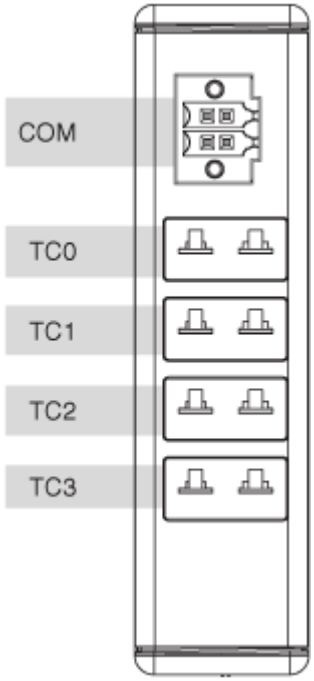
NI 9210

CompactRIO 4-Channel, ±80 mV, 24-Bit Thermocouple Input Module

Software Reference (?)

FPGA Interface

NI 9210 Pinout



Related Topics

FPGA Interface
Detecting Out-of-Range Channels
Converting NI 9210 Data

NI 9210 (FPGA Interface)

CompactRIO 4-Channel, ±80 mV, 24-Bit Thermocouple Input Module

Open example Find related examples

FPGA I/O Node

You can use an FPGA I/O Node, configured for reading, with this device.

Terminals in Software

Use the FPGA I/O Node to access the following terminals for this device.

Terminal	Description
TC**x**	Thermocouple input channel **x**, where **x** is the number of the channel. The NI 9210 has TC channels 0 to 3.
CJC	Cold-junction compensation channel. For the best accuracy, read the CJC channel in the same FPGA I/O Node as the thermocouple input channels. You must convert the CJC data to temperature.
Autozero	Autozero channel. For the best accuracy, read the Autozero channel in the same FPGA I/O Node as the thermocouple input channels.

Arbitration

This device supports only the Arbitrate if Multiple Requestors Only option for arbitration. You cannot configure arbitration settings for this device.

Methods

This device does not support any methods.

I/O Properties

This device does not support any I/O properties.

Module Properties

Use the FPGA I/O Property Node to access the following module properties for this device.

Property	Description
Module ID	Returns the module ID.
Serial Number	Returns the unique serial number of the module .
Vendor ID	Returns the NI vendor ID, 0x1093.

Single-Cycle Timed Loop

This device does not support the single-cycle Timed Loop.

C Series Module Properties Dialog Box for the NI 9210 (FPGA Interface)

Right-click an NI 9210 C Series module in the **Project Explorer** window and select **Properties** from the shortcut menu to display this dialog box.

Use this dialog box to configure a C Series module.

This dialog box includes the following components:

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this option.

- **Location**—Specifies a slot in the chassis for the C Series module.
- **Calibration Mode**—Sets the calibration mode for the C Series module. Select **Calibrated** if you want the FPGA I/O Node to return calibrated, fixed-point data from the module in units of volts. The fixed-point data is signed, with a word length of 24 bits and an integer word length of –2 bits. If you select **Calibrated**, you must convert the fixed-point CJC data to binary CJC data and then convert the binary CJC data to temperature. Select **Raw** if you want the FPGA I/O Node to return calibrated, binary data from the module. If you select **Raw**, you must convert the binary thermocouple values to voltage and convert the binary CJC data to temperature. The default is **Calibrated**.

Converting NI 9210 Data (FPGA Interface)

Set the **Calibration Mode** to **Calibrated** in the C Series Module Properties dialog box for the NI 9210 if you want the FPGA I/O Node to return calibrated, fixed-point data from the module in units of volts. If you set the **Calibration Mode** to **Calibrated**, you must convert the fixed-point CJC data to binary CJC data and then convert the binary CJC data to temperature. Set the **Calibration Mode** to **Raw** if you want the FPGA I/O Node to return calibrated, binary data from the module. If you set the **Calibration Mode** to **Raw**, you must convert the binary thermocouple values to voltage and convert the binary CJC data to temperature. You must convert these values in the host VI.

Using a VI to Convert Data to Temperature

Refer to the Convert to Temperature (NI 9210) polymorphic VI in the `labview\examples\CompactRIO\Module Specific\NI 9210\NI 9210 Support Files.llb` for an example of converting calibrated or raw data to temperature. You can use the Convert to Temperature (NI 9210) VI as a subVI in the host VI.

Using an Equation to Convert Binary Thermocouple Values to Voltage

You can use the following equation in the host VI to convert binary thermocouple values to voltage:

Voltage = **Binary Value** × 80 mV ÷ 8,388,607

where

Binary Value is the value returned by the FPGA I/O Node.

Using an Equation to Convert Fixed-Point CJC Data to Binary CJC Data

You can use the following equation in the host VI to convert fixed-point CJC data to binary CJC data:

Binary CJC Data = (**Fixed-Point CJC Data**) ÷ (0.160 ÷ (2^{24} – 1))

where

Fixed-Point CJC Data is the value returned by the FPGA I/O Node.

Using Equations to Convert Binary CJC Data to Temperature

You can use the following equations in the host VI to convert binary CJC data to temperature:

Calculate the resistance of the thermistor:

$\mathbf{R_T}$ = (10000 × **Binary CJC Data**) ÷ (2^{23} – **Binary CJC Data**)

Calculate the CJC temperature:

T = [1 ÷ [**A** + **B**(ln($\mathbf{R_T}$)) + **C**(ln($\mathbf{R_T}$))^3]] – (273.15 + **OffsetConstant**)

where

T = temperature in °C

A = 1.2873851×10^{-3}

B = 2.3575235×10^{-4}

C = 9.4978060×10^{-8}

$\mathbf{R_T}$ = thermistor resistance reading

OffsetConstant* = 0.1

*The **OffsetConstant** is the typical temperature gradient between the CJC sensor and the thermocouple cold junction.

Refer to the National Institute of Standards and Technology (NIST) Monograph 175 thermocouple reference tables for more information about converting and adjusting thermocouple values.

NI 9210 (Scan Interface)

CompactRIO 4-Channel, ±80 mV, 24-Bit Thermocouple Input Module

Open example

Module I/O Variables

To use I/O from this module in a VI, drag and drop I/O variables from the **Project Explorer** window to the block diagram of the VI. The I/O variables for the channels return calibrated floating-point data in units as specified on the **C Series Module Properties** dialog box.

Note The Scan Interface applies Autozero and cold-junction compensation to NI 9210 data returned in temperature units.

Module Channels

The NI 9210 has the following channels.

Channel	Description
AI**x**	Analog input channel **x**, where **x** is the number of the channel. For the NI 9210, **x** is 0 to 3.

C Series Module Properties Dialog Box

Use this dialog box to configure the NI 9210. Right-click the NI 9210 in the **Project Explorer** window and select **Properties** to display this dialog box. You can configure the following options.

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this value.
- **Location**—Specifies a slot in the chassis for the C Series module.

- **Thermocouple Type**—Specifies the type of thermocouple connected to the channel.
- **Measurement Units**—Specifies the units you want data to be returned in for the channel. You can select **Raw Volts**, **Degrees Kelvin**, **Degrees Celsius**, **Degrees Fahrenheit**, or **Degrees Rankine**.

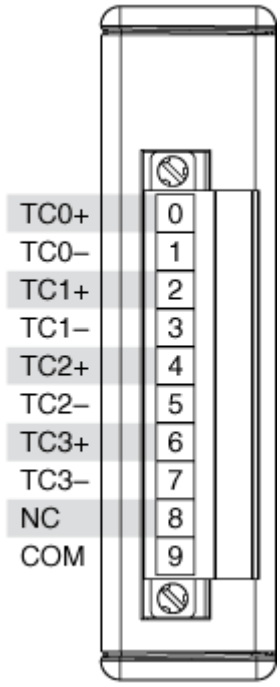
NI 9211

CompactRIO 4-Channel, ±80 mV, 24-Bit Thermocouple Input Module

Software Reference (?)

FPGA Interface | Scan Interface

NI 9211 Pinout



Related Topics

FPGA Interface
Detecting Out-of-Range Channels
Converting NI 9211 Data

NI 9211 (FPGA Interface)

CompactRIO 4-Channel, ±80 mV, 24-Bit Thermocouple Input Module

 Open example

 Find related examples

FPGA I/O Node

You can use an FPGA I/O Node, configured for reading, with this device.

Terminals in Software

Use the FPGA I/O Node to access the following terminals for this device.

Terminal	Description
TC**x**	Thermocouple input channel **x**, where **x** is the number of the channel. The NI 9211 has TC channels 0 to 3.
CJC	Cold-junction compensation channel. For the best accuracy, read the CJC channel in the same FPGA I/O Node as the thermocouple input channels. You must convert the CJC data to temperature.
Autozero	Autozero channel. For the best accuracy, read the Autozero channel in the same FPGA I/O Node as the thermocouple input channels.

Arbitration

This device supports only the Arbitrate if Multiple Requestors Only option for arbitration. You cannot configure arbitration settings for this device.

Methods

This device does not support any methods.

I/O Properties

This device does not support any I/O properties.

Module Properties

Use the FPGA I/O Property Node to access the following module properties for this device.

Property	Description
Module ID	Returns the module ID, 0x70A3.
Serial Number	Returns the unique serial number of the module .
Vendor ID	Returns the NI vendor ID, 0x1093.

Single-Cycle Timed Loop

This device does not support the single-cycle Timed Loop.

C Series Module Properties Dialog Box for the NI 9211 (FPGA Interface)

Right-click an NI 9211 C Series module in the **Project Explorer** window and select **Properties** from the shortcut menu to display this dialog box.

Use this dialog box to configure a C Series module.

This dialog box includes the following components:

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this option.
- **Location**—Specifies a slot in the chassis for the C Series module.
- **Calibration Mode**—Sets the calibration mode for the C Series module. Select **Calibrated** if you want the FPGA I/O Node to return calibrated, fixed-point data from the module in units of volts. The fixed-point data is signed, with a word length of 24 bits and an integer word length of –2 bits. If you select **Calibrated**, you must convert the fixed-point CJC data to binary CJC data and then convert the binary CJC data to temperature. Select **Raw** if you

want the FPGA I/O Node to return calibrated, binary data from the module. If you select **Raw**, you must convert the binary thermocouple values to voltage and convert the binary CJC data to temperature. The default is **Calibrated**.

Converting NI 9211 Data (FPGA Interface)

Set the **Calibration Mode** to **Calibrated** in the C Series Module Properties dialog box for the NI 9211 if you want the FPGA I/O Node to return calibrated, fixed-point data from the module in units of volts. If you set the **Calibration Mode** to **Calibrated**, you must convert the fixed-point CJC data to binary CJC data and then convert the binary CJC data to temperature. Set the **Calibration Mode** to **Raw** if you want the FPGA I/O Node to return calibrated, binary data from the module. If you set the **Calibration Mode** to **Raw**, you must convert the binary thermocouple values to voltage and convert the binary CJC data to temperature. You must convert these values in the host VI.

Note The equations below apply only to the NI 9211. If you are using the NI 9211E board-only module, refer to the KnowledgeBase for the correct equations.

Using a VI to Convert Data to Temperature

Refer to the Convert to Temperature (NI 9211) polymorphic VI in the `labview\examples\CompactRIO\Module Specific\NI 9211\NI 9211 Support Files.llb` for an example of converting calibrated or raw data to temperature. You can use the Convert to Temperature (NI 9211) VI as a subVI in the host VI.

Using an Equation to Convert Binary Thermocouple Values to Voltage

You can use the following equation in the host VI to convert binary thermocouple values to voltage:

Voltage = **Binary Value** × 80 mV ÷ 8,388,607

where

Binary Value is the value returned by the FPGA I/O Node.

Using an Equation to Convert Fixed-Point CJC Data to Binary CJC Data

You can use the following equation in the host VI to convert fixed-point CJC data to binary CJC data:

Binary CJC Data = (**Fixed-Point CJC Data**) ÷ (0.160 ÷ (2^{24} – 1))

where

Fixed-Point CJC Data is the value returned by the FPGA I/O Node.

Using Equations to Convert Binary CJC Data to Temperature

You can use the following equations in the host VI to convert binary CJC data to temperature:

Calculate the resistance of the thermistor:

$\mathbf{R_T}$ = (10000 × **Binary CJC Data**) ÷ (2^{23} – **Binary CJC Data**)

Calculate the CJC temperature:

$\mathbf{T} = [\ 1 \div [\mathbf{A} + \mathbf{B}(\ln(\mathbf{R_T})) + \mathbf{C}(\ln(\mathbf{R_T}))^3]] - (273.15 + \mathbf{OffsetConstant})$

where

T = temperature in °C

A = 1.2873851×10^{-3}

B = 2.3575235×10^{-4}

C = 9.4978060×10^{-8}

$\mathbf{R_T}$ = thermistor resistance reading

OffsetConstant* = 0.7

*The **OffsetConstant** is the typical temperature gradient between the CJC sensor and the thermocouple cold junction.

Refer to the National Institute of Standards and Technology (NIST) Monograph 175 thermocouple reference tables for more information about converting and adjusting thermocouple values.

NI 9211 (Scan Interface)

CompactRIO 4-Channel, ±80 mV, 24-Bit Thermocouple Input Module

Open example

Module I/O Variables

To use I/O from this module in a VI, drag and drop I/O variables from the **Project Explorer** window to the block diagram of the VI. The I/O variables for the channels return calibrated floating-point data in units as specified on the **C Series Module Properties** dialog box.

Note The Scan Interface applies Autozero and cold-junction compensation to NI 9211 data returned in temperature units.

Module Channels

The NI 9211 has the following channels.

Channel	Description
AI**x**	Analog input channel **x**, where **x** is the number of the channel. For the NI 9211, **x** is 0 to 3.

C Series Module Properties Dialog Box

Use this dialog box to configure the NI 9211. Right-click the NI 9211 in the **Project Explorer** window and select **Properties** to display this dialog box. You can configure the following options.

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this value.
- **Location**—Specifies a slot in the chassis for the C Series module.
- **Thermocouple Type**—Specifies the type of thermocouple connected to the channel.

- **Measurement Units**—Specifies the units you want data to be returned in for the channel. You can select **Raw Volts**, **Degrees Kelvin**, **Degrees Celsius**, **Degrees Fahrenheit**, or **Degrees Rankine**.

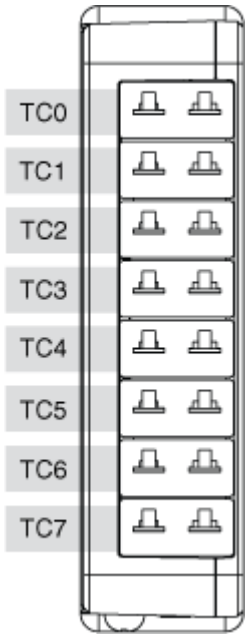
NI 9212

CompactRIO 8-Channel, ±78 mV, 24-Bit Channel-to-Channel Isolated Thermocouple Input Module

Software Reference (?)

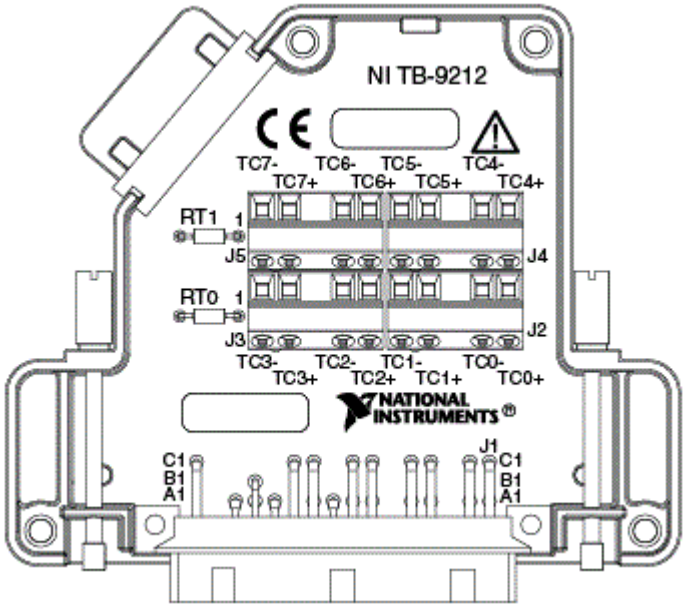
FPGA Interface | Scan Interface

NI 9212 Pinout



NI TB-9212 Pinout

The NI TB-9212 provides connections for eight thermocouple channels on the NI 9212.



Related Topics

FPGA Interface
Detecting Out-of-Range Channels
Converting NI 9212 Data

NI 9212 (FPGA Interface)

CompactRIO 8-Channel, ±78 mV, 24-Bit, Channel-to-Channel Isolated Thermocouple Input Module

Open example

Find related examples

FPGA I/O Node

You can use an FPGA I/O Node, configured for reading, with this device.

Terminals in Software

Use the FPGA I/O Node to access the following terminals for this device.

Terminal	Description

TC**x**	Thermocouple input channel **x**, where **x** is the number of the channel. The NI 9212 has TC channels 0 to 7.
CJC**x**	Cold-junction compensation channel **x**, where **x** is the number of the channel. The NI 9212 has CJC channels 0 to 1. For the best accuracy, read the appropriate CJC channel in the same FPGA I/O Node as the corresponding thermocouple input channels. You must convert the CJC data to temperature. ▪ **CJC 0**—corresponds to thermocouple input channels TC0, TC1, TC2, and TC3. ▪ **CJC 1**—corresponds to thermocouple input channels TC4, TC5, TC6, and TC7.

Arbitration

This device supports only the Arbitrate if Multiple Requestors Only option for arbitration. You cannot configure arbitration settings for this device.

I/O Methods

This device does not support any I/O methods.

Module Methods

Use the FPGA I/O Method Node to access the following module method for this device.

Method	Description
Check Cached Status	Returns Booleans for each channel that indicate whether the channel was out of range or had an open thermocouple since the last execution of the Check Cached Status method. When the FPGA I/O Node reads the channels, the FPGA VI determines the state of the channels and caches any TRUE value until the Check Cached Status method executes.

	▪ **Force Status Read**—When the value of this input is FALSE, the method returns the cached status information since the last time that the Check Cached Status method executed. When the value is TRUE, the method forces the FPGA I/O Node to read all channels and update the status information. Forcing a status read can introduce jitter into an analog input loop. ▪ **Open**—Returns an array of Boolean values. A value of TRUE in any index indicates that the channel sharing a number with that index detected an open thermocouple on the channel at some point after the last time that the Check Cached Status method executed.

I/O Properties

This device does not support any I/O properties.

Module Properties

Use the FPGA I/O Property Node to access the following module properties for this device.

Property	Description
Conversion Time	Sets the time it takes to acquire one point of data from one or more channels in a single FPGA I/O Node. You can select **High Speed**, **Best 60 Hz Rejection**, **Best 50 Hz Rejection**, or **High Resolution**. Refer to the **NI 9212 with NI TB-9212 Datasheet** for more information about the **High Speed**, **Best 60 Hz Rejection**, **Best 50 Hz Rejection**, and **High Resolution** conversion times. This property overwrites the value you configure in the C Series Module Properties dialog box.

	Returns the conversion time setting when configured to read.
Module ID	Returns the module ID, 0x7705.
Serial Number	Returns the unique serial number of the module.
Vendor ID	Returns the NI vendor ID, 0x1093.

Single-Cycle Timed Loop

This device does not support the single-cycle Timed Loop.

C Series Module Properties Dialog Box for the NI 9212 (FPGA Interface)

Right-click an NI 9212 C Series module in the **Project Explorer** window and select **Properties** from the shortcut menu to display this dialog box.

Use this dialog box to configure a C Series module.

This dialog box includes the following components:

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this option.
- **Location**—Specifies a slot in the chassis for the C Series module.
- **Calibration Mode**—Sets the calibration mode for the C Series module. Select **Calibrated** if you want the FPGA I/O Node to return calibrated, fixed-point data from the module in units of volts. The fixed-point data is signed, with a word length of 24 bits and an integer word length of –2 bits. If you select **Calibrated**, you must convert the CJC data from voltage to temperature. Select **Raw** if you want the FPGA I/O Node to return calibrated, binary data from the module. If you select **Raw**, you must convert the binary thermocouple and CJC values to voltage and then convert the CJC data from voltage to temperature. The default is **Calibrated**.

- **Conversion Time**—Specifies the time it takes to acquire one point of data from one or more channels in a single FPGA I/O Node. You can select **High Speed**, **Best 60 Hz Rejection**, **Best 50 Hz Rejection**, or **High Resolution**. The default is **High Resolution**. Refer to the **NI 9212 with NI TB-9212 Datasheet** for more information about the **High Speed**, **Best 60 Hz Rejection**, **Best 50 Hz Rejection**, and **High Resolution** conversion times.

Converting NI 9212 Data (FPGA Interface)

Set the **Calibration Mode** to **Calibrated** in the C Series Module Properties dialog box for the NI 9212 if you want the FPGA I/O Node to return calibrated, fixed-point data from the module in units of volts. If you set the **Calibration Mode** to **Calibrated**, you must convert the CJC data from voltage to temperature. Set the **Calibration Mode** to **Raw** if you want the FPGA I/O Node to return calibrated, binary data from the module. If you set the **Calibration Mode** to **Raw**, you must convert the binary thermocouple and CJC values to voltage and then convert the CJC data from voltage to temperature. You must convert these values in the host VI.

Using a VI to Convert Data to Temperature

Refer to the NI 9212 Convert to Temperature polymorphic VI in the `labview\examples\CompactRIO\Module Specific\NI 9212\NI 9212 Getting Started\NI 9212 Getting Started.lvproj` for an example of converting calibrated or raw data to temperature. You can use the NI 9212 Convert to Temperature VI as a subVI in the host VI.

Using an Equation to Convert Binary Values to Voltage

You can use the following equation in the host VI to convert the binary thermocouple and CJC values to voltage:

Voltage = **Binary Value** × 78.125 mV ÷ 8,388,607

where

Binary Value is the value returned by the FPGA I/O Node.

Converting CJC Data from Voltage to Temperature

The NI 9212 Convert Thermistor Reading VI is a subVI in the NI 9212 Convert to Temperature polymorphic VI that converts CJC data from voltage to temperature.

The VI uses the following equation to calculate the resistance of the thermistor:

$\mathbf{R_T}$ = [(**CJC Data** ÷ 0.078125) ÷ (1 – (**CJC Data** ÷ 0.078125))] × 28,000

Using the resistance of the thermistor, the VI references a look-up table to interpolate the CJC temperature.

Refer to the National Institute of Standards and Technology (NIST) Monograph 175 thermocouple reference tables for more information about converting and adjusting thermocouple values.

NI 9212 (Scan Interface)

CompactRIO 8-Channel, ±78 mV, 24-Bit Channel-to-Channel Isolated Thermocouple Input Module

Open example

Module I/O Variables

To use I/O from this module in a VI, drag and drop I/O variables from the **Project Explorer** window to the block diagram of the VI. The I/O variables for the channels return calibrated floating-point data in units as specified on the **C Series Module Properties** dialog box.

Note The Scan Interface applies cold-junction compensation to NI 9212 data returned in temperature units.

Module Channels

The NI 9212 has the following channels.

Channel	Description
TC**x**	Analog input channel **x**, where **x** is the number of the channel. For the NI 9212, **x** is 0 to 7.

Module-Specific Errors

The NI 9212 can return the following module-specific error.

Error Code	Description
–65582	An open thermocouple was detected.

C Series Module Properties Dialog Box

Use this dialog box to configure the NI 9212. Right-click the NI 9212 in the **Project Explorer** window and select **Properties** to display this dialog box. You can configure the following options.

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this value.
- **Location**—Specifies a slot in the chassis for the C Series module.
- **Conversion Time**—Determines the time it takes to acquire one point of data from one or more channels. You can select **High Speed**, **Best 60 Hz Rejection**, **Best 50 Hz Rejection**, or **High Resolution**. Refer to the **NI 9212 with NI TB-9212 Datasheet** for more information about the **High Speed**, **Best 60 Hz Rejection**, **Best 50 Hz Rejection**, and **High Resolution** conversion times.
- **Channels**—Specifies the channel(s) for which you want to configure settings.
- **Thermocouple Type**—Specifies the type of thermocouple connected to the channel.
- **Measurement Units**—Specifies the units you want data to be returned in for the channel. You can select **Raw Volts**, **Degrees Kelvin**, **Degrees Celsius**, **Degrees Fahrenheit**, or **Degrees Rankine**.

- **Enable Open Thermocouple Detection**—If this box is checked, the NI 9212 returns a zero value and reports an error if it detects an open thermocouple on any channel. This box is checked by default. If you do not check this box, each channel of the NI 9212 independently returns full-scale data and the NI 9212 does not report an error if an open thermocouple is detected

Note Enabling or disabling open thermocouple detection on the NI 9212 has no effect on the accuracy of the measurement because this option on the module is implemented entirely from software.

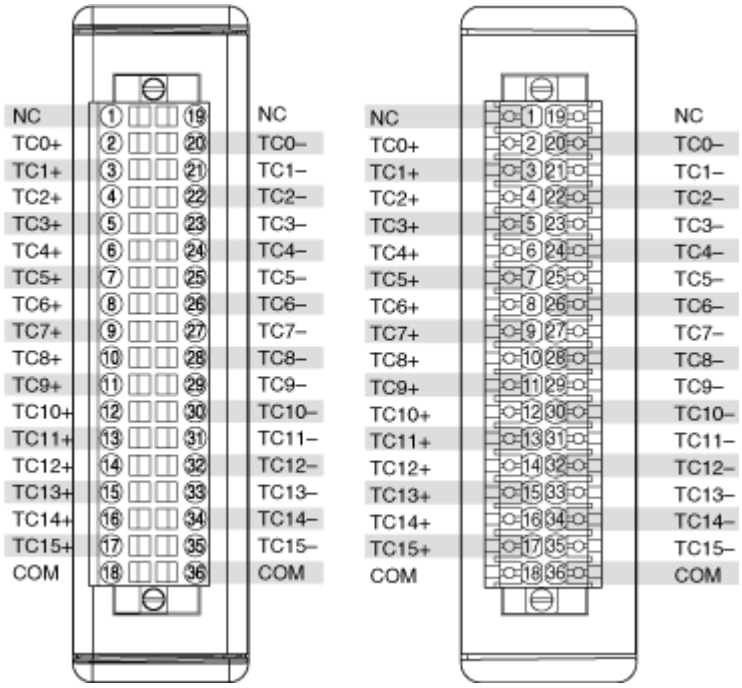
NI 9213

CompactRIO 16-Channel, ±78 mV, 24-Bit Thermocouple Input Module

Software Reference (?)

FPGA Interface | Scan Interface

NI 9213 Pinout



Related Topics

FPGA Interface
Detecting Out-of-Range Channels
Converting NI 9213 Data

NI 9213 (FPGA Interface)

CompactRIO 16-Channel, ±78 mV, 24-Bit Thermocouple Input Module

Open example Find related examples

FPGA I/O Node

You can use an FPGA I/O Node, configured for reading, with this device.

Terminals in Software

Use the FPGA I/O Node to access the following terminals for this device.

Terminal	Description

TC**x**	Thermocouple input channel **x**, where **x** is the number of the channel. The NI 9213 has TC channels 0 to 15.
Autozero	Autozero channel. For the best accuracy, read the Autozero channel in the same FPGA I/O Node as the thermocouple input channels.
CJC	Cold-junction compensation channel. For the best accuracy, read the CJC channel in the same FPGA I/O Node as the thermocouple input channels. You must convert the CJC data to temperature.

Arbitration

This device supports only the Arbitrate if Multiple Requestors Only option for arbitration. You cannot configure arbitration settings for this device.

I/O Methods

This device does not support any I/O methods.

Module Methods

Use the FPGA I/O Method Node to access the following module method for this device.

Method	Description
Check Cached Status	Returns Booleans for each channel that indicate whether the channel was out of range or had an open thermocouple since the last execution of the Check Cached Status method. When the FPGA I/O Node reads the channels, the FPGA VI determines the state of the channels and caches any TRUE value until the Check Cached Status method executes. ▪ **Force Status Read**—When the value of this input is FALSE, the method returns the cached status information since the last time that the Check Cached Status method executed. When the value is TRUE, the

	method forces the FPGA I/O Node to read all channels and update the status information. Forcing a status read can introduce jitter into an analog input loop. ▪ **Out of Range**—Returns an array of Boolean values. A value of TRUE in any index indicates that the channel sharing a number with that index exceeded the common-mode voltage range at some point after the last time that the Check Cached Status method executed. ▪ **Open**—Returns an array of Boolean values. A value of TRUE in any index indicates that the channel sharing a number with that index detected an open thermocouple on the channel at some point after the last time that the Check Cached Status method executed.

I/O Properties

This device does not support any I/O properties.

Module Properties

Use the FPGA I/O Property Node to access the following module properties for this device.

Property	Description
Conversion Time	Sets the time it takes to acquire one point of data from one or more channels in a single FPGA I/O Node. You can select **High Speed** or **High Resolution**. Refer to the NI 9213 hardware documentation on ni.com/manuals for more information about the **High Speed** and **High Resolution** conversion times. This property overwrites the value you configure in the C Series Module Properties dialog box.

	Returns the conversion time setting when configured to read.
Module ID	Returns the module ID, 0x7449.
Serial Number	Returns the unique serial number of the module.
Vendor ID	Returns the NI vendor ID, 0x1093.

Single-Cycle Timed Loop

This device does not support the single-cycle Timed Loop.

C Series Module Properties Dialog Box for the NI 9213 (FPGA Interface)

Right-click an NI 9213 C Series module in the **Project Explorer** window and select **Properties** from the shortcut menu to display this dialog box.

Use this dialog box to configure a C Series module.

This dialog box includes the following components:

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this option.
- **Location**—Specifies a slot in the chassis for the C Series module.
- **Calibration Mode**—Sets the calibration mode for the C Series module. Select **Calibrated** if you want the FPGA I/O Node to return calibrated, fixed-point data from the module in units of volts. The fixed-point data is signed, with a word length of 24 bits and an integer word length of –2 bits. If you select **Calibrated**, you must convert the CJC data from voltage to temperature. Select **Raw** if you want the FPGA I/O Node to return calibrated, binary data from the module. If you select **Raw**, you must convert the binary thermocouple and CJC values to voltage and then convert the CJC data from voltage to temperature. The default is **Calibrated**.

- **Conversion Time**—Specifies the time it takes to acquire one point of data from one or more channels in a single FPGA I/O Node. You can select **High Speed** or **High Resolution**. The default is **High Resolution**. Refer to the NI 9213 hardware documentation on ni.com/manuals for more information about the **High Speed** and **High Resolution** conversion times.

Converting NI 9213 Data (FPGA Interface)

Set the **Calibration Mode** to **Calibrated** in the C Series Module Properties dialog box for the NI 9213 if you want the FPGA I/O Node to return calibrated, fixed-point data from the module in units of volts. If you set the **Calibration Mode** to **Calibrated**, you must convert the CJC data from voltage to temperature. Set the **Calibration Mode** to **Raw** if you want the FPGA I/O Node to return calibrated, binary data from the module. If you set the **Calibration Mode** to **Raw**, you must convert the binary thermocouple and CJC values to voltage and then convert the CJC data from voltage to temperature. You must convert these values in the host VI.

Note The equations below apply only to the NI 9213. If you are using the NI 9213E board-only module, refer to the KnowledgeBase for the correct equations.

Using a VI to Convert Data to Temperature

Refer to the NI 9213 Convert to Temperature polymorphic VI in the `labview\examples\CompactRIO\Module Specific\NI 9213\NI 9213 Getting Started\NI 9213 Getting Started.lvproj` for an example of converting calibrated or raw data to temperature. You can use the NI 9213 Convert to Temperature VI as a subVI in the host VI.

Using an Equation to Convert Binary Values to Voltage

You can use the following equation in the host VI to convert the binary thermocouple and CJC values to voltage:

Voltage = **Binary Value** × 78.125 mV ÷ 8,388,607

where

Binary Value is the value returned by the FPGA I/O Node.

Using Equations to Convert CJC Data from Voltage to Temperature

You can use the following equations in the host VI to convert CJC data from volts to temperature:

Calculate the resistance of the thermistor:

$\mathbf{R_T} = (10000 \times \mathbf{CJC\ Data} \times 32) \div (2.5 - \mathbf{CJC\ Data} \times 32)$

Calculate the CJC temperature:

$\mathbf{T} = [\ 1 \div [\mathbf{A} + \mathbf{B}(\ln(\mathbf{R_T})) + \mathbf{C}(\ln(\mathbf{R_T}))^3]] - (273.15 + \mathbf{OffsetConstant})$

where

T = temperature in °C

A = 1.2873851×10^{-3}

B = 2.3575235×10^{-4}

C = 9.4978060×10^{-8}

$\mathbf{R_T}$ = thermistor resistance reading

OffsetConstant* = 1

*The **OffsetConstant** is the typical temperature gradient between the CJC sensor and the thermocouple cold junction.

Refer to the National Institute of Standards and Technology (NIST) Monograph 175 thermocouple reference tables for more information about converting and adjusting thermocouple values.

NI 9213 (Scan Interface)

CompactRIO 16-Channel, ±78 mV, 24-Bit Thermocouple Input Module

Open example

Module I/O Variables

To use I/O from this module in a VI, drag and drop I/O variables from the **Project Explorer** window to the block diagram of the VI. The I/O variables for the channels

return calibrated floating-point data in units as specified on the **C Series Module Properties** dialog box.

Note The Scan Interface applies Autozero and cold-junction compensation to NI 9213 data returned in temperature units.

Module Channels

The NI 9213 has the following channels.

Channel	Description
TC**x**	Analog input channel **x**, where **x** is the number of the channel. For the NI 9213, **x** is 0 to 15.

C Series Module Properties Dialog Box

Use this dialog box to configure the NI 9213. Right-click the NI 9213 in the **Project Explorer** window and select **Properties** to display this dialog box. You can configure the following options.

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this value.
- **Location**—Specifies a slot in the chassis for the C Series module.
- **Conversion Time**—Determines the time it takes to acquire one point of data from one or more channels. You can select **High Speed** or **High Resolution**. Refer to the NI 9213 hardware documentation on ni.com/manuals for more information about the **High Speed** and **High Resolution** conversion times.
- **Channels**—Specifies the channel(s) for which you want to configure settings.

- **Thermocouple Type**—Specifies the type of thermocouple connected to the channel.
- **Measurement Units**—Specifies the units you want data to be returned in for the channel. You can select **Raw Volts**, **Degrees Kelvin**, **Degrees Celsius**, **Degrees Fahrenheit**, or **Degrees Rankine**.
- **Enable Open Thermocouple Detection**—If this box is checked, the NI 9213 returns a zero value and reports an error if it detects an open thermocouple on any channel. This box is checked by default. If you do not check this box, each channel of the NI 9213 independently returns full-scale data and the NI 9213 does not report an error if an open thermocouple is detected.

Note Enabling or disabling open thermocouple detection on the NI 9213 has no effect on the accuracy of the measurement because this option on the module is implemented entirely from software.

NI 9214

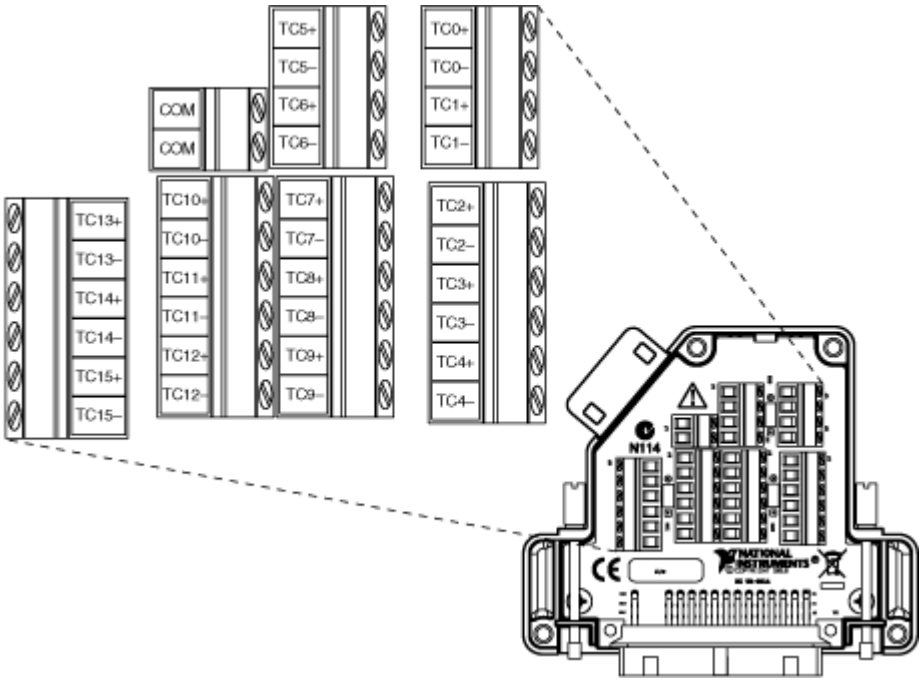
CompactRIO 16-Channel, ±78 mV, 24-Bit Thermocouple Input Module

Software Reference (?)

FPGA Interface | Scan Interface

NI TB-9214 Pinout

The NI TB-9214 provides connections for the 16 thermocouple channels of the NI 9214.



Related Topics

FPGA Interface
Detecting Out-of-Range Channels
Converting NI 9214 Data

NI 9214 (FPGA Interface)

CompactRIO 16-Channel, ±78 mV, 24-Bit Thermocouple Input Module

Open example

Find related examples

FPGA I/O Node

You can use an FPGA I/O Node, configured for reading, with this device.

Terminals in Software

Use the FPGA I/O Node to access the following terminals for this device.

Terminal	Description

TC**x**	Thermocouple input channel **x**, where **x** is the number of the channel. The NI 9214 has TC channels 0 to 15.
Autozero	Autozero channel. For the best accuracy, read the Autozero channel in the same FPGA I/O Node as the thermocouple input channels.
CJC**x**	Cold-junction compensation channel **x**, where **x** is the number of the channel. The NI 9214 has CJC channels 0 to 2. For the best accuracy, read the appropriate CJC channel in the same FPGA I/O Node as the corresponding thermocouple input channels. You must convert the CJC data to temperature. ▪ **CJC 0**—corresponds to thermocouple input channels TC2, TC3, TC4, TC7, TC8, and TC9. ▪ **CJC 1**—corresponds to thermocouple input channels TC10, TC11, TC12, TC13, TC14, and TC15. ▪ **CJC 2**—corresponds to thermocouple input channels TC0, TC1, TC5, and TC6.

Arbitration

This device supports only the Arbitrate if Multiple Requestors Only option for arbitration. You cannot configure arbitration settings for this device.

I/O Methods

This device does not support any I/O methods.

Module Methods

Use the FPGA I/O Method Node to access the following module method for this device.

Method	Description

Check Cached Status	Returns Booleans for each channel that indicate whether the channel was out of range or had an open thermocouple since the last execution of the Check Cached Status method. When the FPGA I/O Node reads the channels, the FPGA VI determines the state of the channels and caches any TRUE value until the Check Cached Status method executes. ▪ **Force Status Read**—When the value of this input is FALSE, the method returns the cached status information since the last time that the Check Cached Status method executed. When the value is TRUE, the method forces the FPGA I/O Node to read all channels and update the status information. Forcing a status read can introduce jitter into an analog input loop. ▪ **Out of Range**—Returns an array of Boolean values. A value of TRUE in any index indicates that the channel sharing a number with that index exceeded the common-mode voltage range at some point after the last time that the Check Cached Status method executed. ▪ **Open**—Returns an array of Boolean values. A value of TRUE in any index indicates that the channel sharing a number with that index detected an open thermocouple on the channel at some point after the last time that the Check Cached Status method executed.

I/O Properties

This device does not support any I/O properties.

Module Properties

Use the FPGA I/O Property Node to access the following module properties for this device.

Property	Description
Conversion Time	Sets the time it takes to acquire one point of data from one or more channels in a single FPGA I/O Node. You can select **High Speed** or **High Resolution**. Refer to the **NI 9214 with NI TB-9214 Operating Instructions and Specifications** for more information about the **High Speed** and **High Resolution** conversion times. This property overwrites the value you configure in the C Series Module Properties dialog box. Returns the conversion time setting when configured to read.
Open TC Detection Enable	Enables open thermocouple detection on the module. When this property is enabled, the NI 9214 returns an error if it detects an open thermocouple on any TC**x** channel. This property overwrites the value you configure in the C Series Module Properties dialog box. **Note** Enabling open thermocouple detection on the NI 9214 results in a small current leakage in the thermocouple measurement. Refer to the Overview of Open Thermocouple Detection support document for more information about compensating for this error. Returns open thermocouple detection setting when configured to read.

Module ID	Returns the module ID, 0x74EE.
Serial Number	Returns the unique serial number of the module .
Vendor ID	Returns the NI vendor ID, 0x1093.

Single-Cycle Timed Loop

This device does not support the single-cycle Timed Loop.

C Series Module Properties Dialog Box for the NI 9214 (FPGA Interface)

Right-click an NI 9214 C Series module in the **Project Explorer** window and select **Properties** from the shortcut menu to display this dialog box.

Use this dialog box to configure a C Series module.

This dialog box includes the following components:

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this option.
- **Location**—Specifies a slot in the chassis for the C Series module.
- **Calibration Mode**—Sets the calibration mode for the C Series module. Select **Calibrated** if you want the FPGA I/O Node to return calibrated, fixed-point data from the module in units of volts. The fixed-point data is signed, with a word length of 24 bits and an integer word length of –2 bits. If you select **Calibrated**, you must convert the CJC data from voltage to temperature. Select **Raw** if you want the FPGA I/O Node to return calibrated, binary data from the module. If you select **Raw**, you must convert the binary thermocouple and CJC values to voltage and then convert the CJC data from voltage to temperature. The default is **Calibrated**.
- **Conversion Time**—Specifies the time it takes to acquire one point of data from one or more channels in a single FPGA I/O Node. You can select **High**

Speed or **High Resolution**. The default is **High Resolution**. Refer to the **NI 9214 with NI TB-9214 Operating Instructions and Specifications** for more information about the **High Speed** and **High Resolution** conversion times.

- **Enable Open Thermocouple Detection**—Place a checkmark in this checkbox if you want to enable open thermocouple detection on the module.

Note Enabling open thermocouple detection on the NI 9214 results in a small current leakage in the thermocouple measurement. Refer to the Overview of Open Thermocouple Detection support document for more information about compensating for this error.

Converting NI 9214 Data (FPGA Interface)

Set the **Calibration Mode** to **Calibrated** in the C Series Module Properties dialog box for the NI 9214 if you want the FPGA I/O Node to return calibrated, fixed-point data from the module in units of volts. If you set the **Calibration Mode** to **Calibrated**, you must convert the CJC data from voltage to temperature. Set the **Calibration Mode** to **Raw** if you want the FPGA I/O Node to return calibrated, binary data from the module. If you set the **Calibration Mode** to **Raw**, you must convert the binary thermocouple and CJC values to voltage and then convert the CJC data from voltage to temperature. You must convert these values in the host VI.

Using a VI to Convert Data to Temperature

Refer to the NI 9214 Convert to Temperature polymorphic VI in the `labview\examples\CompactRIO\Module Specific\NI 9214\NI 9214 Getting Started\NI 9214 Getting Started.lvproj` for an example of converting calibrated or raw data to temperature. You can use the NI 9214 Convert to Temperature VI as a subVI in the host VI.

Using an Equation to Convert Binary Values to Voltage

You can use the following equation in the host VI to convert the binary thermocouple and CJC values to voltage:

Voltage = **Binary Value** × 78.125 mV ÷ 8,388,607

where

Binary Value is the value returned by the FPGA I/O Node.

Converting CJC Data from Voltage to Temperature

The NI 9214 Convert Thermistor Reading VI is a subVI in the NI 9214 Convert to Temperature polymorphic VI that converts CJC data from voltage to temperature.

The VI uses the following equation to calculate the resistance of the thermistor:

$\mathbf{R_T}$ = [(**CJC Data** ÷ 0.078125) ÷ (1 – (**CJC Data** ÷ 0.078125))] × 20,000

Using the resistance of the thermistor, the VI references a look-up table to interpolate the CJC temperature.

Refer to the National Institute of Standards and Technology (NIST) Monograph 175 thermocouple reference tables for more information about converting and adjusting thermocouple values.

NI 9214 (Scan Interface)

CompactRIO 16-Channel, ±78 mV, 24-Bit Thermocouple Input Module

Open example

Module I/O Variables

To use I/O from this module in a VI, drag and drop I/O variables from the **Project Explorer** window to the block diagram of the VI. The I/O variables for the channels return calibrated floating-point data in units as specified on the **C Series Module Properties** dialog box.

Note The Scan Interface applies Autozero and cold-junction compensation to NI 9214 data returned in temperature units.

Module Channels

The NI 9214 has the following channels.

Channel	Description
TC**x**	Analog input channel **x**, where **x** is the number of the channel. For the NI 9214, **x** is 0 to 15.

Module-Specific Errors

The NI 9214 can return the following module-specific errors.

Error Code	Description
–65582	An open thermocouple was detected.
–65583	A common-mode range error was detected.

C Series Module Properties Dialog Box

Use this dialog box to configure the NI 9214. Right-click the NI 9214 in the **Project Explorer** window and select **Properties** to display this dialog box. You can configure the following options.

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this value.
- **Location**—Specifies a slot in the chassis for the C Series module.
- **Conversion Time**—Determines the time it takes to acquire one point of data from one or more channels. You can select **High Speed** or **High Resolution**. Refer to the NI 9214 hardware documentation on ni.com/manuals for more information about the **High Speed** and **High Resolution** conversion times.
- **Channels**—Specifies the channel(s) for which you want to configure settings.
- **Thermocouple Type**—Specifies the type of thermocouple connected to the channel.

- **Measurement Units**—Specifies the units you want data to be returned in for the channel. You can select **Raw Volts**, **Degrees Kelvin**, **Degrees Celsius**, **Degrees Fahrenheit**, or **Degrees Rankine**.
- **Enable Open Thermocouple Detection**—If this box is checked, the NI 9214 returns a zero value and reports an error if it detects an open thermocouple on any channel. This box is checked by default. If you do not check this box, the Open Thermocouple Detection Circuit is disabled and the NI 9214 does not report an error or go to full-scale when an open thermocouple is detected.

Note Enabling open thermocouple detection on the NI 9214 results in a small current leakage in the thermocouple measurement. Refer to the Overview of Open Thermocouple Detection support document for more information about compensating for this error.

NI 9214 OTD Compensation Example VI

Refer to the NI 9214 OTD Compensation VI in the `labview\examples\CompactRIO\NI Scan Engine\Module Specific\Analog Input\NI 9214 - Compensation - Scan Mode\NI 9214 OTD Compensation - Scan Mode.lvproj` for an example that compensates for the error introduced by enabling open thermocouple detection on the NI 9214.

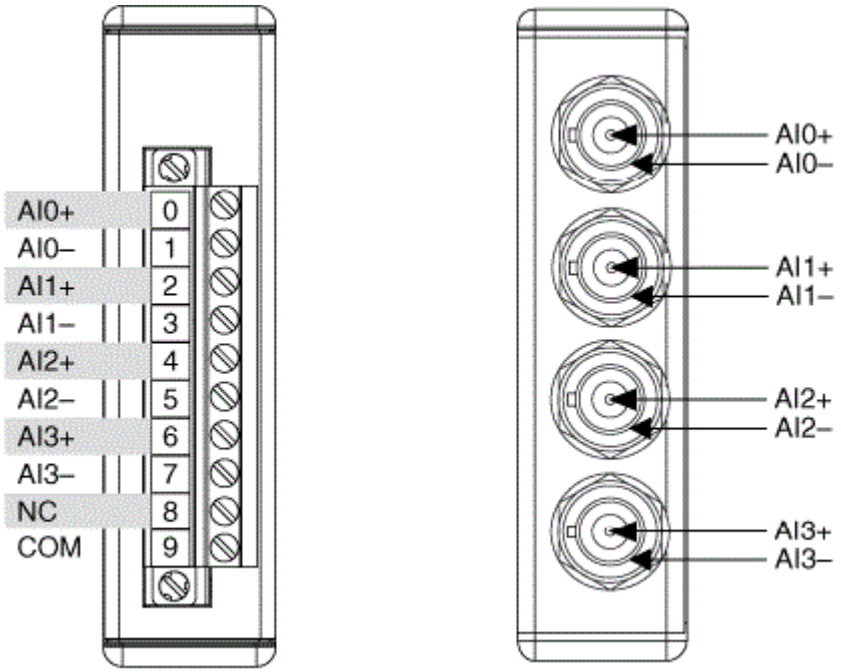
NI 9215

CompactRIO 4-Channel, ±10 V, 16-Bit Simultaneous Analog Input Module

Software Reference (?)

FPGA Interface | Scan Interface

NI 9215 Pinout



Related Topics

FPGA Interface
Converting and Calibrating CompactRIO Analog Input Values
Detecting Out-of-Range Channels

NI 9215 (FPGA Interface)

CompactRIO 4-Channel, ±10 V, 16-Bit Simultaneous Analog Input Module

FPGA I/O Node

You can use an FPGA I/O Node, configured for reading, with this device.

Note You can simultaneously read from multiple channels on the NI 9215.

Terminals in Software

Use the FPGA I/O Node to access the following terminals for this device.

Terminal	Description
AI**x**	Analog input channel **x**, where **x** is the number of the channel. The NI 9215 has AI channels 0 to 3.

Arbitration

This device supports only the Arbitrate if Multiple Requestors Only option for arbitration. You cannot configure arbitration settings for this device.

Methods

This device does not support any methods.

I/O Properties

Use the FPGA I/O Property Node to access the following I/O properties for this device.

Property	Description
LSB Weight	Returns the LSB weight in nV/LSB for the channel. Use this value to convert and calibrate NI 9215 data if you set the **Calibration Mode** to **Raw** in the C Series Module Properties dialog box.
Offset	Returns the calibration offset in nV for the channel. Use this value to convert and calibrate NI 9215 data if you set the **Calibration Mode** to **Raw** in the **C Series Module Properties** dialog box.

Module Properties

Use the FPGA I/O Property Node to access the following module properties for this device.

Property	Description
Module ID	Returns the module ID, 0x7135 (NI 9215 with BNC) or 0x70A6 (NI 9215 with screw terminal).

Serial Number	Returns the unique serial number of the module .
Vendor ID	Returns the NI vendor ID, 0x1093.

Single-Cycle Timed Loop

This device does not support the single-cycle Timed Loop.

C Series Module Properties Dialog Box for the NI 9215 (FPGA Interface)

Right-click an NI 9215 C Series module in the **Project Explorer** window and select **Properties** from the shortcut menu to display this dialog box.

Use this dialog box to configure a C Series module.

This dialog box includes the following components:

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this option.
- **Location**—Specifies a slot in the chassis for the C Series module.
- **Calibration Mode**—Sets the calibration mode for the C Series module. Select **Calibrated** if you want the FPGA I/O Node to return calibrated, fixed-point data for the module in units of volts. The fixed-point data is signed, with a word length of 20 bits and an integer word length of 5 bits. Select **Raw** if you want the FPGA I/O Node to return uncalibrated, binary data for the module. If you select **Raw**, you must convert and calibrate the analog input values in the host VI. The default is **Calibrated**.

NI 9215 (Scan Interface)

CompactRIO 4-Channel, ±10 V, 16-Bit Simultaneous Analog Input Module

 Open example

Module I/O Variables

To use I/O from this module in a VI, drag and drop I/O variables from the **Project Explorer** window to the block diagram of the VI. The I/O variables for the channels return calibrated floating-point data in volts.

Module Channels

The NI 9215 has the following channels.

Channel	Description
AI**x**	Analog input channel **x**, where **x** is the number of the channel. For the NI 9215, **x** is 0 to 3.

C Series Module Properties Dialog Box

Use this dialog box to configure the NI 9215. Right-click the NI 9215 in the **Project Explorer** window and select **Properties** to display this dialog box. You can configure the following options.

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this value.
- **Location**—Specifies a slot in the chassis for the C Series module.

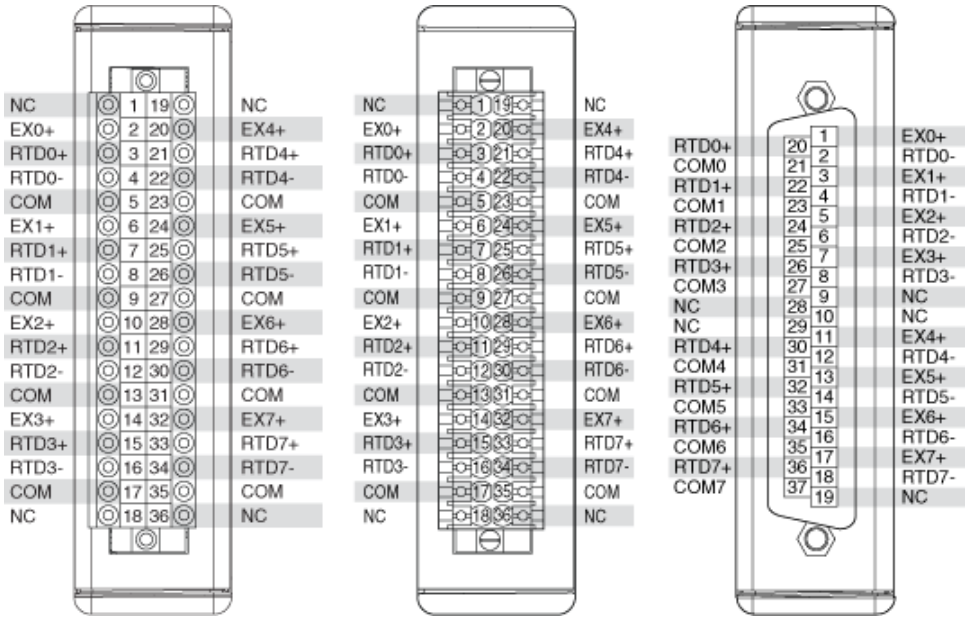
NI 9216

CompactRIO 8-Channel, 24-Bit, 100 Ω RTD Analog Input Module

Software Reference (?)

FPGA Interface

NI 9216 Pinout



Related Topics

FPGA Interface
Converting and Calibrating CompactRIO Analog Input Values
Detecting Out-of-Range Channels
Converting Nominal Values to Temperature Values for the NI 9216

NI 9216 (FPGA Interface)

CompactRIO 8-Channel, 24-Bit, 100 Ω RTD Analog Input Module

Open example Find related examples

FPGA I/O Node

You can use an FPGA I/O Node, configured for reading, with this device.

Terminals in Software

Use the FPGA I/O Node to access the following terminals for this device.

Terminal	Description

RTD**x**	RTD input channel **x**, where **x** is the number of the channel. The NI 9216 has RTD channels 0 to 7.

Arbitration

This device supports only the Arbitrate if Multiple Requestors Only option for arbitration. You cannot configure arbitration settings for this device.

Methods

This device does not support any methods.

I/O Properties

Use the FPGA I/O Property Node to access the following I/O properties for this device.

Property	Description
LSB Weight	Returns the LSB weight in pΩ/LSB for the channel. Use this value to convert and calibrate NI 9216 data if you set the **Calibration Mode** to **Raw** in the C Series Module Properties dialog box.
Offset	Returns the calibration offset in µΩ for the channel. Use this value to convert and calibrate NI 9216 data if you set the **Calibration Mode** to **Raw** in the **C Series Module Properties** dialog box.

Module Properties

Use the FPGA I/O Property Node to access the following module properties for this device.

Property	Description
Conversion Time	Sets the time in milliseconds it takes to acquire conversion data. This property overwrites the value you configure in the C Series Module Properties dialog box.

Module ID	Returns the module ID, 0x77C4 (NI 9216 with spring terminal) or 0x77DF (NI 9216 with DSUB).
Serial Number	Returns the unique serial number of the module.
Vendor ID	Returns the NI vendor ID, 0x1093.

Single-Cycle Timed Loop

This device does not support the single-cycle Timed Loop.

C Series Module Properties Dialog Box for the NI 9216 (FPGA Interface)

Right-click an NI 9216 C Series module in the **Project Explorer** window and select **Properties** from the shortcut menu to display this dialog box.

Use this dialog box to configure a C Series module.

This dialog box includes the following components:

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this option.
- **Location**—Specifies a slot in the chassis for the C Series module.
- **Calibration Mode**—Sets the calibration mode for the C Series module. Select **Calibrated** if you want the FPGA I/O Node to return calibrated, fixed-point data from the module in units of ohms. The fixed-point data is signed, with a word length of 24 bits and an integer word length of 10 bits. Select **Raw** if you want the FPGA I/O Node to return uncalibrated, binary data from the module. If you select **Raw**, you must convert and calibrate the analog input values in the host VI. The default is **Calibrated**.
- **Conversion Time**—Specifies the time it takes to acquire one point of data from all channels. You can select **200 ms** or **2.5 ms**.

Converting Nominal Values to Temperature Values for the NI 9216 (FPGA Interface)

Set the **Calibration Mode** to **Calibrated** in the C Series Module Properties dialog box for the NI 9216 if you want the FPGA I/O Node to return calibrated, fixed-point data for the module in units of ohms. If you set the **Calibration Mode** to **Raw**, the FPGA I/O Node returns uncalibrated, binary values for the module. After you convert these binary values to nominal values, you can convert the nominal resistance values into temperature values. You must convert these values in the host VI.

Using a VI to Convert Values

Refer to the RTD to Temp VI in the `labview\examples\CompactRIO\Module Specific\NI 9216\NI 9216 Getting Started\NI 9216 Getting Started.lvproj` for an example of converting nominal resistance values to temperature. You can use the RTD to Temp VI as a subVI in the host VI to convert nominal resistance values to temperature.

Using an Equation to Measure Temperature

You can use a linearization curve known as the Callendar-Van Dusen equation in the host VI to measure the temperature of RTDs.

NI 9216 (Scan Interface)

CompactRIO 8-Channel, 24-Bit, 100 Ω RTD Analog Input Module

Open example

Module I/O Variables

To use I/O from this module in a VI, drag and drop I/O variables from the **Project Explorer** window to the block diagram of the VI. The I/O variables for the channels return calibrated floating-point data in units as specified on the **C Series Module Properties** dialog box.

Module Channels

The NI 9216 has the following channels.

Channel	Description
RTD**x**	RTD input channel **x**, where **x** is the number of t he channel. The NI 9216 has RTD channels 0 to 7 .

C Series Module Properties Dialog Box

Use this dialog box to configure the NI 9216. Right-click the NI 9216 in the **Project Explorer** window and select **Properties** to display this dialog box. You can configure the following options.

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this value.
- **Location**—Specifies a slot in the chassis for the C Series module.
- **Conversion Time**—Specifies the time it takes to acquire one point of data from all channels. You can select **200 ms** or **2.5 ms**.
- **Channels**—Specifies the channel(s) for which you want to configure settings.
- **Measurement Units**—Specifies the units you want data to be returned in for the channel. You can select **Raw Ohms**, **Degrees Kelvin**, **Degrees Celsius**, **Degrees Fahrenheit**, or **Degrees Rankine**.
- **RTD Type**—Specifies the type of RTD connected to the channel by temperature coefficient of resistance (TCR). If you select **Custom**, you must enter the **Callendar-Van Dusen Coefficients** below.
  - **Callendar-Van Dusen Coefficients**—Specifies the coefficients to use in the Callendar-Van Dusen equation, a linearization curve for measuring the temperature of an RTD.

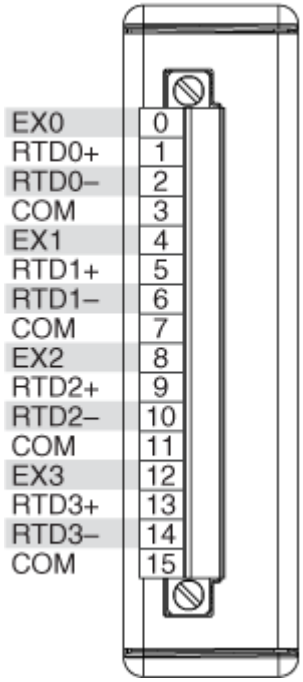
NI 9217

CompactRIO 4-Channel, 24-Bit, 100 Ω RTD Analog Input Module

Software Reference (?)

FPGA Interface | Scan Interface

NI 9217 Pinout



Related Topics

FPGA Interface
Converting and Calibrating CompactRIO Analog Input Values
Detecting Out-of-Range Channels
Converting Nominal Values to Temperature Values for the NI 9217

NI 9217 (FPGA Interface)

CompactRIO 4-Channel, 24-Bit, 100Ω RTD Analog Input Module

Open example Find related examples

FPGA I/O Node

You can use an FPGA I/O Node, configured for reading, with this device.

Terminals in Software

Use the FPGA I/O Node to access the following terminals for this device.

Terminal	Description
RTD**x**	RTD input channel **x**, where **x** is the number of t he channel. The NI 9217 has RTD channels 0 to 3 .

Arbitration

This device supports only the Arbitrate if Multiple Requestors Only option for arbitration. You cannot configure arbitration settings for this device.

Methods

This device does not support any methods.

I/O Properties

Use the FPGA I/O Property Node to access the following I/O properties for this device.

Property	Description
LSB Weight	Returns the LSB weight in pΩ/LSB for the chann el. Use this value to convert and calibrate NI 921 7 data if you set the **Calibration Mode** to **Raw** in the C Series Module Properties dialog box.
Offset	Returns the calibration offset in µΩ for the chan nel. Use this value to convert and calibrate NI 92 17 data if you set the **Calibration Mode** to **Ra w** in the **C Series Module Properties** dialog b ox.

Module Properties

Use the FPGA I/O Property Node to access the following module properties for this device.

Property	Description
Conversion Time	Sets the time in milliseconds it takes to acquire conversion data. This property overwrites the value you configure in the C Series Module Properties dialog box.
Module ID	Returns the module ID, 0x712B.
Serial Number	Returns the unique serial number of the module.
Vendor ID	Returns the NI vendor ID, 0x1093.

Single-Cycle Timed Loop

This device does not support the single-cycle Timed Loop.

C Series Module Properties Dialog Box for the NI 9217 (FPGA Interface)

Right-click an NI 9217 C Series module in the **Project Explorer** window and select **Properties** from the shortcut menu to display this dialog box.

Use this dialog box to configure a C Series module.

This dialog box includes the following components:

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this option.
- **Location**—Specifies a slot in the chassis for the C Series module.
- **Calibration Mode**—Sets the calibration mode for the C Series module. Select **Calibrated** if you want the FPGA I/O Node to return calibrated, fixed-point data from the module in units of ohms. The fixed-point data is signed,

with a word length of 24 bits and an integer word length of 10 bits. Select **Raw** if you want the FPGA I/O Node to return uncalibrated, binary data from the module. If you select **Raw**, you must convert and calibrate the analog input values in the host VI. The default is **Calibrated**.

- **Conversion Time**—Specifies the time it takes to acquire one point of data from all channels. You can select **200 ms** or **2.5 ms**.

Converting Nominal Values to Temperature Values for the NI 9217 (FPGA Interface)

Set the **Calibration Mode** to **Calibrated** in the C Series Module Properties dialog box for the NI 9217 if you want the FPGA I/O Node to return calibrated, fixed-point data for the module in units of ohms. If you set the **Calibration Mode** to **Raw**, the FPGA I/O Node returns uncalibrated, binary values for the module. After you convert these binary values to nominal values, you can convert the nominal resistance values into temperature values. You must convert these values in the host VI.

Using a VI to Convert Values

Refer to the RTD to Temp VI in the `labview\examples\CompactRIO\Module Specific\NI 9217\NI 9217 Getting Started\NI 9217 Getting Started.lvproj` for an example of converting nominal resistance values to temperature. You can use the RTD to Temp VI as a subVI in the host VI to convert nominal resistance values to temperature.

Using an Equation to Measure Temperature

You can use a linearization curve known as the Callendar-Van Dusen equation in the host VI to measure the temperature of RTDs.

NI 9217 (Scan Interface)

CompactRIO 4-Channel, 24-Bit, 100Ω RTD Analog Input Module


Open example

Module I/O Variables

To use I/O from this module in a VI, drag and drop I/O variables from the **Project Explorer** window to the block diagram of the VI. The I/O variables for the channels return calibrated floating-point data in units as specified on the **C Series Module Properties** dialog box.

Module Channels

The NI 9217 has the following channels.

Channel	Description
AI**x**	Analog input channel **x**, where **x** is the number of the channel. For the NI 9217, **x** is 0 to 3.

C Series Module Properties Dialog Box

Use this dialog box to configure the NI 9217. Right-click the NI 9217 in the **Project Explorer** window and select **Properties** to display this dialog box. You can configure the following options.

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this value.
- **Location**—Specifies a slot in the chassis for the C Series module.
- **Conversion Time**—Specifies the time it takes to acquire one point of data from all channels. You can select **200 ms** or **2.5 ms**.
- **Channels**—Specifies the channel(s) for which you want to configure settings.
- **Measurement Units**—Specifies the units you want data to be returned in for the channel. You can select **Raw Ohms**, **Degrees Kelvin**, **Degrees Celsius**, **Degrees Fahrenheit**, or **Degrees Rankine**.

- **RTD Type**—Specifies the type of RTD connected to the channel by temperature coefficient of resistance (TCR). If you select **Custom**, you must enter the **Callendar-Van Dusen Coefficients** below.
  - **Callendar-Van Dusen Coefficients**—Specifies the coefficients to use in the Callendar-Van Dusen equation, a linearization curve for measuring the temperature of an RTD.

NI 9218

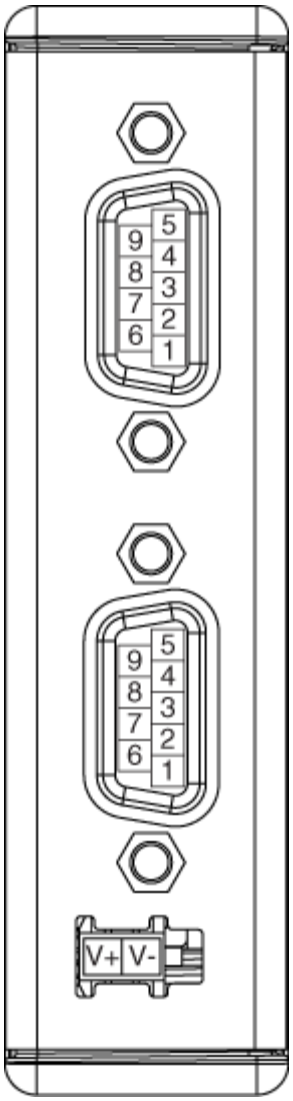
CompactRIO 2-Channel, 24-Bit Dynamic Universal Analog Input Module

Software Reference (?)

FPGA Interface | Scan Interface

NI 9218

NI 9218 Pinout



NI 9218 Pin Assignments by Mode

Pin	Mode				
	Bridge	Voltage		IEPE	TEDS
	±22 mV/V	±65 mV	±16 V	±5 V	Class 1
1	EX+	EX+*	EX+*	—	—
2	—	—	—	AI+	TEDS+

3	EX-	EX-*	AI-, EX-*	AI-	TEDS-
4	RS+	—	—	—	—
5	RS-	—	—	—	—
6	AI+	AI+	AI+	—	—
7	AI-	AI-†	—	—	—
8	SC	—	—	—	—
9	SC	—	—	—	—

*Optional sensor excitation.
†In ±65 mV mode, you must tie pin 7 (AI-) to pin 3 (EX-).

Related Topics

FPGA Interface
Converting and Calibrating CompactRIO Analog Input Values
Detecting Out-of-Range Channels
Accessing TEDS Information from a Module (FPGA Interface)
Acquiring Data from a Module (FPGA Interface)
NI 9218 Data Rates
Configuring the Data Rate for a Module (FPGA Interface)
Understanding Loop Timing for the NI 9218
Synchronizing Multiple C Series Modules

NI 9218 (FPGA Interface)

CompactRIO 2-Channel, 24-Bit Dynamic Universal Analog Input Module

Open example

Find related examples

FPGA I/O Node

You can use an FPGA I/O Node, configured for reading, with this device.

Note You can synchronize an NI 9218 module with other modules that have a selectable timebase source.

Terminals in Software

Use the FPGA I/O Node to access the following terminals for this device.

Terminal	Description
AI**x**	channel **x**, where **x** is the number of the channel. The NI 9218 has channels 0 to 1.
Onboard Clock	Gives access to the onboard clock in the LabVIEW block diagram. The Onboard Clock frequency is 13.1072 MHz. Use the FPGA I/O Node in a single-cycle Timed Loop to access this channel. You must export the Onboard Clock of the NI 9218 to access this channel.
Start	Channel that controls when the NI 9218 starts acquiring data. If TRUE is written to the **Start** channel, the NI 9218 starts acquiring data. When the NI 9218 is acquiring data, you must write TRUE to the **Stop** channel before you can access properties for the module. If FALSE is written to the **Start** channel, no operation is performed.
Stop	Channel that controls when the NI 9218 stops acquiring data. If TRUE is written to the **Stop** channel, the NI 9218 stops acquiring data. When the NI 9218 is acquiring data, you must write TRUE to the **Stop** channel before you can access properties for the module. If FALSE is written to the **Stop** channel, no operation is performed.

You can read TEDS information from the NI 9218.

Arbitration

This device supports only the Arbitrate if Multiple Requestors Only option for arbitration. You cannot configure arbitration settings for this device.

Module Methods

Use the FPGA I/O Method Node to access the following module method for this device.

Method	Description
Check Cached Status	Returns Booleans for each channel that indicate whether there was an excitation fault or open loop on the channel since the last execution of the Check Cached Status method. When the FPGA I/O Node reads the channels, the FPGA VI determines the state of the channels and caches any TRUE value until the Check Cached Status method executes. ▪ **Excitation Fault**—Returns an array of Boolean values. A value of TRUE in any index indicates that the channel sharing a number with that index detected an excitation fault on the channel at some point after the last time that the Check Cached Status method executed. ▪ **Open Loop**—Returns an array of Boolean values. A value of TRUE in any index indicates that the channel sharing a number with that index detected an open loop on the channel at some point after the last time that the Check Cached Status method executed.

I/O Properties

Use the FPGA I/O Property Node to access the following I/O properties for this device.

Property	Description
Input Configuration	Sets the input configuration of the corresponding channel to one of ten modes: ±60 V; ±16 V; ±16 V, 12 V Ex.; ±65 mV; ±65 mV, 12 V Ex.; ±20 mA; ±20 mA, 12 V Ex.; ±22 mV/V Bridge, 2 V Ex.; ±22 mV/V Bridge, 3.3 V Ex.; ±5 V IEPE AC Coupled.
LSB Weight (±16 V range)	Returns the LSB weight in pV/LSB for the ±16 V range.
LSB Weight (±20 mA range)	Returns the LSB weight in fV/LSB for the ±20 mA range.

LSB Weight (±22 mV/V range)	Returns the LSB weight in fV/LSB for the ±22 mV/V range.
LSB Weight (±5 V IEPE range)	Returns the LSB weight in pV/LSB for the ±5 V IEPE range.
LSB Weight (±65 mV range)	Returns the LSB weight in fV/LSB for the ±65 mV range.
LSB Weight (±60 V range)	Returns the LSB weight in pV/LSB for the ±60 V range.
Offset (±16 V range)	Returns the calibration offset in nV for the ±16 V range.
Offset (±20 mA range)	Returns the calibration offset in nV for the ±20 mA range.
Offset (±22 mV/V range)	Returns the calibration offset in nV for the ±22 mV/V range.
Offset (±5 V IEPE range)	Returns the calibration offset in nV for the ±5 V IEPE range.
Offset (±65 mV range)	Returns the calibration offset in nV for the ±65 mV range.
Offset (±60 V range)	Returns the calibration offset in nV for the ±60 V range.
Offset Cal Enable	Enables offset calibration. This disconnects both signal input pins and internally connects a short to the ADC driver circuitry.
Shunt Cal Enable	Controls the shunt calibration switch for each channel.

Module Properties

Use the FPGA I/O Property Node to access the following module properties for this device.

Property	Description
Data Rate	Sets the rate at which the NI 9218 acquires data.
Module ID	Returns the module ID, 0x7757.
Serial Number	Returns the unique serial number of the module.
Vendor ID	Returns the NI vendor ID, 0x1093.

Excitation Protection

The NI 9218 excitation circuit is protected from overcurrent and overvoltage fault conditions. A fault condition also occurs if the voltage supplied to the external power connector on the NI 9218 is below the minimum required voltage, if the excitation pins on the NI 9218 are shorted together, or if the connected load exceeds the powered sensor output current limit. The circuit is automatically disabled in the event of a fault condition. Whenever possible, a channel automatically recovers after the fault is removed.

You must wire error terminals on the FPGA I/O Property Nodes to receive notification of overcurrent and overvoltage faults. LabVIEW returns error 65654 if there is an overcurrent or overvoltage fault on at least one channel. If a warning occurs, only the channel(s) with the fault are affected and all other channels on the module continue to function properly without interruption. If an error occurs, the module is unable to recover from the fault condition and you must restart the module after the fault is removed.

Single-Cycle Timed Loop

This device does not support the single-cycle Timed Loop.

C Series Module Properties Dialog Box for the NI 9218 (FPGA Interface)

Right-click an NI 9218 C Series module in the **Project Explorer** window and select **Properties** from the shortcut menu to display this dialog box.

Use this dialog box to configure a C Series module.

This dialog box includes the following components:

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Type**—Specifies the type of C Series module. You cannot change this option.
- **Location**—Specifies a slot in the chassis for the C Series module.

- **Calibration Mode**—Sets the calibration mode for the C Series module. Select **Calibrated** if you want the FPGA I/O Node to return calibrated, fixed-point data from the module. Refer to the table below for information about the units and encoding of the fixed-point data depending on the channel mode. Select **Raw** if you want the FPGA I/O Node to return calibrated, binary data from the module. If you select **Raw**, you must convert the analog input values in the host VI. The default is **Calibrated**.

Channel Mode	Units of Fixed-Point Data	Integer Type	Word Length	Integer Word Length	Typical Measurement Range
±16 V	Volts	Signed	35 bits	7 bits	±16.3 V
±20 mA	Amps	Signed	35 bits	7 bits	24.4 mA
±22 mV/V Bridge	Volts/volt	Signed	35 bits	7 bits	22.1 mV/V
±5 V IEPE	Volts	Signed	35 bits	7 bits	5.33 V
±60 V	Volts	Signed	35 bits	7 bits	±62.1 V
±65 mV	Volts	Signed	35 bits	7 bits	73.5 mV

- **Data Rate**—Specifies the rate at which the module acquires data.
- **Enable TEDS Support**—Place a checkmark in this checkbox if you want to enable TEDS support in the FPGA and host VIs for this module.
- **Channels**—Specifies the channel(s) for which you want to select the mode and range.
- **Master Timebase Source**—Specifies the master timebase source that the module uses.
- **Export Onboard Clock**—Place a checkmark in this checkbox if you want to make this module accessible as a master timebase source to other modules.
- **Selected Channel(s) Settings**—Specifies the mode and range for each channel.
  - **Input Configuration**—Sets the mode for the selected channel(s).

Note The following channel modes require a connection accessory.

Channel Mode		Connection Accessory
±20 mA		NI 9983D
±22 mV/V Bridge	120 Ω Quarter-Bridge Completion	NI 9984D
	350 Ω Quarter-Bridge Completion	NI 9985D
	Half-Bridge Completion	NI 9986D
±60 V		NI 9987D

NI 9218 Data Rates

The frequency of a master timebase ($\mathbf{f_M}$) controls the data rate ($\mathbf{f_S}$) of the NI 9218. The NI 9218 includes an internal master timebase with a frequency of 13.1072 MHz, but the module can also accept an external master timebase or export its own master timebase.

Internal Master Timebase

The following equation provides the available data rates for the NI 9218 with the internal master timebase.

$$f_s = \frac{f_M \div 256}{n}$$

where n is any integer from 1 to 31.

Refer to the following table for the available data rates with the internal master timebase.

NI 9218 Data Rates (kS/s)			
51.200	5.689	3.012	2.048
25.600	5.120	2.845	1.969
17.067	4.654	2.695	1.896
12.800	4.267	2.560	1.829
10.240	3.938	2.438	1.765

8.533	3.657	2.328	1.707
7.314	3.413	2.226	1.652
6.400	3.200	2.133	—

External Master Timebase

The NI 9218 has a different set of data rates when using an external master timebase with a frequency other than 13.1072 MHz. To synchronize the data rate of an NI 9218 with other modules that use master timebases to control sampling, all of the modules must share a single master timebase source.

Related Topics

FPGA Interface

Synchronizing Multiple C Series Modules Configuring the Data Rate for a Module (FPGA Interface)

Loop Timing for the NI 9218 (FPGA Interface)

The NI 9218 uses an internal master timebase. When creating a loop with an I/O Node that acquires data from the NI 9218, do not use the Loop Timer or Wait functions. If the loop execution time is slower than the data rate of the NI 9218, the FPGA I/O Node returns an overrun warning and continues to read from the module.

The overrun warning means that the data the FPGA I/O Node returns is valid, but the function missed one or more data points since the last time it read data from the NI 9218. The function returns the overrun warning when all of the following conditions are true:

- The NI 9218 is in acquisition mode.
- An FPGA I/O Node that is acquiring data from the module executes at least once after you put the module in acquisition mode.
- The FPGA I/O Node did not read one or more data points since the previous time the function executed.

Avoiding Overrun Warnings with the NI 9218

Follow these guidelines when developing an FPGA VI to avoid overrun warnings.

- Ensure that the loop does not execute slower than the data rate of the NI 9218.
- When reading from the NI 9218 and an additional internally timed module in the same loop, use one FPGA I/O Node to read all module channels. You also must synchronize the NI 9218 and the additional internally timed module.
- You can read from an NI 9218 and a non-internally timed analog input module in the same loop if the other module can acquire data as fast or faster than the data rate of the NI 9218. If you use the same FPGA I/O Node to read data from the modules, the FPGA I/O Node does not return data for the other module until the NI 9218 acquires data.
- Use different loops for the NI 9218 and another analog input module that acquires data slower than the NI 9218.

Note If your application acquires multiple buffers of data from an internally timed module and the timing relationship between them is not important, you can ignore the overrun warning returned with the first point of each buffer.

Related Topics

FPGA Interface
Synchronizing Multiple C Series Modules
Configuring the Data Rate for a Module (FPGA Interface)

NI 9218 (Scan Interface)

CompactRIO 2-Channel, 24-Bit Dynamic Universal Analog Input Module

Open example

Module I/O Variables

To use I/O from this module in a VI, drag and drop I/O variables from the **Project Explorer** window to the block diagram of the VI. The I/O variables for the channels return calibrated floating-point data in units as specified on the **C Series Module Properties** dialog box.

Module Channels

The NI 9218 has the following channels.

Channel	Description
AI**x**	Analog input channel **x**, where **x** is the number of the channel. For the NI 9218, **x** is 0 to 1.

C Series Module Properties Dialog Box

Use this dialog box to configure the NI 9218. Right-click the NI 9218 in the **Project Explorer** window and select **Properties** to display this dialog box. You can configure the following options.

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this value.
- **Location**—Specifies a slot in the chassis for the C Series module.
- **Channels**—Specifies the channel(s) for which you want to configure settings.
- **Input Configuration**—Sets the input configuration of the corresponding channel to one of ten modes: ±60 V; ±16 V; ±16 V, 12 V Ex.; ±65 mV; ±65 mV, 12 V Ex.; ±20 mA; ±20 mA, 12 V Ex.; ±22 mV/V Bridge, 2 V Ex.; ±22 mV/V Bridge, 3.3 V Ex.; ±5 V IEPE AC Coupled.

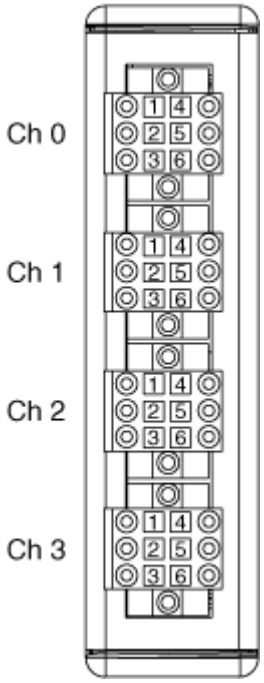
NI 9219

CompactRIO 4-Channel, 24-Bit Universal Analog Input Module

Software Reference (?)

FPGA Interface | Scan Interface

NI 9219 Pinout

Module	Terminal	Signal Name	Signal Description
	1	T+	TEDS Data
	2	T-	TEDS COM
	3	EX+/HI[1]	Positive excitation or input signal
	4	HI	Positive input signal
	5	EX-/LO[1]	Negative excitation or input signal
	6	LO	Negative input signal

[1] Depending on the mode, terminals 3 and 5 are either the excitation or input signals.

NI 9219 Pin Assignments by Mode

Mode	Terminal					
	1	2	3	4	5	6
Voltage	T+	T-	—	HI	LO	—
Current	T+	T-	HI	—	LO	—
4-Wire Resistance	T+	T-	EX+	HI	EX-	LO
2-Wire Resistance	T+	T-	HI	—	LO	—
Thermocouple	T+	T-	—	HI	LO	—
4-Wire RTD	T+	T-	EX+	HI	EX-	LO
3-Wire RTD	T+	T-	EX+	—	EX-	LO
Quarter-Bridge	T+	T-	HI	—	LO	—

Half-Bridge	T+	T-	EX+	HI	EX-	—
Full-Bridge	T+	T-	EX+	HI	EX-	LO
Digital In	T+	T-	—	HI	LO	—
Contact	T+	T-	HI	—	LO	—

Related Topics

FPGA Interface
Detecting Out-of-Range Channels
Accessing TEDS Information from a Module (FPGA Interface)
Converting NI 9219 Data
Configuring Modes and Ranges for the NI 9219
Configuring the Digital In Threshold for the NI 9219

NI 9219 (FPGA Interface)

CompactRIO 4-Channel, 24-Bit Universal Analog Input Module

Open example Find related examples

FPGA I/O Node

You can use an FPGA I/O Node, configured for reading, with this device.

Terminals in Software

Use the FPGA I/O Node to access the following terminals for this device.

Terminal	Description
CH**x**	channel **x**, where **x** is the number of the channel. The NI 9219 has channels 0 to 3.
CJC**x**	Cold-junction compensation channel **x**, where **x** is the number of the channel. The NI 9219 has CJC channels 0 to 3. If a channel is in Thermocouple mode, you can read CJC data for the channel. You must convert the CJC data to temperature.

You can read TEDS information from the NI 9219.

Arbitration

This device supports only the Arbitrate if Multiple Requestors Only option for arbitration. You cannot configure arbitration settings for this device.

Methods

This device does not support any methods.

I/O Properties

Use the FPGA I/O Property Node to access the following I/O properties for this device.

Property	Description
Voltage Range	Sets the range of a channel in Voltage mode.
Resistance Range	Sets the range of a channel in Resistance mode.
RTD Range	Sets the range of a channel in RTD mode.
Quarter Bridge Range	Sets the range of a channel in Quarter Bridge mode.
Full Bridge Range	Sets the range of a channel in Full Bridge mode.
Digital Threshold	Sets the threshold of a channel in Digital In mode.

Module Properties

Use the FPGA I/O Property Node to access the following module properties for this device.

Property	Description
Conversion Time	Sets the time it takes to acquire one point of data from all channels. You can select **High Speed**, **Best 60 Hz Rejection**, **Best 50 Hz Rejection**, or **High Resolution**. Refer to the NI 9219 hardware documentation on ni.com/manuals for more information about these conversion times. This property overwrites the value you configure in the C Series Module Properties dialog box.

Module ID	Returns the module ID, 0x730C.
Serial Number	Returns the unique serial number of the module .
Vendor ID	Returns the NI vendor ID, 0x1093.

Excitation Protection

The NI 9219 excitation circuit is protected from overcurrent and overvoltage fault conditions. The circuit is automatically disabled in the event of a fault condition. Whenever possible, a channel automatically recovers after the fault is removed. You must wire error terminals on the FPGA I/O Property Nodes to receive notification of overcurrent and overvoltage faults. LabVIEW returns error 65544 or 65548 if there is an overcurrent or overvoltage fault on at least one channel. If a warning occurs, only the channel(s) with the fault are affected and all other channels on the module continue to function properly without interruption. If an error occurs, the module is unable to recover from the fault condition and you must restart the module after the fault is removed.

Single-Cycle Timed Loop

This device does not support the single-cycle Timed Loop.

C Series Module Properties Dialog Box for the NI 9219 (FPGA Interface)

Right-click an NI 9219 C Series module in the **Project Explorer** window and select **Properties** from the shortcut menu to display this dialog box.

Use this dialog box to configure a C Series module.

This dialog box includes the following components:

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this option.
- **Location**—Specifies a slot in the chassis for the C Series module.

- **Calibration Mode**—Sets the calibration mode for the C Series module. Select **Calibrated** if you want the FPGA I/O Node to return calibrated, fixed-point data from the module. Refer to the table below for information about the units and encoding of the fixed-point data depending on the channel mode. If you select **Calibrated** and an NI 9219 channel is in Thermocouple mode, you must convert the CJC data in the host VI. Select **Raw** if you want the FPGA I/O Node to return calibrated, binary data from the module. If you select **Raw**, you must convert the analog input values in the host VI. The default is **Calibrated**.

Channel Mode	Units of Fixed-Point Data	Integer Type	Word Length	Integer Word Length
Voltage	Volts	Signed	32 bits	7 bits
Current	Amps	Signed	32 bits	–1 bits
Resistance and RTD	Ohms	Unsigned	32 bits	14 bits
Thermocouple	Volts	Signed	32 bits	–1 bits
Quarter Bridge	Volts/volt	Unsigned	32 bits	14 bits
Half Bridge	Volts/volt	Signed	32 bits	7 bits
Full Bridge	Volts/volt	Signed	32 bits	–1 bits

- **Channels**—Specifies the channel(s) for which you want to select the mode and range.
- **Selected Channel(s) Settings**—Specifies the mode and range for each channel.
  - **Channel Mode**—Sets the mode for the selected channel(s).
  - **Range**—Sets the range for the selected channel(s).
  - **Threshold**—Sets the Digital In threshold for the selected channel(s). This option is available only if you select **Digital In** for the channel mode.
- **Conversion Time**—Specifies the time it takes to acquire one point of data from all channels. You can select **High Speed**, **Best 60 Hz Rejection**, **Best 50 Hz Rejection**, or **High Resolution**. Refer to the NI 9207 hardware

documentation on ni.com/manuals for more information about these conversion times.

- **Enable TEDS Support**—Place a checkmark in this checkbox if you want to enable TEDS support in the FPGA and host VIs for this module.

Converting NI 9219 Data (FPGA Interface)

Set the **Calibration Mode** to **Calibrated** in the C Series Module Properties dialog box for the NI 9219 if you want the FPGA I/O Node to return calibrated, fixed-point data from the module. If you set the **Calibration Mode** to **Calibrated** and an NI 9219 channel is in Thermocouple mode, you must convert the fixed-point CJC data to binary CJC data and then convert the binary CJC data to temperature. Set the **Calibration Mode** to **Raw** if you want the FPGA I/O Node to return binary values from the module that are calibrated based on the range of the selected mode. If you set the **Calibration Mode** to **Raw**, you must convert the binary values to meaningful engineering units. If you set the **Calibration Mode** to **Raw** and an NI 9219 channel is in Thermocouple mode, you also must convert the binary CJC data to temperature. You must convert these values in the host VI.

Note The equations below apply only to the NI 9219. If you are using the NI 9219E board-only module, refer to the KnowledgeBase for the correct equations.

Using a VI to Convert and Adjust Binary Values

Refer to the NI 9219 Binary to Nominal VI in the `labview\examples\CompactRIO\Module Specific\NI 9219\NI 9219 Scaling Utility` directory for an example of converting and adjusting binary input values. You can use the polymorphic NI 9219 Binary to Nominal VI as a subVI in the host VI to convert and adjust binary input values.

Using an Equation to Convert Binary Values

You can use the following equation in the host VI to convert the binary input values to engineering units for each channel:

Engineering Units* = **Binary Value** × (**Range High** – **Range Low**) ÷ 2^{24}

where

Binary Value is the value returned by the FPGA I/O Node

Range High is the upper value of the input range †

Range Low is the lower value of the input range.

*Engineering units are equivalent to the units of the mode input range listed in the NI 9219 hardware documentation on ni.com/manuals.

†Refer to the NI 9219 hardware documentation on ni.com/manuals for the input ranges for each mode. For modes that have only one input range value, use 0 as the lower value of the input range.

Digital In

Digital In mode returns a Boolean value, where FALSE is equivalent to any voltage below the specified threshold and TRUE is equivalent to any voltage above the specified threshold.

Open Contact

Open Contact mode returns a Boolean value, where FALSE indicates a closed circuit and TRUE indicates a open circuit.

Using an Equation to Convert Fixed-Point CJC Data

You can use the following equation in the host VI to convert fixed-point CJC data to binary CJC data:

Binary CJC Data = (**Fixed-Point CJC Data**) ÷ (0.250 ÷ (2^{24} – 1))

Using Equations to Convert Binary CJC Data

You can use the following equations in the host VI to convert binary CJC data to temperature:

Calculate the resistance of the thermistor:

$\mathbf{R_T}$ = 10000 ÷ [(2^{16} ÷ **Binary CJC Data**) – 1]

Calculate the CJC temperature:

$$\mathbf{T} = [\,1 \div [\mathbf{A} + \mathbf{B}(\ln(\mathbf{R_T})) + \mathbf{C}(\ln(\mathbf{R_T}))^3]] - (273.15 + \mathbf{OffsetConstant})$$

where

T = temperature in °C

A = 1.2873851×10^{-3}

B = 2.3575235×10^{-4}

C = 9.4978060×10^{-8}

$\mathbf{R_T}$ = thermistor resistance reading

OffsetConstant* = 1.5

*The **OffsetConstant** is the typical temperature gradient between the CJC sensor and the thermocouple cold junction.

Refer to the National Institute of Standards and Technology (NIST) Monograph 175 thermocouple reference tables for more information about converting and adjusting thermocouple values.

Configuring Modes and Ranges for the NI 9219 (FPGA Interface)

You can configure the mode and range for each channel on the NI 9219 at edit time using the C Series Module Properties dialog box. You can programmatically change the range for each channel at run time using the FPGA I/O Property Node. The execution of an I/O Property Node that is configured with a **Range** property overwrites the value you configured in the **C Series Module Properties** dialog box.

Configuring Modes and Ranges Using the C Series Module Properties Dialog Box

Complete the following steps to configure the channel(s) mode and range using the **C Series Module Properties** dialog box.

1. Configure the CompactRIO system, and add an NI 9219.
2. Right-click the NI 9219 in the **Project Explorer** window and select **Properties** from the shortcut menu to display the **C Series Module Properties** dialog box.

3. Select the channel(s) for which you want to configure the mode and range from the **Channels** table. You can select more than one channel by holding the <Ctrl> or <Shift> key when selecting channels.
4. Select the mode for the channel(s) from the **Channel Mode** pull-down menu. If you select **Digital In** mode, skip the following steps and set the threshold. If you select **Open Contact** mode, skip the following step.
5. Select the range from the **Range** pull-down menu for the selected channel(s).
6. Click the **OK** button.
7. Select **File»Save All** in the **Project Explorer** window.

Configuring Ranges Using the FPGA I/O Property Node

Complete the following steps to configure the channel range using the FPGA I/O Property Node.

1. Create FPGA I/O items for the channel of the NI 9219 for which you want to configure a **Range** property. The channel must be set to Voltage mode, Resistance mode, RTD mode, Quarter Bridge mode, or Full Bridge mode.
2. Place an FPGA I/O Property Node on the block diagram and configure it for the NI 9219 channel for which you want to configure the range.
3. Click the **Property** section and select the **Range** property from the shortcut menu.
4. Right-click the **Range** input and select **Create»Control** from the shortcut menu.
5. On the front panel of the VI, select a rate from the **Range** pull-down menu.

You can change the channel range at run time by writing to the control from the host VI. Refer to the NI 9219 Getting Started VI in the `labview\examples\CompactRIO\Module Specific\NI 9219\NI 9219 Getting Started\NI 9219 Getting Started.lvproj` for an example of changing a channel range using the FPGA I/O Property Node.

Configuring the Digital In Threshold for the NI 9219 (FPGA Interface)

Channels in Digital In mode on the NI 9219 have a 0–60 V unipolar threshold. The default value of the Digital In mode threshold is 1.5 V. You can configure the threshold at edit time using the C Series Module Properties dialog box. You can programmatically change the threshold at run time using the FPGA I/O Property Node. The execution of an I/O Property Node that is configured with a **Digital Threshold** property overwrites the value you configured in the **C Series Module Properties** dialog box.

Configuring the Digital In Threshold Using the C Series Module Properties Dialog Box

Complete the following steps to configure the Digital In threshold for the NI 9219 using the **C Series Module Properties** dialog box.

1. Configure the CompactRIO system, and add an NI 9219.
2. Right-click the NI 9219 in the **Project Explorer** window and select **Properties** from the shortcut menu to display the **C Series Module Properties** dialog box.
3. Select the channel(s) for which you want to configure the Digital In threshold from the **Channels** table. You can select more than one channel by holding the <Ctrl> or <Shift> key when selecting channels.
4. Select **Digital In** from the **Channel Mode** pull-down menu.
5. Enter a value between 0 and 60 in the **Threshold** text box for the selected channel(s).
6. Click the **OK** button.
7. Select **File»Save All** in the **Project Explorer** window.

Configuring the Digital In Threshold Using the FPGA I/O Property Node

Complete the following steps to configure the Digital In threshold using the FPGA I/O Property Node.

1. Create FPGA I/O items for the channel of the NI 9219 for which you want to configure the **Digital Threshold** property. The channel must be set to Digital In mode.
2. Place an FPGA I/O Property Node on the block diagram and configure it for the NI 9219 channel for which you want to configure the Digital In threshold.
3. Click the **Property** section and select **Digital Threshold** from the shortcut menu.
4. Right-click the **Digital Threshold** input and select **Create»Control** from the shortcut menu.
5. On the front panel of the VI, enter a binary value in the **Digital Threshold** control. You can use the following equation in the host VI to calculate the threshold value:

   Threshold (binary) = **Threshold (volts)** x 2^{24} ÷ 60

You can change the Digital In threshold at run time by writing to the control from the host VI. Refer to the NI 9219 Digital Threshold VI in the `labview\examples\CompactRIO\Module Specific\NI 9219\NI 9219 Digital Threshold\NI 9219 Digital Threshold.lvproj` for an example of configuring the NI 9219 Digital In threshold using the FPGA I/O Property Node.

NI 9219 (Scan Interface)

CompactRIO 4-Channel, 24-Bit Universal Analog Input Module

Open example

Module I/O Variables

To use I/O from this module in a VI, drag and drop I/O variables from the **Project Explorer** window to the block diagram of the VI. The I/O variables for the channels return calibrated floating-point data or Boolean data in units determined by the measurement mode you select on the **C Series Module Properties** dialog box. The following table shows the units for the different modes.

Mode	Data Units
Voltage	Volts

Current	Amps
Resistance	Ohms
Thermocouple	Volts or Temperature Units
RTD	Ohms or Temperature Units
Bridge	Volts/Volt
Digital In	Boolean
Open Contact	Boolean

Note The Scan Interface applies Autozero and cold-junction compensation to NI 9219 data on channels configured for thermocouple mode.

Module Channels

The NI 9219 has the following channels.

Channel	Description
CH**x**	Analog input channel **x**, where **x** is the number of the channel. For the NI 9219, **x** is 0 to 3.

C Series Module Properties Dialog Box

Use this dialog box to configure the NI 9219. Right-click the NI 9219 in the **Project Explorer** window and select **Properties** to display this dialog box. You can configure the following options.

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this value.
- **Location**—Specifies a slot in the chassis for the C Series module.
- **Channels**—Specifies the channel(s) for which you want to configure settings.
- **Mode**—Specifies the measurement mode for the selected channel(s).

- **Range**—Specifies the range for the selected channel(s).
- **Thermocouple Type**—Specifies the type of thermocouple connected to a channel in thermocouple mode.
- **Measurement Units**—Specifies the units for data to be returned from the selected channel(s) configured for thermocouple or RTD mode.
- **RTD Type**—Specifies the type of RTD connected to the channel by temperature coefficient of resistance (TCR). If you select **Custom**, you must enter the **Callendar-Van Dusen Coefficients** below.
  - **Callendar-Van Dusen Coefficients**—Specifies the coefficients to use in the Callendar-Van Dusen equation, a linearization curve for measuring the temperature of an RTD.
- **Threshold**—Specifies the minimum high level in volts for the selected channel(s) configured for Digital In mode. The range of valid threshold values is 0–60.
- **Conversion Time**—Determines the time it takes to read all channels of the module. You can select **High Speed**, **Best 60 Hz Rejection**, **Best 50 Hz Rejection**, or **High Resolution**. Refer to the NI 9219 hardware documentation on ni.com/manuals for more information about these conversion times.

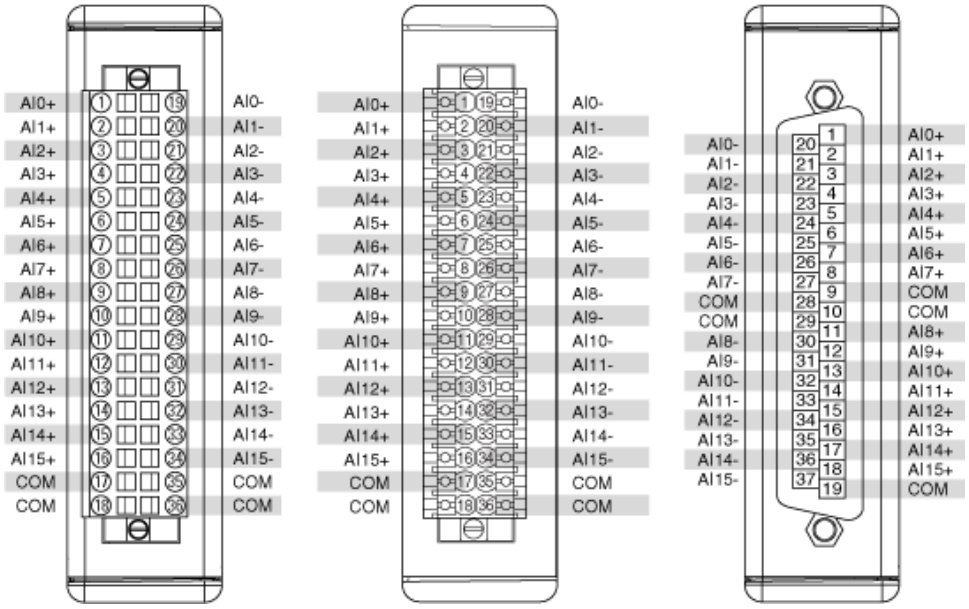
NI 9220

CompactRIO 16-Channel, ±10 V, 16-Bit Simultaneous Analog Input Module

Software Reference (?)

FPGA Interface

NI 9220 Pinout



Related Topics

FPGA Interface
Converting and Calibrating CompactRIO Analog Input Values
Detecting Out-of-Range Channels

NI 9220 (FPGA Interface)

CompactRIO 16-Channel, ±10 V, 16-Bit Simultaneous Analog Input Module

Open example

Find related examples

FPGA I/O Node

You can use an FPGA I/O Node, configured for reading, with this device.

Note You can simultaneously read from multiple channels on the NI 9220.

User-Controlled I/O Sampling

You can use the following User-Controlled I/O Sampling functions to perform I/O with more specific control over the I/O hardware on the FPGA.

Function	Type
Generate I/O Sample Pulse Method	Module function
Get I/O Read Status Method	I/O function
Read I/O Method	I/O function
Reset I/O Method	Module function

Note You must call the Reset I/O Method function first to prepare the NI 9220 to use the other User-Controlled I/O Sampling functions.

Terminals in Software

Use the FPGA I/O Node or User-Controlled I/O Sampling functions to access the following terminals for this device.

Terminal	Description
AI**x**	Analog input channel **x**, where **x** is the number of the channel. The NI 9220 has AI channels 0 to 15.

Arbitration

This device supports only the Arbitrate if Multiple Requestors Only option for arbitration. You cannot configure arbitration settings for this device.

Methods

This device does not support any methods.

I/O Properties

Use the FPGA I/O Property Node to access the following I/O properties for this device.

Property	Description
LSB Weight	Returns the LSB weight in nV/LSB for the channel. Use this value to convert and calibrate NI 9220

	data if you set the **Calibration Mode** to **Raw** in the C Series Module Properties dialog box.
Offset	Returns the calibration offset in nV for the channel. Use this value to convert and calibrate NI 9220 data if you set the **Calibration Mode** to **Raw** in the **C Series Module Properties** dialog box.

Module Properties

Use the FPGA I/O Property Node to access the following module properties for this device.

Property	Description
Module ID	Returns the module ID.
Serial Number	Returns the unique serial number of the module.
Vendor ID	Returns the NI vendor ID, 0x1093.

Single-Cycle Timed Loop

This device does not support the single-cycle Timed Loop.

C Series Module Properties Dialog Box for the NI 9220 (FPGA Interface)

Right-click an NI 9220 C Series module in the **Project Explorer** window and select **Properties** from the shortcut menu to display this dialog box.

Use this dialog box to configure a C Series module.

This dialog box includes the following components:

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this option.

- **Location**—Specifies a slot in the chassis for the C Series module.
- **Calibration Mode**—Sets the calibration mode for the C Series module. Select **Calibrated** if you want the FPGA I/O Node to return calibrated, fixed-point data for the module in units of volts. The fixed-point data is signed, with a word length of 20 bits and an integer word length of 5 bits. Select **Raw** if you want the FPGA I/O Node to return uncalibrated, binary data for the module. If you select **Raw**, you must convert and calibrate the analog input values in the host VI. The default is **Calibrated**.

NI 9220 (Scan Interface)

CompactRIO 16-Channel, ±10 V, 16-Bit Simultaneous Analog Input Module


Open example

Module I/O Variables

To use I/O from this module in a VI, drag and drop I/O variables from the **Project Explorer** window to the block diagram of the VI. The I/O variables for the channels return calibrated floating-point data in volts.

Module Channels

The NI 9220 has the following channels.

Channel	Description
AI**x**	Analog input channel **x**, where **x** is the number of the channel. The NI 9220 has AI channels 0 to 15.

C Series Module Properties Dialog Box

Use this dialog box to configure the NI 9220. Right-click the NI 9220 in the **Project Explorer** window and select **Properties** to display this dialog box. You can configure the following options.

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module

based on the slot number. You can use this field to give the module a descriptive name.

- **Module Type**—Specifies the type of C Series module. You cannot change this value.
- **Location**—Specifies a slot in the chassis for the C Series module.

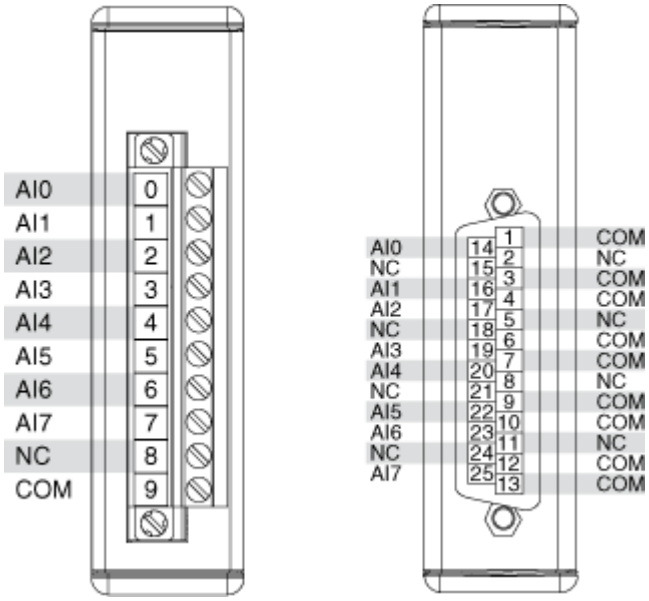
NI 9221

CompactRIO 8-Channel, ±60 V, 12-Bit Analog Input Module

Software Reference (?)

FPGA Interface | Scan Interface

NI 9221 Pinout



Related Topics

FPGA Interface
Converting and Calibrating CompactRIO Analog Input Values
Detecting Out-of-Range Channels
Configuring the Minimum Time Between Conversions for the NI 9201/9221
Understanding NI 9201/9221 Scanning

NI 9221 (FPGA Interface)

CompactRIO 8-Channel, ±60 V, 12-Bit Analog Input Module

FPGA I/O Node

You can use an FPGA I/O Node, configured for reading, with this device.

Terminals in Software

Use the FPGA I/O Node to access the following terminals for this device.

Terminal	Description
AI**x**	Analog input channel **x**, where **x** is the number of the channel. The NI 9221 has AI channels 0 to 7.

You can configure the minimum time between conversions and understand scanning for these channels.

Arbitration

This device supports only the Arbitrate if Multiple Requestors Only option for arbitration. You cannot configure arbitration settings for this device.

Methods

This device does not support any methods.

I/O Properties

Use the FPGA I/O Property Node to access the following I/O properties for this device.

Property	Description
LSB Weight	Returns the LSB weight in nV/LSB for the channel. Use this value to convert and calibrate NI 9221 data if you set the **Calibration Mode** to **Raw** in the C Series Module Properties dialog box.

Offset	Returns the calibration offset in nV for the channel. Use this value to convert and calibrate NI 9221 data if you set the **Calibration Mode** to **Raw** in the **C Series Module Properties** dialog box.

Module Properties

Use the FPGA I/O Property Node to access the following module properties for this device.

Property	Description
Module ID	Returns the module ID, 0x70A5.
Serial Number	Returns the unique serial number of the module.
Vendor ID	Returns the NI vendor ID, 0x1093.

Single-Cycle Timed Loop

This device does not support the single-cycle Timed Loop.

C Series Module Properties Dialog Box for the NI 9201/9221 (FPGA Interface)

Right-click an NI 9201 or NI 9221 C Series module in the **Project Explorer** window and select **Properties** from the shortcut menu to display this dialog box.

Use this dialog box to configure a C Series module.

This dialog box includes the following components:

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this option.
- **Location**—Specifies a slot in the chassis for the C Series module.

- **Calibration Mode**—Sets the calibration mode for the C Series module. Select **Calibrated** if you want the FPGA I/O Node to return calibrated, fixed-point data from the module in units of volts. The fixed-point data is signed, with a word length of 16 bits and an integer word length of 5 bits for the NI 9201 and 7 bits for the NI 9221. Select **Raw** if you want the FPGA I/O Node to return uncalibrated, binary data from the module. If you select **Raw**, you must convert and calibrate the analog input values in the host VI. The default is **Calibrated**.
- **Minimum Time Between Conversions**—Specifies the minimum time between conversions in µs.

Configuring the Minimum Time Between Conversions for the NI 9201/9221 (FPGA Interface)

You can configure the minimum time between conversions for the NI 9201/9221 in the C Series Module Properties dialog box.

Complete the following steps to configure the minimum time between conversions for the NI 9201/9221.

1. Configure the CompactRIO system, and add an NI 9201/9221.
2. Right-click the NI 9201/9221 in the **Project Explorer** window and select **Properties** from the shortcut menu to display the **C Series Module Properties** dialog box.
3. Enter a value between 0 and 10 µs in increments of 25 ns in the **Minimum Time Between Conversions** text box.
4. Click the **OK** button.
5. Select **File»Save All** in the **Project Explorer** window.

Note The default minimum time between conversions for the NI 9201 is 2 µs, and the default minimum time between conversions for the NI 9221 is 1.25 µs. The accuracy specifications in the NI 9201 and NI 9221 hardware documentation on ni.com/manuals are based on these default values. Refer to the

following tables for examples of how the value you enter in the **Minimum Time Between Conversions** text box affects the actual time between conversions and the accuracy of the module.

Refer to the following table if you are using a chassis other than the NI 9151 R Series Expansion chassis.

Module	Sampling Data from a Single or Multiple Channels?	Minimum Time Between Conversions*	Able to Achieve Specified Time Between Conversions?**	Module Accuracy
NI 9201	Single	≥ 1.25 µs	Yes	Module accuracy not affected
		< 1.25 µs	No	Module accuracy not affected
	Multiple	≥ 2 µs	Yes	Module accuracy not affected
		< 2 µs	No	Module accuracy degrades
NI 9221	Single	≥ 1.25 µs	Yes	Module accuracy not affected
		< 1.25 µs	No	Module accuracy not affected
	Multiple	≥ 1.25 µs	Yes	Module accuracy not affected
		< 1.25 µs	No	Module accuracy degrades

Refer to the following table if you are using the NI 9151 R Series Expansion chassis.

Module	Sampling Data from a Single or Multiple Channels?	Minimum Time Between Conversions*	Able to Achieve Specified Time Between Conversions?**	Module Accuracy
NI 9201	Single	≥ 2.1 µs	Yes	Module accuracy not affected

		< 2.1 µs	No	Module accuracy not affected
	Multiple	≥ 2.1 µs	Yes	Module accuracy not affected
		< 2.1 µs and ≥ 2 µs	No	Module accuracy not affected
		< 2 µs	No	Module accuracy degrades
NI 9221	Single	≥ 2.1 µs	Yes	Module accuracy not affected
		< 2.1 µs	No	Module accuracy not affected
	Multiple	≥ 2.1 µs	Yes	Module accuracy not affected
		< 2.1 µs and ≥ 1.25 µs	No	Module accuracy not affected
		< 1.25 µs	No	Module accuracy degrades

* The value you set in the **C Series Module Properties** dialog box.

** The actual time between conversions depends on how you develop the FPGA VI. Yes indicates that it is possible to write an FPGA VI that can sustain the minimum time between conversions specified in the **C Series Module Properties** dialog box. No indicates that the minimum time between conversions specified in the **C Series Module Properties** dialog box is too low and you may not be able to write an FPGA VI that can sustain the specified time.

Understanding NI 9201/9221 Scanning (FPGA Interface)

To scan the channels of the NI 9201/9221, configure an FPGA I/O Node with the channels you want to acquire from the module. The module implements a pipeline that is automatically managed by the FPGA I/O Node. Channels within the FPGA I/O Node are sampled in numerical order regardless of the order they appear in the node.

The first time an FPGA I/O Node configured with channels on an NI 9201/9221 module executes, the module performs two setup conversions before converting

the first channel. The two setup conversions prime the pipeline for subsequent FPGA I/O Node reads. The module does not repeat the setup conversions unless the FPGA I/O Node channel configuration changes and the pipeline needs to be primed again.

NI 9221 (Scan Interface)

CompactRIO 8-Channel, ±60 V, 12-Bit Analog Input Module

Open example

Module I/O Variables

To use I/O from this module in a VI, drag and drop I/O variables from the **Project Explorer** window to the block diagram of the VI. The I/O variables for the channels return calibrated floating-point data in volts.

Module Channels

The NI 9221 has the following channels.

Channel	Description
AI**x**	Analog input channel **x**, where **x** is the number of the channel. For the NI 9221, **x** is 0 to 7.

C Series Module Properties Dialog Box

Use this dialog box to configure the NI 9221. Right-click the NI 9221 in the **Project Explorer** window and select **Properties** to display this dialog box. You can configure the following options.

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this value.

- **Location**—Specifies a slot in the chassis for the C Series module.

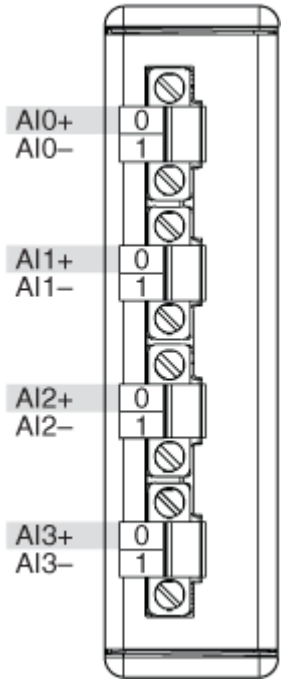
NI 9222

CompactRIO 4-Channel, ±10 V, 16-Bit Simultaneous, Channel-to-Channel Isolated Analog Input Module

Software Reference (?)

FPGA Interface

NI 9222 Pinout



Related Topics

FPGA Interface
Converting and Calibrating CompactRIO Analog Input Values
Detecting Out-of-Range Channels

NI 9222 (FPGA Interface)

CompactRIO 4-Channel, ±10 V, 16-Bit Simultaneous, Channel-to-Channel Isolated Analog Input Module

Open example

Find related examples

FPGA I/O Node

You can use an FPGA I/O Node, configured for reading, with this device.

Note You can simultaneously read from multiple channels on the NI 9222.

User-Controlled I/O Sampling

You can use the following User-Controlled I/O Sampling functions to perform I/O with more specific control over the I/O hardware on the FPGA.

Function	Type
Generate I/O Sample Pulse Method	Module function
Get I/O Read Status Method	I/O function
Read I/O Method	I/O function
Reset I/O Method	Module function

Note You must call the Reset I/O Method function first to prepare the NI 9222 to use the other User-Controlled I/O Sampling functions.

Terminals in Software

Use the FPGA I/O Node or User-Controlled I/O Sampling functions to access the following terminals for this device.

Terminal	Description

AI**x**	Analog input channel **x**, where **x** is the number of the channel. The NI 9222 has AI channels 0 to 3.

Arbitration

This device supports only the Arbitrate if Multiple Requestors Only option for arbitration. You cannot configure arbitration settings for this device.

Methods

This device does not support any methods.

I/O Properties

Use the FPGA I/O Property Node to access the following I/O properties for this device.

Property	Description
LSB Weight	Returns the LSB weight in nV/LSB for the channel. Use this value to convert and calibrate NI 9222 data if you set the **Calibration Mode** to **Raw** in the C Series Module Properties dialog box.
Offset	Returns the calibration offset in nV for the channel. Use this value to convert and calibrate NI 9222 data if you set the **Calibration Mode** to **Raw** in the **C Series Module Properties** dialog box.

Module Properties

Use the FPGA I/O Property Node to access the following module properties for this device.

Property	Description
Module ID	Returns the module ID, 0x7445.
Serial Number	Returns the unique serial number of the module.
Vendor ID	Returns the NI vendor ID, 0x1093.

Single-Cycle Timed Loop

This device does not support the single-cycle Timed Loop.

C Series Module Properties Dialog Box for the NI 9222/9223 (FPGA Interface)

Right-click an NI 9222 or NI 9223 C Series module in the **Project Explorer** window and select **Properties** from the shortcut menu to display this dialog box.

Use this dialog box to configure a C Series module.

This dialog box includes the following components:

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this option.
- **Location**—Specifies a slot in the chassis for the C Series module.
- **Calibration Mode**—Sets the calibration mode for the C Series module. Select **Calibrated** if you want the FPGA I/O Node to return calibrated, fixed-point data for the module in units of volts. The fixed-point data is signed, with a word length of 24 bits and an integer word length of 5 bits. Select **Raw** if you want the FPGA I/O Node to return uncalibrated, binary data for the module. If you select **Raw**, you must convert and calibrate the analog input values in the host VI. The default is **Calibrated**.

NI 9222 (Scan Interface)

CompactRIO 4-Channel, ±10 V, 16-Bit Simultaneous, Channel-to-Channel Isolated Analog Input Module


Open example

Module I/O Variables

To use I/O from this module in a VI, drag and drop I/O variables from the **Project Explorer** window to the block diagram of the VI. The I/O variables for the channels return calibrated floating-point data in volts.

Module Channels

The NI 9222 has the following channels.

Channel	Description
AI**x**	Analog input channel **x**, where **x** is the number of the channel. The NI 9222 has AI channels 0 to 3.

C Series Module Properties Dialog Box

Use this dialog box to configure the NI 9222. Right-click the NI 9222 in the **Project Explorer** window and select **Properties** to display this dialog box. You can configure the following options.

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this value.
- **Location**—Specifies a slot in the chassis for the C Series module.

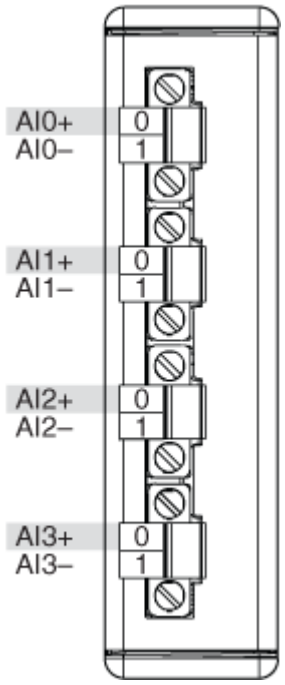
NI 9223

CompactRIO 4-Channel, ±10 V, 16-Bit Simultaneous, Channel-to-Channel Isolated Analog Input Module

Software Reference (?)

FPGA Interface

NI 9223 Pinout



Related Topics

FPGA Interface
Converting and Calibrating CompactRIO Analog Input Values
Detecting Out-of-Range Channels

NI 9223 (FPGA Interface)

CompactRIO 4-Channel, ±10 V, 16-Bit Simultaneous, Channel-to-Channel Isolated Analog Input Module

Open example

Find related examples

FPGA I/O Node

You can use an FPGA I/O Node, configured for reading, with this device.

Note You can simultaneously read from multiple channels on the NI 9223.

User-Controlled I/O Sampling

You can use the following User-Controlled I/O Sampling functions to perform I/O with more specific control over the I/O hardware on the FPGA.

Function	Type
Generate I/O Sample Pulse Method	Module function
Get I/O Read Status Method	I/O function
Read I/O Method	I/O function
Reset I/O Method	Module function

Note You must call the Reset I/O Method function first to prepare the NI 9223 to use the other User-Controlled I/O Sampling functions.

Terminals in Software

Use the FPGA I/O Node or User-Controlled I/O Sampling functions to access the following terminals for this device.

Terminal	Description
AI**x**	Analog input channel **x**, where **x** is the number of the channel. The NI 9223 has AI channels 0 to 3.

Arbitration

This device supports only the Arbitrate if Multiple Requestors Only option for arbitration. You cannot configure arbitration settings for this device.

Methods

This device does not support any methods.

I/O Properties

Use the FPGA I/O Property Node to access the following I/O properties for this device.

Property	Description
LSB Weight	Returns the LSB weight in nV/LSB for the channel. Use this value to convert and calibrate NI 9223 data if you set the **Calibration Mode** to **Raw** in the C Series Module Properties dialog box.
Offset	Returns the calibration offset in nV for the channel. Use this value to convert and calibrate NI 9223 data if you set the **Calibration Mode** to **Raw** in the **C Series Module Properties** dialog box.

Module Properties

Use the FPGA I/O Property Node to access the following module properties for this device.

Property	Description
Module ID	Returns the module ID, 0x74EC.
Serial Number	Returns the unique serial number of the module.
Vendor ID	Returns the NI vendor ID, 0x1093.

Single-Cycle Timed Loop

This device does not support the single-cycle Timed Loop.

C Series Module Properties Dialog Box for the NI 9222/9223 (FPGA Interface)

Right-click an NI 9222 or NI 9223 C Series module in the **Project Explorer** window and select **Properties** from the shortcut menu to display this dialog box.

Use this dialog box to configure a C Series module.

This dialog box includes the following components:

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this option.
- **Location**—Specifies a slot in the chassis for the C Series module.
- **Calibration Mode**—Sets the calibration mode for the C Series module. Select **Calibrated** if you want the FPGA I/O Node to return calibrated, fixed-point data for the module in units of volts. The fixed-point data is signed, with a word length of 24 bits and an integer word length of 5 bits. Select **Raw** if you want the FPGA I/O Node to return uncalibrated, binary data for the module. If you select **Raw**, you must convert and calibrate the analog input values in the host VI. The default is **Calibrated**.

NI 9223 (Scan Interface)

CompactRIO 4-Channel, ±10 V, 16-Bit Simultaneous, Channel-to-Channel Isolated Analog Input Module

Open example

Module I/O Variables

To use I/O from this module in a VI, drag and drop I/O variables from the **Project Explorer** window to the block diagram of the VI. The I/O variables for the channels return calibrated floating-point data in volts.

Module Channels

The NI 9223 has the following channels.

Channel	Description
AI**x**	Analog input channel **x**, where **x** is the number of the channel. The NI 9223 has AI channels 0 to 3.

C Series Module Properties Dialog Box

Use this dialog box to configure the NI 9223. Right-click the NI 9223 in the **Project Explorer** window and select **Properties** to display this dialog box. You can configure the following options.

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this value.
- **Location**—Specifies a slot in the chassis for the C Series module.

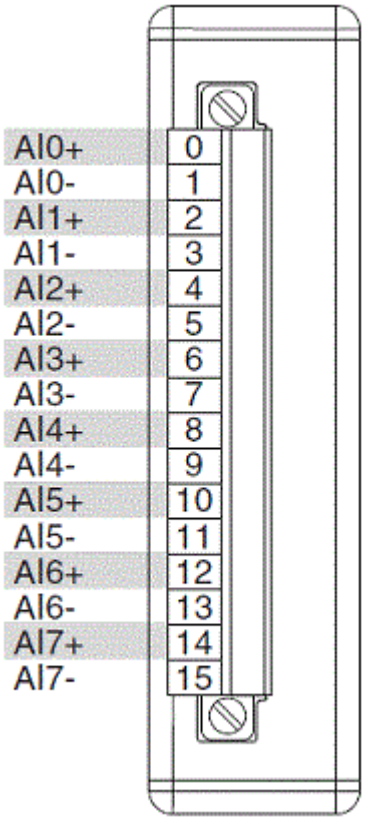
NI 9224

CompactRIO 8-Channel, ±10V 24-Bit Simultaneous Analog Input Module

Software Reference (?)

FPGA Interface

NI 9224 Pinout



Related Topics

FPGA Interface
Converting NI 9224 Data

NI 9224 (FPGA Interface)

CompactRIO 8-Channel, ±10V 24-Bit Simultaneous Analog Input Module

Open example Find related examples

FPGA I/O Node

You can use an FPGA I/O Node, configured for reading, with this device.

Terminals in Software

Use the FPGA I/O Node to access the following terminals for this device.

Terminal	Description
AI**x**	Analog input channel **x**, where **x** is the number of the channel. The NI 9224 has AI channels 0 to 7.

Arbitration

This device supports only the Arbitrate if Multiple Requestors Only option for arbitration. You cannot configure arbitration settings for this device.

I/O Methods

This device does not support any I/O methods.

Module Methods

This device does not support any module methods.

I/O Properties

This device does not support any I/O properties.

Module Properties

Use the FPGA I/O Property Node to access the following module properties for this device.

Property	Description
Conversion Time	Sets the time it takes to acquire one point of data from one or more channels in a single FPGA I/O Node. You can select **High Speed (1k S/s)**, **Medium Speed (100 S/s)**, **Medium Resolution (50/60Hz rejection – 12 S/s)**, or **High Resolution (50/60Hz rejection – 2 S/s)**. This property overwrites the value you configure in the C Series Module Properties dialog box.

	Returns the conversion time setting when configured to read.
Module ID	Returns the module ID, 0x780D.
Serial Number	Returns the unique serial number of the module.
Vendor ID	Returns the NI vendor ID, 0x1093.

Single-Cycle Timed Loop

This device does not support the single-cycle Timed Loop.

C Series Module Properties Dialog Box for the NI 9224 (FPGA Interface)

Right-click an NI 9224 C Series module in the **Project Explorer** window and select **Properties** from the shortcut menu to display this dialog box.

Use this dialog box to configure a C Series module.

This dialog box includes the following components:

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this option.
- **Location**—Specifies a slot in the chassis for the C Series module.
- **Calibration Mode**—Sets the calibration mode for the C Series module. Select **Calibrated** if you want the FPGA I/O Node to return calibrated, fixed-point data from the module in units of volts. The fixed-point data is signed, with a word length of 24 bits and an integer word length of 5 bits. Select **Raw** if you want the FPGA I/O Node to return calibrated, binary data from the module. If you select **Raw**, you must convert the binary values to engineering units. The default is **Calibrated**.

- **Conversion Time**—Specifies the time it takes to acquire one point of data from one or more channels in a single FPGA I/O Node. You can select **High Speed (1k S/s)**, **Medium Speed (100 S/s)**, **Medium Resolution (50/60Hz rejection – 12 S/s)**, or **High Resolution (50/60Hz rejection – 2 S/s)**. The default is **High Resolution (50/60Hz rejection – 2 S/s)**.

Converting NI 9224 Data (FPGA Interface)

Set the **Calibration Mode** to **Calibrated** in the C Series Module Properties dialog box for the NI 9224 if you want the FPGA I/O Node to return calibrated, fixed-point data from the module in units of volts. Set the **Calibration Mode** to **Raw** if you want the FPGA I/O Node to return calibrated, binary data from the module. If you set the **Calibration Mode** to **Raw**, you must convert the binary values to engineering units. You must convert these values in the host VI.

Using an Equation to Convert Binary Values to Voltage

You can use the following equation in the host VI to convert binary voltage values to volts:

Voltage = **Binary Value** × 1257533 pV/LSB

where

Binary Value is the value returned by the FPGA I/O Node.

NI 9224 (Scan Interface)

CompactRIO 8-Channel, ±10V 24-Bit Simultaneous Analog Input Module

Open example

Module I/O Variables

To use I/O from this module in a VI, drag and drop I/O variables from the **Project Explorer** window to the block diagram of the VI. The I/O variables for the channels return calibrated floating-point data in units as specified on the **C Series Module Properties** dialog box.

Module Channels

The NI 9224 has the following channels.

Channel	Description
AI**x**	Analog input channel **x**, where **x** is the number of the channel. For the NI 9224, **x** is 0 to 7.

C Series Module Properties Dialog Box

Use this dialog box to configure the NI 9224. Right-click the NI 9224 in the **Project Explorer** window and select **Properties** to display this dialog box. You can configure the following options.

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this value.
- **Location**—Specifies a slot in the chassis for the C Series module.
- **Conversion Time**—Determines the time it takes to acquire one point of data from one or more channels. You can select **Medium Speed**, **High Speed**, **Medium Resolution**, or **High Resolution**. Refer to the NI 9224 hardware documentation on ni.com/manuals for more information about the **Medium Speed**, **High Speed**, **Medium Resolution**, or **High Resolution** conversion times.

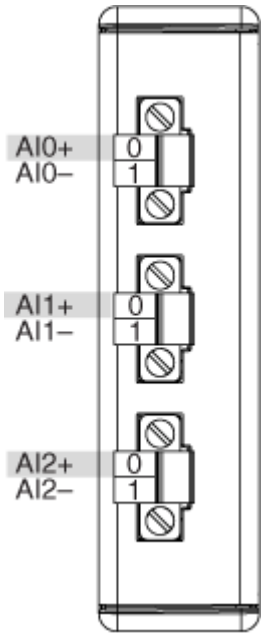
NI 9225

CompactRIO 3-Channel, 300 V_{rms}, 24-Bit Simultaneous Analog Input Module

Software Reference (?)

FPGA Interface | Scan Interface

NI 9225 Pinout



Related Topics

FPGA Interface
Converting and Calibrating CompactRIO Analog Input Values
Detecting Out-of-Range Channels
Acquiring Data from a Module (FPGA Interface)
Configuring the Master Timebase Source for a Module (FPGA Interface)
Configuring the Data Rate for a Module (FPGA Interface)
Synchronizing Multiple NI 9225/9227/9229/923x/924x/9251/9260 Modules
Understanding Loop Timing (FPGA Interface)

NI 9225 (FPGA Interface)

CompactRIO 3-Channel, 300 V_{rms}, 24-Bit Simultaneous Analog Input Module

Open example Find related examples

FPGA I/O Node

You can use an FPGA I/O Node, configured for reading, with this device.

Note You can simultaneously read from or write to multiple channels on the NI 9225. You can also synchronize an NI 9225 module with other modules that have a selectable timebase source.

Terminals in Software

Use the FPGA I/O Node to access the following terminals for this device.

Terminal	Description
AI**x**	Analog input channel **x**, where **x** is the number of the channel. The NI 9225 has AI channels 0 to 2. Do not access AI channels on multiple modules in the same FPGA I/O Node if the modules are not synchronized or do not use the same data rate.
Onboard Clock	Gives access to the onboard clock in the LabVIEW block diagram. The Onboard Clock frequency is 12.8 MHz. Use the FPGA I/O Node in a single-cycle Timed Loop to access this channel. You must export the Onboard Clock of the NI 9225 to access this channel.
Start	Channel that controls when the NI 9225 starts acquiring data. If TRUE is written to the **Start** channel, the NI 9225 starts acquiring data. When the NI 9225 is acquiring data, you must write TRUE to the **Stop** channel before you can access properties for the module. If FALSE is written to the **Start** channel, no operation is performed. Refer to the NI 9225 Getting Started VI in the `labview\examples\CompactRIO\Module Specific\NI 9225\NI 9225 Getting Started\NI 9225 Getting Started.lvproj` for an example of using the **Start** and **Stop** channels. Open example

Stop	Channel that controls when the NI 9225 stops acquiring data. If TRUE is written to the **Stop** channel, the NI 9225 stops acquiring data. When the NI 9225 is acquiring data, you must write TRUE to the **Stop** channel before you can access properties for the module. If FALSE is written to the **Stop** channel, no operation is performed. Refer to the NI 9225 Getting Started VI in the `labview\examples\CompactRIO\Module Specific\NI 9225\NI 9225 Getting Started\NI 9225 Getting Started.lvproj` for an example of using the **Start** and **Stop** channels.  Open example

Arbitration

This device supports only the Arbitrate if Multiple Requestors Only option for arbitration. You cannot configure arbitration settings for this device.

Methods

This device does not support any methods.

I/O Properties

Use the FPGA I/O Property Node to access the following I/O properties for this device.

Property	Description
LSB Weight	Returns the LSB weight in pV/LSB for the channel. Use this value to convert and calibrate NI 9225 data if you set the **Calibration Mode** to **Raw** in the C Series Module Properties dialog box.
Offset	Returns the calibration offset in µV for the channel. Use this value to convert and calibrate NI 9225 data if you set the **Calibration Mode** to **Ra**

	w in the **C Series Module Properties** dialog box.

Module Properties

Use the FPGA I/O Property Node to access the following module properties for this device.

Property	Description
Data Rate	Sets the rate at which the NI 9225 acquires data.
Module ID	Returns the module ID, 0x7383.
Serial Number	Returns the unique serial number of the module.
Vendor ID	Returns the NI vendor ID, 0x1093.

Single-Cycle Timed Loop

You can use the **Onboard Clock** channel in the single-cycle Timed Loop. You cannot use the other channels on the NI 9225 with the single-cycle Timed Loop. Refer to the Understanding Loop Timing (FPGA Interface) topic for information about loop timing for this module.

C Series Module Properties Dialog Box for the NI 9225/9227/9229/9238/9239/9246/9247 (FPGA Interface)

Right-click an NI 9225/NI 9227/NI 9229/NI 9238/NI 9239/NI 9246/NI 9247 C Series module in the **Project Explorer** window and select **Properties** from the shortcut menu to display this dialog box.

Use this dialog box to configure a C Series module.

This dialog box includes the following components:

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.

- **Module Type**—Specifies the type of C Series module. You cannot change this option.
- **Location**—Specifies a slot in the chassis for the C Series module.
- **Calibration Mode**—Sets the calibration mode for the C Series module.
  - Select **Calibrated**, which is the default, if you want the FPGA I/O Node to return calibrated, signed, fixed-point data from the module. The following table describes the units and integer word length of the returned data:

Module	Units	Word Length (bits)	Integer Word Length (bits)
NI 9225	V	24	10
NI 9227	A	24	5
NI 9229	V	24	7
NI 9238	V	24	1
NI 9239	V	24	5
NI 9246	A	24	7
NI 9247	A	24	9

  - Select **Raw** if you want the FPGA I/O Node to return uncalibrated, binary data from the module. If you select **Raw**, you must convert and calibrate the analog input values in the host VI.
- **Master Timebase Source**—Specifies the master timebase source that the module uses.
- **Export Onboard Clock**—Place a checkmark in this checkbox if you want to make this module accessible as a master timebase source to other modules.
- **Data Rate**—Specifies the rate at which the module acquires data.

NI 9225 (Scan Interface)

CompactRIO 3-Channel, 300 V_{rms}, 24-Bit Simultaneous Analog Input Module


Open example

Module I/O Variables

To use I/O from this module in a VI, drag and drop I/O variables from the **Project Explorer** window to the block diagram of the VI. The I/O variables for the channels return calibrated floating-point data in volts.

Module Channels

The NI 9225 has the following channels.

Channel	Description
AI**x**	Analog input channel **x**, where **x** is the number of the channel. For the NI 9225, **x** is 0 to 2.

C Series Module Properties Dialog Box

Use this dialog box to configure the NI 9225. Right-click the NI 9225 in the **Project Explorer** window and select **Properties** to display this dialog box. You can configure the following options.

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this value.
- **Location**—Specifies a slot in the chassis for the C Series module.

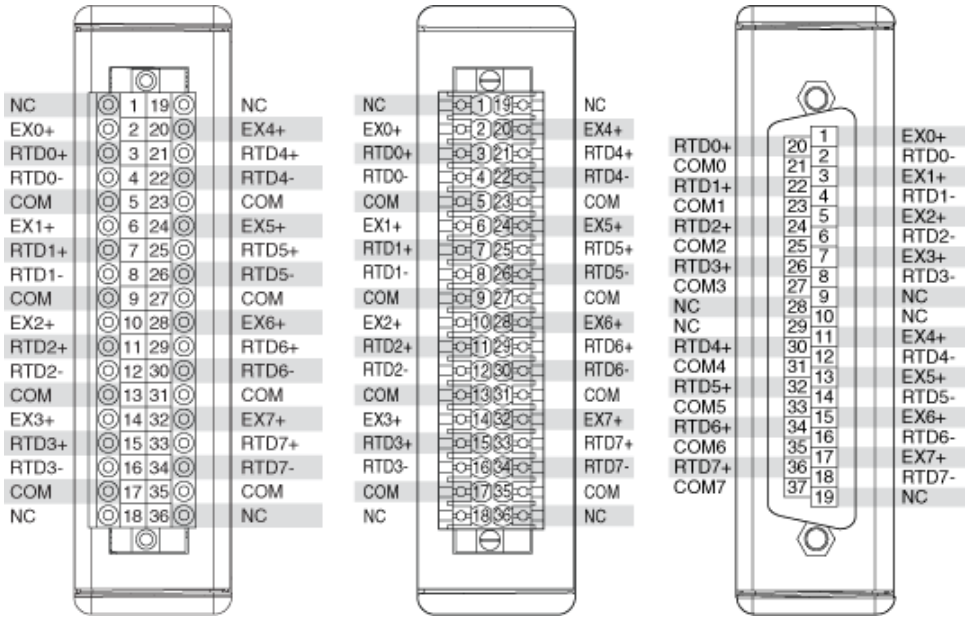
NI 9226

CompactRIO 8-Channel, 24-Bit, 1000 Ω RTD Analog Input Module

Software Reference (?)

FPGA Interface

NI 9226 Pinout



Related Topics

FPGA Interface
Converting and Calibrating CompactRIO Analog Input Values
Detecting Out-of-Range Channels
Converting Nominal Values to Temperature Values for the NI 9226

NI 9226 (FPGA Interface)

CompactRIO 8-Channel, 24-Bit, 1000 Ω RTD Analog Input Module

Open example Find related examples

FPGA I/O Node

You can use an FPGA I/O Node, configured for reading, with this device.

Terminals in Software

Use the FPGA I/O Node to access the following terminals for this device.

Terminal	Description

RTD**x**	RTD input channel **x**, where **x** is the number of the channel. The NI 9226 has RTD channels 0 to 7.

Arbitration

This device supports only the Arbitrate if Multiple Requestors Only option for arbitration. You cannot configure arbitration settings for this device.

Methods

This device does not support any methods.

I/O Properties

Use the FPGA I/O Property Node to access the following I/O properties for this device.

Property	Description
LSB Weight	Returns the LSB weight in pΩ/LSB for the channel. Use this value to convert and calibrate NI 9226 data if you set the **Calibration Mode** to **Raw** in the C Series Module Properties dialog box.
Offset	Returns the calibration offset in µΩ for the channel. Use this value to convert and calibrate NI 9226 data if you set the **Calibration Mode** to **Raw** in the **C Series Module Properties** dialog box.

Module Properties

Use the FPGA I/O Property Node to access the following module properties for this device.

Property	Description
Conversion Time	Sets the time in milliseconds it takes to acquire conversion data. This property overwrites the value you configure in the C Series Module Properties dialog box.

Module ID	Returns the module ID, 0x77C8 (NI 9226 with spring terminal) or 0x77E0 (NI 9226 with DSUB).
Serial Number	Returns the unique serial number of the module.
Vendor ID	Returns the NI vendor ID, 0x1093.

Single-Cycle Timed Loop

This device does not support the single-cycle Timed Loop.

C Series Module Properties Dialog Box for the NI 9226 (FPGA Interface)

Right-click an NI 9226 C Series module in the **Project Explorer** window and select **Properties** from the shortcut menu to display this dialog box.

Use this dialog box to configure a C Series module.

This dialog box includes the following components:

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this option.
- **Location**—Specifies a slot in the chassis for the C Series module.
- **Calibration Mode**—Sets the calibration mode for the C Series module. Select **Calibrated** if you want the FPGA I/O Node to return calibrated, fixed-point data from the module in units of ohms. The fixed-point data is signed, with a word length of 24 bits and an integer word length of 14 bits. Select **Raw** if you want the FPGA I/O Node to return uncalibrated, binary data from the module. If you select **Raw**, you must convert and calibrate the analog input values in the host VI. The default is **Calibrated**.
- **Conversion Time**—Specifies the time it takes to acquire one point of data from all channels. You can select **200 ms** or **2.5 ms**.

Converting Nominal Values to Temperature Values for the NI 9226 (FPGA Interface)

Set the **Calibration Mode** to **Calibrated** in the C Series Module Properties dialog box for the NI 9226 if you want the FPGA I/O Node to return calibrated, fixed-point data for the module in units of ohms. If you set the **Calibration Mode** to **Raw**, the FPGA I/O Node returns uncalibrated, binary values for the module. After you convert these binary values to nominal values, you can convert the nominal resistance values into temperature values. You must convert these values in the host VI.

Using a VI to Convert Values

Refer to the RTD to Temp VI in the `labview\examples\CompactRIO\Module Specific\NI 9226\NI 9226 Getting Started\NI 9226 Getting Started.lvproj` for an example of converting nominal resistance values to temperature. You can use the RTD to Temp VI as a subVI in the host VI to convert nominal resistance values to temperature.

Using an Equation to Measure Temperature

You can use a linearization curve known as the Callendar-Van Dusen equation in the host VI to measure the temperature of RTDs.

NI 9226 (Scan Interface)

CompactRIO 8-Channel, 24-Bit, 1000 Ω RTD Analog Input Module

Open example

Module I/O Variables

To use I/O from this module in a VI, drag and drop I/O variables from the **Project Explorer** window to the block diagram of the VI. The I/O variables for the channels return calibrated floating-point data in units as specified on the **C Series Module Properties** dialog box.

Module Channels

The NI 9226 has the following channels.

Channel	Description
RTD**x**	RTD input channel **x**, where **x** is the number of t he channel. The NI 9226 has RTD channels 0 to 7 .

C Series Module Properties Dialog Box

Use this dialog box to configure the NI 9226. Right-click the NI 9226 in the **Project Explorer** window and select **Properties** to display this dialog box. You can configure the following options.

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this value.
- **Location**—Specifies a slot in the chassis for the C Series module.
- **Conversion Time**—Specifies the time it takes to acquire one point of data from all channels. You can select **200 ms** or **2.5 ms**.
- **Channels**—Specifies the channel(s) for which you want to configure settings.
- **Measurement Units**—Specifies the units you want data to be returned in for the channel. You can select **Raw Ohms**, **Degrees Kelvin**, **Degrees Celsius**, **Degrees Fahrenheit**, or **Degrees Rankine**.
- **RTD Type**—Specifies the type of RTD connected to the channel by temperature coefficient of resistance (TCR). If you select **Custom**, you must enter the **Callendar-Van Dusen Coefficients** below.
  - **Callendar-Van Dusen Coefficients**—Specifies the coefficients to use in the Callendar-Van Dusen equation, a linearization curve for measuring the temperature of an RTD.

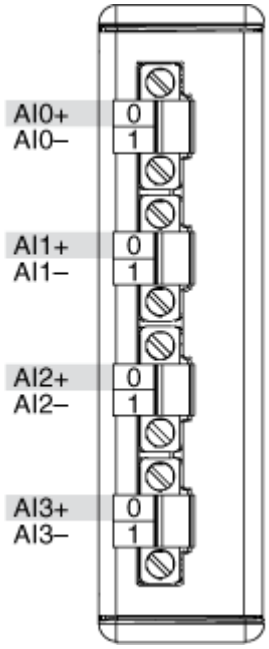
NI 9227

CompactRIO 4-Channel, 5 A_{rms}, 24-Bit Simultaneous Analog Input Module

Software Reference (?)

FPGA Interface | Scan Interface

NI 9227 Pinout



Related Topics

FPGA Interface
Converting and Calibrating CompactRIO Analog Input Values
Detecting Out-of-Range Channels
Acquiring Data from a Module (FPGA Interface)
Configuring the Master Timebase Source for a Module (FPGA Interface)
Configuring the Data Rate for a Module (FPGA Interface)
Synchronizing Multiple NI 9225/9227/9229/923x/924x/9251/9260 Modules
Understanding Loop Timing (FPGA Interface)

NI 9227 (FPGA Interface)

CompactRIO 4-Channel, 5 A_{rms}, 24-Bit Simultaneous Analog Input Module

Open example

Find related examples

FPGA I/O Node

You can use an FPGA I/O Node, configured for reading, with this device.

Note You can simultaneously read from or write to multiple channels on the NI 9227. You can also synchronize an NI 9227 module with other modules that have a selectable timebase source.

Terminals in Software

Use the FPGA I/O Node to access the following terminals for this device.

Terminal	Description
AI**x**	Analog input channel **x**, where **x** is the number of the channel. The NI 9227 has AI channels 0 to 3. Do not access AI channels on multiple modules in the same FPGA I/O Node if the modules are not synchronized or do not use the same data rate.
Onboard Clock	Gives access to the onboard clock in the LabVIEW block diagram. The Onboard Clock frequency is 12.8 MHz. Use the FPGA I/O Node in a single-cycle Timed Loop to access this channel. You must export the Onboard Clock of the NI 9227 to access this channel.
Start	Channel that controls when the NI 9227 starts acquiring data. If TRUE is written to the **Start** channel, the NI 9227 starts acquiring data. When the NI 9227 is acquiring data, you must write TRUE to the **Stop** channel before you can access properties for the module. If FALSE is written to the **Start** channel, no operation is performed.

	Refer to the NI 9227 Getting Started VI in the `labview\examples\CompactRIO\Module Specific\NI 9227\NI 9227 Getting Started\NI 9227 Getting Started.lvproj` for an example of using the **Start** and **Stop** channels. Open example
Stop	Channel that controls when the NI 9227 stops acquiring data. If TRUE is written to the **Stop** channel, the NI 9227 stops acquiring data. When the NI 9227 is acquiring data, you must write TRUE to the **Stop** channel before you can access properties for the module. If FALSE is written to the **Stop** channel, no operation is performed. Refer to the NI 9227 Getting Started VI in the `labview\examples\CompactRIO\Module Specific\NI 9227\NI 9227 Getting Started\NI 9227 Getting Started.lvproj` for an example of using the **Start** and **Stop** channels. Open example

Arbitration

This device supports only the Arbitrate if Multiple Requestors Only option for arbitration. You cannot configure arbitration settings for this device.

Methods

This device does not support any methods.

I/O Properties

Use the FPGA I/O Property Node to access the following I/O properties for this device.

Property	Description

LSB Weight	Returns the LSB weight in pA/LSB for the channel. Use this value to convert and calibrate NI 9227 data if you set the **Calibration Mode** to **Raw** in the C Series Module Properties dialog box.
Offset	Returns the calibration offset in nA for the channel. Use this value to convert and calibrate NI 9227 data if you set the **Calibration Mode** to **Raw** in the **C Series Module Properties** dialog box.

Module Properties

Use the FPGA I/O Property Node to access the following module properties for this device.

Property	Description
Data Rate	Sets the rate at which the NI 9227 acquires data.
Module ID	Returns the module ID, 0x7416.
Serial Number	Returns the unique serial number of the module.
Vendor ID	Returns the NI vendor ID, 0x1093.

Single-Cycle Timed Loop

You can use the **Onboard Clock** channel in the single-cycle Timed Loop. You cannot use the other channels on the NI 9227 with the single-cycle Timed Loop. Refer to the Understanding Loop Timing (FPGA Interface) topic for information about loop timing for this module.

C Series Module Properties Dialog Box for the NI 9225/9227/9229/9238/9239/9246/9247 (FPGA Interface)

Right-click an NI 9225/NI 9227/NI 9229/NI 9238/NI 9239/NI 9246/NI 9247 C Series module in the **Project Explorer** window and select **Properties** from the shortcut menu to display this dialog box.

Use this dialog box to configure a C Series module.

This dialog box includes the following components:

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this option.
- **Location**—Specifies a slot in the chassis for the C Series module.
- **Calibration Mode**—Sets the calibration mode for the C Series module.
  - Select **Calibrated**, which is the default, if you want the FPGA I/O Node to return calibrated, signed, fixed-point data from the module. The following table describes the units and integer word length of the returned data:

Module	Units	Word Length (bits)	Integer Word Length (bits)
NI 9225	V	24	10
NI 9227	A	24	5
NI 9229	V	24	7
NI 9238	V	24	1
NI 9239	V	24	5
NI 9246	A	24	7
NI 9247	A	24	9

  - Select **Raw** if you want the FPGA I/O Node to return uncalibrated, binary data from the module. If you select **Raw**, you must convert and calibrate the analog input values in the host VI.
- **Master Timebase Source**—Specifies the master timebase source that the module uses.
- **Export Onboard Clock**—Place a checkmark in this checkbox if you want to make this module accessible as a master timebase source to other modules.
- **Data Rate**—Specifies the rate at which the module acquires data.

NI 9227 (Scan Interface)

CompactRIO 4-Channel, 5 A_{rms}, 24-Bit Simultaneous Analog Input Module

Open example

Module I/O Variables

To use I/O from this module in a VI, drag and drop I/O variables from the **Project Explorer** window to the block diagram of the VI. The I/O variables for the channels return calibrated floating-point data in amps.

Module Channels

The NI 9227 has the following channels.

Channel	Description
AI**x**	Analog input channel **x**, where **x** is the number of the channel. For the NI 9227, **x** is 0 to 3.

C Series Module Properties Dialog Box

Use this dialog box to configure the NI 9227. Right-click the NI 9227 in the **Project Explorer** window and select **Properties** to display this dialog box. You can configure the following options.

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this value.
- **Location**—Specifies a slot in the chassis for the C Series module.

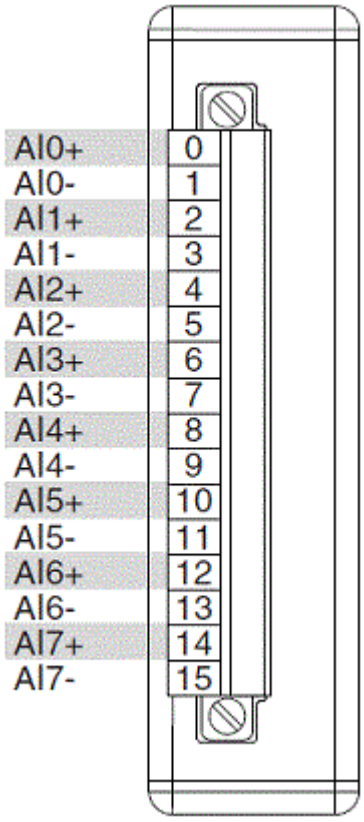
NI 9228

CompactRIO 8-Channel, ±60V 24-Bit Simultaneous Analog Input Module

Software Reference (?)

FPGA Interface

NI 9228 Pinout



Related Topics

FPGA Interface
Converting NI 9228 Data

NI 9228 (FPGA Interface)

CompactRIO 8-Channel, ±60V 24-Bit Simultaneous Analog Input Module

Open example

Find related examples

FPGA I/O Node

You can use an FPGA I/O Node, configured for reading, with this device.

Terminals in Software

Use the FPGA I/O Node to access the following terminals for this device.

Terminal	Description
AI**x**	Analog input channel **x**, where **x** is the number of the channel. The NI 9228 has AI channels 0 to 7.

Arbitration

This device supports only the Arbitrate if Multiple Requestors Only option for arbitration. You cannot configure arbitration settings for this device.

I/O Methods

This device does not support any I/O methods.

Module Methods

This device does not support any module methods.

I/O Properties

This device does not support any I/O properties.

Module Properties

Use the FPGA I/O Property Node to access the following module properties for this device.

Property	Description
Conversion Time	Sets the time it takes to acquire one point of dat a from one or more channels in a single FPGA I/ O Node. You can select **High Speed (1k S/s)**,

	Medium Speed (100 S/s), **Medium Resolution (50/60Hz rejection – 12 S/s)**, or **High Resolution (50/60Hz rejection – 2 S/s)**. This property overwrites the value you configure in the C Series Module Properties dialog box. Returns the conversion time setting when configured to read.
Module ID	Returns the module ID, 0x780E.
Serial Number	Returns the unique serial number of the module.
Vendor ID	Returns the NI vendor ID, 0x1093.

Single-Cycle Timed Loop

This device does not support the single-cycle Timed Loop.

C Series Module Properties Dialog Box for the NI 9228 (FPGA Interface)

Right-click an NI 9228 C Series module in the **Project Explorer** window and select **Properties** from the shortcut menu to display this dialog box.

Use this dialog box to configure a C Series module.

This dialog box includes the following components:

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this option.
- **Location**—Specifies a slot in the chassis for the C Series module.
- **Calibration Mode**—Sets the calibration mode for the C Series module. Select **Calibrated** if you want the FPGA I/O Node to return calibrated, fixed-point data from the module in units of volts. The fixed-point data is signed, with a word length of 24 bits and an integer word length of 7 bits. Select **Raw**

if you want the FPGA I/O Node to return calibrated, binary data from the module. If you select **Raw**, you must convert the binary values to engineering units. The default is **Calibrated**.

- **Conversion Time**—Specifies the time it takes to acquire one point of data from one or more channels in a single FPGA I/O Node. You can select **High Speed (1k S/s)**, **Medium Speed (100 S/s)**, **Medium Resolution (50/60Hz rejection – 12 S/s)**, or **High Resolution (50/60Hz rejection – 2 S/s)**. The default is **High Resolution (50/60Hz rejection – 2 S/s)**.

Converting NI 9228 Data (FPGA Interface)

Set the **Calibration Mode** to **Calibrated** in the C Series Module Properties dialog box for the NI 9228 if you want the FPGA I/O Node to return calibrated, fixed-point data from the module in units of volts. Set the **Calibration Mode** to **Raw** if you want the FPGA I/O Node to return calibrated, binary data from the module. If you set the **Calibration Mode** to **Raw**, you must convert the binary values to engineering units. You must convert these values in the host VI.

Using an Equation to Convert Binary Values to Voltage

You can use the following equation in the host VI to convert binary voltage values to volts:

Voltage = **Binary Value** × 7602677 pV/LSB

where **Binary Value** is the value returned by the FPGA I/O Node.

NI 9228 (Scan Interface)

CompactRIO 8-Channel, ±60V 24-Bit Simultaneous Analog Input Module


Open example

Module I/O Variables

To use I/O from this module in a VI, drag and drop I/O variables from the **Project Explorer** window to the block diagram of the VI. The I/O variables for the channels

return calibrated floating-point data in units as specified on the **C Series Module Properties** dialog box.

Module Channels

The NI 9228 has the following channels.

Channel	Description
AI**x**	Analog input channel **x**, where **x** is the number of the channel. For the NI 9228, **x** is 0 to 7.

C Series Module Properties Dialog Box

Use this dialog box to configure the NI 9228. Right-click the NI 9228 in the **Project Explorer** window and select **Properties** to display this dialog box. You can configure the following options.

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this value.
- **Location**—Specifies a slot in the chassis for the C Series module.
- **Conversion Time**—Determines the time it takes to acquire one point of data from one or more channels. You can select **Medium Speed**, **High Speed**, **Medium Resolution**, or **High Resolution**. Refer to the NI 9228 hardware documentation on ni.com/manuals for more information about the **Medium Speed**, **High Speed**, **Medium Resolution**, or **High Resolution** conversion times.

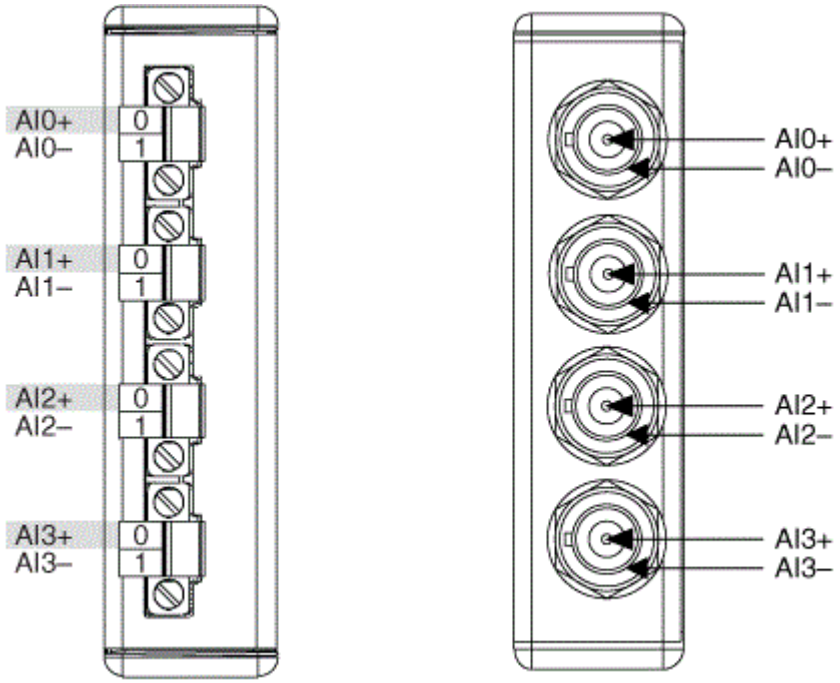
NI 9229

CompactRIO 4-Channel, ±60 V, 24-Bit Simultaneous Analog Input Module

Software Reference (?)

FPGA Interface | Scan Interface

NI 9229 Pinout



Related Topics

FPGA Interface
Converting and Calibrating CompactRIO Analog Input Values
Detecting Out-of-Range Channels
Acquiring Data from a Module (FPGA Interface)
Configuring the Master Timebase Source for a Module (FPGA Interface)
Configuring the Data Rate for a Module (FPGA Interface)
Synchronizing Multiple NI 9225/9227/9229/923x/924x/9251/9260 Modules
Understanding Loop Timing (FPGA Interface)

NI 9229 (FPGA Interface)

CompactRIO 4-Channel, ±60 V, 24-Bit Simultaneous Analog Input Module

Open example Find related examples

FPGA I/O Node

You can use an FPGA I/O Node, configured for reading, with this device.

Note You can simultaneously read from or write to multiple channels on the NI 9229. You also can synchronize an NI 9229 module with other modules that have a selectable timebase source.

Terminals in Software

Use the FPGA I/O Node to access the following terminals for this device.

Terminal	Description
AI**x**	Analog input channel **x**, where **x** is the number of the channel. The NI 9229 has AI channels 0 to 3. Do not access AI channels on multiple modules in the same FPGA I/O Node if the modules are not synchronized or do not use the same data rate.
Onboard Clock	Gives access to the onboard clock in the LabVIEW block diagram. The Onboard Clock frequency is 12.8 MHz. Use the FPGA I/O Node in a single-cycle Timed Loop to access this channel. You must export the Onboard Clock of the NI 9229 to access this channel.
Start	Channel that controls when the NI 9229 starts acquiring data. If TRUE is written to the **Start** channel, the NI 9229 starts acquiring data. When the NI 9229 is acquiring data, you must write TRUE to the **Stop** channel before you can access properties for the module. If FALSE is written to the **Start** channel, no operation is performed. Refer to the NI 9229 Getting Started VI in the `labview\examples\CompactRIO\Module Specific\NI 9229\NI 9229 Getting Started\NI 9229 Getting Started.lvproj` for an example of using the **Start** and

	Stop channels. Open example
Stop	Channel that controls when the NI 9229 stops acquiring data. If TRUE is written to the **Stop** channel, the NI 9229 stops acquiring data. When the NI 9229 is acquiring data, you must write TRUE to the **Stop** channel before you can access properties for the module. If FALSE is written to the **Stop** channel, no operation is performed. Refer to the NI 9229 Getting Started VI in the `labview\examples\CompactRIO\Module Specific\NI 9229\NI 9229 Getting Started\NI 9229 Getting Started.lvproj` for an example of using the **Start** and **Stop** channels. Open example

Arbitration

This device supports only the Arbitrate if Multiple Requestors Only option for arbitration. You cannot configure arbitration settings for this device.

Methods

This device does not support any methods.

I/O Properties

Use the FPGA I/O Property Node to access the following I/O properties for this device.

Property	Description
LSB Weight	Returns the LSB weight in pV/LSB for the channel. Use this value to convert and calibrate NI 9229 data if you set the **Calibration Mode** to **Raw** in the C Series Module Properties dialog box.

Offset	Returns the calibration offset in nV for the channel. Use this value to convert and calibrate NI 9229 data if you set the **Calibration Mode** to **Raw** in the **C Series Module Properties** dialog box.

Module Properties

Use the FPGA I/O Property Node to access the following module properties for this device.

Property	Description
Data Rate	Sets the rate at which the NI 9229 acquires data.
Module ID	Returns the module ID.
Serial Number	Returns the unique serial number of the module.
Vendor ID	Returns the NI vendor ID, 0x1093.

Single-Cycle Timed Loop

You can use the **Onboard Clock** channel in the single-cycle Timed Loop. You cannot use the other channels on the NI 9229 with the single-cycle Timed Loop. Refer to the Understanding Loop Timing (FPGA Interface) topic for information about loop timing for this module.

C Series Module Properties Dialog Box for the NI 9225/9227/9229/9238/9239/9246/9247 (FPGA Interface)

Right-click an NI 9225/NI 9227/NI 9229/NI 9238/NI 9239/NI 9246/NI 9247 C Series module in the **Project Explorer** window and select **Properties** from the shortcut menu to display this dialog box.

Use this dialog box to configure a C Series module.

This dialog box includes the following components:

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module

based on the slot number. You can use this field to give the module a descriptive name.

- **Module Type**—Specifies the type of C Series module. You cannot change this option.
- **Location**—Specifies a slot in the chassis for the C Series module.
- **Calibration Mode**—Sets the calibration mode for the C Series module.
  - Select **Calibrated**, which is the default, if you want the FPGA I/O Node to return calibrated, signed, fixed-point data from the module. The following table describes the units and integer word length of the returned data:

Module	Units	Word Length (bits)	Integer Word Length (bits)
NI 9225	V	24	10
NI 9227	A	24	5
NI 9229	V	24	7
NI 9238	V	24	1
NI 9239	V	24	5
NI 9246	A	24	7
NI 9247	A	24	9

  - Select **Raw** if you want the FPGA I/O Node to return uncalibrated, binary data from the module. If you select **Raw**, you must convert and calibrate the analog input values in the host VI.
- **Master Timebase Source**—Specifies the master timebase source that the module uses.
- **Export Onboard Clock**—Place a checkmark in this checkbox if you want to make this module accessible as a master timebase source to other modules.
- **Data Rate**—Specifies the rate at which the module acquires data.

NI 9229 (Scan Interface)

CompactRIO 4-Channel, ±60 V, 24-Bit Simultaneous Analog Input Module

Open example

Module I/O Variables

To use I/O from this module in a VI, drag and drop I/O variables from the **Project Explorer** window to the block diagram of the VI. The I/O variables for the channels return calibrated floating-point data in volts.

Module Channels

The NI 9229 has the following channels.

Channel	Description
AI**x**	Analog input channel **x**, where **x** is the number of the channel. For the NI 9229, **x** is 0 to 3.

C Series Module Properties Dialog Box

Use this dialog box to configure the NI 9229. Right-click the NI 9229 in the **Project Explorer** window and select **Properties** to display this dialog box. You can configure the following options.

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this value.
- **Location**—Specifies a slot in the chassis for the C Series module.

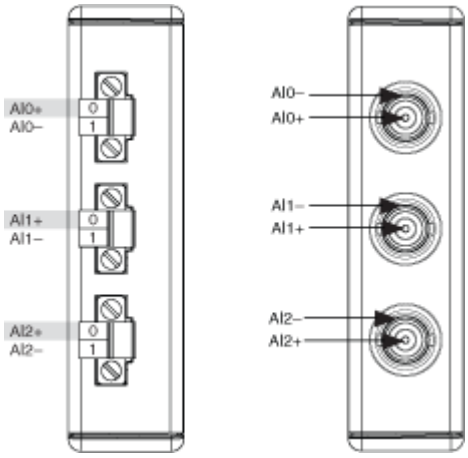
NI 9230

CompactRIO 3-Channel, ±30 V, 12.8 kS/s, 24-Bit Software Selectable IEPE and AC/DC Analog Input Module

Software Reference (?)

FPGA Interface

NI 9230 Pinout



Related Topics

FPGA Interface
Converting and Calibrating CompactRIO Analog Input Values
Detecting Out-of-Range Channels
Accessing TEDS Information from a Module (FPGA Interface)
Acquiring Data from a Module (FPGA Interface)
Configuring the Master Timebase Source for a Module (FPGA Interface)
Configuring the NI 9230/9232/9234 Channel Input Modes
Configuring the Data Rate for a Module (FPGA Interface)
Synchronizing Multiple NI 9225/9227/9229/923x/924x/9251/9260 Modules
Understanding Loop Timing (FPGA Interface)

NI 9230 (FPGA Interface)

CompactRIO 3-Channel, ±30 V, 12.8 kS/s, 24-Bit Software Selectable IEPE and AC/DC Analog Input Module

Open example

Find examples

FPGA I/O Node

You can use an FPGA I/O Node, configured for reading, with this device.

Note You can synchronize an NI 9230 with other modules that have a selectable timebase source.

Terminals in Software

Use the FPGA I/O Node to access the following terminals for this device.

Terminal	Description
AI**x**	Analog input channel **x**, where **x** is the number of the channel. The NI 9230 has AI channels 0 to 2. Do not access AI channels on multiple modules in the same FPGA I/O Node if the modules are not synchronized or do not use the same data rate.
Onboard Clock	13.1072 MHz internal clock of the NI 9230. Use the FPGA I/O Node in a single-cycle Timed Loop to access this channel. You must export the onboard clock of the NI 9230 to access this channel. If you do not export the onboard clock and try to access the **Onboard Clock** channel, LabVIEW returns a code generation error when you try to compile the FPGA VI.
Start	Channel that controls when the NI 9230 starts acquiring data. If TRUE is written to the **Start** channel, the NI 9230 starts acquiring data. When the NI 9230 is acquiring data, you must write TRUE to the **Stop** channel before you can access properties or TEDS information for the module. If FALSE is written to the **Start** channel, no operation is performed. Refer to the NI 9230 Getting Started VI in the `labview\examples\CompactRIO\Module Specific\NI 9230\NI 9230 Getting Started\NI 9230 Getting Started.`

	lvproj for an example of using the **Start** and **Stop** channels. Open example
Stop	Channel that controls when the NI 9230 stops acquiring data. If TRUE is written to the **Stop** channel, the NI 9230 stops acquiring data. When the NI 9230 is acquiring data, you must write TRUE to the **Stop** channel before you can access properties or TEDS information for the module. If FALSE is written to the **Stop** channel, no operation is performed. Refer to the NI 9230 Getting Started VI in the labview\examples\CompactRIO\Module Specific\NI 9230\NI 9230 Getting Started\NI 9230 Getting Started.lvproj for an example of using the **Start** and **Stop** channels. Open example

Arbitration

This device supports only the Arbitrate if Multiple Requestors Only option for arbitration. You cannot configure arbitration settings for this device.

Module Methods

Use the FPGA I/O Method Node to access the following module method for this device.

Method	Description
Check Cached Status	Returns Booleans for each channel that indicate whether there was a short circuit or open loop on the channel since the last execution of the Check Cached Status method. When the FPGA I/O Node reads the channels, the FPGA VI determines the state of the channels and caches any TRUE v

	alue until the Check Cached Status method exec utes. ▪ **Short Circuit**—Returns an array of Boo lean values. A value of TRUE in any index i ndicates that the channel sharing a numb er with that index detected a short circuit on the channel at some point after the las t time that the Check Cached Status meth od executed. ▪ **Open Loop**—Returns an array of Boole an values. A value of TRUE in any index in dicates that the channel sharing a numbe r with that index detected an open loop o n the channel at some point after the last time that the Check Cached Status metho d executed.

I/O Properties

Use the FPGA I/O Property Node to access the following I/O properties for this device.

Property	Description
Input Configuration	Sets the input configuration of the correspondin g channel to one of three modes: AC coupled, D C coupled, or IEPE AC coupled.
LSB Weight	Returns the LSB weight in pV/LSB for the channe l. Use this value to convert and calibrate NI 9230 data if you set the **Calibration Mode** to **Raw** i n the C Series Module Properties dialog box.
Offset	Returns the calibration offset in nV for the chan nel. Use this value to convert and calibrate NI 92 30 data if you set the **Calibration Mode** to **Ra w** in the **C Series Module Properties** dialog b ox.

Module Properties

Use the FPGA I/O Property Node to access the following module properties for this device.

Property	Description
Data Rate	Sets the rate at which the NI 9230 acquires data.
Module ID	Returns the module ID, 0x77CC.
Serial Number	Returns the unique serial number of the module .
Vendor ID	Returns the NI vendor ID, 0x1093.

Single-Cycle Timed Loop

You can use the **Onboard Clock** channel in the single-cycle Timed Loop. You cannot use the other channels on the NI 9230 with the single-cycle Timed Loop. Refer to the Understanding Loop Timing (FPGA Interface) topic for information about loop timing for this module.

C Series Module Properties Dialog Box for the NI 9230/9232/9234 (FPGA Interface)

Right-click an NI 9230, NI 9232, or NI 9234 C Series module in the **Project Explorer** window and select **Properties** from the shortcut menu to display this dialog box.

Use this dialog box to configure a C Series module.

This dialog box includes the following components:

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this option.
- **Location**—Specifies a slot in the chassis for the C Series module.
- **Calibration Mode**—Sets the calibration mode for the C Series module. Select **Calibrated** if you want the FPGA I/O Node to return calibrated, fixed-

point data from the module in units of volts. The fixed-point data is signed, with a word length of 24 bits and an integer word length of 7 bits for the NI 9230/9232 and 4 bits for the NI 9234. Select **Raw** if you want the FPGA I/O Node to return uncalibrated, binary data from the module. If you select **Raw**, you must convert and calibrate the analog input values in the host VI. The default is **Calibrated**.

- **Master Timebase Source**—Specifies the master timebase source that the module uses.
- **Export Onboard Clock**—Place a checkmark in this checkbox if you want to make this module accessible as a master timebase source to other modules.
- **Data Rate**—Specifies the rate at which the module acquires data.
- **Enable TEDS Support**—Place a checkmark in this checkbox if you want to enable TEDS support in the FPGA and host VIs for this module.
- **Channels**—Specifies the channel(s) for which you want to select the input configuration.
- **Selected Channel(s) Settings**—Specifies the input configuration for each channel.
  - **Input Configuration**—Sets the input configuration for the selected channel(s). Select **AC Coupled** for AC coupling with IEPE excitation off, **DC Coupled** for DC coupling with IEPE excitation off, or **IEPE AC Coupled** for AC coupling with IEPE excitation on.

Configuring the NI 9230/9232/9234 Channel Input Modes (FPGA Interface)

You can configure the input mode for each channel of the NI 9230, NI 9232, or NI 9234 at edit time using the C Series Module Properties dialog box. You can programmatically change the input mode for each channel at run time using the FPGA I/O Property Node. The execution of an FPGA I/O Property Node that is configured with an **Input Configuration** property overwrites the value you configured in the **C Series Module Properties** dialog box for the corresponding channel.

Configuring the Channel Input Modes Using the C Series Module Properties Dialog Box

Complete the following steps to configure the channel input modes using the **C Series Module Properties** dialog box.

1. Configure the CompactRIO system, and add an module.
2. Right-click the module in the **Project Explorer** window and select **Properties** to display the **C Series Module Properties** dialog box.
3. Select the channel(s) for which you want to configure the input mode from the **Channels** table. You can select more than one channel by holding the <Ctrl> or <Shift> key when selecting channels.
4. Select the input mode for the selected channel(s) from the **Input Configuration** pull-down menu.
5. Click the **OK** button.
6. Select **File»Save All** in the **Project Explorer** window.

Configuring the Channel Input Modes Using the FPGA I/O Property Node

Complete the following steps to configure the channel input modes using the FPGA I/O Property Node.

1. Create FPGA I/O items for the channels of the module for which you want to configure the **Input Configuration** property.
2. Place an FPGA I/O Property Node on the block diagram and configure it for the module channel for which you want to configure the input mode.
3. Click the **Property** section and select **Input Configuration** from the shortcut menu.
4. Right-click the **Input Configuration** input and select **Create»Control** from the shortcut menu.
5. On the front panel of the VI, select an input mode for the channel from the **Input Configuration** pull-down menu.

You can change the channel input modes at run time by writing to the control from the host VI. Refer to the following getting started VIs for examples of how to configure the input modes using the FPGA I/O Property Node.

Module	Example File Path	Open Example
NI 9230	`labview\examples\CompactRIO\Module Specific\NI 9230\NI 9230 Getting Started\NI 9230 Getting Started.lvproj`	Open example (NI 9230)
NI 9232	`labview\examples\CompactRIO\Module Specific\NI 9232\NI 9232 Getting Started\NI 9232 Getting Started.lvproj`	Open example (NI 9232)
NI 9234	`labview\examples\CompactRIO\Module Specific\NI 9234\NI 9234 Getting Started\NI 9234 Getting Started.lvproj`	Open example (NI 9234)

Note The **Input Configuration** property returns error 65538 if the module is acquiring data. You must use the Stop channel to stop acquiring data before you can write properties to the modules.

NI 9231

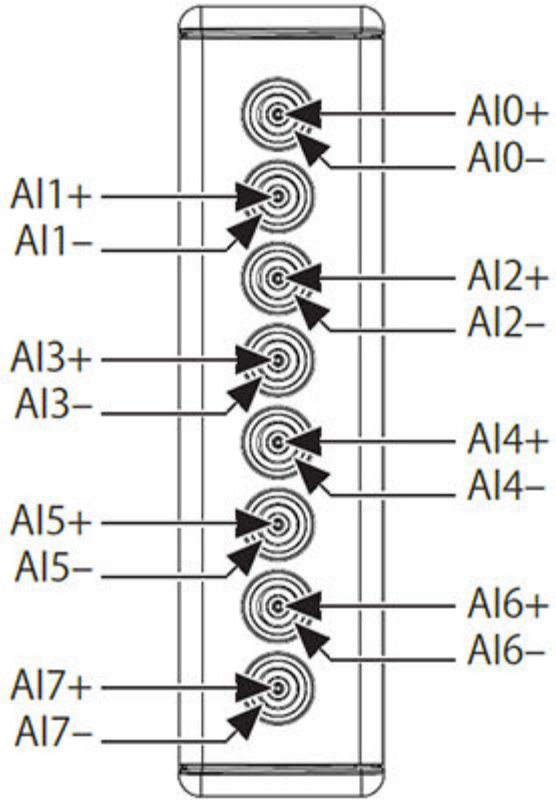
8 AI, ±5 V, 24 Bit, 51.2 kS/s/ch Simultaneous, AC/DC Coupling, IEPE AC Coupling

Software Reference (?)

FPGA Interface |

NI 9231

NI 9231 Pinout



Related Topics

FPGA Interface
C Series Module Properties Dialog Box
Converting and Calibrating CompactRIO Analog Input Values
Detecting Out-of-Range Channels for CompactRIO Analog Input Channels
Acquiring Data from an NI 9231
Configuring the Data Rate for a Module (FPGA Interface)
Converting NI 9231 Data
Synchronizing Multiple Modules
Understanding Loop Timing (FPGA Interface)

NI 9231 (FPGA Interface)

8 AI, ±5 V, 24 Bit, 51.2 kS/s/ch Simultaneous, AC/DC Coupling, IEPE AC Coupling

Open example

Find related examples

FPGA I/O Node

You can use an FPGA I/O Node, configured for reading, with this device.

Note You can synchronize an NI 9231 module with other modules that have a selectable timebase source.

Terminals in Software

Use the FPGA I/O Node to access the following terminals for this device.

Terminal	Description
AI**x**	Analog input channel **x**, where **x** is the number of the channel. The NI 9231 has channels 0 to 7.
Onboard Clock	Gives access to the onboard clock in the LabVIEW block diagram. The onboard clock frequency is 13.1072 MHz. Use the FPGA I/O Node in a single-cycle timed loop to access this channel. You must export the onboard clock of the NI 9231 to access this channel.
Start	Channel that controls when the NI 9231 starts acquiring data. If TRUE is written to the **Start** channel, the NI 9231 starts acquiring data. When the NI 9231 is acquiring data, you must write TRUE to the **Stop** channel before you can access properties for the module. If FALSE is written to the **Start** channel, no operation is performed.
Stop	Channel that controls when the NI 9231 stops acquiring data. If TRUE is written to the **Stop** channel, the NI 9231 stops acquiring data. When the NI 9231 is acquiring data, you must write TRUE to the **Stop** channel before you can access prope

	rties for the module. If FALSE is written to the **Stop** channel, no operation is performed.

Arbitration

This device supports only the Arbitrate if Multiple Requestors Only option for arbitration. You cannot configure arbitration settings for this device.

Module Methods

Use the FPGA I/O Method Node to access the following module method for this device.

Method	Description
Check Cached Status	Returns Booleans for each channel that indicate whether there was a short circuit or open loop on the channel since the last execution of the Check Cached Status method. When the FPGA I/O Node reads the channels, the FPGA VI determines the state of the channels and caches any TRUE value until the Check Cached Status method executes. ▪ **Short Circuit**—Returns an array of Boolean values. A value of TRUE in any index indicates that the channel sharing a number with that index detected a short circuit on the channel at some point after the last time that the Check Cached Status method executed. ▪ **Open Loop**—Returns an array of Boolean values. A value of TRUE in any index indicates that the channel sharing a number with that index detected an open loop on the channel at some point after the last time that the Check Cached Status method executed.

I/O Properties

Use the FPGA I/O Property Node to access the following I/O properties for this device.

Property	Description
Input Configuration	Sets the input configuration of the corresponding channel to one of three modes: AC Coupled, DC Coupled, IEPE AC Coupled.

Module Properties

Use the FPGA I/O Property Node to access the following module properties for this device.

Property	Description
Data Rate	Sets the rate at which the NI 9231 acquires data.
Module ID	Returns the module ID, 0x7930.
Serial Number	Returns the unique serial number of the module.
Vendor ID	Returns the NI vendor ID, 0x1093.

Single-Cycle Timed Loop

This device does not support the single-cycle Timed Loop.

C Series Module Properties Dialog Box for the NI 9231 (FPGA Interface)

Right-click an NI 9231 C Series module in the **Project Explorer** window and select **Properties** from the shortcut menu to display this dialog box.

Use this dialog box to configure a C Series module.

This dialog box includes the following components:

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.

- **Type**—Specifies the type of C Series module. You cannot change this option.
- **Location**—Specifies a slot in the chassis for the C Series module.
- **Calibration Mode**—Sets the calibration mode for the C Series module. Select **Calibrated** if you want the FPGA I/O Node to return calibrated, fixed-point data from the module. The fixed-point data is signed, with 24-bits word length and 4-bits integer word length. Select **Raw** if you want the FPGA I/O Node to return calibrated, binary data from the module. If you select **Raw**, you must convert the binary data to the actual analog input values in the host VI. The default is **Calibrated**.
- **Master Timebase Source**—Specifies the master timebase source that the module uses.
- **Export Onboard Clock**—Place a checkmark in this checkbox if you want to make this module accessible as a master timebase source to other modules.
- **Data Rate**—Specifies the rate at which the module acquires data.
- **Enable TEDS Support**—Place a checkmark in this checkbox if you want to enable TEDS support in the FPGA and host VIs for this module.
- **Channels**—Specifies the channel(s) for which you want to select the input configuration.
- **Selected Channel(s) Settings**—Specifies the input configuration for each channel.
  - **Input Configuration**—Sets the input configuration for the selected channel(s). Select AC Coupled for AC coupling, DC Coupled for DC coupling, IEPE AC Coupled for AC coupling with IEPE enabled.

Configuring the NI 9231 Channel Input Modes (FPGA Interface)

You can configure the input mode for each channel of the NI 9231 at edit time using the C Series Module Properties dialog box. You can programmatically change the input mode for each channel at run time using the FPGA I/O Property Node. The execution of an FPGA I/O Property Node that is configured with an **Input**

Configuration property overwrites the value you configured in the **C Series Module Properties** dialog box for the corresponding channel.

Configuring the Channel Input Modes Using the C Series Module Properties Dialog Box

Complete the following steps to configure the channel input modes using the **C Series Module Properties** dialog box.

1. Configure the CompactRIO system, and add an module.
2. Right-click the module in the **Project Explorer** window and select **Properties** to display the **C Series Module Properties** dialog box.
3. Select the channel(s) for which you want to configure the input mode from the **Channels** table. You can select more than one channel by holding the <Ctrl> or <Shift> key when selecting channels.
4. Select the input mode for the selected channel(s) from the **Input Configuration** pull-down menu.
5. Click the **OK** button.
6. Select **File»Save All** in the **Project Explorer** window.

Configuring the Channel Input Modes Using the FPGA I/O Property Node

Complete the following steps to configure the channel input modes using the FPGA I/O Property Node.

1. Create FPGA I/O items for the channels of the module for which you want to configure the **Input Configuration** property.
2. Place an FPGA I/O Property Node on the block diagram and configure it for the module channel for which you want to configure the input mode.
3. Click the **Property** section and select **Input Configuration** from the shortcut menu.
4. Right-click the **Input Configuration** input and select **Create»Control** from the shortcut menu.

5. On the front panel of the VI, select an input mode for the channel from the **Input Configuration** pull-down menu.

You can change the channel input modes at run time by writing to the control from the host VI. Refer to the following getting started VIs for examples of how to configure the input modes using the FPGA I/O Property Node.

Module	Example File Path	Open Example
NI 9231	`labview\examples\CompactRIO\Module Specific\NI 9231\NI 9231 Getting Started\NI 9231 Getting Started.lvproj`	Open example (NI 9231)

Note The **Input Configuration** property returns error 65538 if the module is acquiring data. You must use the Stop channel to stop acquiring data before you can write properties to the modules.

Converting NI 9231 Data (FPGA Interface)

Set the **Calibration Mode** to **Calibrated** in the C Series Module Properties dialog box for the NI 9231 if you want the FPGA I/O Node to return calibrated, fixed-point data from the module. Set the **Calibration Mode** to **Raw** if you want the FPGA I/O Node to return calibrated, binary data from the module. If you set the **Calibration Mode** to **Raw**, you must convert the binary values to engineering units. You must convert these values in the host VI.

You can use the following equations in the host VI to convert binary voltage values to volts:

Volts = **Binary Value** × 610714.8 pV/LSB

where

Binary Value is the value returned by the FPGA I/O Node.

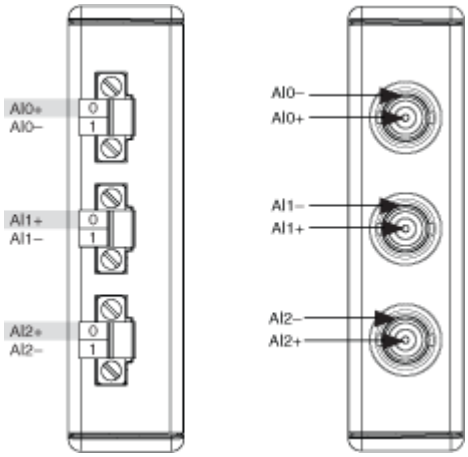
NI 9232

CompactRIO 3-Channel, ±30 V, 102.4 kS/s, 24-Bit Software Selectable IEPE and AC/DC Analog Input Module

Software Reference (?)

FPGA Interface

NI 9232 Pinout



Related Topics

FPGA Interface
Converting and Calibrating CompactRIO Analog Input Values
Detecting Out-of-Range Channels
Accessing TEDS Information from a Module (FPGA Interface)
Acquiring Data from a Module (FPGA Interface)
Configuring the Master Timebase Source for a Module (FPGA Interface)
Configuring the NI 9230/9232/9234 Channel Input Modes
Configuring the Data Rate for a Module (FPGA Interface)
Synchronizing Multiple NI 9225/9227/9229/923x/924x/9251/9260 Modules
Understanding Loop Timing (FPGA Interface)

NI 9232 (FPGA Interface)

CompactRIO 3-Channel, ±30 V, 102.4 kS/s, 24-Bit Software Selectable IEPE and AC/DC Analog Input Module

Open example

Find related examples

FPGA I/O Node

You can use an FPGA I/O Node, configured for reading, with this device.

Note You can synchronize an NI 9232 with other modules that have a selectable timebase source.

Terminals in Software

Use the FPGA I/O Node to access the following terminals for this device.

Terminal	Description
AI**x**	Analog input channel **x**, where **x** is the number of the channel. The NI 9232 has AI channels 0 to 2. Do not access AI channels on multiple modules in the same FPGA I/O Node if the modules are not synchronized or do not use the same data rate.
Onboard Clock	13.1072 MHz internal clock of the NI 9232. Use the FPGA I/O Node in a single-cycle Timed Loop to access this channel. You must export the onboard clock of the NI 9232 to access this channel. If you do not export the onboard clock and try to access the **Onboard Clock** channel, LabVIEW returns a code generation error when you try to compile the FPGA VI.
Start	Channel that controls when the NI 9232 starts acquiring data. If TRUE is written to the **Start** channel, the NI 9232 starts acquiring data. When the NI 9232 is acquiring data, you must write TRUE to the **Stop** channel before you can access properties or TEDS information for the module. If FALSE is written to the **Start** channel, no operatio

	n is performed. Refer to the NI 9232 Getting Started VI in the `labview\examples\CompactRIO\Module Specific\NI 9232\NI 9232 Getting Started\NI 9232 Getting Started.lvproj` for an example of using the **Start** and **Stop** channels. Open example
Stop	Channel that controls when the NI 9232 stops acquiring data. If TRUE is written to the **Stop** channel, the NI 9232 stops acquiring data. When the NI 9232 is acquiring data, you must write TRUE to the **Stop** channel before you can access properties or TEDS information for the module. If FALSE is written to the **Stop** channel, no operation is performed. Refer to the NI 9232 Getting Started VI in the `labview\examples\CompactRIO\Module Specific\NI 9232\NI 9232 Getting Started\NI 9232 Getting Started.lvproj` for an example of using the **Start** and **Stop** channels. Open example

Arbitration

This device supports only the Arbitrate if Multiple Requestors Only option for arbitration. You cannot configure arbitration settings for this device.

Module Methods

Use the FPGA I/O Method Node to access the following module method for this device.

Method	Description

Check Cached Status	Returns Booleans for each channel that indicate whether there was a short circuit or open loop on the channel since the last execution of the Check Cached Status method. When the FPGA I/O Node reads the channels, the FPGA VI determines the state of the channels and caches any TRUE value until the Check Cached Status method executes. ▪ **Short Circuit**—Returns an array of Boolean values. A value of TRUE in any index indicates that the channel sharing a number with that index detected a short circuit on the channel at some point after the last time that the Check Cached Status method executed. ▪ **Open Loop**—Returns an array of Boolean values. A value of TRUE in any index indicates that the channel sharing a number with that index detected an open loop on the channel at some point after the last time that the Check Cached Status method executed.

I/O Properties

Use the FPGA I/O Property Node to access the following I/O properties for this device.

Property	Description
Input Configuration	Sets the input configuration of the corresponding channel to one of three modes: AC coupled, DC coupled, or IEPE AC coupled.
LSB Weight	Returns the LSB weight in pV/LSB for the channel. Use this value to convert and calibrate NI 9232 data if you set the **Calibration Mode** to **Raw** in the C Series Module Properties dialog box.
Offset	Returns the calibration offset in nV for the channel. Use this value to convert and calibrate NI 9232 data if you set the **Calibration Mode** to **Ra**

	w in the **C Series Module Properties** dialog box.

Module Properties

Use the FPGA I/O Property Node to access the following module properties for this device.

Property	Description
Data Rate	Sets the rate at which the NI 9232 acquires data.
Module ID	Returns the module ID, 0x753F.
Serial Number	Returns the unique serial number of the module.
Vendor ID	Returns the NI vendor ID, 0x1093.

Single-Cycle Timed Loop

You can use the **Onboard Clock** channel in the single-cycle Timed Loop. You cannot use the other channels on the NI 9232 with the single-cycle Timed Loop. Refer to the Understanding Loop Timing (FPGA Interface) topic for information about loop timing for this module.

C Series Module Properties Dialog Box for the NI 9230/9232/9234 (FPGA Interface)

Right-click an NI 9230, NI 9232, or NI 9234 C Series module in the **Project Explorer** window and select **Properties** from the shortcut menu to display this dialog box.

Use this dialog box to configure a C Series module.

This dialog box includes the following components:

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this option.
- **Location**—Specifies a slot in the chassis for the C Series module.

- **Calibration Mode**—Sets the calibration mode for the C Series module. Select **Calibrated** if you want the FPGA I/O Node to return calibrated, fixed-point data from the module in units of volts. The fixed-point data is signed, with a word length of 24 bits and an integer word length of 7 bits for the NI 9230/9232 and 4 bits for the NI 9234. Select **Raw** if you want the FPGA I/O Node to return uncalibrated, binary data from the module. If you select **Raw**, you must convert and calibrate the analog input values in the host VI. The default is **Calibrated**.
- **Master Timebase Source**—Specifies the master timebase source that the module uses.
- **Export Onboard Clock**—Place a checkmark in this checkbox if you want to make this module accessible as a master timebase source to other modules.
- **Data Rate**—Specifies the rate at which the module acquires data.
- **Enable TEDS Support**—Place a checkmark in this checkbox if you want to enable TEDS support in the FPGA and host VIs for this module.
- **Channels**—Specifies the channel(s) for which you want to select the input configuration.
- **Selected Channel(s) Settings**—Specifies the input configuration for each channel.
  - **Input Configuration**—Sets the input configuration for the selected channel(s). Select **AC Coupled** for AC coupling with IEPE excitation off, **DC Coupled** for DC coupling with IEPE excitation off, or **IEPE AC Coupled** for AC coupling with IEPE excitation on.

Configuring the NI 9230/9232/9234 Channel Input Modes (FPGA Interface)

You can configure the input mode for each channel of the NI 9230, NI 9232, or NI 9234 at edit time using the C Series Module Properties dialog box. You can programmatically change the input mode for each channel at run time using the FPGA I/O Property Node. The execution of an FPGA I/O Property Node that is configured with an **Input Configuration** property overwrites the value you

configured in the **C Series Module Properties** dialog box for the corresponding channel.

Configuring the Channel Input Modes Using the C Series Module Properties Dialog Box

Complete the following steps to configure the channel input modes using the **C Series Module Properties** dialog box.

1. Configure the CompactRIO system, and add an module.
2. Right-click the module in the **Project Explorer** window and select **Properties** to display the **C Series Module Properties** dialog box.
3. Select the channel(s) for which you want to configure the input mode from the **Channels** table. You can select more than one channel by holding the <Ctrl> or <Shift> key when selecting channels.
4. Select the input mode for the selected channel(s) from the **Input Configuration** pull-down menu.
5. Click the **OK** button.
6. Select **File»Save All** in the **Project Explorer** window.

Configuring the Channel Input Modes Using the FPGA I/O Property Node

Complete the following steps to configure the channel input modes using the FPGA I/O Property Node.

1. Create FPGA I/O items for the channels of the module for which you want to configure the **Input Configuration** property.
2. Place an FPGA I/O Property Node on the block diagram and configure it for the module channel for which you want to configure the input mode.
3. Click the **Property** section and select **Input Configuration** from the shortcut menu.
4. Right-click the **Input Configuration** input and select **Create»Control** from the shortcut menu.

5. On the front panel of the VI, select an input mode for the channel from the **Input Configuration** pull-down menu.

You can change the channel input modes at run time by writing to the control from the host VI. Refer to the following getting started VIs for examples of how to configure the input modes using the FPGA I/O Property Node.

Module	Example File Path	Open Example
NI 9230	`labview\examples\CompactRIO\Module Specific\NI 9230\NI 9230 Getting Started\NI 9230 Getting Started.lvproj`	Open example (NI 9230)
NI 9232	`labview\examples\CompactRIO\Module Specific\NI 9232\NI 9232 Getting Started\NI 9232 Getting Started.lvproj`	Open example (NI 9232)
NI 9234	`labview\examples\CompactRIO\Module Specific\NI 9234\NI 9234 Getting Started\NI 9234 Getting Started.lvproj`	Open example (NI 9234)

Note The **Input Configuration** property returns error 65538 if the module is acquiring data. You must use the Stop channel to stop acquiring data before you can write properties to the modules.

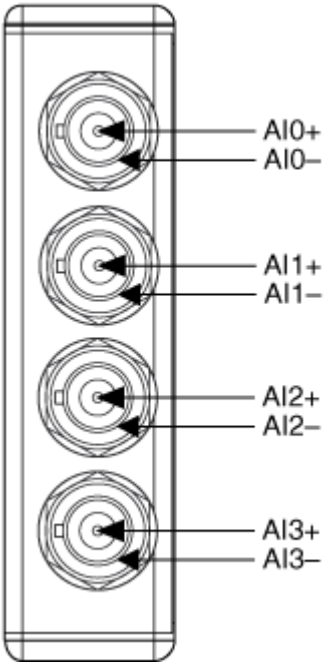
NI 9234

CompactRIO 4-Channel, ±5 V, 51.2 KS/s, 24-Bit Software Selectable IEPE and AC/DC Analog Input Module

Software Reference (?)

FPGA Interface | Scan Interface

NI 9234 Pinout



Related Topics

FPGA Interface
Converting and Calibrating CompactRIO Analog Input Values
Detecting Out-of-Range Channels
Accessing TEDS Information from a Module (FPGA Interface)
Acquiring Data from a Module (FPGA Interface)
Configuring the Master Timebase Source for a Module (FPGA Interface)
Configuring the NI 9230/9232/9234 Channel Input Modes
Configuring the Data Rate for a Module (FPGA Interface)
Synchronizing Multiple NI 9225/9227/9229/923x/924x/9251/9260 Modules
Understanding Loop Timing (FPGA Interface)

NI 9234 (FPGA Interface)

CompactRIO 4-Channel, ±5 V, 51.2 KS/s, 24-Bit Software Selectable IEPE and AC/DC Analog Input Module

Open example

Find related examples

FPGA I/O Node

You can use an FPGA I/O Node, configured for reading, with this device.

Note You can synchronize an NI 9234 with other modules that have a selectable timebase source.

Terminals in Software

Use the FPGA I/O Node to access the following terminals for this device.

Terminal	Description
AI**x**	Analog input channel **x**, where **x** is the number of the channel. The NI 9234 has AI channels 0 to 3. Do not access AI channels on multiple modules in the same FPGA I/O Node if the modules are not synchronized or do not use the same data rate.
Onboard Clock	13.1072 MHz internal clock of the NI 9234. Use the FPGA I/O Node in a single-cycle Timed Loop to access this channel. You must export the onboard clock of the NI 9234 to access this channel. If you do not export the onboard clock and try to access the **Onboard Clock** channel, LabVIEW returns a code generation error when you try to compile the FPGA VI.
Start	Channel that controls when the NI 9234 starts acquiring data. If TRUE is written to the **Start** channel, the NI 9234 starts acquiring data. When the NI 9234 is acquiring data, you must write TRUE to the **Stop** channel before you can access properties or TEDS information for the module. If FALSE is written to the **Start** channel, no operation is performed. Refer to the NI 9234 Getting Started VI in the `labview\examples\CompactRIO\Module Specific\NI 9234\NI 9234 Getting Started\NI 9234 Getting Started.`

	`lvproj` for an example of using the **Start** and **Stop** channels.  Open example
Stop	Channel that controls when the NI 9234 stops acquiring data. If TRUE is written to the **Stop** channel, the NI 9234 stops acquiring data. When the NI 9234 is acquiring data, you must write TRUE to the **Stop** channel before you can access properties or TEDS information for the module. If FALSE is written to the **Stop** channel, no operation is performed. Refer to the NI 9234 Getting Started VI in the `labview\examples\CompactRIO\Module Specific\NI 9234\NI 9234 Getting Started\NI 9234 Getting Started.lvproj` for an example of using the **Start** and **Stop** channels.  Open example

Arbitration

This device supports only the Arbitrate if Multiple Requestors Only option for arbitration. You cannot configure arbitration settings for this device.

Methods

This device does not support any methods.

I/O Properties

Use the FPGA I/O Property Node to access the following I/O properties for this device.

Property	Description
Input Configuration	Sets the input configuration of the corresponding channel to one of three modes: AC coupled, DC coupled, or IEPE AC coupled.

LSB Weight	Returns the LSB weight in pV/LSB for the channel. Use this value to convert and calibrate NI 9234 data if you set the **Calibration Mode** to **Raw** in the C Series Module Properties dialog box.
Offset	Returns the calibration offset in nV for the channel. Use this value to convert and calibrate NI 9234 data if you set the **Calibration Mode** to **Raw** in the **C Series Module Properties** dialog box.

Module Properties

Use the FPGA I/O Property Node to access the following module properties for this device.

Property	Description
Data Rate	Sets the rate at which the NI 9234 acquires data.
Module ID	Returns the module ID, 0x72B5.
Serial Number	Returns the unique serial number of the module.
Vendor ID	Returns the NI vendor ID, 0x1093.

Single-Cycle Timed Loop

You can use the **Onboard Clock** channel in the single-cycle Timed Loop. You cannot use the other channels on the NI 9234 with the single-cycle Timed Loop. Refer to the Understanding Loop Timing (FPGA Interface) topic for information about loop timing for this module.

C Series Module Properties Dialog Box for the NI 9230/9232/9234 (FPGA Interface)

Right-click an NI 9230, NI 9232, or NI 9234 C Series module in the **Project Explorer** window and select **Properties** from the shortcut menu to display this dialog box.

Use this dialog box to configure a C Series module.

This dialog box includes the following components:

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this option.
- **Location**—Specifies a slot in the chassis for the C Series module.
- **Calibration Mode**—Sets the calibration mode for the C Series module. Select **Calibrated** if you want the FPGA I/O Node to return calibrated, fixed-point data from the module in units of volts. The fixed-point data is signed, with a word length of 24 bits and an integer word length of 7 bits for the NI 9230/9232 and 4 bits for the NI 9234. Select **Raw** if you want the FPGA I/O Node to return uncalibrated, binary data from the module. If you select **Raw**, you must convert and calibrate the analog input values in the host VI. The default is **Calibrated**.
- **Master Timebase Source**—Specifies the master timebase source that the module uses.
- **Export Onboard Clock**—Place a checkmark in this checkbox if you want to make this module accessible as a master timebase source to other modules.
- **Data Rate**—Specifies the rate at which the module acquires data.
- **Enable TEDS Support**—Place a checkmark in this checkbox if you want to enable TEDS support in the FPGA and host VIs for this module.
- **Channels**—Specifies the channel(s) for which you want to select the input configuration.
- **Selected Channel(s) Settings**—Specifies the input configuration for each channel.
  - **Input Configuration**—Sets the input configuration for the selected channel(s). Select **AC Coupled** for AC coupling with IEPE excitation off, **DC Coupled** for DC coupling with IEPE excitation off, or **IEPE AC Coupled** for AC coupling with IEPE excitation on.

Configuring the NI 9230/9232/9234 Channel Input Modes (FPGA Interface)

You can configure the input mode for each channel of the NI 9230, NI 9232, or NI 9234 at edit time using the C Series Module Properties dialog box. You can programmatically change the input mode for each channel at run time using the FPGA I/O Property Node. The execution of an FPGA I/O Property Node that is configured with an **Input Configuration** property overwrites the value you configured in the **C Series Module Properties** dialog box for the corresponding channel.

Configuring the Channel Input Modes Using the C Series Module Properties Dialog Box

Complete the following steps to configure the channel input modes using the **C Series Module Properties** dialog box.

1. Configure the CompactRIO system, and add an module.
2. Right-click the module in the **Project Explorer** window and select **Properties** to display the **C Series Module Properties** dialog box.
3. Select the channel(s) for which you want to configure the input mode from the **Channels** table. You can select more than one channel by holding the <Ctrl> or <Shift> key when selecting channels.
4. Select the input mode for the selected channel(s) from the **Input Configuration** pull-down menu.
5. Click the **OK** button.
6. Select **File»Save All** in the **Project Explorer** window.

Configuring the Channel Input Modes Using the FPGA I/O Property Node

Complete the following steps to configure the channel input modes using the FPGA I/O Property Node.

1. Create FPGA I/O items for the channels of the module for which you want to configure the **Input Configuration** property.

2. Place an FPGA I/O Property Node on the block diagram and configure it for the module channel for which you want to configure the input mode.
3. Click the **Property** section and select **Input Configuration** from the shortcut menu.
4. Right-click the **Input Configuration** input and select **Create»Control** from the shortcut menu.
5. On the front panel of the VI, select an input mode for the channel from the **Input Configuration** pull-down menu.

You can change the channel input modes at run time by writing to the control from the host VI. Refer to the following getting started VIs for examples of how to configure the input modes using the FPGA I/O Property Node.

Module	Example File Path	Open Example
NI 9230	`labview\examples\CompactRIO\Module Specific\NI 9230\NI 9230 Getting Started\NI 9230 Getting Started.lvproj`	Open example (NI 9230)
NI 9232	`labview\examples\CompactRIO\Module Specific\NI 9232\NI 9232 Getting Started\NI 9232 Getting Started.lvproj`	Open example (NI 9232)
NI 9234	`labview\examples\CompactRIO\Module Specific\NI 9234\NI 9234 Getting Started\NI 9234 Getting Started.lvproj`	Open example (NI 9234)

Note The **Input Configuration** property returns error 65538 if the module is acquiring data. You must use the Stop channel to stop acquiring data before you can write properties to the modules.

NI 9234 (Scan Interface)

CompactRIO 4-Channel, ±5 V, 51.2 KS/s, 24-Bit Software Selectable IEPE and AC/DC Analog Input Module

Open example

Module I/O Variables

To use I/O from this module in a VI, drag and drop I/O variables from the **Project Explorer** window to the block diagram of the VI. The I/O variables for the channels return calibrated floating-point data in volts.

Module Channels

The NI 9234 has the following channels.

Channel	Description
AI**x**	Analog input channel **x**, where **x** is the number of the channel. For the NI 9234, **x** is 0 to 3.

C Series Module Properties Dialog Box

Use this dialog box to configure the NI 9234. Right-click the NI 9234 in the **Project Explorer** window and select **Properties** to display this dialog box. You can configure the following options.

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this value.
- **Location**—Specifies a slot in the chassis for the C Series module.
- **Channels**—Specifies the channel(s) for which you want to select the input configuration.

- **Input Configuration**—Specifies the input configuration for the selected channel(s). You can select one of three modes: AC coupled, DC coupled, or IEPE AC coupled.

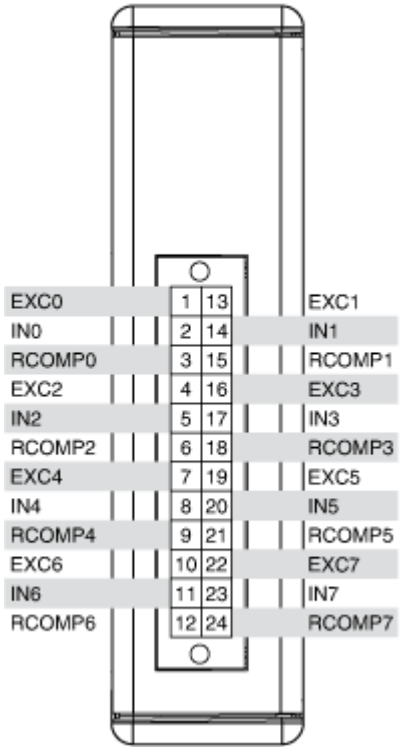
NI 9235

CompactRIO 8-Channel, 24-Bit Quarter-Bridge Analog Input Module

Software Reference (?)

FPGA Interface | Scan Interface

NI 9235 Pinout



Related Topics

FPGA Interface
Converting and Calibrating CompactRIO Analog Input Values
Detecting Out-of-Range Channels
Acquiring Data from a Module (FPGA Interface)
Configuring the Master Timebase Source for a Module (FPGA Interface)

Configuring the Data Rate for a Module (FPGA Interface)
Synchronizing Multiple NI 9225/9227/9229/923x/924x/9251/9260 Modules
Understanding Loop Timing (FPGA Interface)

NI 9235 (FPGA Interface)

CompactRIO 8-Channel, 24-Bit Quarter-Bridge Analog Input Module

Open example Find related examples

FPGA I/O Node

You can use an FPGA I/O Node, configured for reading, with this device.

Note You can synchronize an NI 9235 module with other modules that have a selectable timebase source.

Terminals in Software

Use the FPGA I/O Node to access the following terminals for this device.

Terminal	Description
AI**x**	Analog input channel **x**, where **x** is the number of the channel. The NI 9235 has AI channels 0 to 7. Do not access AI channels on multiple modules in the same FPGA I/O Node if the modules are not synchronized or do not use the same data rate.
Onboard Clock	12.8 MHz internal clock of the NI 9235. Use the FPGA I/O Node in a single-cycle Timed Loop to access this channel. You must export the Onboard Clock of the NI 9235 to access this channel.
Start	Channel that controls when the NI 9235 starts acquiring data. If TRUE is written to the **Start** channel, the NI 9235 starts acquiring data. When the NI 9235 is acquiring data, you must write TRUE to the **Stop** channel before you can access properties for the module. If FALSE is written to the **Start** channel, no operation is performed.

	Refer to the NI 9235 Getting Started VI in the `labview\examples\CompactRIO\Module Specific\NI 9235\NI 9235 Getting Started\NI 9235 Getting Started.lvproj` for an example of using the **Start** and **Stop** channels.  Open example
Stop	Channel that controls when the NI 9235 stops acquiring data. If TRUE is written to the **Stop** channel, the NI 9235 stops acquiring data. When the NI 9235 is acquiring data, you must write TRUE to the **Stop** channel before you can access properties for the module. If FALSE is written to the **Stop** channel, no operation is performed. Refer to the NI 9235 Getting Started VI in the `labview\examples\CompactRIO\Module Specific\NI 9235\NI 9235 Getting Started\NI 9235 Getting Started.lvproj` for an example of using the **Start** and **Stop** channels.  Open example

Arbitration

This device supports only the Arbitrate if Multiple Requestors Only option for arbitration. You cannot configure arbitration settings for this device.

Methods

This device does not support any methods.

I/O Properties

Use the FPGA I/O Property Node to access the following I/O properties for this device.

Property	Description
LSB Weight	Returns the LSB weight in units of 100 fV/V per LSB for the channel. 100 fV is equal to 10^{-13} volts. Use this value to convert and calibrate NI 9235 data if you set the **Calibration Mode** to **Raw** in the C Series Module Properties dialog box.
Offset	Returns the calibration offset in units of 100 nV/V for the channel. Use this value to convert and calibrate NI 9235 data if you set the **Calibration Mode** to **Raw** in the **C Series Module Properties** dialog box.
Shunt Cal Enable	Controls the shunt calibration switch for each channel. Refer to the NI 9235 Getting Started VI in the `labview\examples\CompactRIO\Module Specific\NI 9235\NI 9235 Getting Started\NI 9235 Getting Started.lvproj` for an example of using the **Shunt Cal Enable** property.  Open example

Module Properties

Use the FPGA I/O Property Node to access the following module properties for this device.

Property	Description
Data Rate	Sets the rate at which the NI 9235 acquires data.
Module ID	Returns the module ID, 0x732A.
Serial Number	Returns the unique serial number of the module.
Vendor ID	Returns the NI vendor ID, 0x1093.

Single-Cycle Timed Loop

You can use the **Onboard Clock** channel in the single-cycle Timed Loop. You cannot use the other channels on the NI 9235 with the single-cycle Timed Loop. Refer to the Understanding Loop Timing (FPGA Interface) topic for information about loop timing for this module.

C Series Module Properties Dialog Box for the NI 9235/9236 (FPGA Interface)

Right-click an NI 9235 or NI 9236 C Series module in the **Project Explorer** window and select **Properties** from the shortcut menu to display this dialog box.

Use this dialog box to configure a C Series module.

This dialog box includes the following components:

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this option.
- **Location**—Specifies a slot in the chassis for the C Series module.
- **Calibration Mode**—Sets the calibration mode for the C Series module. Select **Calibrated** if you want the FPGA I/O Node to return calibrated, fixed-point data from the module in units of volts/volt. The fixed-point data is signed, with a word length of 24 bits and an integer word length of –4 bits. Select **Raw** if you want the FPGA I/O Node to return uncalibrated, binary data from the module. If you select **Raw**, you must convert and calibrate the analog input values in the host VI. The default is **Calibrated**.
- **Master Timebase Source**—Specifies the master timebase source that the module uses.
- **Export Onboard Clock**—Place a checkmark in this checkbox if you want to make this module accessible as a master timebase source to other modules.

- **Data Rate**—Specifies the rate at which the module acquires data.

NI 9235 (Scan Interface)

CompactRIO 8-Channel, 24-Bit Quarter-Bridge Analog Input Module

 Open example

Module I/O Variables

To use I/O from this module in a VI, drag and drop I/O variables from the **Project Explorer** window to the block diagram of the VI. The I/O variables for the channels return calibrated floating-point data in volts/volts (channel voltage/excitation voltage).

Module Channels

The NI 9235 has the following channels.

Channel	Description
AI**x**	Analog input channel **x**, where **x** is the number of the channel. For the NI 9235, **x** is 0 to 7.

C Series Module Properties Dialog Box

Use this dialog box to configure the NI 9235. Right-click the NI 9235 in the **Project Explorer** window and select **Properties** to display this dialog box. You can configure the following options.

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this value.
- **Location**—Specifies a slot in the chassis for the C Series module.

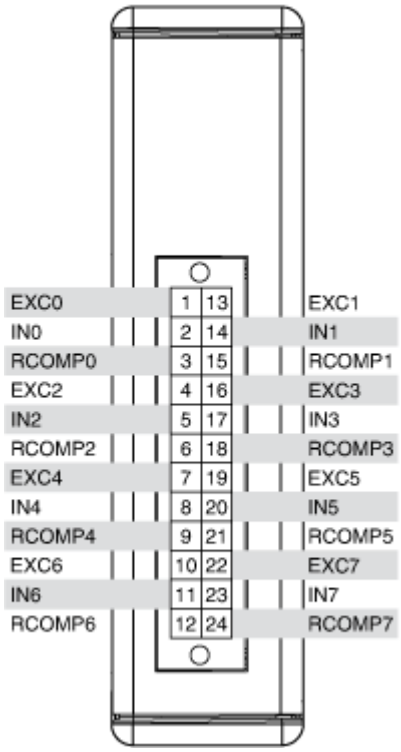
NI 9236

CompactRIO 8-Channel, 24-Bit Quarter-Bridge Analog Input Module

Software Reference (?)

FPGA Interface | Scan Interface

NI 9236 Pinout



Related Topics

FPGA Interface
Converting and Calibrating CompactRIO Analog Input Values
Detecting Out-of-Range Channels
Acquiring Data from a Module (FPGA Interface)
Configuring the Master Timebase Source for a Module (FPGA Interface)
Configuring the Data Rate for a Module (FPGA Interface)
Synchronizing Multiple NI 9225/9227/9229/923x/924x/9251/9260 Modules
Understanding Loop Timing (FPGA Interface)

NI 9236 (FPGA Interface)

CompactRIO 8-Channel, 24-Bit Quarter-Bridge Analog Input Module

Open example

Find related examples

FPGA I/O Node

You can use an FPGA I/O Node, configured for reading, with this device.

Note You can synchronize an NI 9236 module with other modules that have a selectable timebase source.

Terminals in Software

Use the FPGA I/O Node to access the following terminals for this device.

Terminal	Description
AI**x**	Analog input channel **x**, where **x** is the number of the channel. The NI 9236 has AI channels 0 to 7. Do not access AI channels on multiple modules in the same FPGA I/O Node if the modules are not synchronized or do not use the same data rate.
Onboard Clock	12.8 MHz internal clock of the NI 9236. Use the FPGA I/O Node in a single-cycle Timed Loop to access this channel. You must export the Onboard Clock of the NI 9236 to access this channel.
Start	Channel that controls when the NI 9236 starts acquiring data. If TRUE is written to the **Start** channel, the NI 9236 starts acquiring data. When the NI 9236 is acquiring data, you must write TRUE to the **Stop** channel before you can access properties for the module. If FALSE is written to the **Start** channel, no operation is performed. Refer to the NI 9236 Getting Started VI in the `labview\examples\CompactRIO\Module Specific\NI 9236\NI 9236 Getting Started\NI 9236 Getting Started.`

	lvproj for an example of using the **Start** and **Stop** channels.  Open example
Stop	Channel that controls when the NI 9236 stops acquiring data. If TRUE is written to the **Stop** channel, the NI 9236 stops acquiring data. When the NI 9236 is acquiring data, you must write TRUE to the **Stop** channel before you can access properties for the module. If FALSE is written to the **Stop** channel, no operation is performed. Refer to the NI 9236 Getting Started VI in the labview\examples\CompactRIO\Module Specific\NI 9236\NI 9236 Getting Started\NI 9236 Getting Started.lvproj for an example of using the **Start** and **Stop** channels.  Open example

Arbitration

This device supports only the Arbitrate if Multiple Requestors Only option for arbitration. You cannot configure arbitration settings for this device.

Methods

This device does not support any methods.

I/O Properties

Use the FPGA I/O Property Node to access the following I/O properties for this device.

Property	Description
LSB Weight	Returns the LSB weight in units of 100 fV/V per LSB for the channel. 100 fV is equal to 10^{-13} volts. Use this value to convert and calibrate NI 9236 d

	ata if you set the **Calibration Mode** to **Raw** in the C Series Module Properties dialog box.
Offset	Returns the calibration offset in units of 100 nV/V for the channel. Use this value to convert and calibrate NI 9236 data if you set the **Calibration Mode** to **Raw** in the **C Series Module Properties** dialog box.
Shunt Cal Enable	Controls the shunt calibration switch for each channel. Refer to the NI 9236 Getting Started VI in the `labview\examples\CompactRIO\Module Specific\NI 9236\NI 9236 Getting Started\NI 9236 Getting Started.lvproj` for an example of using the **Shunt Cal Enable** property.  Open example

Module Properties

Use the FPGA I/O Property Node to access the following module properties for this device.

Property	Description
Data Rate	Sets the rate at which the NI 9236 acquires data.
Module ID	Returns the module ID, 0x732B.
Serial Number	Returns the unique serial number of the module.
Vendor ID	Returns the NI vendor ID, 0x1093.

Single-Cycle Timed Loop

You can use the **Onboard Clock** channel in the single-cycle Timed Loop. You cannot use the other channels on the NI 9236 with the single-cycle Timed Loop. Refer to the Understanding Loop Timing (FPGA Interface) topic for information about loop timing for this module.

C Series Module Properties Dialog Box for the NI 9235/9236 (FPGA Interface)

Right-click an NI 9235 or NI 9236 C Series module in the **Project Explorer** window and select **Properties** from the shortcut menu to display this dialog box.

Use this dialog box to configure a C Series module.

This dialog box includes the following components:

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this option.
- **Location**—Specifies a slot in the chassis for the C Series module.
- **Calibration Mode**—Sets the calibration mode for the C Series module. Select **Calibrated** if you want the FPGA I/O Node to return calibrated, fixed-point data from the module in units of volts/volt. The fixed-point data is signed, with a word length of 24 bits and an integer word length of –4 bits. Select **Raw** if you want the FPGA I/O Node to return uncalibrated, binary data from the module. If you select **Raw**, you must convert and calibrate the analog input values in the host VI. The default is **Calibrated**.
- **Master Timebase Source**—Specifies the master timebase source that the module uses.
- **Export Onboard Clock**—Place a checkmark in this checkbox if you want to make this module accessible as a master timebase source to other modules.
- **Data Rate**—Specifies the rate at which the module acquires data.

NI 9236 (Scan Interface)

CompactRIO 8-Channel, 24-Bit Quarter-Bridge Analog Input Module


Open example

Module I/O Variables

To use I/O from this module in a VI, drag and drop I/O variables from the **Project Explorer** window to the block diagram of the VI. The I/O variables for the channels return calibrated floating-point data in volts/volts (channel voltage/excitation voltage).

Module Channels

The NI 9236 has the following channels.

Channel	Description
AI**x**	Analog input channel **x**, where **x** is the number of the channel. For the NI 9236, **x** is 0 to 7.

C Series Module Properties Dialog Box

Use this dialog box to configure the NI 9236. Right-click the NI 9236 in the **Project Explorer** window and select **Properties** to display this dialog box. You can configure the following options.

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this value.
- **Location**—Specifies a slot in the chassis for the C Series module.

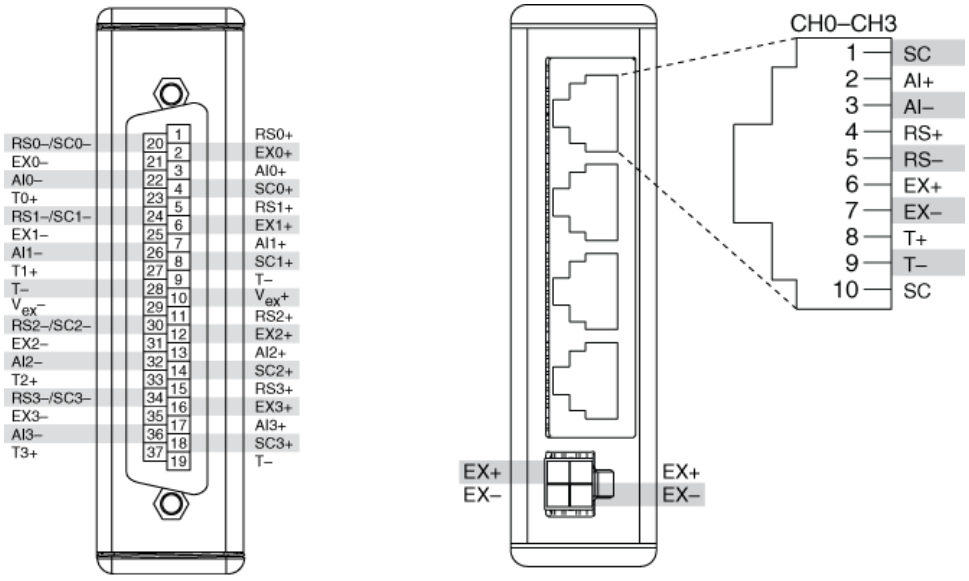
NI 9237

CompactRIO 4-Channel, 24-Bit Half/Full-Bridge Analog Input Module

Software Reference (?)

FPGA Interface | Scan Interface

NI 9237 Pinout



Related Topics

FPGA Interface
Converting and Calibrating CompactRIO Analog Input Values
Detecting Out-of-Range Channels
Acquiring Data from a Module (FPGA Interface)
Configuring the Master Timebase Source for a Module (FPGA Interface)
Configuring the Data Rate for a Module (FPGA Interface)
Synchronizing Multiple NI 9225/9227/9229/923x/924x/9251/9260 Modules
Understanding Loop Timing (FPGA Interface)

NI 9237 (FPGA Interface)

CompactRIO 4-Channel, 24-Bit Half/Full-Bridge Analog Input Module

Open example Find related examples

FPGA I/O Node

You can use an FPGA I/O Node, configured for reading, with this device.

Note You can synchronize an NI 9237 module with other modules that have a selectable timebase source.

Terminals in Software

Use the FPGA I/O Node to access the following terminals for this device.

Terminal	Description
AI**x**	Analog input channel **x**, where **x** is the number of the channel. The NI 9237 has AI channels 0 to 3. Do not access AI channels on multiple modules in the same FPGA I/O Node if the modules are not synchronized or do not use the same data rate.
Onboard Clock	12.8 MHz internal clock of the NI 9237. Use the FPGA I/O Node in a single-cycle Timed Loop to access this channel. You must export the Onboard Clock of the NI 9237 to access this channel.
Start	Channel that controls when the NI 9237 starts acquiring data. If TRUE is written to the **Start** channel, the NI 9237 starts acquiring data. When the NI 9237 is acquiring data, you must write TRUE to the **Stop** channel before you can access properties or TEDS information for the module. If FALSE is written to the **Start** channel, no operation is performed. Refer to the NI 9237 Getting Started VI in the `labview\examples\CompactRIO\Module Specific\NI 9237\NI 9237 Getting Started\NI 9237 Getting Started.lvproj` for an example of using the **Start** and **Stop** channels. Open example
Stop	Channel that controls when the NI 9237 stops acquiring data. If TRUE is written to the **Stop** channel, the NI 9237 stops acquiring data. When the NI 9237 is acquiring data, you must write TRUE t

	o the **Stop** channel before you can access prope rties or TEDS information for the module. If FAL SE is written to the **Stop** channel, no operation i s performed. Refer to the NI 9237 Getting Started VI in the `la bview\examples\CompactRIO\Module Specific\NI 9237\NI 9237 Getting Started\NI 9237 Getting Started.lvproj` for an example of using the **Start** and **Stop** channels.  Open example

Arbitration

This device supports only the Arbitrate if Multiple Requestors Only option for arbitration. You cannot configure arbitration settings for this device.

Methods

This device does not support any methods.

I/O Properties

Use the FPGA I/O Property Node to access the following I/O properties for this device.

Property	Description
Half-Bridge Enable	Controls the half-bridge completion option for e ach channel.
LSB Weight	Returns the LSB weight in units of 100 fV/V per L SB for the channel. 100 fV is equal to 10^{-13} volts. Use this value to convert and calibrate NI 9237 d ata if you set the **Calibration Mode** to **Raw** in the C Series Module Properties dialog box.
Offset	Returns the calibration offset in units of 10 nV/V for the channel. Use this value to convert and ca librate NI 9237 data if you set the **Calibration**

	Mode to **Raw** in the **C Series Module Properties** dialog box.
Offset Cal Enable	Enables offset calibration. This disconnects both signal input pins and forces the channel inputs to zero.
Shunt Cal Enable	Controls the shunt calibration switch for each channel.

Module Properties

Use the FPGA I/O Property Node to access the following module properties for this device.

Property	Description
Data Rate	Sets the rate at which the NI 9237 acquires data.
Excitation Voltage	Sets the excitation voltage level. All channels share the same excitation voltage.
Module ID	Returns the module ID, 0x73A4 (NI 9237 with DSUB) or 0x71C3 (NI 9237 with RJ-50).
Serial Number	Returns the unique serial number of the module.
Vendor ID	Returns the NI vendor ID, 0x1093.

Single-Cycle Timed Loop

You can use the **Onboard Clock** channel in the single-cycle Timed Loop. You cannot use the other channels on the NI 9237 with the single-cycle Timed Loop. Refer to the Understanding Loop Timing (FPGA Interface) topic for information about loop timing for this module.

C Series Module Properties Dialog Box for the NI 9237 (FPGA Interface)

Right-click an NI 9237 C Series module in the **Project Explorer** window and select **Properties** from the shortcut menu to display this dialog box.

Use this dialog box to configure a C Series module.

This dialog box includes the following components:

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this option.
- **Location**—Specifies a slot in the chassis for the C Series module.
- **Calibration Mode**—Sets the calibration mode for the C Series module. Select **Calibrated** if you want the FPGA I/O Node to return calibrated, fixed-point data from the module in units of volts/volt. The fixed-point data is signed, with a word length of 24 bits and an integer word length of –4 bits. Select **Raw** if you want the FPGA I/O Node to return uncalibrated, binary data from the module. If you select **Raw**, you must convert and calibrate the analog input values in the host VI. The default is **Calibrated**.
- **Master Timebase Source**—Specifies the master timebase source that the module uses.
- **Export Onboard Clock**—Place a checkmark in this checkbox if you want to make this module accessible as a master timebase source to other modules.
- **Data Rate**—Specifies the rate at which the module acquires data.
- **Enable TEDS Support**—Place a checkmark in this checkbox if you want to enable TEDS support in the FPGA and host VIs for this module.
- **Excitation Voltage**—Specifies the excitation voltage for the module to output to bridges, or specifies external excitation.
- **Enable Half-Bridge Completion**—Enables half-bridge completion for individual channels.

NI 9237 (Scan Interface)

CompactRIO 4-Channel, 24-Bit Half/Full-Bridge Analog Input Module

Open example

Module I/O Variables

To use I/O from this module in a VI, drag and drop I/O variables from the **Project Explorer** window to the block diagram of the VI. The I/O variables for the channels return calibrated floating-point data in volts/volts (channel voltage/excitation voltage).

Module Channels

The NI 9237 has the following channels.

Channel	Description
AI**x**	Analog input channel **x**, where **x** is the number of the channel. For the NI 9237, **x** is 0 to 3.

C Series Module Properties Dialog Box

Use this dialog box to configure the NI 9237. Right-click the NI 9237 in the **Project Explorer** window and select **Properties** to display this dialog box. You can configure the following options.

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this value.
- **Location**—Specifies a slot in the chassis for the C Series module.
- **Excitation Voltage**—Specifies the excitation voltage for the module to output to bridges, or specifies external excitation.
- **Enable Half-Bridge Completion**—Enables half-bridge completion for individual channels.

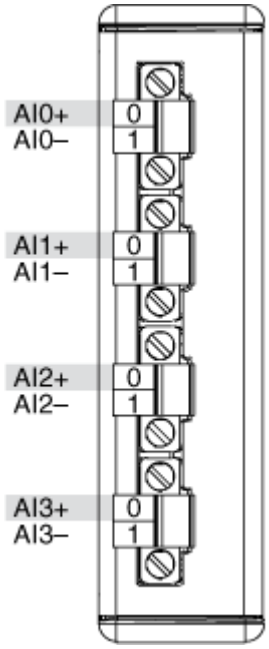
NI 9238

CompactRIO 4-Channel, ±0.5 V, 24-Bit Simultaneous Analog Input Module

Software Reference (?)

FPGA Interface

NI 9238 Pinout



Related Topics

FPGA Interface
Converting and Calibrating CompactRIO Analog Input Values
Detecting Out-of-Range Channels
Acquiring Data from a Module (FPGA Interface)
Configuring the Master Timebase Source for a Module (FPGA Interface)
Configuring the Data Rate for a Module (FPGA Interface)
Synchronizing Multiple NI 9225/9227/9229/923x/924x/9251/9260 Modules
Understanding Loop Timing (FPGA Interface)

NI 9238 (FPGA Interface)

CompactRIO 4-Channel, ±0.5 V, 24-Bit Simultaneous Analog Input Module

Open example

Find related examples

FPGA I/O Node

You can use an FPGA I/O Node, configured for reading, with this device.

Note You can simultaneously read from or write to multiple channels on the NI 9238. You can also synchronize an NI 9238 module with other modules that have a selectable timebase source.

Terminals in Software

Use the FPGA I/O Node to access the following terminals for this device.

Terminal	Description
AI**x**	Analog input channel **x**, where **x** is the number of the channel. The NI 9238 has AI channels 0 to 3. Do not access AI channels on multiple modules in the same FPGA I/O Node if the modules are not synchronized or do not use the same data rate.
Onboard Clock	Gives access to the onboard clock in the LabVIEW block diagram. The Onboard Clock frequency is 12.8 MHz. Use the FPGA I/O Node in a single-cycle Timed Loop to access this channel. You must export the Onboard Clock of the NI 9238 to access this channel.
Start	Channel that controls when the NI 9238 starts acquiring data. If TRUE is written to the **Start** channel, the NI 9238 starts acquiring data. When the NI 9238 is acquiring data, you must write TRUE to the **Stop** channel before you can access properties for the module. If FALSE is written to the **Start** channel, no operation is performed.
Stop	Channel that controls when the NI 9238 stops acquiring data. If TRUE is written to the **Stop** channel, the NI 9238 stops acquiring data. When the NI 9238 is acquiring data, you must write TRUE to the **Stop** channel before you can access prope

	rties for the module. If FALSE is written to the **Stop** channel, no operation is performed.

Arbitration

This device supports only the Arbitrate if Multiple Requestors Only option for arbitration. You cannot configure arbitration settings for this device.

Methods

This device does not support any methods.

I/O Properties

Use the FPGA I/O Property Node to access the following I/O properties for this device.

Property	Description
LSB Weight	Returns the LSB weight in fV/LSB for the channel. Use this value to convert and calibrate NI 9238 data if you set the **Calibration Mode** to **Raw** in the C Series Module Properties dialog box.
Offset	Returns the calibration offset in nV for the channel. Use this value to convert and calibrate NI 9238 data if you set the **Calibration Mode** to **Raw** in the **C Series Module Properties** dialog box.

Module Properties

Use the FPGA I/O Property Node to access the following module properties for this device.

Property	Description
Data Rate	Sets the rate at which the NI 9238 acquires data.
Module ID	Returns the module ID, 0x7750.
Serial Number	Returns the unique serial number of the module.
Vendor ID	Returns the NI vendor ID, 0x1093.

Single-Cycle Timed Loop

You can use the **Onboard Clock** channel in the single-cycle Timed Loop. You cannot use the other channels on the NI 9238 with the single-cycle Timed Loop. Refer to the Understanding Loop Timing (FPGA Interface) topic for information about loop timing for this module.

C Series Module Properties Dialog Box for the NI 9225/9227/9229/9238/9239/9246/9247 (FPGA Interface)

Right-click an NI 9225/NI 9227/NI 9229/NI 9238/NI 9239/NI 9246/NI 9247 C Series module in the **Project Explorer** window and select **Properties** from the shortcut menu to display this dialog box.

Use this dialog box to configure a C Series module.

This dialog box includes the following components:

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this option.
- **Location**—Specifies a slot in the chassis for the C Series module.
- **Calibration Mode**—Sets the calibration mode for the C Series module.
  - Select **Calibrated**, which is the default, if you want the FPGA I/O Node to return calibrated, signed, fixed-point data from the module. The following table describes the units and integer word length of the returned data:

Module	Units	Word Length (bits)	Integer Word Length (bits)
NI 9225	V	24	10
NI 9227	A	24	5
NI 9229	V	24	7

NI 9238	V	24	1
NI 9239	V	24	5
NI 9246	A	24	7
NI 9247	A	24	9

  - Select **Raw** if you want the FPGA I/O Node to return uncalibrated, binary data from the module. If you select **Raw**, you must convert and calibrate the analog input values in the host VI.

- **Master Timebase Source**—Specifies the master timebase source that the module uses.
- **Export Onboard Clock**—Place a checkmark in this checkbox if you want to make this module accessible as a master timebase source to other modules.
- **Data Rate**—Specifies the rate at which the module acquires data.

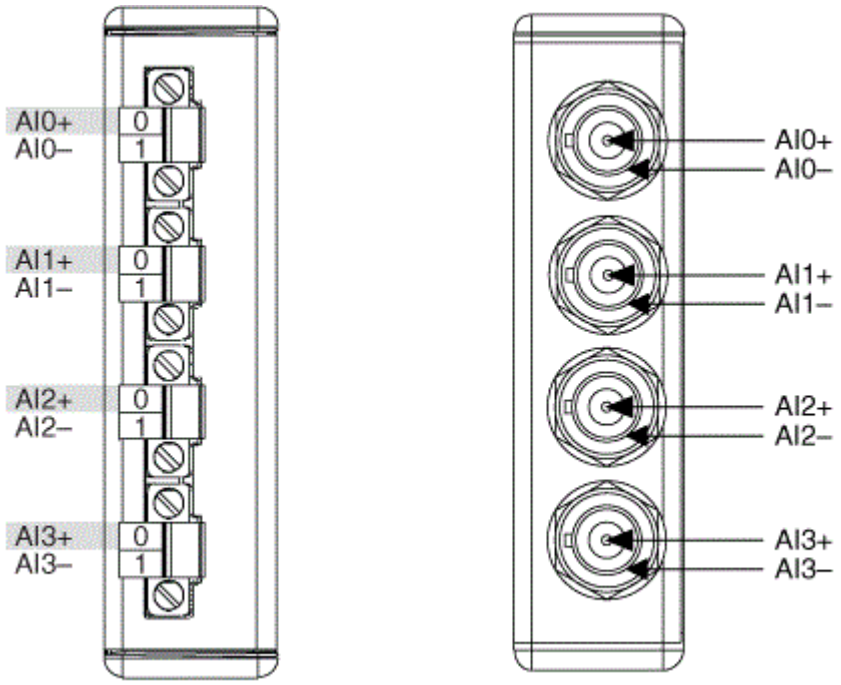
NI 9239

CompactRIO 4-Channel, ±10 V, 24-Bit Simultaneous Analog Input Module

Software Reference (?)

FPGA Interface | Scan Interface

NI 9239 Pinout



Related Topics

FPGA Interface
Converting and Calibrating CompactRIO Analog Input Values
Detecting Out-of-Range Channels
Acquiring Data from a Module (FPGA Interface)
Configuring the Master Timebase Source for a Module (FPGA Interface)
Configuring the Data Rate for a Module (FPGA Interface)
Synchronizing Multiple NI 9225/9227/9229/923x/924x/9251/9260 Modules
Understanding Loop Timing (FPGA Interface)

NI 9239 (FPGA Interface)

CompactRIO 4-Channel, ±10 V, 24-Bit Simultaneous Analog Input Module

Open example Find related examples

FPGA I/O Node

You can use an FPGA I/O Node, configured for reading, with this device.

Note You can simultaneously read from or write to multiple channels on the NI 9239. You also can synchronize an NI 9239 module with other modules that have a selectable timebase source.

Terminals in Software

Use the FPGA I/O Node to access the following terminals for this device.

Terminal	Description
AI**x**	Analog input channel **x**, where **x** is the number of the channel. The NI 9239 has AI channels 0 to 3. Do not access AI channels on multiple modules in the same FPGA I/O Node if the modules are not synchronized or do not use the same data rate.
Onboard Clock	Gives access to the onboard clock in the LabVIEW block diagram. The Onboard Clock frequency is 12.8 MHz. Use the FPGA I/O Node in a single-cycle Timed Loop to access this channel. You must export the Onboard Clock of the NI 9239 to access this channel.
Start	Channel that controls when the NI 9239 starts acquiring data. If TRUE is written to the **Start** channel, the NI 9239 starts acquiring data. When the NI 9239 is acquiring data, you must write TRUE to the **Stop** channel before you can access properties for the module. If FALSE is written to the **Start** channel, no operation is performed. Refer to the NI 9239 Getting Started VI in the `labview\examples\CompactRIO\Module Specific\NI 9239\NI 9239 Getting Started\NI 9239 Getting Started.lvproj` for an example of using the **Start** and **Stop** channels. Open example

Stop	Channel that controls when the NI 9239 stops acquiring data. If TRUE is written to the **Stop** channel, the NI 9239 stops acquiring data. When the NI 9239 is acquiring data, you must write TRUE to the **Stop** channel before you can access properties for the module. If FALSE is written to the **Stop** channel, no operation is performed. Refer to the NI 9239 Getting Started VI in the `labview\examples\CompactRIO\Module Specific\NI 9239\NI 9239 Getting Started\NI 9239 Getting Started.lvproj` for an example of using the **Start** and **Stop** channels.  Open example

Arbitration

This device supports only the Arbitrate if Multiple Requestors Only option for arbitration. You cannot configure arbitration settings for this device.

Methods

This device does not support any methods.

I/O Properties

Use the FPGA I/O Property Node to access the following I/O properties for this device.

Property	Description
LSB Weight	Returns the LSB weight in pV/LSB for the channel. Use this value to convert and calibrate NI 9239 data if you set the **Calibration Mode** to **Raw** in the C Series Module Properties dialog box.
Offset	Returns the calibration offset in nV for the channel. Use this value to convert and calibrate NI 9239 data if you set the **Calibration Mode** to **Ra**

	w in the **C Series Module Properties** dialog box.

Module Properties

Use the FPGA I/O Property Node to access the following module properties for this device.

Property	Description
Data Rate	Sets the rate at which the NI 9239 acquires data.
Module ID	Returns the module ID, 0x71C2.
Serial Number	Returns the unique serial number of the module.
Vendor ID	Returns the NI vendor ID, 0x1093.

Single-Cycle Timed Loop

You can use the **Onboard Clock** channel in the single-cycle Timed Loop. You cannot use the other channels on the NI 9239 with the single-cycle Timed Loop. Refer to the Understanding Loop Timing (FPGA Interface) topic for information about loop timing for this module.

C Series Module Properties Dialog Box for the NI 9225/9227/9229/9238/9239/9246/9247 (FPGA Interface)

Right-click an NI 9225/NI 9227/NI 9229/NI 9238/NI 9239/NI 9246/NI 9247 C Series module in the **Project Explorer** window and select **Properties** from the shortcut menu to display this dialog box.

Use this dialog box to configure a C Series module.

This dialog box includes the following components:

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.

- **Module Type**—Specifies the type of C Series module. You cannot change this option.
- **Location**—Specifies a slot in the chassis for the C Series module.
- **Calibration Mode**—Sets the calibration mode for the C Series module.
  - Select **Calibrated**, which is the default, if you want the FPGA I/O Node to return calibrated, signed, fixed-point data from the module. The following table describes the units and integer word length of the returned data:

Module	Units	Word Length (bits)	Integer Word Length (bits)
NI 9225	V	24	10
NI 9227	A	24	5
NI 9229	V	24	7
NI 9238	V	24	1
NI 9239	V	24	5
NI 9246	A	24	7
NI 9247	A	24	9

  - Select **Raw** if you want the FPGA I/O Node to return uncalibrated, binary data from the module. If you select **Raw**, you must convert and calibrate the analog input values in the host VI.
- **Master Timebase Source**—Specifies the master timebase source that the module uses.
- **Export Onboard Clock**—Place a checkmark in this checkbox if you want to make this module accessible as a master timebase source to other modules.
- **Data Rate**—Specifies the rate at which the module acquires data.

NI 9239 (Scan Interface)

CompactRIO 4-Channel, ±10 V, 24-Bit Simultaneous Analog Input Module

 Open example

Module I/O Variables

To use I/O from this module in a VI, drag and drop I/O variables from the **Project Explorer** window to the block diagram of the VI. The I/O variables for the channels return calibrated floating-point data in volts.

Module Channels

The NI 9239 has the following channels.

Channel	Description
AI**x**	Analog input channel **x**, where **x** is the number of the channel. For the NI 9239, **x** is 0 to 3.

C Series Module Properties Dialog Box

Use this dialog box to configure the NI 9239. Right-click the NI 9239 in the **Project Explorer** window and select **Properties** to display this dialog box. You can configure the following options.

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this value.
- **Location**—Specifies a slot in the chassis for the C Series module.

Hardware Documentation

Refer to the NI 9239 hardware documentation on ni.com/manuals for information about module specifications and how to use the module. Refer to the CompactRIO Related Documentation topic for additional CompactRIO documentation resources.

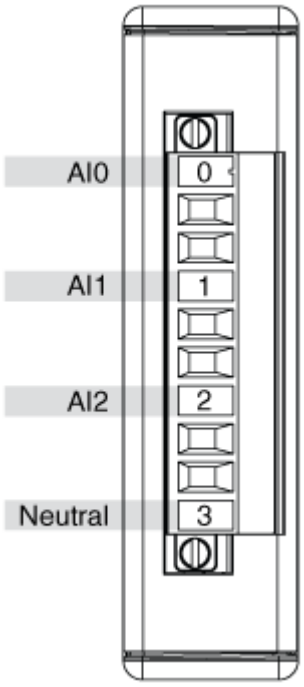
NI 9242

CompactRIO 4-Channel, 250 V_{rms}, 24-Bit Simultaneous Analog Input Module

Software Reference (?)

FPGA Interface

NI 9242 Pinout



Related Topics

FPGA Interface
Detecting Out-of-Range Channels
Acquiring Data from a Module (FPGA Interface)
Configuring the Master Timebase Source for a Module (FPGA Interface)
Configuring the Data Rate for a Module (FPGA Interface)
Converting NI 9242 and NI 9244 Data
Synchronizing Multiple NI 9225/9227/9229/923x/924x/9251/9260 Modules
Understanding Loop Timing (FPGA Interface)

NI 9242 (FPGA Interface)

CompactRIO 4-Channel, 250 V_{rms}, 24-Bit Simultaneous Analog Input Module

FPGA I/O Node

You can use an FPGA I/O Node, configured for reading, with this device.

Note You can simultaneously read from or write to multiple channels on the NI 9242. You can also synchronize an NI 9242 module with other modules that have a selectable timebase source.

Terminals in Software

Use the FPGA I/O Node to access the following terminals for this device.

Terminal	Description
AI**x**	Analog input channel **x**, where **x** is the number of the channel. The NI 9242 has AI channels 0 to 2. Do not access AI channels on multiple modules in the same FPGA I/O Node if the modules are not synchronized or do not use the same data rate.
Neutral	Neutral input channel. Do not access Neutral channels on multiple modules in the same FPGA I/O Node if the modules are not synchronized or do not use the same data rate.
Onboard Clock	Gives access to the onboard clock in the LabVIEW block diagram. The Onboard Clock frequency is 12.8 MHz. Use the FPGA I/O Node in a single-cycle Timed Loop to access this channel. You must export the Onboard Clock of the NI 9242 to access this channel.
Start	Channel that controls when the NI 9242 starts acquiring data. If TRUE is written to the **Start** channel, the NI 9242 starts acquiring data. When the NI 9242 is acquiring data, you must write TRUE to the **Stop** channel before you can access properties for the module. If FALSE is written to the **Start** channel, no operation is performed.
Stop	Channel that controls when the NI 9242 stops acquiring data. If TRUE is written to the **Stop** chan

	nel, the NI 9242 stops acquiring data. When the NI 9242 is acquiring data, you must write TRUE t o the **Stop** channel before you can access prope rties for the module. If FALSE is written to the **St op** channel, no operation is performed.

Arbitration

This device supports only the Arbitrate if Multiple Requestors Only option for arbitration. You cannot configure arbitration settings for this device.

Methods

This device does not support any methods.

I/O Properties

This device does not support any I/O properties.

Module Properties

Use the FPGA I/O Property Node to access the following module properties for this device.

Property	Description
Data Rate	Sets the rate at which the NI 9242 acquires data.
Module ID	Returns the module ID, 0x772A.
Serial Number	Returns the unique serial number of the module .
Vendor ID	Returns the NI vendor ID, 0x1093.

Single-Cycle Timed Loop

You can use the **Onboard Clock** channel in the single-cycle Timed Loop. You cannot use the other channels on the NI 9242 with the single-cycle Timed Loop. Refer to the Understanding Loop Timing (FPGA Interface) topic for information about loop timing for this module.

C Series Module Properties Dialog Box for the NI 9242/9244 (FPGA Interface)

Right-click an NI 9242 or NI 9244 C Series module in the **Project Explorer** window and select **Properties** from the shortcut menu to display this dialog box.

Use this dialog box to configure a C Series module.

This dialog box includes the following components:

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this option.
- **Location**—Specifies a slot in the chassis for the C Series module.
- **Calibration Mode**—Sets the calibration mode for the C Series module. Select **Calibrated** if you want the FPGA I/O Node to return calibrated, fixed-point data from the module in units of volts. The fixed-point data is signed, with a word length of 24 bits and an integer word length of 10 bits. Select **Raw** if you want the FPGA I/O Node to return calibrated, binary data from the module. If you select **Raw**, you must scale the analog input values in the host VI. The default is **Calibrated**.
- **Master Timebase Source**—Specifies the master timebase source that the module uses.
- **Export Onboard Clock**—Place a checkmark in this checkbox if you want to make this module accessible as a master timebase source to other modules.
- **Data Rate**—Specifies the rate at which the module acquires data.

Converting NI 9242 and NI 9244 Data (FPGA Interface)

Set the **Calibration Mode** to **Calibrated** in the C Series Module Properties dialog box for the NI 9242 and the NI 9244 if you want the FPGA I/O Node to return calibrated, fixed-point data from the module. Set the **Calibration Mode** to **Raw** if you want the FPGA I/O Node to return calibrated, binary data from the module. If

you set the **Calibration Mode** to **Raw**, you must convert the binary values to engineering units. You must convert these values in the host VI.

You can use the following equations in the host VI to convert binary voltage values to volts:

NI 9242

Volts = **Binary Value** × 500 V ÷ 8,388,607

where	**Binary Value** is the value returned by the FPGA I/O Node.

NI 9244

Volts = **Binary Value** × 997.5 V ÷ 8,388,607

where	**Binary Value** is the value returned by the FPGA I/O Node.

NI 9242 (Scan Interface)

CompactRIO 4-Channel, 250 V_{rms}, 24-Bit Simultaneous Analog Input Module

Module I/O Variables

To use I/O from this module in a VI, drag and drop I/O variables from the **Project Explorer** window to the block diagram of the VI. The I/O variables for the channels return calibrated floating-point data in volts.

Module Channels

The NI 9242 has the following channels.

Channel	Description
AI**x**	Analog input channel **x**, where **x** is the number of the channel. The NI 9242 has AI channels 0 to 2.

C Series Module Properties Dialog Box

Use this dialog box to configure the NI 9242. Right-click the NI 9242 in the **Project Explorer** window and select **Properties** to display this dialog box. You can configure the following options.

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this value.
- **Location**—Specifies a slot in the chassis for the C Series module.
- **Data Rate**—Specifies the rate at which the NI 9242 acquires and returns data. The data rate must remain within the appropriate data rate range listed in the NI 9242 hardware documentation on ni.com/manuals.

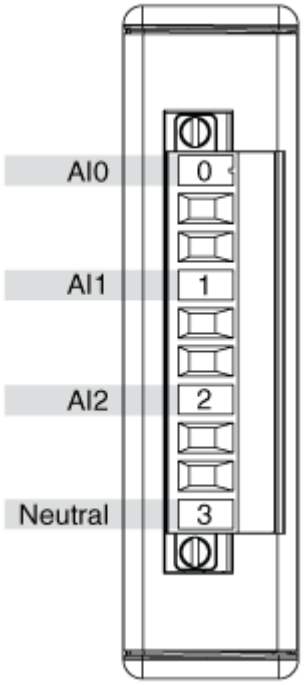
NI 9244

CompactRIO 4-Channel, 400 V_{rms} L-N, 800 V_{rms} L-L, 24-Bit Simultaneous Analog Input Module

Software Reference (?)

FPGA Interface

NI 9244 Pinout



Related Topics

FPGA Interface
Detecting Out-of-Range Channels
Acquiring Data from a Module (FPGA Interface)
Configuring the Master Timebase Source for a Module (FPGA Interface)
Configuring the Data Rate for a Module (FPGA Interface)
Converting NI 9242 and NI 9244 Data
Synchronizing Multiple NI 9225/9227/9229/923x/924x/9251/9260 Modules
Understanding Loop Timing (FPGA Interface)

NI 9244 (FPGA Interface)

CompactRIO 4-Channel, 400 V_{rms} L-N, 800 V_{rms} L-L, 24-Bit Simultaneous Analog Input Module

FPGA I/O Node

You can use an FPGA I/O Node, configured for reading, with this device.

Note You can simultaneously read from or write to multiple channels on the NI 9244. You can also synchronize an NI 9244 module with other modules that have a selectable timebase source.

Terminals in Software

Use the FPGA I/O Node to access the following terminals for this device.

Terminal	Description
AI**x**	Analog input channel **x**, where **x** is the number of the channel. The NI 9244 has AI channels 0 to 2. Do not access AI channels on multiple modules in the same FPGA I/O Node if the modules are not synchronized or do not use the same data rate.
Neutral	Neutral input channel. Do not access Neutral channels on multiple modules in the same FPGA I/O Node if the modules are not synchronized or do not use the same data rate.
Onboard Clock	Gives access to the onboard clock in the LabVIEW block diagram. The Onboard Clock frequency is 12.8 MHz. Use the FPGA I/O Node in a single-cycle Timed Loop to access this channel. You must export the Onboard Clock of the NI 9244 to access this channel.
Start	Channel that controls when the NI 9244 starts acquiring data. If TRUE is written to the **Start** channel, the NI 9244 starts acquiring data. When the NI 9244 is acquiring data, you must write TRUE to the **Stop** channel before you can access properties for the module. If FALSE is written to the **Start** channel, no operation is performed.
Stop	Channel that controls when the NI 9244 stops acquiring data. If TRUE is written to the **Stop** chan

	nel, the NI 9244 stops acquiring data. When the NI 9244 is acquiring data, you must write TRUE t o the **Stop** channel before you can access prope rties for the module. If FALSE is written to the **St op** channel, no operation is performed.

Arbitration

This device supports only the Arbitrate if Multiple Requestors Only option for arbitration. You cannot configure arbitration settings for this device.

Methods

This device does not support any methods.

I/O Properties

This device does not support any I/O properties.

Module Properties

Use the FPGA I/O Property Node to access the following module properties for this device.

Property	Description
Data Rate	Sets the rate at which the NI 9244 acquires data.
Module ID	Returns the module ID, 0x76E8.
Serial Number	Returns the unique serial number of the module .
Vendor ID	Returns the NI vendor ID, 0x1093.

Single-Cycle Timed Loop

You can use the **Onboard Clock** channel in the single-cycle Timed Loop. You cannot use the other channels on the NI 9244 with the single-cycle Timed Loop. Refer to the Understanding Loop Timing (FPGA Interface) topic for information about loop timing for this module.

C Series Module Properties Dialog Box for the NI 9242/9244 (FPGA Interface)

Right-click an NI 9242 or NI 9244 C Series module in the **Project Explorer** window and select **Properties** from the shortcut menu to display this dialog box.

Use this dialog box to configure a C Series module.

This dialog box includes the following components:

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this option.
- **Location**—Specifies a slot in the chassis for the C Series module.
- **Calibration Mode**—Sets the calibration mode for the C Series module. Select **Calibrated** if you want the FPGA I/O Node to return calibrated, fixed-point data from the module in units of volts. The fixed-point data is signed, with a word length of 24 bits and an integer word length of 10 bits. Select **Raw** if you want the FPGA I/O Node to return calibrated, binary data from the module. If you select **Raw**, you must scale the analog input values in the host VI. The default is **Calibrated**.
- **Master Timebase Source**—Specifies the master timebase source that the module uses.
- **Export Onboard Clock**—Place a checkmark in this checkbox if you want to make this module accessible as a master timebase source to other modules.
- **Data Rate**—Specifies the rate at which the module acquires data.

Converting NI 9242 and NI 9244 Data (FPGA Interface)

Set the **Calibration Mode** to **Calibrated** in the C Series Module Properties dialog box for the NI 9242 and the NI 9244 if you want the FPGA I/O Node to return calibrated, fixed-point data from the module. Set the **Calibration Mode** to **Raw** if you want the FPGA I/O Node to return calibrated, binary data from the module. If

you set the **Calibration Mode** to **Raw**, you must convert the binary values to engineering units. You must convert these values in the host VI.

You can use the following equations in the host VI to convert binary voltage values to volts:

NI 9242

Volts = **Binary Value** × 500 V ÷ 8,388,607

where	**Binary Value** is the value returned by the FPGA I/O Node.

NI 9244

Volts = **Binary Value** × 997.5 V ÷ 8,388,607

where	**Binary Value** is the value returned by the FPGA I/O Node.

NI 9244 (Scan Interface)

CompactRIO 4-Channel, 400 V_{rms} L-N, 800 V_{rms} L-L, 24-Bit Simultaneous Analog Input Module

Module I/O Variables

To use I/O from this module in a VI, drag and drop I/O variables from the **Project Explorer** window to the block diagram of the VI. The I/O variables for the channels return calibrated floating-point data in volts.

Module Channels

The NI 9244 has the following channels.

Channel	Description
AI**x**	Analog input channel **x**, where **x** is the number of the channel. The NI 9244 has AI channels 0 to 2.

C Series Module Properties Dialog Box

Use this dialog box to configure the NI 9244. Right-click the NI 9244 in the **Project Explorer** window and select **Properties** to display this dialog box. You can configure the following options.

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this value.
- **Location**—Specifies a slot in the chassis for the C Series module.
- **Data Rate**—Specifies the rate at which the NI 9244 acquires and returns data. The data rate must remain within the appropriate data rate range listed in the NI 9244 hardware documentation on ni.com/manuals.

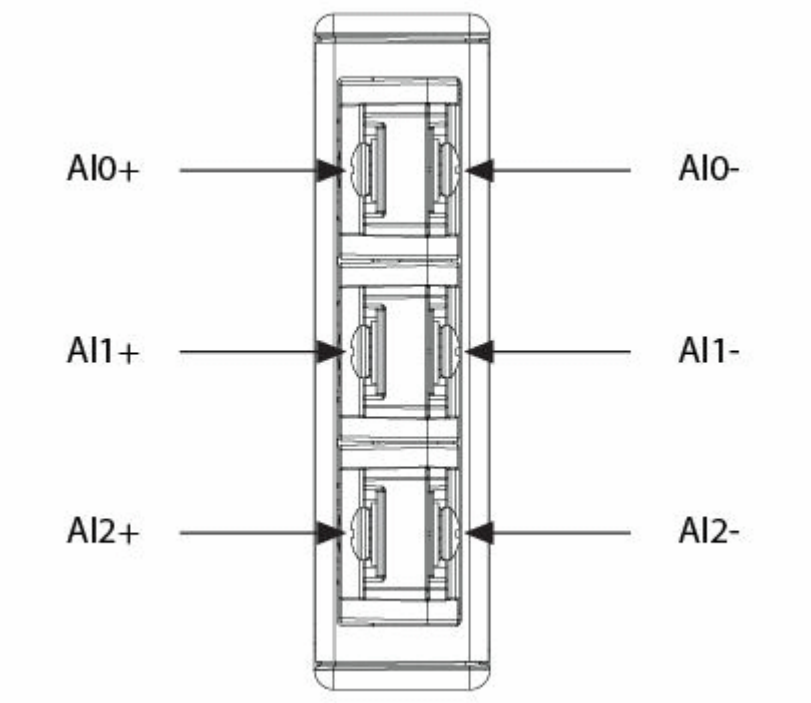
NI 9246

CompactRIO 3-Channel, 20 A_{rms} Continuous, 24-Bit, Analog Input Module

Software Reference (?)

FPGA Interface

NI 9246 Pinout



Related Topics

FPGA Interface
Converting and Calibrating CompactRIO Analog Input Values
Detecting Out-of-Range Channels
Acquiring Data from a Module (FPGA Interface)
Configuring the Master Timebase Source for a Module (FPGA Interface)
Configuring the Data Rate for a Module (FPGA Interface)
Synchronizing Multiple NI 9225/9227/9229/923x/924x/9251/9260 Modules
Understanding Loop Timing (FPGA Interface)

NI 9246 (FPGA Interface)

CompactRIO 3-Channel, 20 A_{rms} Continuous, 24-Bit, Analog Input Module

Open example

Find related examples

FPGA I/O Node

You can use an FPGA I/O Node, configured for reading, with this device.

Note You can simultaneously read from or write to multiple channels on the NI 9246. You can also synchronize an NI 9246 module with other modules that have a selectable timebase source.

Terminals in Software

Use the FPGA I/O Node to access the following terminals for this device.

Terminal	Description
AI**x**	Analog input channel **x**, where **x** is the number of the channel. The NI 9246 has AI channels 0 to 2. Do not access AI channels on multiple modules in the same FPGA I/O Node if the modules are not synchronized or do not use the same data rate.
Onboard Clock	Gives access to the onboard clock in the LabVIEW block diagram. The Onboard Clock frequency is 13.1 MHz. Use the FPGA I/O Node in a single-cycle Timed Loop to access this channel. You must export the Onboard Clock of the NI 9246 to access this channel.
Start	Channel that controls when the NI 9246 starts acquiring data. If TRUE is written to the **Start** channel, the NI 9246 starts acquiring data. When the NI 9246 is acquiring data, you must write TRUE to the **Stop** channel before you can access properties for the module. If FALSE is written to the **Start** channel, no operation is performed. Refer to the NI 9246 Getting Started VI in the `labview\examples\CompactRIO\Module Specific\NI 9246\NI 9246 Getting Started\NI 9246 Getting Started.lvproj` for an example of using the **Start** and

	Stop channels. Open example
Stop	Channel that controls when the NI 9246 stops acquiring data. If TRUE is written to the **Stop** channel, the NI 9246 stops acquiring data. When the NI 9246 is acquiring data, you must write TRUE to the **Stop** channel before you can access properties for the module. If FALSE is written to the **Stop** channel, no operation is performed. Refer to the NI 9246 Getting Started VI in the `labview\examples\CompactRIO\Module Specific\NI 9246\NI 9246 Getting Started\NI 9246 Getting Started.lvproj` for an example of using the **Start** and **Stop** channels. Open example

Arbitration

This device supports only the Arbitrate if Multiple Requestors Only option for arbitration. You cannot configure arbitration settings for this device.

Methods

This device does not support any methods.

I/O Properties

Use the FPGA I/O Property Node to access the following I/O properties for this device.

Property	Description
LSB Weight	Returns the LSB weight in pV/LSB for the channel. Use this value to convert and calibrate NI 9246 data if you set the **Calibration Mode** to **Raw** in the C Series Module Properties dialog box.

Offset	Returns the calibration offset in µV for the channel. Use this value to convert and calibrate NI 9246 data if you set the **Calibration Mode** to **Raw** in the **C Series Module Properties** dialog box.

Module Properties

Use the FPGA I/O Property Node to access the following module properties for this device.

Property	Description
Data Rate	Sets the rate at which the NI 9246 acquires data.
Module ID	Returns the module ID, 0x77E3.
Serial Number	Returns the unique serial number of the module.
Vendor ID	Returns the NI vendor ID, 0x1093.

Single-Cycle Timed Loop

You can use the **Onboard Clock** channel in the single-cycle Timed Loop. You cannot use the other channels on the NI 9246 with the single-cycle Timed Loop. Refer to the Understanding Loop Timing (FPGA Interface) topic for information about loop timing for this module.

C Series Module Properties Dialog Box for the NI 9225/9227/9229/9238/9239/9246/9247 (FPGA Interface)

Right-click an NI 9225/NI 9227/NI 9229/NI 9238/NI 9239/NI 9246/NI 9247 C Series module in the **Project Explorer** window and select **Properties** from the shortcut menu to display this dialog box.

Use this dialog box to configure a C Series module.

This dialog box includes the following components:

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module

based on the slot number. You can use this field to give the module a descriptive name.

- **Module Type**—Specifies the type of C Series module. You cannot change this option.
- **Location**—Specifies a slot in the chassis for the C Series module.
- **Calibration Mode**—Sets the calibration mode for the C Series module.
  - Select **Calibrated**, which is the default, if you want the FPGA I/O Node to return calibrated, signed, fixed-point data from the module. The following table describes the units and integer word length of the returned data:

Module	Units	Word Length (bits)	Integer Word Length (bits)
NI 9225	V	24	10
NI 9227	A	24	5
NI 9229	V	24	7
NI 9238	V	24	1
NI 9239	V	24	5
NI 9246	A	24	7
NI 9247	A	24	9

  - Select **Raw** if you want the FPGA I/O Node to return uncalibrated, binary data from the module. If you select **Raw**, you must convert and calibrate the analog input values in the host VI.
- **Master Timebase Source**—Specifies the master timebase source that the module uses.
- **Export Onboard Clock**—Place a checkmark in this checkbox if you want to make this module accessible as a master timebase source to other modules.
- **Data Rate**—Specifies the rate at which the module acquires data.

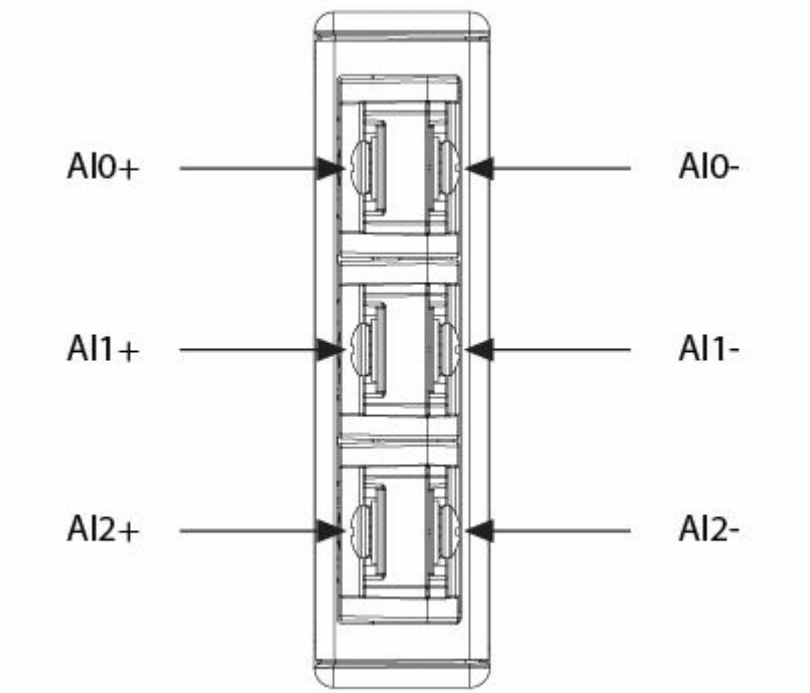
NI 9247

CompactRIO 3-Channel, 50 A_{rms} Continuous, 24-Bit, Analog Input Module

Software Reference (?)

FPGA Interface

NI 9247 Pinout



Related Topics

FPGA Interface
Converting and Calibrating CompactRIO Analog Input Values
Detecting Out-of-Range Channels
Acquiring Data from a Module (FPGA Interface)
Configuring the Master Timebase Source for a Module (FPGA Interface)
Configuring the Data Rate for a Module (FPGA Interface)
Synchronizing Multiple NI 9225/9227/9229/923x/924x/9251/9260 Modules
Understanding Loop Timing (FPGA Interface)

NI 9247 (FPGA Interface)

CompactRIO 3-Channel, 50 A_{rms} Continuous, 24-Bit, Analog Input Module

Open example

Find related examples

FPGA I/O Node

You can use an FPGA I/O Node, configured for reading, with this device.

Note You can simultaneously read from or write to multiple channels on the NI 9247. You can also synchronize an NI 9247 module with other modules that have a selectable timebase source.

Terminals in Software

Use the FPGA I/O Node to access the following terminals for this device.

Terminal	Description
AI**x**	Analog input channel **x**, where **x** is the number of the channel. The NI 9247 has AI channels 0 to 2. Do not access AI channels on multiple modules in the same FPGA I/O Node if the modules are not synchronized or do not use the same data rate.
Onboard Clock	Gives access to the onboard clock in the LabVIEW block diagram. The Onboard Clock frequency is 13.1 MHz. Use the FPGA I/O Node in a single-cycle Timed Loop to access this channel. You must export the Onboard Clock of the NI 9247 to access this channel.
Start	Channel that controls when the NI 9247 starts acquiring data. If TRUE is written to the **Start** channel, the NI 9247 starts acquiring data. When the NI 9247 is acquiring data, you must write TRUE to the **Stop** channel before you can access properties for the module. If FALSE is written to the **Start** channel, no operation is performed. Refer to the NI 9247 Getting Started VI in the `labview\examples\CompactRIO\Module Specific\NI 9247\NI 9247 Getting Started\NI 9247 Getting Started.`

	lvproj for an example of using the **Start** and **Stop** channels. Open example
Stop	Channel that controls when the NI 9247 stops acquiring data. If TRUE is written to the **Stop** channel, the NI 9247 stops acquiring data. When the NI 9247 is acquiring data, you must write TRUE to the **Stop** channel before you can access properties for the module. If FALSE is written to the **Stop** channel, no operation is performed. Refer to the NI 9247 Getting Started VI in the labview\examples\CompactRIO\Module Specific\NI 9247\NI 9247 Getting Started\NI 9247 Getting Started.lvproj for an example of using the **Start** and **Stop** channels. Open example

Arbitration

This device supports only the Arbitrate if Multiple Requestors Only option for arbitration. You cannot configure arbitration settings for this device.

Methods

This device does not support any methods.

I/O Properties

Use the FPGA I/O Property Node to access the following I/O properties for this device.

Property	Description
LSB Weight	Returns the LSB weight in pV/LSB for the channel. Use this value to convert and calibrate NI 9247

	data if you set the **Calibration Mode** to **Raw** in the C Series Module Properties dialog box.
Offset	Returns the calibration offset in µV for the channel. Use this value to convert and calibrate NI 9247 data if you set the **Calibration Mode** to **Raw** in the **C Series Module Properties** dialog box.

Module Properties

Use the FPGA I/O Property Node to access the following module properties for this device.

Property	Description
Data Rate	Sets the rate at which the NI 9247 acquires data.
Module ID	Returns the module ID, 0x77B8.
Serial Number	Returns the unique serial number of the module.
Vendor ID	Returns the NI vendor ID, 0x1093.

Single-Cycle Timed Loop

You can use the **Onboard Clock** channel in the single-cycle Timed Loop. You cannot use the other channels on the NI 9247 with the single-cycle Timed Loop. Refer to the Understanding Loop Timing (FPGA Interface) topic for information about loop timing for this module.

C Series Module Properties Dialog Box for the NI 9225/9227/9229/9238/9239/9246/9247 (FPGA Interface)

Right-click an NI 9225/NI 9227/NI 9229/NI 9238/NI 9239/NI 9246/NI 9247 C Series module in the **Project Explorer** window and select **Properties** from the shortcut menu to display this dialog box.

Use this dialog box to configure a C Series module.

This dialog box includes the following components:

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this option.
- **Location**—Specifies a slot in the chassis for the C Series module.
- **Calibration Mode**—Sets the calibration mode for the C Series module.
  - Select **Calibrated**, which is the default, if you want the FPGA I/O Node to return calibrated, signed, fixed-point data from the module. The following table describes the units and integer word length of the returned data:

Module	Units	Word Length (bits)	Integer Word Length (bits)
NI 9225	V	24	10
NI 9227	A	24	5
NI 9229	V	24	7
NI 9238	V	24	1
NI 9239	V	24	5
NI 9246	A	24	7
NI 9247	A	24	9

  - Select **Raw** if you want the FPGA I/O Node to return uncalibrated, binary data from the module. If you select **Raw**, you must convert and calibrate the analog input values in the host VI.
- **Master Timebase Source**—Specifies the master timebase source that the module uses.
- **Export Onboard Clock**—Place a checkmark in this checkbox if you want to make this module accessible as a master timebase source to other modules.
- **Data Rate**—Specifies the rate at which the module acquires data.

NI 9250

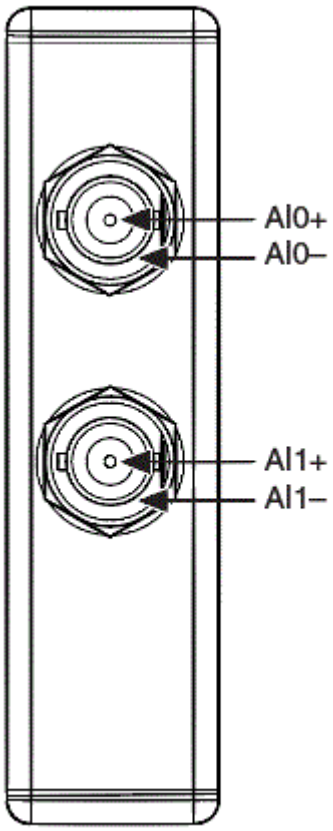
CompactRIO 2-Ch, ±5 V, 24-Bit, Analog Input Software Selectable IEPE & AC/DC

Software Reference (?)

FPGA Interface |

NI 9250

NI 9250 Pinout



Related Topics

FPGA Interface
C Series Module Properties Dialog Box
Converting and Calibrating CompactRIO Analog Input Values
Detecting Out-of-Range Channels for CompactRIO Analog Input Channels
Acquiring Data from an NI 9250
Configuring the Data Rate for a Module (FPGA Interface)
Converting NI 9250 Data
Synchronizing Multiple Modules
Understanding Loop Timing (FPGA Interface)

NI 9250 (FPGA Interface)

CompactRIO 2-Ch, ±5 V, 24-Bit, Analog Input Software Selectable IEPE & AC/DC

Open example

Find related examples

FPGA I/O Node

You can use an FPGA I/O Node, configured for reading, with this device.

Note You can synchronize an NI 9250 module with other modules that have a selectable timebase source.

Terminals in Software

Use the FPGA I/O Node to access the following terminals for this device.

Terminal	Description
AI**x**	Analog input channel **x**, where **x** is the number of the channel. The NI 9250 has channels 0 to 1.
Onboard Clock	Gives access to the onboard clock in the LabVIEW block diagram. The onboard clock frequency is 13.1072 MHz. Use the FPGA I/O Node in a single-cycle timed loop to access this channel. You m

	ust export the onboard clock of the NI 9250 to access this channel.
Start	Channel that controls when the NI 9250 starts acquiring data. If TRUE is written to the **Start** channel, the NI 9250 starts acquiring data. When the NI 9250 is acquiring data, you must write TRUE to the **Stop** channel before you can access properties for the module. If FALSE is written to the **Start** channel, no operation is performed.
Stop	Channel that controls when the NI 9250 stops acquiring data. If TRUE is written to the **Stop** channel, the NI 9250 stops acquiring data. When the NI 9250 is acquiring data, you must write TRUE to the **Stop** channel before you can access properties for the module. If FALSE is written to the **Stop** channel, no operation is performed.

Arbitration

This device supports only the Arbitrate if Multiple Requestors Only option for arbitration. You cannot configure arbitration settings for this device.

I/O Properties

Use the FPGA I/O Property Node to access the following I/O properties for this device.

Property	Description
Input Configuration	Sets the input configuration of the corresponding channel to one of three modes: AC Coupled, DC Coupled, IEPE AC Coupled.

Module Properties

Use the FPGA I/O Property Node to access the following module properties for this device.

Property	Description
Data Rate	Sets the rate at which the NI 9250 acquires data.

Module ID	Returns the module ID, 0x77EA.
Serial Number	Returns the unique serial number of the module .
Vendor ID	Returns the NI vendor ID, 0x1093.

Single-Cycle Timed Loop

This device does not support the single-cycle Timed Loop.

C Series Module Properties Dialog Box for the NI 9250 (FPGA Interface)

Right-click an NI 9250 C Series module in the **Project Explorer** window and select **Properties** from the shortcut menu to display this dialog box.

Use this dialog box to configure a C Series module.

This dialog box includes the following components:

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Type**—Specifies the type of C Series module. You cannot change this option.
- **Location**—Specifies a slot in the chassis for the C Series module.
- **Calibration Mode**—Sets the calibration mode for the C Series module. Select **Calibrated** if you want the FPGA I/O Node to return calibrated, fixed-point data from the module. The fixed-point data is signed, with 24-bits word length and 4-bits integer word length. Select **Raw** if you want the FPGA I/O Node to return calibrated, binary data from the module. If you select **Raw**, you must convert the binary data to the actual analog input values in the host VI. The default is **Calibrated**.
- **Master Timebase Source**—Specifies the master timebase source that the module uses.

- **Export Onboard Clock**—Place a checkmark in this checkbox if you want to make this module accessible as a master timebase source to other modules.
- **Data Rate**—Specifies the rate at which the module acquires data.
- **Enable TEDS Support**—Place a checkmark in this checkbox if you want to enable TEDS support in the FPGA and host VIs for this module.
- **Channels**—Specifies the channel(s) for which you want to select the input configuration.
- **Selected Channel(s) Settings**—Specifies the input configuration for each channel.
  - **Input Configuration**—Sets the input configuration for the selected channel(s). Select AC Coupled for AC coupling, DC Coupled for DC coupling, IEPE AC Coupled for AC coupling with IEPE enabled.

Configuring the NI 9250 Channel Input Modes (FPGA Interface)

You can configure the input mode for each channel of the NI 9250 at edit time using the C Series Module Properties dialog box. You can programmatically change the input mode for each channel at run time using the FPGA I/O Property Node. The execution of an FPGA I/O Property Node that is configured with an **Input Configuration** property overwrites the value you configured in the **C Series Module Properties** dialog box for the corresponding channel.

Configuring the Channel Input Modes Using the C Series Module Properties Dialog Box

Complete the following steps to configure the channel input modes using the **C Series Module Properties** dialog box.

1. Configure the CompactRIO system, and add an module.
2. Right-click the module in the **Project Explorer** window and select **Properties** to display the **C Series Module Properties** dialog box.

3. Select the channel(s) for which you want to configure the input mode from the **Channels** table. You can select more than one channel by holding the <Ctrl> or <Shift> key when selecting channels.
4. Select the input mode for the selected channel(s) from the **Input Configuration** pull-down menu.
5. Click the **OK** button.
6. Select **File»Save All** in the **Project Explorer** window.

Configuring the Channel Input Modes Using the FPGA I/O Property Node

Complete the following steps to configure the channel input modes using the FPGA I/O Property Node.

1. Create FPGA I/O items for the channels of the module for which you want to configure the **Input Configuration** property.
2. Place an FPGA I/O Property Node on the block diagram and configure it for the module channel for which you want to configure the input mode.
3. Click the **Property** section and select **Input Configuration** from the shortcut menu.
4. Right-click the **Input Configuration** input and select **Create»Control** from the shortcut menu.
5. On the front panel of the VI, select an input mode for the channel from the **Input Configuration** pull-down menu.

You can change the channel input modes at run time by writing to the control from the host VI. Refer to the following getting started VIs for examples of how to configure the input modes using the FPGA I/O Property Node.

Module	Example File Path	Open Example
NI 9250	`labview\examples\CompactRIO\Module Specific\NI 9250\NI 9250 Getting Started\NI 9250 Getting Started.lvproj`	Open example (NI 9250)

Note The **Input Configuration** property returns error 65538 if the module is acquiring data. You must use the Stop channel to stop acquiring data before you can write properties to the modules.

Converting NI 9250 Data (FPGA Interface)

Set the **Calibration Mode** to **Calibrated** in the C Series Module Properties dialog box for the NI 9250 if you want the FPGA I/O Node to return calibrated, fixed-point data from the module. Set the **Calibration Mode** to **Raw** if you want the FPGA I/O Node to return calibrated, binary data from the module. If you set the **Calibration Mode** to **Raw**, you must convert the binary values to engineering units. You must convert these values in the host VI.

You can use the following equations in the host VI to convert binary voltage values to volts:

Volts = **Binary Value** × 608896 pV/LSB

where **Binary Value** is the value returned by the FPGA I/O Node.

NI 9251

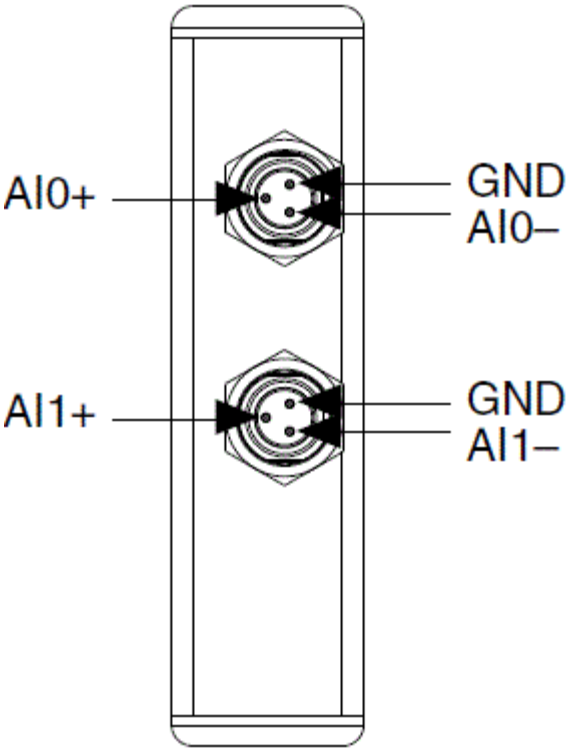
CompactRIO 2-Channel, 3 Vrms, 24-Bit Differential Analog Input Module

Software Reference (?)

FPGA Interface |

NI 9251

NI 9251 Pinout



Related Topics

FPGA Interface
C Series Module Properties Dialog Box
Converting and Calibrating CompactRIO Analog Input Values
Detecting Out-of-Range Channels for CompactRIO Analog Input Channels
Acquiring Data from a Module
Configuring the Data Rate for a Module (FPGA Interface)
Converting NI 9251 Data
Synchronizing Multiple NI 9225/9227/9229/923x/924x/9251/9260 Modules
Understanding Loop Timing (FPGA Interface)

NI 9251 (FPGA Interface)

CompactRIO 2-Channel, 3 Vrms, 24-Bit Differential Analog Input Module

Open example

Find related examples

FPGA I/O Node

You can use an FPGA I/O Node, configured for reading, with this device.

Note You can synchronize an NI 9251 module with other modules that have a selectable timebase source.

Terminals in Software

Use the FPGA I/O Node to access the following terminals for this device.

Terminal	Description
AI**x**	Analog input channel **x**, where **x** is the number of the channel. The NI 9251 has channels 0 to 1.
Onboard Clock	Gives access to the onboard clock in the LabVIEW block diagram. The onboard clock frequency is 13.1072 MHz. Use the FPGA I/O Node in a single-cycle timed loop to access this channel. You must export the onboard clock of the NI 9251 to access this channel.
Start	Channel that controls when the NI 9251 starts acquiring data. If TRUE is written to the **Start** channel, the NI 9251 starts acquiring data. When the NI 9251 is acquiring data, you must write TRUE to the **Stop** channel before you can access properties for the module. If FALSE is written to the **Start** channel, no operation is performed.
Stop	Channel that controls when the NI 9251 stops acquiring data. If TRUE is written to the **Stop** channel, the NI 9251 stops acquiring data. When the NI 9251 is acquiring data, you must write TRUE to the **Stop** channel before you can access prope

	rties for the module. If FALSE is written to the **Stop** channel, no operation is performed.

Arbitration

This device supports only the Arbitrate if Multiple Requestors Only option for arbitration. You cannot configure arbitration settings for this device.

I/O Properties

Use the FPGA I/O Property Node to access the following I/O properties for this device.

Property	Description
Input Configuration	Sets the input configuration of the corresponding channel to one of two modes: AC Coupled; DC Coupled.

Module Properties

Use the FPGA I/O Property Node to access the following module properties for this device.

Property	Description
Data Rate	Sets the rate at which the NI 9251 acquires data.
Module ID	Returns the module ID, 0x77E9.
Serial Number	Returns the unique serial number of the module.
Vendor ID	Returns the NI vendor ID, 0x1093.

Single-Cycle Timed Loop

This device does not support the single-cycle Timed Loop.

C Series Module Properties Dialog Box for the NI 9251 (FPGA Interface)

Right-click an NI 9251 C Series module in the **Project Explorer** window and select **Properties** from the shortcut menu to display this dialog box.

Use this dialog box to configure a C Series module.

This dialog box includes the following components:

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Type**—Specifies the type of C Series module. You cannot change this option.
- **Location**—Specifies a slot in the chassis for the C Series module.
- **Calibration Mode**—Sets the calibration mode for the C Series module. Select **Calibrated** if you want the FPGA I/O Node to return calibrated, fixed-point data from the module. The fixed-point data is signed, with 24-bits word length and 4-bits integer word length. Select **Raw** if you want the FPGA I/O Node to return calibrated, binary data from the module. If you select **Raw**, you must convert the binary data to the actual analog input values in the host VI. The default is **Calibrated**.
- **Master Timebase Source**—Specifies the master timebase source that the module uses.
- **Export Onboard Clock**—Place a checkmark in this checkbox if you want to make this module accessible as a master timebase source to other modules.
- **Data Rate**—Specifies the rate at which the module acquires data.
- **Channels**—Specifies the channel(s) for which you want to select the input configuration.
- **Selected Channel(s) Settings**—Specifies the input configuration for each channel.
  - **Input Configuration**—Sets the input configuration for the selected channel(s). Select **AC Coupled** for AC coupling, **DC Coupled** for DC coupling.

Configuring the NI 9251 Channel Input Modes (FPGA Interface)

You can configure the input mode for each channel of the NI 9251 at edit time using the C Series Module Properties dialog box. You can programmatically change the input mode for each channel at run time using the FPGA I/O Property Node. The execution of an FPGA I/O Property Node that is configured with an **Input Configuration** property overwrites the value you configured in the **C Series Module Properties** dialog box for the corresponding channel.

Configuring the Channel Input Modes Using the C Series Module Properties Dialog Box

Complete the following steps to configure the channel input modes using the **C Series Module Properties** dialog box.

1. Configure the CompactRIO system, and add an module.
2. Right-click the module in the **Project Explorer** window and select **Properties** to display the **C Series Module Properties** dialog box.
3. Select the channel(s) for which you want to configure the input mode from the **Channels** table. You can select more than one channel by holding the <Ctrl> or <Shift> key when selecting channels.
4. Select the input mode for the selected channel(s) from the **Input Configuration** pull-down menu.
5. Click the **OK** button.
6. Select **File»Save All** in the **Project Explorer** window.

Configuring the Channel Input Modes Using the FPGA I/O Property Node

Complete the following steps to configure the channel input modes using the FPGA I/O Property Node.

1. Create FPGA I/O items for the channels of the module for which you want to configure the **Input Configuration** property.
2. Place an FPGA I/O Property Node on the block diagram and configure it for the module channel for which you want to configure the input mode.

3. Click the **Property** section and select **Input Configuration** from the shortcut menu.
4. Right-click the **Input Configuration** input and select **Create»Control** from the shortcut menu.
5. On the front panel of the VI, select an input mode for the channel from the **Input Configuration** pull-down menu.

You can change the channel input modes at run time by writing to the control from the host VI. Refer to the following getting started VIs for examples of how to configure the input modes using the FPGA I/O Property Node.

Module	Example File Path	Open Example
NI 9251	`labview\examples\CompactRIO\Module Specific\NI 9251\NI 9251 Getting Started\NI 9251 Getting Started.lvproj`	Open example (NI 9251)

Note The **Input Configuration** property returns error 65538 if the module is acquiring data. You must use the Stop channel to stop acquiring data before you can write properties to the modules.

Converting NI 9251 Data (FPGA Interface)

Set the **Calibration Mode** to **Calibrated** in the C Series Module Properties dialog box for the NI 9251 if you want the FPGA I/O Node to return calibrated, fixed-point data from the module. Set the **Calibration Mode** to **Raw** if you want the FPGA I/O Node to return calibrated, binary data from the module. If you set the **Calibration Mode** to **Raw**, you must convert the binary values to engineering units. You must convert these values in the host VI.

You can use the following equations in the host VI to convert binary voltage values to volts:

Volts = **Binary Value** × 515589 pV/LSB

where

Binary Value is the value returned by the FPGA I/O Node.

NI 9252

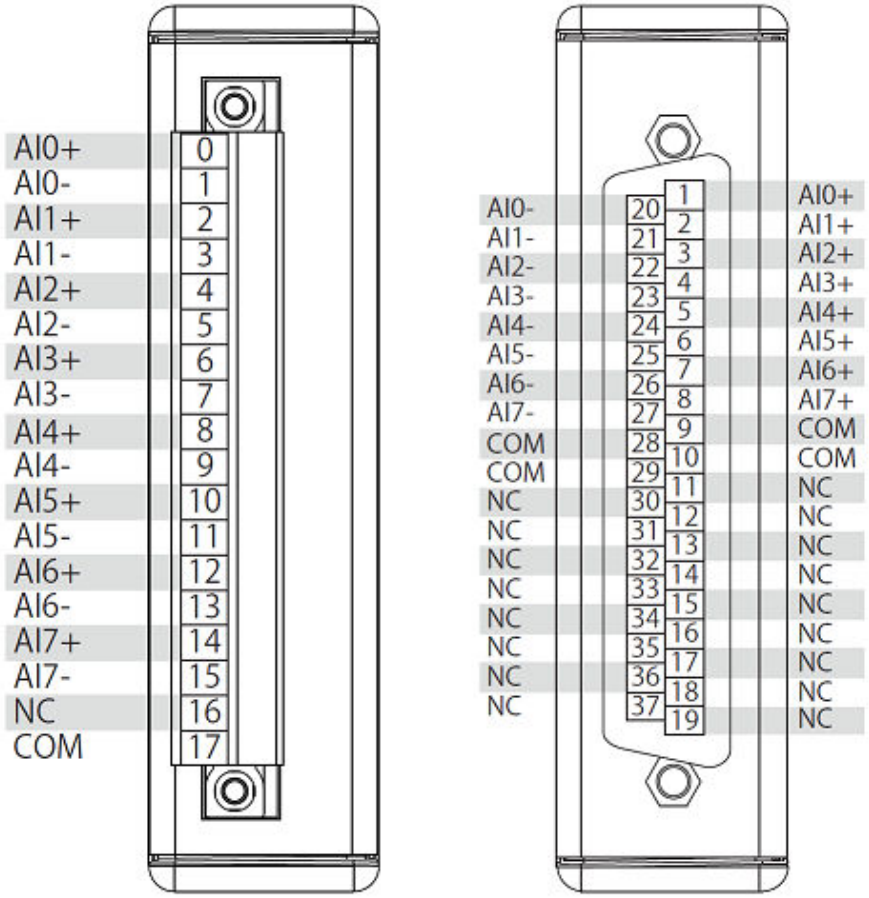
CompactRIO 8-Channel, ±10 V, 24-Bit Differential Analog Input Module

Software Reference (?)

FPGA Interface |

NI 9252

NI 9252 Pinout



Related Topics

FPGA Interface
C Series Module Properties Dialog Box
Converting and Calibrating CompactRIO Analog Input Values
Detecting Out-of-Range Channels for CompactRIO Analog Input Channels
Acquiring Data from a Module
Configuring the Data Rate for a Module (FPGA Interface)
Converting NI 9252 Data
Synchronizing Multiple NI 9225/9227/9229/923x/924x/9202/9260 Modules
Understanding Loop Timing (FPGA Interface)

NI 9252 (FPGA Interface)

CompactRIO 8-Channel, ±10 V, 24-Bit Differential Analog Input Module

 Open example

 Find related examples

FPGA I/O Node

You can use an FPGA I/O Node, configured for reading, with this device.

Terminals in Software

Use the FPGA I/O Node to access the following terminals for this device.

Terminal	Description
AI**x**	Analog input channel **x**, where **x** is the number of the channel. The NI 9252 has channels 0 to 7.
Onboard Clock	Gives access to the onboard clock in the LabVIEW block diagram. The onboard clock frequency is 12.8 MHz. Use the FPGA I/O Node in a single-cycle timed loop to access this channel. You must export the onboard clock of the NI 9252 to access this channel.
Start	Channel that controls when the NI 9252 starts acquiring data. If TRUE is written to the **Start** cha

	nnel, the NI 9252 starts acquiring data. When th e NI 9252 is acquiring data, you must write TRUE to the **Stop** channel before you can access prop erties for the module. If FALSE is written to the **S tart** channel, no operation is performed.
Stop	Channel that controls when the NI 9252 stops ac quiring data. If TRUE is written to the **Stop** chan nel, the NI 9252 stops acquiring data. When the NI 9252 is acquiring data, you must write TRUE t o the **Stop** channel before you can access prope rties for the module. If FALSE is written to the **St op** channel, no operation is performed.

Arbitration

This device supports only the Arbitrate if Multiple Requestors Only option for arbitration. You cannot configure arbitration settings for this device.

Module Properties

Use the FPGA I/O Property Node to access the following module properties for this device.

Property	Description
Data Rate	Sets the rate at which the NI 9252 acquires data.
Module ID	Returns the module ID.
Serial Number	Returns the unique serial number of the module .
Vendor ID	Returns the NI vendor ID, 0x1093.
Filter Response	Sets the AI filter types supported by the device. The filters supported by this module are the Co mb (default) and Butterworth filter.
Filter Order	Sets the Filter Order for the Butterworth filter. T his setting would only take effect if the module i s currently configured to the Butterworth filter.
Filter Frequency	Sets the AI filter's cutoff frequency.

Single-Cycle Timed Loop

This device does not support the single-cycle Timed Loop.

C Series Module Properties Dialog Box for the NI 9252 (FPGA Interface)

Right-click an NI 9252 C Series module in the **Project Explorer** window and select **Properties** from the shortcut menu to display this dialog box.

Use this dialog box to configure a C Series module.

This dialog box includes the following components:

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Type**—Specifies the type of C Series module. You cannot change this option.
- **Location**—Specifies a slot in the chassis for the C Series module.
- **Calibration Mode**—Sets the calibration mode for the C Series module. Select **Calibrated** if you want the FPGA I/O Node to return calibrated, fixed-point data from the module. The fixed-point data is signed, with 24-bits word length and 4-bits integer word length. Select **Raw** if you want the FPGA I/O Node to return calibrated, binary data from the module. If you select **Raw**, you must convert the binary data to the actual analog input values in the host VI. The default is **Calibrated**.
- **Master Timebase Source**—Specifies the master timebase source that the module uses.
- **Export Onboard Clock**—Place a checkmark in this checkbox if you want to make this module accessible as a master timebase source to other modules.
- **Data Rate**—Specifies the rate at which the module acquires data.

- **Filter Response**—Sets the AI digital filter types supported by the device. Filters supported by this module are the Comb (default) and Butterworth filter.
- **Filter Order**—Sets the Filter Order for the Butterworth filter. This setting would only take effect if the module is currently configured to the Butterworth filter.
- **Filter Frequency**—Configures the cut-off frequency of the filter. It is dependent on the data rate. Available values:

Filter Settings	Cut-off Frequency		
	Comb	Butterworth	
		12.8 MHz	13.1 MHz
Filter Frequency - 1	Data Rate/1	4000 Hz	4096 Hz
Filter Frequency - 2	Data Rate/2	2000 Hz	2048 Hz
Filter Frequency - 3	Data Rate/4	1000 Hz	1024 Hz
Filter Frequency - 4	Data Rate/8	500 Hz	512 Hz
Filter Frequency - 5	Data Rate/16	250 Hz	256 Hz
Filter Frequency - 6	Data Rate/16	125 Hz	128 Hz

Notes:
When the module is configured to the Comb filter, Filter Frequency - 5 and Filter Frequency - 6 sets the Notch Frequency at Data Rate/16.

Converting NI 9252 Data (FPGA Interface)

Set the **Calibration Mode** to **Calibrated** in the C Series Module Properties dialog box for the NI 9252 if you want the FPGA I/O Node to return calibrated, fixed-point data from the module. Set the **Calibration Mode** to **Raw** if you want the FPGA I/O Node to return calibrated, binary data from the module. If you set the **Calibration Mode** to **Raw**, you must convert the binary values to engineering units. You must convert these values in the host VI.

You can use the following equations in the host VI to convert binary voltage values to volts:

Volts = **Binary Value** × 1261243 pV/LSB

where

Binary Value is the value returned by the FPGA I/O Node.

NI 9253

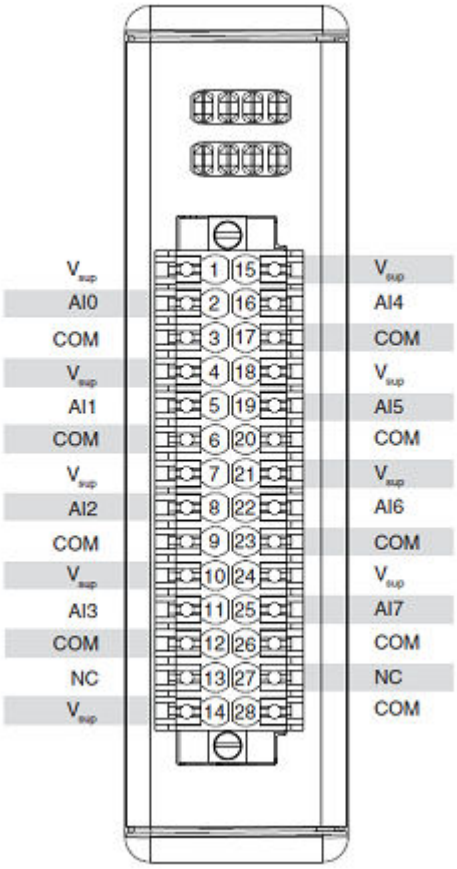
CompactRIO 8-Channel, ±20 mA, 24-Bit Differential Analog Input Module

Software Reference (?)

FPGA Interface |

NI 9253

NI 9253 Pinout



Related Topics

FPGA Interface
C Series Module Properties Dialog Box
Converting and Calibrating CompactRIO Analog Input Values
Detecting Out-of-Range Channels for CompactRIO Analog Input Channels
Acquiring Data from a Module
Configuring the Data Rate for a Module (FPGA Interface)
Converting NI 9253 Data
Synchronizing Multiple NI 9225/9227/9229/923x/924x/9202/9260 Modules
Understanding Loop Timing (FPGA Interface)

NI 9253 (FPGA Interface)

CompactRIO 8-Channel, ±20 mA, 24-Bit Single-ended Analog Input Module

Open example Find related examples

FPGA I/O Node

You can use an FPGA I/O Node, configured for reading, with this device.

Terminals in Software

Use the FPGA I/O Node to access the following terminals for this device.

Terminal	Description
AI**x**	Analog input channel **x**, where **x** is the number of the channel. The NI 9253 has channels 0 to 7.
Onboard Clock	Gives access to the onboard clock in the LabVIEW block diagram. The onboard clock frequency is 12.8 MHz. Use the FPGA I/O Node in a single-cycle timed loop to access this channel. You must export the onboard clock of the NI 9253 to access this channel.
Start	Channel that controls when the NI 9253 starts acquiring data. If TRUE is written to the **Start** cha

	nnel, the NI 9253 starts acquiring data. When th e NI 9253 is acquiring data, you must write TRUE to the **Stop** channel before you can access prop erties for the module. If FALSE is written to the **S tart** channel, no operation is performed.
Stop	Channel that controls when the NI 9253 stops ac quiring data. If TRUE is written to the **Stop** chan nel, the NI 9253 stops acquiring data. When the NI 9253 is acquiring data, you must write TRUE t o the **Stop** channel before you can access prope rties for the module. If FALSE is written to the **St op** channel, no operation is performed.

Arbitration

This device supports only the Arbitrate if Multiple Requestors Only option for arbitration. You cannot configure arbitration settings for this device.

Module Methods

Use the FPGA I/O Method Node to access the following module method for this device.

Method	Description
Check Cached Status	Returns Booleans for each channel that indicate whether there was a input limits fault, overcurre nt, or field side power fault on the channel since the last execution of the Check Cached Status m ethod. When the FPGA I/O Node reads the chan nels, the FPGA VI determines the state of the cha nnels and caches any TRUE value until the Chec k Cached Status method executes. ▪ **Channel Input Limits Fault**—Return s an array of Boolean values. A value of TR UE in any index indicates that the channel sharing a number with that index detecte d the channel input is out of range of Low er Fault Detection Limit and Upper Fault D etection Limit on the channel at some poi

	nt after the last time that the Check Cached Status method executed. ▪ **Channel Overcurrent**—Returns an array of Boolean values. A value of TRUE in any index indicates that the channel sharing a number with that index detected an overcurrent on the channel at some point after the last time that the Check Cached Status method executed. ▪ **Field-Side Power Fault**—Returns a single Boolean value. A value of TRUE indicates that the module detected Field-Side Power Fault on the module at some point after the last time that the Check Cached Status method executed.

I/O Properties

Use the FPGA I/O Property Node to access the following I/O properties for this device.

Property	Description
Input Limits Fault Detection Enable	Enable the module to detect Input Limit Fault on the corresponding channel. Set the input to TRUE to enable and FALSE (default) to disable the Input Limit Fault Detection.
Lower Fault Detection Limit	Sets the Channel's Lower Fault Detection Limit of the corresponding channel. The range of valid current limit values is 0—0.0219 A (default value is 0.0 A).
Upper Fault Detection Limit	Sets the Channel's Upper Fault Detection Limit of the corresponding channel. The range of valid current limit values is 0—0.0219 A (default value is 0.0219 A).

Module Properties

Use the FPGA I/O Property Node to access the following module properties for this device.

Property	Description
Data Rate	Sets the rate at which the NI 9253 acquires data.
Module ID	Returns the module ID.
Serial Number	Returns the unique serial number of the module .
Vendor ID	Returns the NI vendor ID, 0x1093.
Filter Response	Sets the AI filter types supported by the device. The filters supported by this module are the Co mb (default) and Butterworth filter.
Filter Order	Sets the Filter Order for the Butterworth filter. T his setting would only take effect if the module i s currently configured to the Butterworth filter.
Filter Frequency	Sets the AI filter's cutoff frequency.
Field-Side Power Fault Detection Enable	Enable the module to detect Field-Side Power S upplied to the module. Set the input to TRUE to enable and FALSE (default) to disable the Field-Side Power Fault Detection.

Single-Cycle Timed Loop

This device does not support the single-cycle Timed Loop.

C Series Module Properties Dialog Box for the NI 9253 (FPGA Interface)

Right-click an NI 9253 C Series module in the **Project Explorer** window and select **Properties** from the shortcut menu to display this dialog box.

Use this dialog box to configure a C Series module.

This dialog box includes the following components:

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Type**—Specifies the type of C Series module. You cannot change this option.

- **Location**—Specifies a slot in the chassis for the C Series module.
- **Calibration Mode**—Sets the calibration mode for the C Series module. Select **Calibrated** if you want the FPGA I/O Node to return calibrated, fixed-point data from the module. The fixed-point data is signed, with 24-bits word length and -4-bits integer word length. Select **Raw** if you want the FPGA I/O Node to return calibrated, binary data from the module. If you select **Raw**, you must convert the binary data to the actual analog input values in the host VI. The default is **Calibrated**.
- **Master Timebase Source**—Specifies the master timebase source that the module uses.
- **Export Onboard Clock**—Place a checkmark in this checkbox if you want to make this module accessible as a master timebase source to other modules.
- **Data Rate**—Specifies the rate at which the module acquires data.
- **Filter Response**—Sets the AI digital filter types supported by the device. Filters supported by this module are the Comb (default) and Butterworth filter.
- **Filter Order**—Sets the Filter Order for the Butterworth filter. This setting would only take effect if the module is currently configured to the Butterworth filter.
- **Filter Frequency**—Configures the cut-off frequency of the filter. It is dependent on the data rate. Available values:

Filter Settings	Cut-off Frequency		
	Comb	Butterworth	
		12.8 MHz	13.1 MHz
Filter Frequency - 1	Data Rate/1	4000 Hz	4096 Hz
Filter Frequency - 2	Data Rate/2	2000 Hz	2048 Hz
Filter Frequency - 3	Data Rate/4	1000 Hz	1024 Hz
Filter Frequency - 4	Data Rate/8	500 Hz	512 Hz
Filter Frequency - 5	Data Rate/16	250 Hz	256 Hz
Filter Frequency - 6	Data Rate/16	125 Hz	128 Hz

Notes:
When the module is configured to the Comb filter, Filter Frequency - 5 and Filter Frequency - 6 sets the Notch Frequency at Data Rate/16.

- **Diagnostic Settings**—Clicking on this button brings up a new dialog box which allows the diagnostics of the module to be selected.
  - **Field-Side Power Fault Detection Enable**—Placing a checkmark in the checkbox will enable the module to detect field-side power fault.
  - **Input Limits Fault Detection Enable**—Placing a checkmark in the checkbox enables the module to detect if the readings are within the set limits. It will also bring up the option to set the upper limit and the lower limit.
  - **Lower Fault Detection Limit**—Sets the Channel's Lower Fault Detection Limit of the corresponding channel. The range of valid current limit values is 0—0.0219 A (default value is 0.0 A).
  - **Upper Fault Detection Limit**—Sets the Channel's Upper Fault Detection Limit of the corresponding channel. The range of valid current limit values is 0—0.0219 A (default value is 0.0219 A).

Converting NI 9253 Data (FPGA Interface)

Set the **Calibration Mode** to **Calibrated** in the C Series Module Properties dialog box for the NI 9253 if you want the FPGA I/O Node to return calibrated, fixed-point data from the module. Set the **Calibration Mode** to **Raw** if you want the FPGA I/O Node to return calibrated, binary data from the module. If you set the **Calibration Mode** to **Raw**, you must convert the binary values to engineering units. You must convert these values in the host VI.

You can use the following equations in the host VI to convert binary current values to amperes:

Current = **Binary Value** × 2615.02 pA/LSB

where

Binary Value is the value returned by the FPGA I/O Node.

NI 9253 (Scan Interface)

CompactRIO 8-Channel, ±20 mA, 24-Bit Single-ended Analog Input Module

Open example

Module I/O Variables

To use I/O from this module in a VI, drag and drop I/O variables from the **Project Explorer** window to the block diagram of the VI. The I/O variables for the channels return calibrated floating-point data in amps.

Module Channels

The NI 9253 has the following channels.

Channel	Description
AI**x**	Analog input channel **x**, where **x** is the number of the channel. For the NI 9253, **x** is 0 to 7.

C Series Module Properties Dialog Box

Use this dialog box to configure the NI 9253. Right-click the NI 9253 in the **Project Explorer** window and select **Properties** to display this dialog box. You can configure the following options.

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this value.
- **Location**—Specifies a slot in the chassis for the C Series module.
- **Data Rate**—Sets the rate at which the module acquires data.
- **Filter Response**—Sets the AI filter types supported by the device. The filters supported by this module are the Comb (default) and Butterworth filter.

- **Filter Order**—Sets the Filter Order for the Butterworth filter. This setting would only take effect if the module is currently configured to the Butterworth filter.
- **Filter Frequency**—Sets the AI filter's cutoff frequency.
- **Diagnostic Settings**—You can set diagnostic functions for the module.
  - **Module Settings**
    - **Field-side Power Fault Detection Enable**—Enable the module to detect Field-Side Power Supplied to the module. Select the checkbox to enable and unselect (default) to disable the Field-Side Power Fault Detection.
  - **Channel Configuration**
    - **Input Limits Fault Detection Enable**—Enable the module to detect Input Limit Fault on the corresponding channel. Select the checkbox to enable and unselect (default) to disable the Input Limits Fault Detection.
    - **Lower Fault Detection Limit**—Sets the Channel's Lower Fault Detection Limit of the corresponding channel. The range of valid current limit values is 0—0.0219 A (default value is 0.0 A).
    - **Upper Fault Detection Limit**—Sets the Channel's Upper Fault Detection Limit of the corresponding channel. The range of valid current limit values is 0—0.0219 A (default value is 0.0219 A).

Module Methods

Use the Invoke Node to access the following module properties for this device.

Method	Description
Check Cached Status	Returns Booleans for each channel that indicate whether there was an input limits fault, overcurrent, or field side power fault on the channel since the last execution of the Check Cached Status method. When I/O variables or shared variables read the channels, the scan driver determines the state of the channels and caches any TRUE v

	alue until the Check Cached Status method executes. ▪ **Channel Input Limits Fault**—Returns an array of Boolean values. A value of TRUE in any index indicates that the channel sharing a number with that index detected the channel input is out of range of Lower Fault Detection Limit and Upper Fault Detection Limit on the channel at some point after the last time that the Check Cached Status method executed. ▪ **Channel Overcurrent**—Returns an array of Boolean values. A value of TRUE in any index indicates that the channel sharing a number with that index detected an overcurrent on the channel at some point after the last time that the Check Cached Status method executed. ▪ **Field-Side Power Fault**—Returns a single Boolean value. A value of TRUE indicates that the module detected Field-Side Power Fault on the module at some point after the last time that the Check Cached Status method executed.

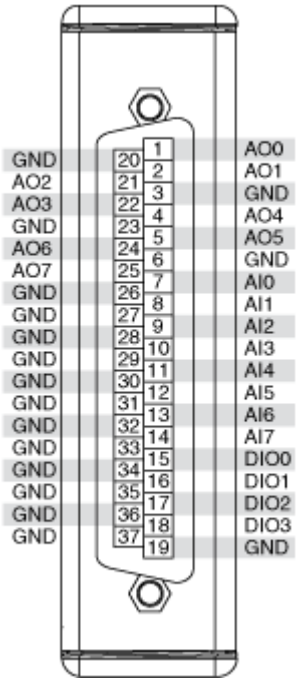
NI 9381

CompactRIO 0 V to 5 V, 12-bit, Multifunction Input/Output Module

Software Reference (?)

FPGA Interface | Scan Interface

NI 9381 Pinout



Running AI and AO Operations Concurrently on the NI 9381

AI and AO operations that are run concurrently may exhibit jitter. Access both subsystems using a single I/O Node to avoid jitter in your application. Refer to the Avoiding Timing Uncertainty topic for more information.

Related Topics

FPGA Interface
Converting and Calibrating CompactRIO Analog Input Values
Detecting Out-of-Range Channels
Avoiding Timing Uncertainty with the NI 9381
Converting Voltage Values to Binary Values for the NI 9381

NI 9381 (FPGA Interface)

CompactRIO 0 V to 5 V, 12-bit, Multifunction Input/Output Module

Find NI 9381 examples

FPGA I/O Node

You can use an FPGA I/O Node, configured for reading and writing, with this device.

Terminal	Description
AI**x**	Analog input channel **x**, where **x** is the number of the channel. The NI 9381 has AI channels 0 to 7.
AO**x**	Analog output channel **x**, where **x** is the number of the channel. The NI 9381 has AO channels 0 to 3.
DIO**x**	Digital input/output channel **x**, where **x** is the number of the channel. The NI 9381 has DIO channels 0 to 3.
DIO3:0	Digital port consisting of channels 0 through 3. Channel 3 is returned in the MSB, and channel 0 is returned in the LSB.

Caution AI and AO operations that are run concurrently may exhibit jitter. Access both subsystems using a single I/O Node to avoid jitter in your application. Refer to the Avoiding Timing Uncertainty topic for more information.

Arbitration

Analog input and analog output channels of this device support only the Arbitrate if Multiple Requestors Only option for arbitration. You cannot configure arbitration settings for analog input and analog output channels of this device.

You can configure the arbitration settings for digital output channels of this device in the Advanced Code Generation page of the FPGA I/O Properties dialog box. The default arbitration setting is Never Arbitrate.

Digital input channels of this device support only the **Never Arbitrate** option for arbitration. You cannot configure arbitration settings for the digital input channels of this device.

I/O Methods

Use the FPGA I/O Method Node to access the following I/O methods for the DIO channels of this device.

Method	Description
Set Output Data	Refer to the FPGA I/O Method Node (FPGA Module) topic for a description of this method. This method is available only when you set the DIO line direction to output. You can set the DIO line direction in the C Series Module Properties dialog box.
Set Output Enable	Sets the line direction of the digital channel or the DIO3:0 digital port. Refer to the FPGA I/O Method Node (FPGA Module) topic for more information on this method. This method can introduce jitter in an analog input or analog output loop. This method is available only when you enable programmable DIO line changes on the module. You can enable programmable DIO line changes on the module in the C Series Module Properties dialog box.
Wait on Any Edge	Pauses the execution of the I/O Method Node until the next falling or rising edge of the digital signal. The **Timeout** input specifies in FPGA clock ticks how long the Wait on Any Edge method waits for the next falling or rising edge. A value of 0 causes the method to time out immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.  **Notes** This method is not available on the DIO3:0 port. For the first two seconds after resetting the F

	PGA VI, the time out wil l not start counting unt il the module is identifi ed.
Wait on Falling Edge	Pauses the execution of the I/O Method Node un til the next falling edge of the digital signal. The **Timeout** input specifies in FPGA clock ticks ho w long the Wait on Falling Edge method waits fo r the next falling edge. A value of 0 causes the m ethod to time out immediately, a negative value causes the method to wait indefinitely, and a po sitive value causes the method to wait for that n umber of clock ticks before timing out.  **Notes** This method is not available on the DI O3:0 port. For the first two secon ds after resetting the F PGA VI, the time out wil l not start counting unt il the module is identifi ed.
Wait on High Level	Pauses the execution of the I/O Method Node un til the digital signal is high. The **Timeout** input specifies in FPGA clock ticks how long the Wait o n High Level method waits for the next high leve l. A value of 0 causes the method to time out im mediately, a negative value causes the method t o wait indefinitely, and a positive value causes t he method to wait for that number of clock ticks before timing out.  **Notes** This method is not available on the DI O3:0 port. For the first two secon ds after resetting the F PGA VI, the time out wil

	l not start counting unt il the module is identifi ed.
Wait on Low Level	Pauses the execution of the I/O Method Node un til the digital signal is low. The **Timeout** input s pecifies in FPGA clock ticks how long the Wait o n Low Level method waits for the next low level. A value of 0 causes the method to time out imm ediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks be fore timing out. **Notes** This method is not available on the DI O3:0 port. For the first two secon ds after resetting the F PGA VI, the time out wil l not start counting unt il the module is identifi ed.
Wait on Rising Edge	Pauses the execution of the I/O Method Node un til the next rising edge of the digital signal. The **Timeout** input specifies in FPGA clock ticks ho w long the Wait on Rising Edge method waits for the next rising edge. A value of 0 causes the met hod to time out immediately, a negative value c auses the method to wait indefinitely, and a pos itive value causes the method to wait for that nu mber of clock ticks before timing out. **Notes** This method is not available on the DI O3:0 port. For the first two secon ds after resetting the F PGA VI, the time out wil l not start counting unt

	il the module is identifi ed.

Module Method

Use the FPGA I/O Method Node to access the following module method for this device.

Method	Description
Check Status	Returns a Boolean value that indicates whether the module is ready.

I/O Properties

Use the FPGA I/O Property Node to access the following I/O properties for AI and AO channels of this device.

Property	Description
LSB Weight	Returns the LSB weight in nV/LSB for the channe l. Use this value to convert and calibrate NI 9381 data if you set the **Calibration Mode** to **Raw** i n the C Series Module Properties dialog box.
Offset	Returns the calibration offset in nV for the chan nel. Use this value to convert and calibrate NI 93 81 data if you set the **Calibration Mode** to **Ra w** in the **C Series Module Properties** dialog b ox.

Module Properties

Use the FPGA I/O Property Node to access the following module properties for this device.

Property	Description
Module ID	Returns the module ID.
Serial Number	Returns the unique serial number of the module .
Vendor ID	Returns the NI vendor ID, 0x1093.

Single-Cycle Timed Loop

This device supports the single-cycle Timed Loop. Configure the number of input synchronizing registers for the channels of this device in the Advanced Code Generation page of the FPGA I/O Node Properties dialog box. Configure the number of output synchronizing registers for the channels of this device in the Advanced Code Generation page of the FPGA I/O Properties dialog box.

This device supports the Number of Synchronizing Registers for Output Data synchronizing register option when used in SCTL output. This option supports the same functionality as the **Number of Synchronizing Registers for Output Data** option described in the Advanced Code Generation FPGA I/O Properties Page (FPGA Module) topic, with the exception that you can use this option only in a single-cycle Timed Loop. You can implement either 0 or 1 synchronizing registers inside the single-cycle Timed Loop, however, if you configure 0 synchronizing registers outside of the single-cycle Timed Loop, the FPGA VI implements 1 synchronizing register by default.

When the device is within a single-cycle Timed Loop, it must be ready to perform digital I/O before a loop containing digital I/O starts. Poll the **Ready** output of the Check Status method to determine whether the module is ready. Digital input operations return invalid data if the module is not ready. The module also might ignore or delay digital output operations if it is not ready.

While the digital is performing digital I/O within a single-cycle Timed Loop, do not perform property reads or remove the module from the chassis. Doing any of these actions causes the module to be unable to perform digital I/O and the **Ready** output of the Check Status method to return FALSE.

FPGA Target Clock Support

This device supports only top-level FPGA target clock rates and single-cycle Timed Loop clock rates that are multiples of 40 MHz, such as 40 MHz, 80 MHz, 120 MHz, and so on.

Avoiding Timing Uncertainty with the NI 9381 (FPGA Interface)

Follow these guidelines to avoid introducing timing uncertainty into AI node, AO Node, DO Node, and Set Output Data method calls. Additionally, failing to follow

these guidelines may result in lost data points for DO Node calls or Set Output Data method calls when either of them are made from inside a single-cycle Timed Loop.

- Use a single I/O Node to access AI and AO operations to ensure proper sequencing.
- Do not run the Set Output Enable method when an AI, AO, or DO subsystems is active.
- Do not perform the following operations concurrently:
  - AI Node call
  - AO Node call
  - Set Output Enable method call
  - Automatic line direction change when a DO call is made under the following conditions:
    - The call is made from outside of a single-cycle Timed Loop.
    - The **Allow programmatic DIO line direction** checkbox is checked in the C Series Module Properties dialog box.
    - The DIO channel is configured as an input at the time when the DO node is called.

Refer to the NI 9381 Advanced IO VI in the `labview\examples\CompactRIO\Module Specific\NI 9381\NI 9381 Advanced IO\NI 9381 Advanced IO.lvproj` for an example of the recommended way to use the AI, AO , and DIO subsystems.

C Series Module Properties Dialog Box for the NI 9381 (FPGA Interface)

Right-click an NI 9381 C Series module in the **Project Explorer** window and select **Properties** from the shortcut menu to display this dialog box.

Use this dialog box to configure a C Series module.

This dialog box includes the following components:

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this option.
- **Location**—Specifies a slot in the chassis for the C Series module.
- **Calibration Mode**—Sets the calibration mode for the C Series module. Select **Calibrated** if you want the FPGA I/O Node to return calibrated, fixed-point data from the module in units of volts. The fixed-point data is unsigned, with a word length of 18 bits and an integer word length of 3 bits for the analog input channels and a word length of 16 bits and an integer word length of 3 bits for the analog output channels. Select **Raw** if you want the FPGA I/O Node to return uncalibrated, binary data from the module. If you select **Raw**, you must convert and calibrate the analog input values in the host VI. The default is **Calibrated**.
- **Channels**—Specifies the channel(s) for which you want to select the direction.
- **Selected Channel(s) Settings**—Specifies the direction for each channel.
- **Hot Swap Behavior (Analog Output)**—Specifies the state of the analog output channels when the C Series module is removed and reinserted with the FPGA VI loaded and running. The power-on output state is the state that a C Series output module is in when power is applied to the module. The default is Last output value.
- **Allow Programmatic DIO Line Direction Change**—Place a checkmark in this checkbox if you want to enable programmable DIO line changes on the module.

Caution Performing a DIO line direction change will affect the timing of any concurrent AI, AO, and DO operations. Refer to the Avoiding Timing Uncertainty topic for more information.

Converting Voltage Values to Binary Values for the NI 9381 (FPGA Interface)

Set the **Calibration Mode** to **Calibrated** in the C Series Module Properties dialog box for the NI 9381 if you want the FPGA I/O Node to accept fixed-point data in units of volts when writing to the module. If you set the **Calibration Mode** to **Raw**, the FPGA I/O Node accepts only binary values when writing to the module. You must convert output voltage values to binary values before you write them to the module. You must convert these values in the host VI.

Using an Equation to Convert Voltage to Binary

You can use the following equation in the host VI to convert the analog output values to binary values:

Binary Value = (**Voltage Value** – **Offset**) ÷ **LSB Weight**

where

Binary Value is the value you write to the FPGA I/O Node

Current Value is the voltage in V that you want the channel to output

Offset is the value returned by the Offset property

LSB Weight is the value returned by the LSB Weight property

NI recommends using calibrated values for analog output. To convert calibrated voltage values, use the FPGA I/O Property Node to read the LSB Weight and Offset properties. If you do not want to read the LSB Weight and Offset values from the module, you can convert uncalibrated voltage values by using the following values for **Offset** and **LSB Weight**:

Offset = –5249

LSB Weight = $5.105\ V \div 2^{\textbf{DAC Resolution}}$

where

DAC Resolution is the DAC resolution value in the **NI 9381 Operating Instructions and Specifications**.

NI 9381 (Scan Interface)

CompactRIO 0 V to 5 V, 12-bit, Multifunction Input/Output Module

Module I/O Variables

To use I/O from this module in a VI, drag and drop I/O variables from the **Project Explorer** window to the block diagram of the VI. The I/O variables for the AI channels return floating-point data in volts. The I/O variables for the AO channels write floating-point data in volts. The I/O variables for the DIO channels read and write boolean values.

Module Channels

The NI 9381 has the following channels.

Channel	Description
AI**x**	Analog input channel **x**, where **x** is the number of the channel. For the NI 9381, **x** is 0 to 7.
AO**x**	Analog output channel **x**, where **x** is the number of the channel. For the NI 9381, **x** is 0 to 7.
DIO**x**	Digital input/output channel **x**, where **x** is the n umber of the channel. For the NI 9381, **x** is 0 to 3 .

C Series Module Properties Dialog Box

Use this dialog box to configure the NI 9381. Right-click the NI 9381 in the **Project Explorer** window and select **Properties** to display this dialog box. You can configure the following options.

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Type**—Specifies the type of C Series module. You cannot change this value.
- **Location**—Specifies a slot in the chassis for the C Series module.

- **Channels**—Specifies the channel(s) for which you want to configure settings.
- **Direction**—Specifies the initial line direction of the selected channel(s) as input or output.

Note If you are using direct access to read from or write to AI or AO channels of the NI 9381, the conversion time is somewhat longer than 50 µs.

Analog Output Modules

Use this book as a reference for the following information:

- FPGA I/O functions, I/O resources, arbitration options, methods, and properties each C Series analog output module supports in FPGA Interface mode
- I/O variables and properties each C Series analog output module supports in Scan Interface mode
- Instructions for using LabVIEW with CompactRIO analog output devices

To view related topics, click the **Locate** button, shown at left, in the toolbar at the top of this window. The **LabVIEW Help** highlights this topic in the **Contents** tab so you can navigate the related topics.

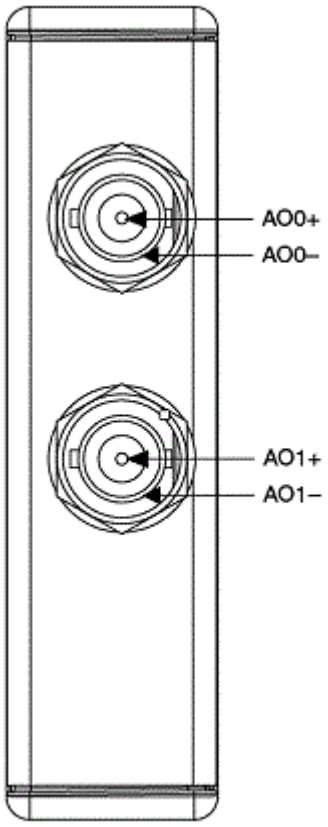
NI 9260

CompactRIO 2-Channel, 3 Vrms, 24-Bit Single-Ended Analog Output Module

Software Reference (?)

FPGA Interface

NI 9260 Pinout



Related Topics

FPGA Interface
9260 Properties Dialog Box
Configuring the Master Timebase Source for a Module (FPGA Interface)
Configuring the Data Rate for a Module (FPGA Interface)
Outputting Data from the NI 9260
Converting Voltage Values to Binary Values for the NI 9260
Synchronizing Multiple NI 9225/9227/9229/923x/924x/9251/9260 Modules

NI 9260 (FPGA Interface)

CompactRIO 2-Channel, 3 Vrms, 24-Bit Single-Ended Analog Output Module

FPGA I/O Node

You can use an FPGA I/O Node, configured for reading, with this device.

Terminals in Software

Use the FPGA I/O Node to access the following terminals for this device.

Terminal	Description
AO**x**	Analog output channel **x**, where **x** is the number of the channel. The NI 9260 has channels 0 to 1. Do not access AO channels on multiple modules in the same FPGA I/O Node if the modules are not synchronized or do not use the same data rate.
Start	Channel that controls when the NI 9260 starts outputting data. If TRUE is written to the **Start** channel, the NI 9260 starts outputting data. The AO**x** will be reset to 0 volts every time this I/O node is executed. When the NI 9260 is outputting data, you must write TRUE to the **Stop** channel before you can access properties. If FALSE is written to the **Start** channel, no operation is performed.
Stop	Channel that controls when the NI 9260 stops outputting data. If TRUE is written to the **Stop** channel, the NI 9260 stops outputting data. When the NI 9260 is outputting data, you must write TRUE to the **Stop** channel before you can access properties. If FALSE is written to the **Stop** channel, no operation is performed.

Arbitration

This device supports only the Arbitrate if Multiple Requestors Only option for arbitration. You cannot configure arbitration settings for this device.

I/O Methods

This device contains no I/O methods.

Module Methods

Use the FPGA I/O Method Node to access the following I/O properties for this device.

Method	Description
Check Cached Status	Returns Booleans for each channel that indicates whether there was underflow or overvoltage on the channel since the last execution of the Check Cached Status method. When the FPGA I/O Node reads the channels, the FPGA VI determines the state of the channels and caches any TRUE value until the Check Cached Status method executes. ▪ **Underflow**—Returns an array of Boolean values. A value of TRUE in any index indicates that the channel sharing a number with that index has missed one or more output samples at some point after the last time that the Check Cached Status method executed. ▪ **Overvoltage**—Returns an array of Boolean values. A value of TRUE in any index indicates that the channel sharing a number with that index detected an overvoltage on the channel at some point after the last time that the Check Cached Status method executed.

I/O Properties

Use the FPGA I/O Property Node to access the following I/O properties for this device.

Property	Description

LSB Weight	Returns the LSB weight in nV/LSB for the channel. Use this value to convert NI 9260 data if you set the **Calibration Mode** to **Raw** in the C Series Module Properties dialog box.
Offset	Returns the calibration offset in nV for the channel. Use this value to convert NI 9264 data if you set the **Calibration Mode** to **Raw** in the **C Series Module Properties** dialog box.

Module Properties

Use the FPGA I/O Property Node to access the following module properties for this device.

Property	Description
Data Rate	Sets the rate at which the NI 9260 outputs data.
Module ID	Returns the module ID, 0x7786 for BNC, 0x778C for mini-XLR.
Serial Number	Returns the unique serial number of the module.
Vendor ID	Returns the NI vendor ID, 0x1093.

Excitation Protection

The NI 9260 excitation circuit is protected from overvoltage fault conditions. The circuit is automatically disabled in the event of a fault condition. Whenever possible, a channel automatically recovers after the fault is removed. You must wire error terminals on the FPGA I/O Property Nodes to receive notification of overvoltage faults. LabVIEW returns warning 65548 if there is an overvoltage fault on at least one channel. Only the channel(s) with the fault are affected and all other channels on the module continue to function properly without interruption.

Single-Cycle Timed Loop

This device does not support the single-cycle Timed Loop.

C Series Module Properties Dialog Box for the NI 9260 (FPGA Interface)

Right-click an NI 9260 C Series module in the **Project Explorer** window and select **Properties** from the shortcut menu to display this dialog box.

Use this dialog box to configure a C Series module.

This dialog box includes the following components:

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this option.
- **Location**—Specifies a slot in the chassis for the C Series module.
- **Calibration Mode**—Sets the calibration mode for the C Series module. Select **Calibrated** if you want the FPGA I/O Node to accept fixed-point data in units of volts when writing to the module. The fixed-point data is signed, with a word length of 24 bits and an integer word length of 4 bits. Select **Raw** if you want the FPGA I/O Node to accept calibrated, binary data when writing to the module. If you select **Raw**, you must convert the analog output values in the host VI before you write them to the module. The default is **Calibrated**.
- **Master Timebase Source**—Specifies the master timebase source that the module uses.
- **Export Onboard Clock**—Place a checkmark in this checkbox if you want to make this module accessible as a master timebase source to other modules.
- **Data Rate**—Specifies the rate at which the module acquires data.

Converting Voltage Values to Binary Values for the NI 9260 (FPGA Interface)

Set the **Calibration Mode** to **Calibrated** in the C Series Module Properties dialog box for the NI 9260 if you want the FPGA I/O Node to accept fixed-point data in units of volts when writing to the module. If you set the Calibration Mode to Raw, the FPGA I/O Node accepts only binary values when writing to the module. You must

convert output voltage values to binary values before you write them to the module. You must convert these values in the host VI.

Note The equations below apply only to the NI 9260.

Using an Equation to Convert Voltage to Binary

You can use the following equation in the host VI to convert the analog output values to binary:

Binary Value = (**Voltage Value** - (**Offset** × $\mathbf{10^{-9}}$)) × (**LSB Weight** × $\mathbf{10^{-12}}$)

where

Binary Value is the value you write to the FPGA I/O Node

Voltage Value is the voltage in V that you want the channel to output †

Offset is the value returned by the Offset property

LSB Weight is the value returned by the LSB Weight property.

NI recommends using calibrated values for analog output. To convert calibrated voltage values, use the FPGA I/O Property Node to read the LSB Weight and Offset properties. If you do not want to read the LSB Weight and Offset values from the module, you can convert uncalibrated voltage values by using the following values for **Offset** and **LSB Weight**:

Offset = 0

LSB Weight = **Typical Output Span** ÷ $2^{\mathbf{DAC\ Resolution}}$ × 10^{12}

where **Typical Output Span** is 8.71 V for the NI 9260 **DAC Resolution** is the DAC resolution value in the hardware documentation for the module.

Outputting Data from an NI 9260 (FPGA Interface)

The NI 9260 has two analog output channels that simultaneously output at the data rate for which you have configured the module. Use the **Start** and **Stop** channels of

the NI 9260 to put the module in and out of data mode. In data mode, the NI 9260 can only output data. You can use the FPGA I/O Node to write the data to the module. You cannot access properties while the module is in data mode.

Note You must create FPGA I/O items for the NI 9260 before you can configure the items using the FPGA I/O Node.

Putting the Module in Data Mode

Configure an FPGA I/O Node with the **Start** channel of the NI 9260. Wire a Boolean constant set to TRUE to the **Start** input of the FPGA I/O Node to send a synchronization pulse to the module. The AO**x** will be reset to 0 volts every time the device is put back into data mode.

Writing Data to the Module

When the module is in data mode, you can use an FPGA I/O Node to write data to the module. You can connect the AO input of the FPGA I/O Node to various types of functions, including an FPGA Memory function or an FPGA FIFO function. If you write to multiple channels on the module, place the channels in the same FPGA I/O Node to ensure that the VI writes the data synchronously.

Because the NI 9260 internally outputs data at a specified rate, the FPGA I/O Node does not finish until new data has been written to the module. If the NI 9260 is not in data mode while an FPGA I/O Node is running, the FPGA I/O Node returns an I/O Not Started error.

Exiting Data Mode

Configure an FPGA I/O Node with the **Stop** channel of the NI 9260. Write a TRUE to the **Stop** input. The module is no longer in data mode and you can now access NI 9260 properties.

NI recommends you ramp down to 0 volts before exiting data mode to prevent overshooting and ringing of the outputs due to the **Start** behavior. See **Putting the Module in Data Mode** above for the **Start** behavior.

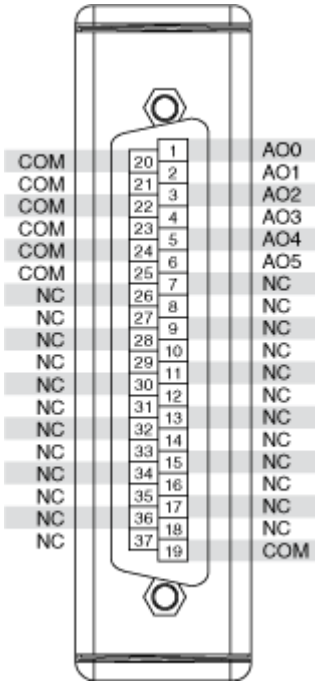
NI 9262

CompactRIO 1 MS/s/ch Simultaneous, ±10 V, 6-Channel C Series Voltage Output Module

Software Reference (?)

FPGA Interface

NI 9262 Pinout



Related Topics

FPGA Interface
Converting Voltage Values to Binary Values for the NI 9262/9263/9264/9269

NI 9262 (FPGA Interface)

CompactRIO 1 MS/s/ch Simultaneous, ±10 V, 6-Channel C Series Voltage Output Module

FPGA I/O Node

You can use an FPGA I/O Node, configured for writing, with this device.

Note You can simultaneously write to multiple channels on the NI 9262.

User-Controlled I/O Sampling

You can use the following User-Controlled I/O Sampling functions to perform I/O with more specific control over the I/O hardware on the FPGA.

Function	Type
Generate I/O Sample Pulse Method	Module function
Get I/O Write Status Method	I/O function
Write I/O Method	I/O function
Reset I/O Method	Module function

Note You must call the Reset I/O Method function first to prepare the NI 9262 to use the other User-Controlled I/O Sampling functions.

Terminals in Software

Use the FPGA I/O Node to access the following terminals for this device.

Terminal	Description
AO**x**	Analog output channel **x**, where **x** is the number of the channel. The NI 9262 has AO channels 0 to 5.

Arbitration

This device supports only the Arbitrate if Multiple Requestors Only option for arbitration. You cannot configure arbitration settings for this device.

Methods

This device does not support any methods.

I/O Properties

Use the FPGA I/O Property Node to access the following I/O properties for this device.

Property	Description
LSB Weight	Returns the LSB weight in nV/LSB for the channel. Use this value to convert NI 9262 data if you set the **Calibration Mode** to **Raw** in the C Series Module Properties dialog box.
Offset	Returns the calibration offset in nV for the channel. Use this value to convert NI 9262 data if you set the **Calibration Mode** to **Raw** in the **C Series Module Properties** dialog box.

Module Properties

Use the FPGA I/O Property Node to access the following module properties for this device.

Property	Description
Module ID	Returns the module ID.
Serial Number	Returns the unique serial number of the module.
Vendor ID	Returns the NI vendor ID, 0x1093.

Single-Cycle Timed Loop

This device does not support the single-cycle Timed Loop.

C Series Module Properties Dialog Box for the NI 9262/9263/9264/9269 (FPGA Interface)

Right-click an NI 9262, NI 9263, NI 9264, or NI 9269 C Series module in the **Project Explorer** window and select **Properties** from the shortcut menu to display this dialog box.

Use this dialog box to configure a C Series module.

This dialog box includes the following components:

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this option.
- **Location**—Specifies a slot in the chassis for the C Series module.
- **Calibration Mode**—Sets the calibration mode for the C Series module. Select **Calibrated** if you want the FPGA I/O Node to accept fixed-point data in units of volts when writing to the module. The fixed-point data is signed, with a word length of 20 bits and an integer word length of 5 bits. Select **Raw** if you want the FPGA I/O Node to accept calibrated, binary data when writing to the module. If you select **Raw**, you must convert the analog output values in the host VI before you write them to the module. The default is **Calibrated**.
- **Hot Swap Behavior**—Specifies the state of the output channels when the C Series module is removed and reinserted with the FPGA VI loaded and running. The power-on output state is the state that a C Series output module is in when power is applied to the module. The default is **Last output value**.

Converting Voltage Values to Binary Values for the NI 9262/9263/9264/9269 (FPGA Interface)

Set the **Calibration Mode** to **Calibrated** in the C Series Module Properties dialog box for the NI 9262/NI 9263/NI 9264/NI 9269 if you want the FPGA I/O Node to accept fixed-point data in units of volts when writing to the module. If you set the **Calibration Mode** to **Raw**, the FPGA I/O Node accepts only binary values when

writing to the module. You must convert output voltage values to binary values before you write them to the module. You must convert these values in the host VI.

Using an Equation to Convert Voltage to Binary

You can use the following equation in the host VI to convert the analog output values to binary values:

Binary Value = (**Voltage Value** × 10^9 – **Offset**) ÷ **LSB Weight**,

where

Binary Value is the value you write to the FPGA I/O Node

Voltage Value is the voltage in V that you want the channel to output

Offset is the value returned by the Offset property

LSB Weight is the value returned by the LSB Weight property.

NI recommends using calibrated values for analog output. To convert calibrated voltage values, use the FPGA I/O Property Node to read the LSB Weight and Offset properties. If you do not want to read the LSB Weight and Offset values from the module, you can convert uncalibrated voltage values by using the following values for **Offset** and **LSB Weight**:

Offset = 0

LSB Weight = **Typical Output Span** ÷ $2^{\textbf{DAC Resolution}}$ × 10^9

where

Typical Output Span is 21.4 V for the NI 9263, 21 V for the NI 9264, and 20.98 V for the NI 9269

DAC Resolution is the DAC resolution value in the hardware documentation for the module.

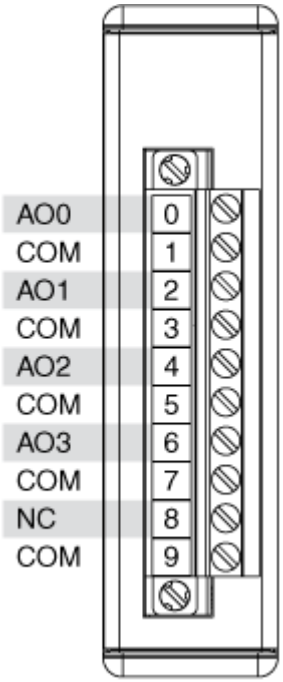
NI 9263

CompactRIO 4-Channel, ±10 V, 16-Bit Simultaneous Analog Output Module

Software Reference (?)

FPGA Interface | Scan Interface

NI 9263 Pinout



Related Topics

FPGA Interface
Converting Voltage Values to Binary Values for the NI 9263/9264/9269

NI 9263 (FPGA Interface)

CompactRIO 4-Channel, ±10 V, 16-Bit Simultaneous Analog Output Module

FPGA I/O Node

You can use an FPGA I/O Node, configured for writing, with this device.

Note You can simultaneously write to multiple channels on the NI 9263.

Terminals in Software

Use the FPGA I/O Node to access the following terminals for this device.

Terminal	Description
AO**x**	Analog output channel **x**, where **x** is the number of the channel. The NI 9263 has AO channels 0 t o 3.

Arbitration

This device supports only the Arbitrate if Multiple Requestors Only option for arbitration. You cannot configure arbitration settings for this device.

I/O Methods

This device does not support any I/O methods.

Module Methods

Use the FPGA I/O Method Node to access the following module methods for this device.

You should use these three methods in conjunction with each other. The Write Data method stores data values before writing the data to a channel, the Update method writes the stored data values to the output channel, and the Wait for Update method waits until the Update method updates the output channels.

Refer to the NI 9264 Advanced Write Methods VI in the `labview\examples\CompactRIO\Module Specific\NI 9264\NI 9264 Advanced Write Methods\NI 9264 Advanced Write Methods.lvproj` for an example of using these methods.

Method	Description
Update	Writes stored data values to the output channel. ▪ **Overrun**—Returns a Boolean value. A v alue of TRUE indicates an overrun warnin g. The overrun warning means that the Up

	date method is trying to run while the Write Data method is running, typically in a different loop. Either the Write Data method is writing data to the module too quickly or the Update method is running too slowly. ▪ **Underflow**—Returns a Boolean value. A value of TRUE indicates an underflow warning. The underflow warning means that the Write Data method has not written new data to the module since the last time the Update method ran. Either the Write Data method is writing data to the module too slowly or the Update method is running too quickly.
Wait for Update	Waits until the Update method updates the output channels. ▪ **Timeout (Ticks)**—Specifies in FPGA clock ticks how long the Wait for Update method waits for the Update method to update the output channels. A value of 0 causes the Wait for Update method to time out immediately, a negative value causes the Wait for Update method to wait indefinitely, and a positive value causes the Wait for Update method to wait for that number of clock ticks before timing out. ▪ **Timeout Occurred?**—Returns a Boolean value. A value of TRUE indicates that a timeout occurred.
Write Data	Stores data values before writing the data to a channel. ▪ **Channel**—Specifies the channel to which you want to write data. ▪ **Data**—Specifies the data you want to write to the channel.

I/O Properties

Use the FPGA I/O Property Node to access the following I/O properties for this device.

Property	Description
LSB Weight	Returns the LSB weight in nV/LSB for the channel. Use this value to convert NI 9263 data if you set the **Calibration Mode** to **Raw** in the C Series Module Properties dialog box.
Offset	Returns the calibration offset in nV for the channel. Use this value to convert NI 9263 data if you set the **Calibration Mode** to **Raw** in the **C Series Module Properties** dialog box.

Module Properties

Use the FPGA I/O Property Node to access the following module properties for this device.

Property	Description
Module ID	Returns the module ID.
Serial Number	Returns the unique serial number of the module.
Vendor ID	Returns the NI vendor ID, 0x1093.

Single-Cycle Timed Loop

This device does not support the single-cycle Timed Loop.

Converting Voltage Values to Binary Values for the NI 9262/9263/9264/9269 (FPGA Interface)

Set the **Calibration Mode** to **Calibrated** in the C Series Module Properties dialog box for the NI 9262/NI 9263/NI 9264/NI 9269 if you want the FPGA I/O Node to accept fixed-point data in units of volts when writing to the module. If you set the **Calibration Mode** to **Raw**, the FPGA I/O Node accepts only binary values when

writing to the module. You must convert output voltage values to binary values before you write them to the module. You must convert these values in the host VI.

Using an Equation to Convert Voltage to Binary

You can use the following equation in the host VI to convert the analog output values to binary values:

Binary Value = (**Voltage Value** × 10^9 – **Offset**) ÷ **LSB Weight**,

where

Binary Value is the value you write to the FPGA I/O Node

Voltage Value is the voltage in V that you want the channel to output

Offset is the value returned by the Offset property

LSB Weight is the value returned by the LSB Weight property.

NI recommends using calibrated values for analog output. To convert calibrated voltage values, use the FPGA I/O Property Node to read the LSB Weight and Offset properties. If you do not want to read the LSB Weight and Offset values from the module, you can convert uncalibrated voltage values by using the following values for **Offset** and **LSB Weight**:

Offset = 0

LSB Weight = **Typical Output Span** ÷ $2^{\textbf{DAC Resolution}}$ × 10^9

where

Typical Output Span is 21.4 V for the NI 9263, 21 V for the NI 9264, and 20.98 V for the NI 9269

DAC Resolution is the DAC resolution value in the hardware documentation for the module.

C Series Module Properties Dialog Box for the NI 9262/9263/9264/9269 (FPGA Interface)

Right-click an NI 9262, NI 9263, NI 9264, or NI 9269 C Series module in the **Project Explorer** window and select **Properties** from the shortcut menu to display this dialog box.

Use this dialog box to configure a C Series module.

This dialog box includes the following components:

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this option.
- **Location**—Specifies a slot in the chassis for the C Series module.
- **Calibration Mode**—Sets the calibration mode for the C Series module. Select **Calibrated** if you want the FPGA I/O Node to accept fixed-point data in units of volts when writing to the module. The fixed-point data is signed, with a word length of 20 bits and an integer word length of 5 bits. Select **Raw** if you want the FPGA I/O Node to accept calibrated, binary data when writing to the module. If you select **Raw**, you must convert the analog output values in the host VI before you write them to the module. The default is **Calibrated**.
- **Hot Swap Behavior**—Specifies the state of the output channels when the C Series module is removed and reinserted with the FPGA VI loaded and running. The power-on output state is the state that a C Series output module is in when power is applied to the module. The default is **Last output value**.

NI 9263 (Scan Interface)

CompactRIO 4-Channel, ±10 V, 16-Bit Simultaneous Analog Output Module


Open example

Module I/O Variables

To use I/O from this module in a VI, drag and drop I/O variables from the **Project Explorer** window to the block diagram of the VI. The I/O variables write floating-point values to the channels in volts.

Module Channels

The NI 9263 has the following channels.

Channel	Description
AO**x**	Analog output channel **x**, where **x** is the number of the channel. For the NI 9263, **x** is 0 to 3.

C Series Module Properties Dialog Box

Use this dialog box to configure the NI 9263. Right-click the NI 9263 in the **Project Explorer** window and select **Properties** to display this dialog box. You can configure the following options.

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this value.
- **Location**—Specifies a slot in the chassis for the C Series module.

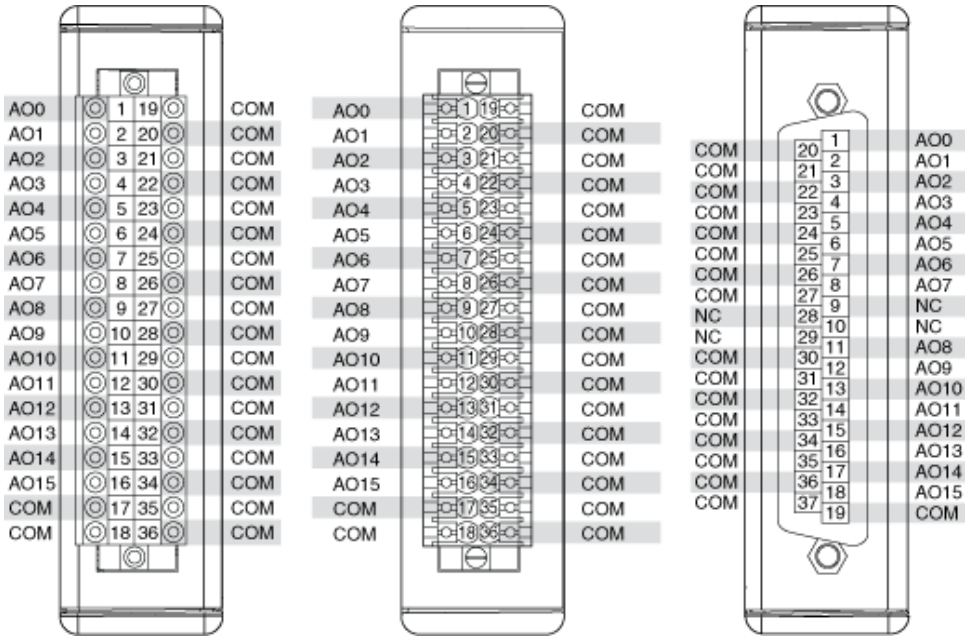
NI 9264

CompactRIO 16-Channel, ±10 V, 16-Bit Simultaneous Analog Voltage Output Module

Software Reference (?)

FPGA Interface | Scan Interface

NI 9264 Pinout



Related Topics

FPGA Interface
Converting Voltage Values to Binary Values for the NI 9263/9264/9269

NI 9264 (FPGA Interface)

CompactRIO 16-Channel, ±10 V, 16-Bit Simultaneous Analog Voltage Output Module

FPGA I/O Node

You can use an FPGA I/O Node, configured for writing, with this device.

Note You can simultaneously write to multiple channels on the NI 9264.

Terminals in Software

Use the FPGA I/O Node to access the following terminals for this device.

Terminal	Description

AO**x**	Analog output channel **x**, where **x** is the number of the channel. The NI 9264 has AO channels 0 to 15.

Arbitration

This device supports only the Arbitrate if Multiple Requestors Only option for arbitration. You cannot configure arbitration settings for this device.

I/O Methods

This device does not support any I/O methods.

Module Methods

Use the FPGA I/O Method Node to access the following module methods for this device.

You should use these three methods in conjunction with each other. The Write Data method stores data values before writing the data to a channel, the Update method writes the stored data values to the output channel, and the Wait for Update method waits until the Update method updates the output channels.

Refer to the NI 9264 Advanced Write Methods VI in the `labview\examples\CompactRIO\Module Specific\NI 9264\NI 9264 Advanced Write Methods\NI 9264 Advanced Write Methods.lvproj` for an example of using these methods.

Method	Description
Update	Writes stored data values to the output channel. ▪ **Overrun**—Returns a Boolean value. A value of TRUE indicates an overrun warning. The overrun warning means that the Update method is trying to run while the Write Data method is running, typically in a different loop. Either the Write Data method is writing data to the module too quickly o

	r the Update method is running too slowly . ▪ **Underflow**—Returns a Boolean value. A value of TRUE indicates an underflow w arning. The underflow warning means tha t the Write Data method has not written n ew data to the module since the last time the Update method ran. Either the Write D ata method is writing data to the module t oo slowly or the Update method is runnin g too quickly.
Wait for Update	Waits until the Update method updates the out put channels. ▪ **Timeout (Ticks)**—Specifies in FPGA cl ock ticks how long the Wait for Update me thod waits for the Update method to upda te the output channels. A value of 0 cause s the Wait for Update method to time out i mmediately, a negative value causes the Wait for Update method to wait indefinitel y, and a positive value causes the Wait for Update method to wait for that number of clock ticks before timing out. ▪ **Timeout Occurred?**—Returns a Boole an value. A value of TRUE indicates that a timeout occurred.
Write Data	Stores data values before writing the data to a c hannel. ▪ **Channel**—Specifies the channel to whi ch you want to write data. ▪ **Data**—Specifies the data you want to w rite to the channel.

I/O Properties

Use the FPGA I/O Property Node to access the following I/O properties for this device.

Property	Description
LSB Weight	Returns the LSB weight in nV/LSB for the channel. Use this value to convert NI 9264 data if you set the **Calibration Mode** to **Raw** in the C Series Module Properties dialog box.
Offset	Returns the calibration offset in nV for the channel. Use this value to convert NI 9264 data if you set the **Calibration Mode** to **Raw** in the **C Series Module Properties** dialog box.

Module Properties

Use the FPGA I/O Property Node to access the following module properties for this device.

Property	Description
Module ID	Returns the module ID.
Serial Number	Returns the unique serial number of the module.
Vendor ID	Returns the NI vendor ID, 0x1093.

Single-Cycle Timed Loop

This device does not support the single-cycle Timed Loop.

C Series Module Properties Dialog Box for the NI 9262/9263/9264/9269 (FPGA Interface)

Right-click an NI 9262, NI 9263, NI 9264, or NI 9269 C Series module in the **Project Explorer** window and select **Properties** from the shortcut menu to display this dialog box.

Use this dialog box to configure a C Series module.

This dialog box includes the following components:

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.

- **Module Type**—Specifies the type of C Series module. You cannot change this option.
- **Location**—Specifies a slot in the chassis for the C Series module.
- **Calibration Mode**—Sets the calibration mode for the C Series module. Select **Calibrated** if you want the FPGA I/O Node to accept fixed-point data in units of volts when writing to the module. The fixed-point data is signed, with a word length of 20 bits and an integer word length of 5 bits. Select **Raw** if you want the FPGA I/O Node to accept calibrated, binary data when writing to the module. If you select **Raw**, you must convert the analog output values in the host VI before you write them to the module. The default is **Calibrated**.
- **Hot Swap Behavior**—Specifies the state of the output channels when the C Series module is removed and reinserted with the FPGA VI loaded and running. The power-on output state is the state that a C Series output module is in when power is applied to the module. The default is **Last output value**.

Converting Voltage Values to Binary Values for the NI 9262/9263/9264/9269 (FPGA Interface)

Set the **Calibration Mode** to **Calibrated** in the C Series Module Properties dialog box for the NI 9262/NI 9263/NI 9264/NI 9269 if you want the FPGA I/O Node to accept fixed-point data in units of volts when writing to the module. If you set the **Calibration Mode** to **Raw**, the FPGA I/O Node accepts only binary values when writing to the module. You must convert output voltage values to binary values before you write them to the module. You must convert these values in the host VI.

Using an Equation to Convert Voltage to Binary

You can use the following equation in the host VI to convert the analog output values to binary values:

Binary Value = (**Voltage Value** × 10^9 – **Offset**) ÷ **LSB Weight**,

where

Binary Value is the value you write to the FPGA I/O Node

Voltage Value is the voltage in V that you want the channel to output

Offset is the value returned by the Offset property

LSB Weight is the value returned by the LSB Weight property.

NI recommends using calibrated values for analog output. To convert calibrated voltage values, use the FPGA I/O Property Node to read the LSB Weight and Offset properties. If you do not want to read the LSB Weight and Offset values from the module, you can convert uncalibrated voltage values by using the following values for **Offset** and **LSB Weight**:

Offset = 0

$$\textbf{LSB Weight} = \textbf{Typical Output Span} \div 2^{\textbf{DAC Resolution}} \times 10^{9}$$

where

Typical Output Span is 21.4 V for the NI 9263, 21 V for the NI 9264, and 20.98 V for the NI 9269

DAC Resolution is the DAC resolution value in the hardware documentation for the module.

NI 9264 (Scan Interface)

CompactRIO 16-Channel, ±10 V, 16-Bit Simultaneous Analog Voltage Output Module

Open example

Module I/O Variables

To use I/O from this module in a VI, drag and drop I/O variables from the **Project Explorer** window to the block diagram of the VI. The I/O variables write floating-point values to the channels in volts.

Module Channels

The NI 9264 has the following channels.

Channel	Description
AO**x**	Analog output channel **x**, where **x** is the number of the channel. For the NI 9264, **x** is 0 to 15.

C Series Module Properties Dialog Box

Use this dialog box to configure the NI 9264. Right-click the NI 9264 in the **Project Explorer** window and select **Properties** to display this dialog box. You can configure the following options.

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this value.
- **Location**—Specifies a slot in the chassis for the C Series module.

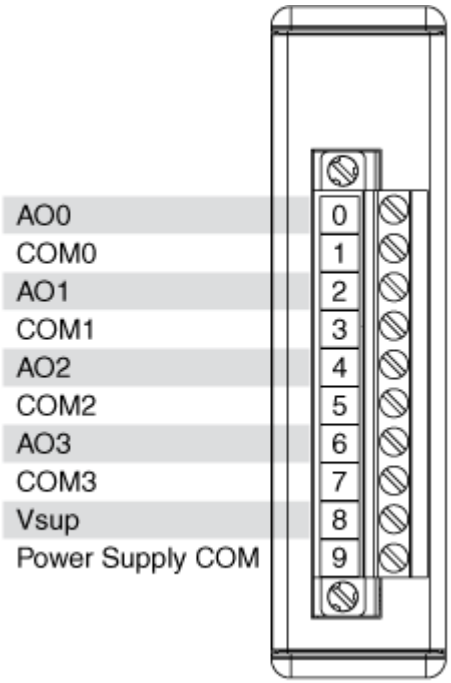
NI 9265

CompactRIO 4-Channel, 0–20 mA, 16-Bit Simultaneous Analog Current Output Module

Software Reference (?)

FPGA Interface | Scan Interface

NI 9265 Pinout



Related Topics

FPGA Interface
Converting Current Values to Binary Values for the NI 9265/9266

NI 9265 (FPGA Interface)

CompactRIO 4-Channel, 0–20 mA, 16-Bit Simultaneous Analog Current Output Module

Open example

Find related examples

FPGA I/O Node

You can use an FPGA I/O Node, configured for writing, with this device.

Note You can simultaneously write to multiple channels on the NI 9265.

Terminals in Software

Use the FPGA I/O Node to access the following terminals for this device.

Terminal	Description
AO**x**	Analog output channel **x**, where **x** is the number of the channel. The NI 9265 has AO channels 0 to 3.

Arbitration

This device supports only the Arbitrate if Multiple Requestors Only option for arbitration. You cannot configure arbitration settings for this device.

I/O Methods

This device does not support any I/O methods.

Module Methods

Use the FPGA I/O Method Node to access the following module methods for this device.

Refer to the NI 9265 Getting Started VI in the `labview\examples\CompactRIO\Module Specific\NI 9265\NI 9265 Getting Started\NI 9265 Getting Started.lvproj` for an example of using the Check Output Status methods.

You should use the Update, Wait for Update, and Write Data methods in conjunction with each other. The Write Data method stores data values before writing the data to a channel, the Update method writes the stored data values to the output channel, and the Wait for Update method waits until the Update method updates the output channels.

Refer to the NI 9264 Advanced Write Methods VI in the `labview\examples\CompactRIO\Module Specific\NI 9264\NI 9264 Advanced Write Methods\NI 9264 Advanced Write Methods.lvproj` for an example of using the Update, Wait for Update, and Write Data methods.

Method	Description
Check Cached Output Status	Returns Booleans that indicate whether the module or channels reported a power supply fault or an open current loop since the last execution of the Check Cached Output Status method. When the FPGA I/O Node communicates with the module, the FPGA VI samples the states of the module and channels and caches any TRUE value until the Check Cached Output Status method executes. ▪ **Force Status Read**—When the value of this input is FALSE, the method returns the cached status information since the last time that the Check Cached Output Status method executed. When the value is TRUE, the method forces the FPGA I/O Node to communicate with the module and update the status information. Forcing a status read can introduce jitter into an analog output loop. ▪ **Any Fault**—Returns a Boolean value. A value of TRUE indicates that the module has a power supply fault or at least one channel has an open current loop. ▪ **Power Supply Fault**—Returns a Boolean value. A value of TRUE indicates that the external power supply is out of the expected range. ▪ **Open Current Loop**—Returns an array of Boolean values. A value of TRUE in any index indicates that the channel sharing a number with that index has an open current loop and is configured to output a nonzero current value.
Check Output Status	Returns Booleans that indicate whether the module or channels reported a power supply fault or an open current loop during the last time the FPGA I/O Node communicated with the module. When the FPGA I/O Node communicates with th

	e module, the FPGA VI samples the states of the module and channels and overwrites the previo us output status with the latest state of the mod ule and channels. ▪ **Force Status Read**—When the value o f this input is FALSE, the method returns t he status information from the last time t he FPGA I/O Node communicated with the module. When the value is TRUE, the met hod forces the FPGA I/O Node to communi cate with the module and update the stat us information. Forcing a status read can i ntroduce jitter into an analog output loop. ▪ **Any Fault**—Returns a Boolean value. A value of TRUE indicates that the module h as a power supply fault or at least one cha nnel has an open current loop. ▪ **Power Supply Fault**—Returns a Bool ean value. A value of TRUE indicates that t he external power supply is out of the exp ected range. ▪ **Open Current Loop**—Returns an arra y of Boolean values. A value of TRUE in an y index indicates that the channel sharing a number with that index has an open cur rent loop and is configured to output a no nzero current value.
Update	Writes stored data values to the output channel. ▪ **Overrun**—Returns a Boolean value. A v alue of TRUE indicates an overrun warnin g. The overrun warning means that the Up date method is trying to run while the Che ck Cached Output Status, Check Output St atus, or Write Data method is running, typ ically in a different loop. The Update meth od cannot run while the Check Cached Ou tput Status, Check Output Status, or Write Data method is running. If the Update met hod is running at the same time as the Wri

	te Data method, then either the Write Dat a method is writing data to the module to o quickly or the Update method is runnin g too slowly. ▪ **Underflow**—Returns a Boolean value. A value of TRUE indicates an underflow w arning. The underflow warning means tha t the Write Data method has not written n ew data to the module since the last time the Update method ran. Either the Write D ata method is writing data to the module t oo slowly or the Update method is runnin g too quickly.
Wait for Update	Waits until the Update method updates the out put channels. ▪ **Timeout (Ticks)**—Specifies in FPGA cl ock ticks how long the Wait for Update me thod waits for the Update method to upda te the output channels. A value of 0 cause s the Wait for Update method to time out i mmediately, a negative value causes the Wait for Update method to wait indefinitel y, and a positive value causes the Wait for Update method to wait for that number of clock ticks before timing out. ▪ **Timeout Occurred?**—Returns a Boole an value. A value of TRUE indicates that a timeout occurred.
Write Data	Stores data values before writing the data to a c hannel. ▪ **Channel**—Specifies the channel to whi ch you want to write data. ▪ **Data**—Specifies the data you want to w rite to the channel.

I/O Properties

Use the FPGA I/O Property Node to access the following I/O properties for this device.

Property	Description
LSB Weight	Returns the LSB weight in pA/LSB for the channel. Use this value to convert NI 9265 data if you set the **Calibration Mode** to **Raw** in the C Series Module Properties dialog box.
Offset	Returns the calibration offset in pA for the channel. Use this value to convert NI 9265 data if you set the **Calibration Mode** to **Raw** in the **C Series Module Properties** dialog box.

Module Properties

Use the FPGA I/O Property Node to access the following module properties for this device.

Property	Description
Module ID	Returns the module ID.
Serial Number	Returns the unique serial number of the module.
Vendor ID	Returns the NI vendor ID, 0x1093.

Single-Cycle Timed Loop

This device does not support the single-cycle Timed Loop.

C Series Module Properties Dialog Box for the NI 9265 (FPGA Interface)

Right-click an NI 9265 C Series module in the **Project Explorer** window and select **Properties** from the shortcut menu to display this dialog box.

Use this dialog box to configure a C Series module.

This dialog box includes the following components:

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this option.
- **Location**—Specifies a slot in the chassis for the C Series module.
- **Calibration Mode**—Sets the calibration mode for the C Series module. Select **Calibrated** if you want the FPGA I/O Node to accept fixed-point data in units of amps when writing to the module. The fixed-point data is unsigned, with a word length of 20 bits and an integer word length of –5 bits. Select **Raw** if you want the FPGA I/O Node to accept calibrated, binary data when writing to the module. If you select **Raw**, you must convert the analog output values in the host VI before you write them to the module. The default is **Calibrated**.
- **Hot Swap Behavior**—Specifies the state of the output channels when the C Series module is removed and reinserted with the FPGA VI loaded and running. The power-on output state is the state that a C Series output module is in when power is applied to the module. The default is **Last output value**.

Converting Current Values to Binary Values for the NI 9265 (FPGA Interface)

Set the **Calibration Mode** to **Calibrated** in the C Series Module Properties dialog box for the NI 9265 if you want the FPGA I/O Node to accept fixed-point data in units of amps when writing to the module. If you set the **Calibration Mode** to **Raw**, the FPGA I/O Node accepts only binary values when writing to the module. You must convert output current values to binary values before you write them to the module. You must convert these values in the host VI.

Using an Equation to Convert Current to Binary

You can use the following equation in the host VI to convert the analog output values to binary values:

Binary Value = (**Current Value** × 10^{12} – **Offset**) ÷ **LSB Weight**

where

Binary Value is the value you write to the FPGA I/O Node

Current Value is the current in mA that you want the channel to output

Offset is the value returned by the Offset property

LSB Weight is the value returned by the LSB Weight property.

NI recommends using calibrated values for analog output. To convert calibrated current values, use the FPGA I/O Property Node to read the LSB Weight and Offset properties. If you do not want to read the LSB Weight and Offset values from the module, you can convert uncalibrated current values by using the following values for **Offset** and **LSB Weight**:

Offset = 0

LSB Weight = $20.6\ \text{mA} \div 2^{\textbf{DAC Resolution}} \times 10^{12}$

where

DAC Resolution is the DAC resolution value listed in the NI 9265 hardware documentation on ni.com/manuals.

NI 9265 (Scan Interface)

CompactRIO 4-Channel, 0–20 mA, 16-Bit Simultaneous Analog Current Output Module

Open example

Module I/O Variables

To use I/O from this module in a VI, drag and drop I/O variables from the **Project Explorer** window to the block diagram of the VI. The I/O variables write floating-point values to the channels in amps.

Module Channels

The NI 9265 has the following channels.

Channel	Description
AO**x**	Analog output channel **x**, where **x** is the number of the channel. For the NI 9265, **x** is 0 to 3.

Module-Specific Errors

The NI 9265 can return the following module-specific errors.

Error Code	Description
65542	One or more channels have detected an open current loop. Check the module connections.
65543	The power supply voltage level is out of range. Check the supply voltage and the module connections.

C Series Module Properties Dialog Box

Use this dialog box to configure the NI 9265. Right-click the NI 9265 in the **Project Explorer** window and select **Properties** to display this dialog box. You can configure the following options.

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this value.
- **Location**—Specifies a slot in the chassis for the C Series module.

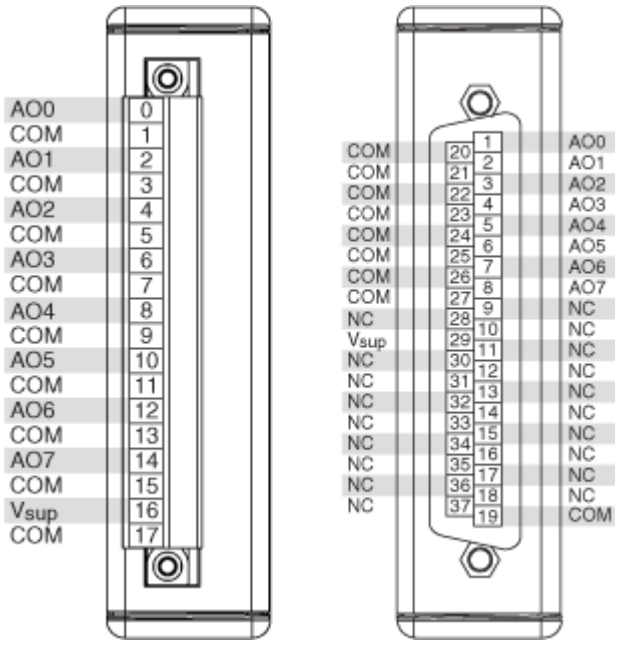
NI 9266

CompactRIO 8 AO, 0-20 mA, 16-Bit Simultaneous Analog Current Output Module

Software Reference (?)

FPGA Interface

NI 9266 Pinout



Related Topics

FPGA Interface
Converting Current Values to Binary Values for the NI 9266

NI 9266 (FPGA Interface)

CompactRIO 8 AO, 0-20 mA, 16-Bit Simultaneous Analog Current Output Module

Open example Find related examples

FPGA I/O Node

You can use an FPGA I/O Node, configured for writing, with this device.

Terminals in Software

Use the FPGA I/O Node to access the following terminals for this device.

Terminal	Description

AO**x**	Analog output channel **x**, where **x** is the number of the channel. The NI 9266 has AO channels 0 t o 7.

Arbitration

This device supports only the Arbitrate if Multiple Requestors Only option for arbitration. You cannot configure arbitration settings for this device.

I/O Methods

This device does not support any I/O methods.

Module Methods

Use the FPGA I/O Method Node to access the following module methods for this device.

Refer to the NI 9266 Getting Started VI in the `labview\examples\CompactRIO\Module Specific\NI 9266\NI 9266 Getting Started\NI 9266 Getting Started.lvproj` for an example of using the Check Output Status methods.

You should use the Update, Wait for Update, and Write Data methods in conjunction with each other. The Write Data method stores data values before writing the data to a channel, the Update method writes the stored data values to the output channel, and the Wait for Update method waits until the Update method updates the output channels.

Refer to the NI 9264 Advanced Write Methods VI in the `labview\examples\CompactRIO\Module Specific\NI 9264\NI 9264 Advanced Write Methods\NI 9264 Advanced Write Methods.lvproj` for an example of using the Update, Wait for Update, and Write Data methods.

Method	Description
Check Cached Output Status	Returns Booleans that indicate whether the mo dule or channels reported a power supply fault or an open current loop since the last execution of the Check Cached Output Status method. Wh

	en the FPGA I/O Node communicates with the module, the FPGA VI samples the states of the module and channels and caches any TRUE value until the Check Cached Output Status method executes. ▪ **Force Status Read**—When the value of this input is FALSE, the method returns the cached status information since the last time that the Check Cached Output Status method executed. When the value is TRUE, the method forces the FPGA I/O Node to communicate with the module and update the status information. Forcing a status read can introduce jitter into an analog output loop. ▪ **Any Fault**—Returns a Boolean value. A value of TRUE indicates that the module has a power supply fault or at least one channel has an open current loop. ▪ **Power Supply Fault**—Returns a Boolean value. A value of TRUE indicates that the external power supply is out of the expected range. ▪ **Open Current Loop**—Returns an array of Boolean values. A value of TRUE in any index indicates that the channel sharing a number with that index has an open current loop and is configured to output a nonzero current value.
Check Output Status	Returns Booleans that indicate whether the module or channels reported a power supply fault or an open current loop during the last time the FPGA I/O Node communicated with the module. When the FPGA I/O Node communicates with the module, the FPGA VI samples the states of the module and channels and overwrites the previous output status with the latest state of the module and channels.

	▪ **Force Status Read**—When the value of this input is FALSE, the method returns the status information from the last time the FPGA I/O Node communicated with the module. When the value is TRUE, the method forces the FPGA I/O Node to communicate with the module and update the status information. Forcing a status read can introduce jitter into an analog output loop. ▪ **Any Fault**—Returns a Boolean value. A value of TRUE indicates that the module has a power supply fault or at least one channel has an open current loop. ▪ **Power Supply Fault**—Returns a Boolean value. A value of TRUE indicates that the external power supply is out of the expected range. ▪ **Open Current Loop**—Returns an array of Boolean values. A value of TRUE in any index indicates that the channel sharing a number with that index has an open current loop and is configured to output a nonzero current value.
Update	Writes stored data values to the output channel. ▪ **Overrun**—Returns a Boolean value. A value of TRUE indicates an overrun warning. The overrun warning means that the Update method is trying to run while the Check Cached Output Status, Check Output Status, or Write Data method is running, typically in a different loop. The Update method cannot run while the Check Cached Output Status, Check Output Status, or Write Data method is running. If the Update method is running at the same time as the Write Data method, then either the Write Data method is writing data to the module too quickly or the Update method is running too slowly.

	▪ **Underflow**—Returns a Boolean value. A value of TRUE indicates an underflow warning. The underflow warning means that the Write Data method has not written new data to the module since the last time the Update method ran. Either the Write Data method is writing data to the module too slowly or the Update method is running too quickly.
Wait for Update	Waits until the Update method updates the output channels. ▪ **Timeout (Ticks)**—Specifies in FPGA clock ticks how long the Wait for Update method waits for the Update method to update the output channels. A value of 0 causes the Wait for Update method to time out immediately, a negative value causes the Wait for Update method to wait indefinitely, and a positive value causes the Wait for Update method to wait for that number of clock ticks before timing out. ▪ **Timeout Occurred?**—Returns a Boolean value. A value of TRUE indicates that a timeout occurred.
Write Data	Stores data values before writing the data to a channel. ▪ **Channel**—Specifies the channel to which you want to write data. ▪ **Data**—Specifies the data you want to write to the channel.

I/O Properties

Use the FPGA I/O Property Node to access the following I/O properties for this device.

Property	Description

LSB Weight	Returns the LSB weight in pA/LSB for the channel. Use this value to convert NI 9266 data if you set the **Calibration Mode** to **Raw** in the C Series Module Properties dialog box.
Offset	Returns the calibration offset in pA for the channel. Use this value to convert NI 9266 data if you set the **Calibration Mode** to **Raw** in the **C Series Module Properties** dialog box.

Module Properties

Use the FPGA I/O Property Node to access the following module properties for this device.

Property	Description
Module ID	Returns the module ID.
Serial Number	Returns the unique serial number of the module.
Vendor ID	Returns the NI vendor ID, 0x1093.

Single-Cycle Timed Loop

This device does not support the single-cycle Timed Loop.

C Series Module Properties Dialog Box for the NI 9266 (FPGA Interface)

Right-click an NI 9266 C Series module in the **Project Explorer** window and select **Properties** from the shortcut menu to display this dialog box.

Use this dialog box to configure a C Series module.

This dialog box includes the following components:

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this option.

- **Location**—Specifies a slot in the chassis for the C Series module.
- **Calibration Mode**—Sets the calibration mode for the C Series module. Select **Calibrated** if you want the FPGA I/O Node to accept fixed-point data in units of amps when writing to the module. The fixed-point data is unsigned, with a word length of 20 bits and an integer word length of –5 bits. Select **Raw** if you want the FPGA I/O Node to accept calibrated, binary data when writing to the module. If you select **Raw**, you must convert the analog output values in the host VI before you write them to the module. The default is **Calibrated**.
- **Hot Swap Behavior**—Specifies the state of the output channels when the C Series module is removed and reinserted with the FPGA VI loaded and running. The power-on output state is the state that a C Series output module is in when power is applied to the module. The default is **Last output value**.

Converting Current Values to Binary Values for the NI 9266 (FPGA Interface)

Set the **Calibration Mode** to **Calibrated** in the C Series Module Properties dialog box for the NI 9266 if you want the FPGA I/O Node to accept fixed-point data in units of amps when writing to the module. If you set the **Calibration Mode** to **Raw**, the FPGA I/O Node accepts only binary values when writing to the module. You must convert output current values to binary values before you write them to the module. You must convert these values in the host VI.

Using an Equation to Convert Current to Binary

You can use the following equation in the host VI to convert the analog output values to binary values:

Binary Value = (**Current Value** × 10^{12} – **Offset**) ÷ **LSB Weight**

where

Binary Value is the value you write to the FPGA I/O Node

Current Value is the current in mA that you want the channel to output

Offset is the value returned by the Offset property

LSB Weight is the value returned by the LSB Weight property.

NI recommends using calibrated values for analog output. To convert calibrated current values, use the FPGA I/O Property Node to read the LSB Weight and Offset properties. If you do not want to read the LSB Weight and Offset values from the module, you can convert uncalibrated current values by using the following values for **Offset** and **LSB Weight**:

Offset = 0

LSB Weight = $20.89\ mA \div 2^{\textbf{DAC Resolution}} \times 10^{12}$

where	**DAC Resolution** is the DAC resolution value listed in the NI 9266 hardware documentation on ni.com/manuals.

NI 9266 (Scan Interface)

CompactRIO 8 AO, 0-20 mA, 16-Bit Simultaneous Analog Current Output Module


Open example

Module I/O Variables

To use I/O from this module in a VI, drag and drop I/O variables from the **Project Explorer** window to the block diagram of the VI. The I/O variables write floating-point values to the channels in amps.

Module Channels

The NI 9266 has the following channels.

Channel	Description
AO**x**	Analog output channel **x**, where **x** is the number of the channel. For the NI 9266, **x** is 0 to 7.

Module-Specific Errors

The NI 9266 can return the following module-specific errors.

Error Code	Description

65542	One or more channels have detected an open current loop. Check the module connections.
65543	The power supply voltage level is out of range. Check the supply voltage and the module connections.

C Series Module Properties Dialog Box

Use this dialog box to configure the NI 9266. Right-click the NI 9266 in the **Project Explorer** window and select **Properties** to display this dialog box. You can configure the following options.

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this value.
- **Location**—Specifies a slot in the chassis for the C Series module.

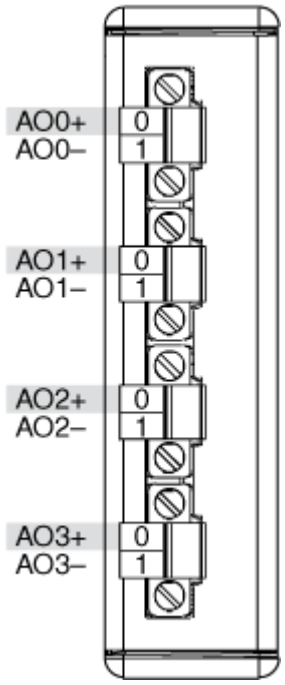
NI 9269

CompactRIO 4-Channel, ±10 V, 16-Bit Simultaneous Isolated Analog Output Module

Software Reference (?)

FPGA Interface | Scan Interface

NI 9269 Pinout



Related Topics

FPGA Interface
Converting Voltage Values to Binary Values for the NI 9263/9264/9269

NI 9269 (FPGA Interface)

CompactRIO 4-Channel, ±10 V, 16-Bit Simultaneous Isolated Analog Output Module

FPGA I/O Node

You can use an FPGA I/O Node, configured for writing, with this device.

Note You can simultaneously write to multiple channels on the NI 9269.

Terminals in Software

Use the FPGA I/O Node to access the following terminals for this device.

Terminal	Description

AO**x**	Analog output channel **x**, where **x** is the number of the channel. The NI 9269 has AO channels 0 to 3.

Arbitration

This device supports only the Arbitrate if Multiple Requestors Only option for arbitration. You cannot configure arbitration settings for this device.

I/O Methods

This device does not support any I/O methods.

Module Methods

Use the FPGA I/O Method Node to access the following module methods for this device.

Refer to the NI 9269 Status Methods VI in the `labview\examples\CompactRIO\Module Specific\NI 9269\NI 9269 Status Methods\NI 9269 Status Methods.lvproj` for an example of using the Check Cached Output Status and Check Output Status methods.

You should use the Update, Wait for Update, and Write Data methods in conjunction with each other. The Write Data method stores data values before writing the data to a channel, the Update method writes the stored data values to the output channel, and the Wait for Update method waits until the Update method updates the output channels.

Refer to the NI 9264 Advanced Write Methods VI in the `labview\examples\CompactRIO\Module Specific\NI 9264\NI 9264 Advanced Write Methods\NI 9264 Advanced Write Methods.lvproj` for an example of using the Update, Wait for Update, and Write Data methods.

Method	Description
Check Cached Output Status	Returns Booleans for the module and each channel that indicate whether the module or channels reported an overcurrent condition since the last execution of the Check Cached Output Status

	method. When the FPGA I/O Node communicates with the module, the FPGA VI samples the overcurrent states of the module and channels and caches any TRUE value until the Check Cached Output Status method executes. ▪ **Force Status Read**—When the value of this input is FALSE, the method returns the cached status information since the last time that the Check Cached Output Status method executed. When the value is TRUE, the method forces the FPGA I/O Node to communicate with the module and update the status information. Forcing a status read can introduce jitter into an analog output loop. ▪ **Any Fault**—Returns a Boolean value. A value of TRUE indicates that the module or at least one channel is in an overcurrent condition. ▪ **Module Overcurrent**—Returns a Boolean value. A value of TRUE indicates that the module is in an overcurrent condition. ▪ **Channel Overcurrent**—Returns an array of Boolean values. A value of TRUE in any index indicates that the channel sharing a number with that index is in an overcurrent condition.
Check Output Status	Returns Booleans for the module and each channel that indicate whether the module or channels reported an overcurrent condition during the last time the FPGA I/O Node communicated with the module. When the FPGA I/O Node communicates with the module, the FPGA VI samples the overcurrent states of the module and channels and overwrites the previous output status with the latest overcurrent state of the module and channels. ▪ **Force Status Read**—When the value of this input is FALSE, the method returns t

	he status information from the last time t he FPGA I/O Node communicated with the module. When the value is TRUE, the met hod forces the FPGA I/O Node to communi cate with the module and update the stat us information. Forcing a status read can i ntroduce jitter into an analog output loop. ▪ **Any Fault**—Returns a Boolean value. A value of TRUE indicates that the module o r at least one channel is in an overcurrent condition. ▪ **Module Overcurrent**—Returns a Bool ean value. A value of TRUE indicates that t he module is in an overcurrent condition. ▪ **Channel Overcurrent**—Returns an ar ray of Boolean values. A value of TRUE in a ny index indicates that the channel sharin g a number with that index is in an overcu rrent condition.
Update	Writes stored data values to the output channel. ▪ **Overrun**—Returns a Boolean value. A v alue of TRUE indicates an overrun warnin g. The overrun warning means that the Up date method is trying to run while the Che ck Cached Output Status, Check Output St atus, or Write Data method is running, typ ically in a different loop. The Update meth od cannot run while the Check Cached Ou tput Status, Check Output Status, or Write Data method is running. If the Update met hod is running at the same time as the Wri te Data method, then either the Write Dat a method is writing data to the module to o quickly or the Update method is runnin g too slowly. ▪ **Underflow**—Returns a Boolean value. A value of TRUE indicates an underflow w arning. The underflow warning means tha t the Write Data method has not written n

	ew data to the module since the last time the Update method ran. Either the Write Data method is writing data to the module too slowly or the Update method is running too quickly.
Wait for Update	Waits until the Update method updates the output channels. ▪ **Timeout (Ticks)**—Specifies in FPGA clock ticks how long the Wait for Update method waits for the Update method to update the output channels. A value of 0 causes the Wait for Update method to time out immediately, a negative value causes the Wait for Update method to wait indefinitely, and a positive value causes the Wait for Update method to wait for that number of clock ticks before timing out. ▪ **Timeout Occurred?**—Returns a Boolean value. A value of TRUE indicates that a timeout occurred.
Write Data	Stores data values before writing the data to a channel. ▪ **Channel**—Specifies the channel to which you want to write data. ▪ **Data**—Specifies the data you want to write to the channel.

I/O Properties

Use the FPGA I/O Property Node to access the following I/O properties for this device.

Property	Description
LSB Weight	Returns the LSB weight in nV/LSB for the channel. Use this value to convert NI 9269 data if you set the **Calibration Mode** to **Raw** in the C Series Module Properties dialog box.

Offset	Returns the calibration offset in nV for the channel. Use this value to convert NI 9269 data if you set the **Calibration Mode** to **Raw** in the **C Series Module Properties** dialog box.

Module Properties

Use the FPGA I/O Property Node to access the following module properties for this device.

Property	Description
Module ID	Returns the module ID.
Serial Number	Returns the unique serial number of the module.
Vendor ID	Returns the NI vendor ID, 0x1093.

Single-Cycle Timed Loop

This device does not support the single-cycle Timed Loop.

C Series Module Properties Dialog Box for the NI 9262/9263/9264/9269 (FPGA Interface)

Right-click an NI 9262, NI 9263, NI 9264, or NI 9269 C Series module in the **Project Explorer** window and select **Properties** from the shortcut menu to display this dialog box.

Use this dialog box to configure a C Series module.

This dialog box includes the following components:

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this option.
- **Location**—Specifies a slot in the chassis for the C Series module.

- **Calibration Mode**—Sets the calibration mode for the C Series module. Select **Calibrated** if you want the FPGA I/O Node to accept fixed-point data in units of volts when writing to the module. The fixed-point data is signed, with a word length of 20 bits and an integer word length of 5 bits. Select **Raw** if you want the FPGA I/O Node to accept calibrated, binary data when writing to the module. If you select **Raw**, you must convert the analog output values in the host VI before you write them to the module. The default is **Calibrated**.
- **Hot Swap Behavior**—Specifies the state of the output channels when the C Series module is removed and reinserted with the FPGA VI loaded and running. The power-on output state is the state that a C Series output module is in when power is applied to the module. The default is **Last output value**.

Converting Voltage Values to Binary Values for the NI 9262/9263/9264/9269 (FPGA Interface)

Set the **Calibration Mode** to **Calibrated** in the C Series Module Properties dialog box for the NI 9262/NI 9263/NI 9264/NI 9269 if you want the FPGA I/O Node to accept fixed-point data in units of volts when writing to the module. If you set the **Calibration Mode** to **Raw**, the FPGA I/O Node accepts only binary values when writing to the module. You must convert output voltage values to binary values before you write them to the module. You must convert these values in the host VI.

Using an Equation to Convert Voltage to Binary

You can use the following equation in the host VI to convert the analog output values to binary values:

Binary Value = (**Voltage Value** × 10^9 – **Offset**) ÷ **LSB Weight**,

where

Binary Value is the value you write to the FPGA I/O Node

Voltage Value is the voltage in V that you want the channel to output

Offset is the value returned by the Offset property

LSB Weight is the value returned by the LSB Weight property.

NI recommends using calibrated values for analog output. To convert calibrated voltage values, use the FPGA I/O Property Node to read the LSB Weight and Offset properties. If you do not want to read the LSB Weight and Offset values from the module, you can convert uncalibrated voltage values by using the following values for **Offset** and **LSB Weight**:

Offset = 0

LSB Weight = **Typical Output Span** ÷ $2^{\textbf{DAC Resolution}}$ × 10^{9}

where

Typical Output Span is 21.4 V for the NI 9263, 21 V for the NI 9264, and 20.98 V for the NI 9269

DAC Resolution is the DAC resolution value in the hardware documentation for the module.

NI 9269 (Scan Interface)

CompactRIO 4-Channel, ±10 V, 16-Bit Simultaneous Isolated Analog Output Module


Open example

Module I/O Variables

To use I/O from this module in a VI, drag and drop I/O variables from the **Project Explorer** window to the block diagram of the VI. The I/O variables write floating-point values to the channels in volts.

Module Channels

The NI 9269 has the following channels.

Channel	Description
AO**x**	Analog output channel **x**, where **x** is the number of the channel. For the NI 9269, **x** is 0 to 3.

Module-Specific Errors

The NI 9269 can return the following module-specific errors.

Error Code	Description

65548	One or more channels are in overcurrent or over voltage protection mode. Check the terminals fo r any fault condition that could be causing an ou t-of-range voltage or current on the channels.
65579	The module is in overcurrent protection mode. Check the terminals for any fault condition that could be causing an out-of-range current.

C Series Module Properties Dialog Box

Use this dialog box to configure the NI 9269. Right-click the NI 9269 in the **Project Explorer** window and select **Properties** to display this dialog box. You can configure the following options.

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this value.
- **Location**—Specifies a slot in the chassis for the C Series module.

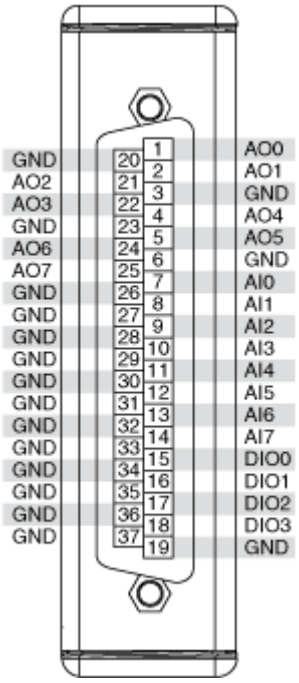
NI 9381

CompactRIO 0 V to 5 V, 12-bit, Multifunction Input/Output Module

Software Reference (?)

FPGA Interface | Scan Interface

NI 9381 Pinout



Running AI and AO Operations Concurrently on the NI 9381

AI and AO operations that are run concurrently may exhibit jitter. Access both subsystems using a single I/O Node to avoid jitter in your application. Refer to the Avoiding Timing Uncertainty topic for more information.

Related Topics

FPGA Interface
Converting and Calibrating CompactRIO Analog Input Values
Detecting Out-of-Range Channels
Avoiding Timing Uncertainty with the NI 9381
Converting Voltage Values to Binary Values for the NI 9381

NI 9381 (FPGA Interface)

CompactRIO 0 V to 5 V, 12-bit, Multifunction Input/Output Module

Find NI 9381 examples

FPGA I/O Node

You can use an FPGA I/O Node, configured for reading and writing, with this device.

Terminal	Description
AI**x**	Analog input channel **x**, where **x** is the number of the channel. The NI 9381 has AI channels 0 to 7.
AO**x**	Analog output channel **x**, where **x** is the number of the channel. The NI 9381 has AO channels 0 to 3.
DIO**x**	Digital input/output channel **x**, where **x** is the number of the channel. The NI 9381 has DIO channels 0 to 3.
DIO3:0	Digital port consisting of channels 0 through 3. Channel 3 is returned in the MSB, and channel 0 is returned in the LSB.

Caution AI and AO operations that are run concurrently may exhibit jitter. Access both subsystems using a single I/O Node to avoid jitter in your application. Refer to the Avoiding Timing Uncertainty topic for more information.

Arbitration

Analog input and analog output channels of this device support only the Arbitrate if Multiple Requestors Only option for arbitration. You cannot configure arbitration settings for analog input and analog output channels of this device.

You can configure the arbitration settings for digital output channels of this device in the Advanced Code Generation page of the FPGA I/O Properties dialog box. The default arbitration setting is Never Arbitrate.

Digital input channels of this device support only the **Never Arbitrate** option for arbitration. You cannot configure arbitration settings for the digital input channels of this device.

I/O Methods

Use the FPGA I/O Method Node to access the following I/O methods for the DIO channels of this device.

Method	Description
Set Output Data	Refer to the FPGA I/O Method Node (FPGA Module) topic for a description of this method. This method is available only when you set the DIO line direction to output. You can set the DIO line direction in the C Series Module Properties dialog box.
Set Output Enable	Sets the line direction of the digital channel or the DIO3:0 digital port. Refer to the FPGA I/O Method Node (FPGA Module) topic for more information on this method. This method can introduce jitter in an analog input or analog output loop. This method is available only when you enable programmable DIO line changes on the module. You can enable programmable DIO line changes on the module in the C Series Module Properties dialog box.
Wait on Any Edge	Pauses the execution of the I/O Method Node until the next falling or rising edge of the digital signal. The **Timeout** input specifies in FPGA clock ticks how long the Wait on Any Edge method waits for the next falling or rising edge. A value of 0 causes the method to time out immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out. **Notes** This method is not available on the DIO3:0 port. For the first two seconds after resetting the F

	PGA VI, the time out wil l not start counting unt il the module is identifi ed.
Wait on Falling Edge	Pauses the execution of the I/O Method Node un til the next falling edge of the digital signal. The **Timeout** input specifies in FPGA clock ticks ho w long the Wait on Falling Edge method waits fo r the next falling edge. A value of 0 causes the m ethod to time out immediately, a negative value causes the method to wait indefinitely, and a po sitive value causes the method to wait for that n umber of clock ticks before timing out.  **Notes** This method is not available on the DI O3:0 port. For the first two secon ds after resetting the F PGA VI, the time out wil l not start counting unt il the module is identifi ed.
Wait on High Level	Pauses the execution of the I/O Method Node un til the digital signal is high. The **Timeout** input specifies in FPGA clock ticks how long the Wait o n High Level method waits for the next high leve l. A value of 0 causes the method to time out im mediately, a negative value causes the method t o wait indefinitely, and a positive value causes t he method to wait for that number of clock ticks before timing out.  **Notes** This method is not available on the DI O3:0 port. For the first two secon ds after resetting the F PGA VI, the time out wil

	l not start counting unt il the module is identifi ed.
Wait on Low Level	Pauses the execution of the I/O Method Node un til the digital signal is low. The **Timeout** input s pecifies in FPGA clock ticks how long the Wait o n Low Level method waits for the next low level. A value of 0 causes the method to time out imm ediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks be fore timing out. **Notes** This method is not available on the DI O3:0 port. For the first two secon ds after resetting the F PGA VI, the time out wil l not start counting unt il the module is identifi ed.
Wait on Rising Edge	Pauses the execution of the I/O Method Node un til the next rising edge of the digital signal. The **Timeout** input specifies in FPGA clock ticks ho w long the Wait on Rising Edge method waits for the next rising edge. A value of 0 causes the met hod to time out immediately, a negative value c auses the method to wait indefinitely, and a pos itive value causes the method to wait for that nu mber of clock ticks before timing out. **Notes** This method is not available on the DI O3:0 port. For the first two secon ds after resetting the F PGA VI, the time out wil l not start counting unt

	il the module is identifi ed.

Module Method

Use the FPGA I/O Method Node to access the following module method for this device.

Method	Description
Check Status	Returns a Boolean value that indicates whether the module is ready.

I/O Properties

Use the FPGA I/O Property Node to access the following I/O properties for AI and AO channels of this device.

Property	Description
LSB Weight	Returns the LSB weight in nV/LSB for the channe l. Use this value to convert and calibrate NI 9381 data if you set the **Calibration Mode** to **Raw** i n the C Series Module Properties dialog box.
Offset	Returns the calibration offset in nV for the chan nel. Use this value to convert and calibrate NI 93 81 data if you set the **Calibration Mode** to **Ra w** in the **C Series Module Properties** dialog b ox.

Module Properties

Use the FPGA I/O Property Node to access the following module properties for this device.

Property	Description
Module ID	Returns the module ID.
Serial Number	Returns the unique serial number of the module .
Vendor ID	Returns the NI vendor ID, 0x1093.

Single-Cycle Timed Loop

This device supports the single-cycle Timed Loop. Configure the number of input synchronizing registers for the channels of this device in the Advanced Code Generation page of the FPGA I/O Node Properties dialog box. Configure the number of output synchronizing registers for the channels of this device in the Advanced Code Generation page of the FPGA I/O Properties dialog box.

This device supports the Number of Synchronizing Registers for Output Data synchronizing register option when used in SCTL output. This option supports the same functionality as the **Number of Synchronizing Registers for Output Data** option described in the Advanced Code Generation FPGA I/O Properties Page (FPGA Module) topic, with the exception that you can use this option only in a single-cycle Timed Loop. You can implement either 0 or 1 synchronizing registers inside the single-cycle Timed Loop, however, if you configure 0 synchronizing registers outside of the single-cycle Timed Loop, the FPGA VI implements 1 synchronizing register by default.

When the device is within a single-cycle Timed Loop, it must be ready to perform digital I/O before a loop containing digital I/O starts. Poll the **Ready** output of the Check Status method to determine whether the module is ready. Digital input operations return invalid data if the module is not ready. The module also might ignore or delay digital output operations if it is not ready.

While the digital is performing digital I/O within a single-cycle Timed Loop, do not perform property reads or remove the module from the chassis. Doing any of these actions causes the module to be unable to perform digital I/O and the **Ready** output of the Check Status method to return FALSE.

FPGA Target Clock Support

This device supports only top-level FPGA target clock rates and single-cycle Timed Loop clock rates that are multiples of 40 MHz, such as 40 MHz, 80 MHz, 120 MHz, and so on.

Avoiding Timing Uncertainty with the NI 9381 (FPGA Interface)

Follow these guidelines to avoid introducing timing uncertainty into AI node, AO Node, DO Node, and Set Output Data method calls. Additionally, failing to follow

these guidelines may result in lost data points for DO Node calls or Set Output Data method calls when either of them are made from inside a single-cycle Timed Loop.

- Use a single I/O Node to access AI and AO operations to ensure proper sequencing.
- Do not run the Set Output Enable method when an AI, AO, or DO subsystems is active.
- Do not perform the following operations concurrently:
  - AI Node call
  - AO Node call
  - Set Output Enable method call
  - Automatic line direction change when a DO call is made under the following conditions:
    - The call is made from outside of a single-cycle Timed Loop.
    - The **Allow programmatic DIO line direction** checkbox is checked in the C Series Module Properties dialog box.
    - The DIO channel is configured as an input at the time when the DO node is called.

Refer to the NI 9381 Advanced IO VI in the `labview\examples\CompactRIO\Module Specific\NI 9381\NI 9381 Advanced IO\NI 9381 Advanced IO.lvproj` for an example of the recommended way to use the AI, AO , and DIO subsystems.

C Series Module Properties Dialog Box for the NI 9381 (FPGA Interface)

Right-click an NI 9381 C Series module in the **Project Explorer** window and select **Properties** from the shortcut menu to display this dialog box.

Use this dialog box to configure a C Series module.

This dialog box includes the following components:

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this option.
- **Location**—Specifies a slot in the chassis for the C Series module.
- **Calibration Mode**—Sets the calibration mode for the C Series module. Select **Calibrated** if you want the FPGA I/O Node to return calibrated, fixed-point data from the module in units of volts. The fixed-point data is unsigned, with a word length of 18 bits and an integer word length of 3 bits for the analog input channels and a word length of 16 bits and an integer word length of 3 bits for the analog output channels. Select **Raw** if you want the FPGA I/O Node to return uncalibrated, binary data from the module. If you select **Raw**, you must convert and calibrate the analog input values in the host VI. The default is **Calibrated**.
- **Channels**—Specifies the channel(s) for which you want to select the direction.
- **Selected Channel(s) Settings**—Specifies the direction for each channel.
- **Hot Swap Behavior (Analog Output)**—Specifies the state of the analog output channels when the C Series module is removed and reinserted with the FPGA VI loaded and running. The power-on output state is the state that a C Series output module is in when power is applied to the module. The default is Last output value.
- **Allow Programmatic DIO Line Direction Change**—Place a checkmark in this checkbox if you want to enable programmable DIO line changes on the module.

Caution Performing a DIO line direction change will affect the timing of any concurrent AI, AO, and DO operations. Refer to the Avoiding Timing Uncertainty topic for more information.

Converting Voltage Values to Binary Values for the NI 9381 (FPGA Interface)

Set the **Calibration Mode** to **Calibrated** in the C Series Module Properties dialog box for the NI 9381 if you want the FPGA I/O Node to accept fixed-point data in units of volts when writing to the module. If you set the **Calibration Mode** to **Raw**, the FPGA I/O Node accepts only binary values when writing to the module. You must convert output voltage values to binary values before you write them to the module. You must convert these values in the host VI.

Using an Equation to Convert Voltage to Binary

You can use the following equation in the host VI to convert the analog output values to binary values:

Binary Value = (**Voltage Value** – **Offset**) ÷ **LSB Weight**

where	**Binary Value** is the value you write to the FPGA I/O Node
	Current Value is the voltage in V that you want the channel to output
	Offset is the value returned by the Offset property
	LSB Weight is the value returned by the LSB Weight property

NI recommends using calibrated values for analog output. To convert calibrated voltage values, use the FPGA I/O Property Node to read the LSB Weight and Offset properties. If you do not want to read the LSB Weight and Offset values from the module, you can convert uncalibrated voltage values by using the following values for **Offset** and **LSB Weight**:

Offset = –5249

LSB Weight = $5.105\ V \div 2^{\textbf{DAC Resolution}}$

where	**DAC Resolution** is the DAC resolution value in the **NI 9381 Operating Instructions and Specifications**.

NI 9381 (Scan Interface)

CompactRIO 0 V to 5 V, 12-bit, Multifunction Input/Output Module

Module I/O Variables

To use I/O from this module in a VI, drag and drop I/O variables from the **Project Explorer** window to the block diagram of the VI. The I/O variables for the AI channels return floating-point data in volts. The I/O variables for the AO channels write floating-point data in volts. The I/O variables for the DIO channels read and write boolean values.

Module Channels

The NI 9381 has the following channels.

Channel	Description
AI**x**	Analog input channel **x**, where **x** is the number of the channel. For the NI 9381, **x** is 0 to 7.
AO**x**	Analog output channel **x**, where **x** is the number of the channel. For the NI 9381, **x** is 0 to 7.
DIO**x**	Digital input/output channel **x**, where **x** is the n umber of the channel. For the NI 9381, **x** is 0 to 3 .

C Series Module Properties Dialog Box

Use this dialog box to configure the NI 9381. Right-click the NI 9381 in the **Project Explorer** window and select **Properties** to display this dialog box. You can configure the following options.

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Type**—Specifies the type of C Series module. You cannot change this value.
- **Location**—Specifies a slot in the chassis for the C Series module.

- **Channels**—Specifies the channel(s) for which you want to configure settings.
- **Direction**—Specifies the initial line direction of the selected channel(s) as input or output.

Note If you are using direct access to read from or write to AI or AO channels of the NI 9381, the conversion time is somewhat longer than 50 µs.

Counter Input Modules

Use this book as a reference for the following information:

- FPGA I/O functions, I/O resources, arbitration options, methods, and properties each C Series counter input module supports in FPGA Interface mode
- Instructions for using LabVIEW with CompactRIO counter input devices

To view related topics, click the **Locate** button, shown at left, in the toolbar at the top of this window. The **LabVIEW Help** highlights this topic in the **Contents** tab so you can navigate the related topics.

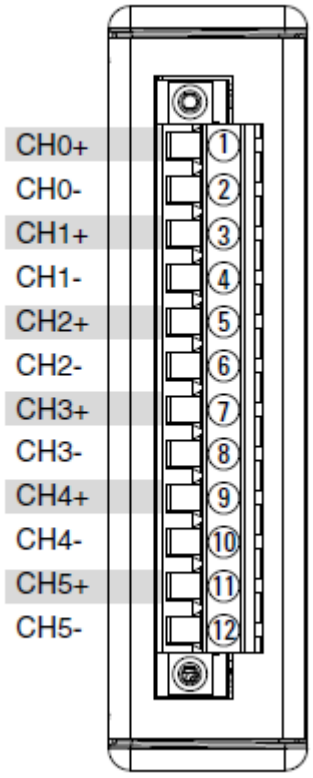
NI 9326

CompactRIO 6-Channel, Frequency Input Module

Software Reference (?)

FPGA Interface

NI 9326 Pinout



Related Topics

FPGA Interface

Synchronizing Multiple NI 9326 Modules

NI 9326 (FPGA Interface)

CompactRIO 6-Channel, Frequency Input Module

FPGA I/O Node

You can use an FPGA I/O Node, configured for reading, with this device.

Terminals in Software

Use the FPGA I/O Node to access the following terminals for this device.

Terminal	Description
CTR**x**	Counter input channel **x**, where **x** is the number of the channel. The counter I/O node returns a cluster of three items, consisting of two unsigned 32-bit integers called A and B as well as the counter status enum. The **Start** input I/O node must be executed before counter or DI data can be read. The NI 9326 has counters 0 through 5.
DI**x**	Digital input channel **x**, where **x** is the number of the channel. The NI 9326 has DI channels 0 through 5. Supported in Digital Input Mode.
Start	Channel that controls when the counters begin monitoring their input terminals. If TRUE is written to the **Start** channel, the NI 9326 counters are reset, armed, and begin monitoring their input terminals to perform the currently configured measurement (such as Edge Counting). Once the NI 9326 counters are armed, you may execute the **CTRx** and **DIx** I/O nodes to read the counter data. You may not execute any NI 9326 I/O Method or Property nodes while the counters are armed. To disarm the counters, use the **Stop** channel. If FALSE is written to the **Start** channel, no operation is performed. The **Start** channel is also used to synchronize multiple NI 9326 modules.
Stop	Channel that controls when the counters are disarmed. If TRUE is written to the **Stop** channel, the counters are stopped. When the counters are stopped, you may change the counter configuration by executing I/O Method and Property nodes. If FALSE is written to the **Stop** channel, no operation is performed.

The definition of **A** and **B** values vary according to the measurement mode you select. The following table defines the **A** and **B** values for each measurement mode option.

Measurement Mode	A	B	Status

Edge Counting	Number of edges.	Unused. Always returns 0.	Not applicable.
Period	Amount of time elapsed during **B** signal periods, measured in units of counter timebase ticks.	Scaling factor for **A** value. Divide **A** by **B** to calculate the measured period.	Applicable.

Period measurements are returned based on ticks of the module's 100 MHz timebase. Each tick corresponds to 10 ns. The actual measured period is calculated as:

Measured Period = (Number of Ticks * Timebase)/Scaling Factor = (**A** * 10 ns)/**B**

Example measurement of 1 kHz input signal:

A = 3,200,000
B = 32

Measured Period = (3,200,000 * 10 ns)/32 = 1 ms

Counter statuses are applicable for selected measurement modes. The following table describes the different statuses.

Status	Description
No Sample	The first measurement data is not ready yet for this **CTRx** channel. This occurs as a result of the following factors: the amount of time elapsed since the counter was armed via the **Start** channel, the current counter settings, and the input signal behavior. In this case, the **A** and **B** values will each return a default value of 0.
New	A new, valid measurement for this **CTRx** channel.
Repeated	The same measurement returned the last time a read was performed on this **CTRx** channel. This measurement is valid, and occurs when the **CTRx** I/O Node reads are performed faster than the counter can produce new measurements.
Timeout	A timeout has occurred.

New and Missed	A new, valid measurement for this **CTRx** channel. The counter also produced one or more new measurements that were never read. This occurs when the counter produces measurements faster than the **CTRx** I/O Node reads are performed.
Timeout and Missed	A timeout has occurred. In addition, the counter produced one or more new measurements that were never read.

Timeout is applicable for period measurement mode only, and the definition of Timeout varies according to the setting of the Butterworth filter. The following table defines Timeout for each option.

Measurement Mode	Timeout Definition
Period (Butterworth filter enabled)	Timeout occurs when the actual input signal period is greater than the internal counter limit at 2^{32} x 10 ns and the counter returns a value of 0.
Period (Butterworth filter disabled)	Timeout occurs when the actual input signal period is greater than the maximum measurable period and the counter returns a value of 0.

Arbitration

This device supports only the Arbitrate if Multiple Requestors Only option for arbitration. You cannot configure arbitration settings for this device.

I/O Methods

Use the FPGA I/O Method Node to access the following I/O methods for this device. You can also use the properties dialog box to configure the measurement modes for this device.

Configure Edge Counting—Configures the corresponding counter for any edge counting application. The Method Node returns an error if invoked while the counters are armed. The Initial Count and Reset Count are in units of number of edges.

Parameters	Description

Terminal	Source input terminal of the counter.
Initial Count	Initial counter value once the counter is armed.
Direction	Sets the count direction to either count up, cou nt down or to be externally controlled.
Direction Terminal	Configures the terminal that is used to control t he count direction. This needs to be set when Di rection is configured to "Externally Controlled". I f not set, the parameter value defaults to DI0 ter minal.
Reset Enable	Enables or disables Hardware Reset.
Reset Terminal	Configures the terminal that is used to reset the counter. This needs to be set when Hardware Re set is enabled. If not set, the parameter value de faults to DI0 terminal.
Reset Count	Sets the count value to load to the counter upon reset. If not set, the parameter value defaults to zero.
Pause Enable	Enables or disables the pause trigger.
Pause Terminal	Configures the terminal that is used to pause th e counter. This needs to be set when pause trigg er is enabled. If not set, the parameter value def aults to DI0 terminal.

Configure Edge Counting Simple—Configures the corresponding counter for simple edge counting. The simple configuration for edge counting sets Direction to Count Up and disables both Reset and Pause. The Method Node returns an error if invoked while the counters are armed. The Initial Count is in units of number of edges.

Parameters	Description
Terminal	Source input terminal of the counter.
Initial Count	Initial counter value once the counter is armed.

Configure Period—Configures the corresponding counter for period measurement. The Method Node returns an error if invoked while the counters are armed.

Parameters	Description

Terminal	Source input terminal of the counter.
Enable Butterworth Filter	Enables or disables Butterworth filter. If Butterworth Filter is enabled, set the Filter Frequency parameter accordingly to filter out the higher frequency noise. If disabled, configure the counter settings based on Divisor, Measurement Time and Maximum Measurable Period before the start of an acquisition.
Filter Frequency	Configures the Butterworth filter's cut-off frequency to filter out variations in the period measurements.
Measurement Time	Configures the amount of time over which to measure and average to determine the input signal period. This value is specified in units of counter timebase ticks. Set to 0 to disable the **Measurement Time**, in which case the measurement will be completed using only the **Divisor** setting.
Divisor	Configures the number of periods of the input signal to measure and average to determine the input signal period. Set to 0 to disable the **Divisor**, in which case the measurement will be completed using only the **Measurement Time** setting.
Maximum Measurable Period	Configures the maximum (slowest) period of the input signal that can be measured. If the actual input signal period is longer than this value, the measurement will timeout and the counter returns a value of 0. This value is specified in units of counter timebase ticks. Set this value to 0 to disable enforcing the maximum period.
	**Note** Setting both **Measurement Time** and **Divisor** to 0 is invalid, and will cause the counter to always return a value of 0.

Configure Period Simple—Configures the corresponding counter for simple period measurement. The simple configuration for period measurement enables

the Butterworth filter. The Method Node returns an error if invoked while the counters are armed.

Parameters	Description
Terminal	Source input terminal of the counter.
Filter Frequency	Configures the Butterworth filter's cut-off frequency to filter out variations in the period measurements.

Module Methods

Use the FPGA I/O Method Node to access the following module methods for this device.

Method	Description
Check Status	Returns a Boolean value that indicates whether the module is ready. Supported in Digital Input Mode.

I/O Properties

Use the FPGA I/O Property Node to access the following I/O properties for this device.

Property	Description
Digital Filter Enable	Enables the digital glitch filter for the corresponding digital line.
Digital Filter Minimum Pulse Width*	Configures the minimum pulse width for the digital glitch filter of the corresponding digital line in increments of 80 ns, up to 5.24 ms.
Digital Logic Threshold	Configures the digital logic threshold for the channel.
Hysteresis Value	Configures the hysteresis value for the channel.
Active Edge**	Configures the triggering edge of the input signal.

* Unit in ticks, whereby 1 tick = 80 ns.

Example: Minimum Pulse Width = 1 ms. Therefore, input to the Digital Filter Minimum Pulse Width property node is 1 ms / 80 ns = 12500 ticks.

** The definition of Active Edge varies according to the measurement mode. The following table defines Active Edge for each option.

Measurement Mode	Active Edge Description
Edge Counting	▪ **Input Terminal:** Configures the triggering edge of the input signal. Rising indicates the counter would count on every rising edge and vice versa. ▪ **Direction Terminal:** Configures the terminal that is used to control the count direction. When set to rising edge, the counter counts up when signal on the direction terminal is high. This applies only when the Direction parameter is set to "Externally Controlled". If the Direction Terminal is not set and the Direction parameter is set to "Externally Controlled", the default setting is to count up when signal is high. ▪ **Reset Terminal:** Configures the triggering edge of the reset signal. This applies only when the Reset Enable parameter is set to true. If the Reset Terminal is not set and the Reset Enable parameter is set to true, the default setting is to reset on the rising edge of the signal. ▪ **Pause Terminal:** Configures the terminal that is used to pause the counter. When set to rising edge, the counter pauses when the signal on the pause terminal is high. This applies only when the Pause Enable parameter is set to true. If the Pause Terminal is not set and the Pause Enable parameter is set to true, the default setting is to pause when signal is high.
Period (Butterworth filter enabled)	**Input Terminal:** Configures the triggering edge of the input signal.

Period (Butterworth filter disabled)	**Input Terminal:** Configures the triggering edge of the input signal.

Module Properties

Use the FPGA I/O Property Node to access the following module properties for this device.

Property	Description
Module ID	Returns the module ID, 0x7A5E.
Serial Number	Returns the unique serial number of the module.
Vendor ID	Returns the NI vendor ID, 0x1093.

Single-Cycle Timed Loop

This device supports the single-cycle Timed Loop when Digital Input Mode is set in the properties dialog box. The input channels of this device are synchronized with two synchronizing registers.

When the module is within a single-cycle Timed Loop, it must be ready to perform digital input before a loop containing digital input starts. Poll the **Ready** output of the Check Status method to determine whether the module is ready. Digital input operations return null data if the module is not ready.

FPGA Target Clock Support

This device supports only top-level FPGA target clock rates that are multiples of 40 MHz, such as 40 MHz, 80 MHz, 120 MHz, and 160 MHz.

C Series Module Properties Dialog Box for the NI 9326 (FPGA Interface)

Right-click an NI 9326 C Series module in the **Project Explorer** window and select **Properties** from the shortcut menu to launch the **C Series Module Properties** dialog box, that includes the following components, which you can use to configure a C Series module.

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. Use this field to assign a descriptive name to the module.
- **Type**—Specifies the type of C Series module. You cannot change this option.
- **Location**—Specifies the slot in the chassis used by the C Series module.
- **Digital Input Mode**—Specifies the mode of module. If this property is checked, only digital input channel, DIx will be supported.
  - Digital Input Channels—Specifies the list of input channels available in the module, which you can select to configure.
  - Active Edge—Sets the triggering edge of the input signal.
  - Threshold (V)—Sets the threshold value for the input channel.
  - Hysteresis Value (V)—Sets the hysteresis value for the input channel.

Note Changing this option will change the FPGA interface.

- **Channel**—Specifies the list of counters available in the module, which you can select to configure.
- **Measurement**—Specifies the selected measurement mode of the corresponding counter.
- **Terminals**—Specifies the selected terminal settings of the corresponding counter.
- **Settings**—Specifies the selected configuration of the corresponding counter.
- **Measurement Mode**—Sets the measurement mode of the corresponding counter.

Measurement Mode	Configuration Type	Description
Edge Counting	Initial Count	Sets the initial counter value.
	Pause	Enables or disables the Paus e feature.

	HW Reset	Enables or disables the Hard ware Reset.
	Reset Count	Sets the value the counter res ets to when HW Reset is trigg ered.
	Direction	Sets the count direction to C ount Up, Count Down, or Exte rnally Controlled.
Period	Enable Butterworth Filter	Enables or disables Butterwo rth filter.
	Filter Frequency*	Sets the Butterworth filter's c ut-off frequency.
	Sample Rate (Hz)	Specifies the rate at which da ta is being sampled from the counter. This value is used to calculate the Measurement Ti me and Divisor of the counter .
	Maximum Measurable Period (ms)	Specifies the maximum (slow est) period of the input signal that can be measured.
	Maximum Freq (Hz)	Specifies the maximum input frequency. This value is used along with the Sample Rate t o calculate the Measurement Time and Divisor of the count er.

* The following table specifies the available cut-off frequecies.

Filter Frequency	Cut-off Frequency
Filter Frequency—1	6167 Hz
Filter Frequency—2	2941 Hz
Filter Frequency—3	1439 Hz
Filter Frequency—4	712 Hz
Filter Frequency—5	354 Hz
Filter Frequency—6	177 Hz
Filter Frequency—7	88 Hz

Filter Frequency—8	44 Hz
Filter Frequency—9	22 Hz
Filter Frequency—10	11 Hz
Filter Frequency—11	6 Hz
Filter Frequency—12	3 Hz
Filter Frequency—13	1 Hz

- **Advanced Configuration**—Launches the Advanced Configuration dialog box.

Advanced Configuration Dialog Box (FPGA Interface)

Click the **Advanced Configuration** button on the C Series Module Properties dialog box for the NI 9326 to launch the **Advanced Configuration** dialog box, which you can use to configure the counter input terminals and each digital input line.

- **Counters**—Configures the corresponding counter terminal.
  - Measurement Mode—Displays the measurement mode of the selected counter.
  - Reset Terminals to Default—Reset the terminal settings to the factory defaults.
  - Terminals of the selected counters:
    - For Edge Counting, there are up to 4 terminals per counter (Input, Reset, Direction, and Pause).
    - For Period, there is only one terminal per counter.
- **Digital Inputs**—Configures the corresponding digital inputs lines.
  - Digital Input Channels—Selects the Digital Inputs to configure.
  - Active Edge—Sets the triggering edge of the input signal.
  - Digital Filter—Enables or disables the digital input filter.
  - Minimum Pulse Width (ms)—Configures the minimum pulse width of the digital input filter. Pulses that are shorter than the minimum pulse width will be filtered out (Applies only when Digital Filter is enabled).

- Threshold (V)—Sets the threshold value for the digital input.
- Hysteresis Value (V)—Sets the hysteresis value for the digital input.

Synchronizing Multiple NI 9326 Modules (FPGA Interface)

Complete the following steps to synchronize multiple NI 9326 modules that are connected to the same FPGA device.

1. Create the FPGA I/O items with all the I/O channels to be synchronized, within a single FPGA I/O Node. Otherwise, the FPGA I/O Node will not return synchronized data.
2. Configure an FPGA I/O Node with **Start** channels for the NI 9326 modules you want to synchronize.
3. Wire a Boolean constant set to TRUE to each **Start** channel.

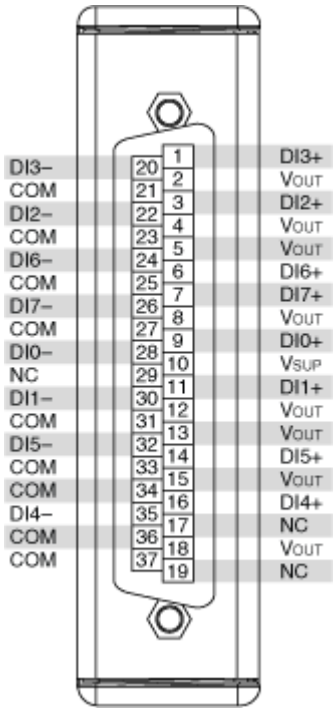
NI 9361

CompactRIO 8-Channel, Counter Input Module

Software Reference (?)

FPGA Interface

NI 9361 Pinout



Related Topics

FPGA Interface

Synchronizing Multiple NI 9361 Modules

NI 9361 (FPGA Interface)

CompactRIO 8-Channel, Counter Input Module

FPGA I/O Node

You can use an FPGA I/O Node, configured for reading, with this device.

Terminals in Software

Use the FPGA I/O Node to access the following terminals for this device.

Terminal	Description
CTR**x**	Counter input channel **x**, where **x** is the number of the channel. The counter I/O node returns a c

	luster of three items, consisting of two unsigned 32-bit integers called A and B as well as the cou nter status enum. The **Start** input I/O node mus t be executed before counter or DI data can be r ead. The NI 9361 has counters 0 through 7.
DI**x**	Digital input channel **x**, where **x** is the number o f the channel. The NI 9361 has DI channels 0 thr ough 7.
DI7:0	Digital Port consisting of channels 0 through 7. Channel 7 is returned in the Most Significant Bit (MSB), and channel 0 is returned in the Least Sig nificant Bit (LSB).
Start	Channel that controls when the counters begin monitoring their input terminals. If TRUE is writt en to the **Start** channel, the NI 9361 counters ar e reset, armed, and begin monitoring their input terminals to perform the currently configured m easurement (such as Edge Counting). Once the NI 9361 counters are armed, you may execute th e **CTRx** and **DIx** I/O nodes to read the counter d ata. You may not execute any NI 9361 I/O Metho d or Property nodes while the counters are arm ed. To disarm the counters, use the **Stop** chann el. If FALSE is written to the **Start** channel, no o peration is performed. The **Start** channel is also used to synchronize multiple NI 9361 modules.
Stop	Channel that controls when the counters are dis armed. If TRUE is written to the **Stop** channel, t he counters are stopped. When the counters are stopped, you may change the counter configura tion by executing I/O Method and Property node s. If FALSE is written to the **Stop** channel, no op eration is performed.

The definition of **A** and **B** values vary according to the measurement mode you select. The following table defines the **A** and **B** values for each measurement mode option.

Measurement Mode	A	B	Status

Edge Counting	Number of edges.	Unused. Always returns 0.	Not applicable.
Period	Amount of time elapsed during **B** signal periods, measured in units of counter timebase ticks.	Number of signal periods measured.	Applicable.
Pulse	Width of High portion of input signal period, measured in units of counter timebase ticks.	Width of Low portion of input signal period, measured in units of counter timebase ticks.	Applicable.
Pulse Width	Width of input pulse, measured in units of counter timebase ticks.	Unused. Always returns 0.	Applicable.
Two Edge Separation	Amount of time between two input edges, measured in units of counter timebase ticks.	Unused. Always returns 0.	Applicable.
Encoder Position	Number of encoder counts.	Unused. Always returns 0.	Not applicable.
Encoder Velocity	Amount of time elapsed during **B** encoder counts, measured in units of counter timebase ticks.	Signed number of counter encoder counts and direction. Positive values indicate counting in the positive direction, and negative values indicate counting in the opposite direction. You must use the **To Long Integer** function to convert the unsigned **B** value (U32) to a signed value (I32) when performing an Encoder Velocity measurement.	Applicable.

All values that are based on ticks use the module's timebase of 100 MHz. Each tick corresponds to 10 ns. The actual value is calculated as:

Actual = Number of ticks * 10 ns
Examples:

1. Period Measurement Mode—A is 100000. B is 1. Measured period = (A * 10 ns)/B = 1 ms.
2. Encoder Velocity Measurement Mode—A is 100000. B is 1. Measured Encoder Velocity = B/(A * 10 ns) = 1000 count/s.
3. Pulse Width and Two Edge Separation Measurement Mode—A is 100000. Measured Pulse Width or Two Edge Separation = A * 10 ns = 1 ms.
4. Pulse Measurement Mode—A is 100000. B is 100000. Measured High Pulse = A * 10 ns = 1 ms. Measured Low Pulse = B * 10 ns = 1 ms.

Counter statuses are applicable for selected measurement modes. The following table describes the different statuses.

Status	Description
No Sample	The first measurement data is not ready yet for this **CTRx** channel. This occurs as a result of the following factors: the amount of time elapsed since the counter was armed via the **Start** channel, the current counter settings, and the input signal behavior. In this case, the **A** and **B** values will each return a default value of 0.
New	A new, valid measurement for this **CTRx** channel.
Repeated	The same measurement returned the last time a read was performed on this **CTRx** channel. This measurement is valid, and occurs when the **CTRx** I/O Node reads are performed faster than the counter can produce new measurements.
Timeout	A timeout has occurred.
New and Missed	A new, valid measurement for this **CTRx** channel. The counter also produced one or more new measurements that were never read. This occurs when the counter produces measurements faster than the **CTRx** I/O Node reads are performed.

Timeout and Missed	A timeout has occurred. In addition, the counter produced one or more new measurements that were never read.

Timeout is applicable for selected measurement modes, and the definition of Timeout varies according to the measurement mode you select. The following table defines Timeout for each measurement mode option.

Measurement Mode	Timeout Definition
Period	Timeout occurs when the actual input signal period is greater than the maximum measurable period and the counter returns a value of 0.
Pulse	Timeout occurs when the actual input signal period is greater than the maximum measurable period. If the input signal remains high when timeout occurs, the counter returns a non-zero value for the high pulse and a value of 0 for the low pulse. If the input signal remains low when timeout occurs, the counter returns a non-zero value for the low pulse and a value of 0 for the high pulse.
Pulse Width	Timeout occurs when the actual input signal period is greater than the maximum measurable period and the counter returns a value of 0.
Two Edge Separation	Timeout occurs when the actual input signal period is greater than the maximum measurable separation and the counter returns a value of 0.
Quadrature Encoder Velocity	Timeout occurs when the actual input signal period is greater than the maximum measurable count period and the counter returns a value of 0.
Two Pulse Encoder Velocity	Timeout occurs when the actual input signal period is greater than the maximum measurable count period and the counter returns a value of 0.

Arbitration

This device supports only the Arbitrate if Multiple Requestors Only option for arbitration. You cannot configure arbitration settings for this device.

I/O Methods

Use the FPGA I/O Method Node to access the following I/O methods for this device. You can also use the properties dialog box to configure the measurement modes for this device.

Module Methods

This device does not support any module methods.

I/O Properties

Use the FPGA I/O Property Node to access the following I/O properties for this device.

Property	Description
Digital Filter Enable	Enables the digital filter for the corresponding digital line.
Digital Filter Minimum Pulse Width*	Configures the minimum pulse width for the digital filter of the corresponding digital line in increments of 80 ns, up to 5.24 ms.
Terminal Mode	Configures the terminal mode of the corresponding digital line (Differential, Single-ended, and Single-ended with Pull-up).

* Unit in ticks, whereby 1 tick = 80 ns.

Example: Minimum Pulse Width = 1 ms. Therefore, input to the Digital Filter Minimum Pulse Width property node is 1 ms / 80 ns = 12500 ticks.

Module Properties

Use the FPGA I/O Property Node to access the following module properties for this device.

Property	Description
Module ID	Returns the module ID, 0x777E.
Serial Number	Returns the unique serial number of the module.

Vendor ID	Returns the NI vendor ID, 0x1093.
Digital Logic Threshold	Configures the digital logic threshold for the module. Does not apply to terminals that are configured as Differential.

Single-Cycle Timed Loop

This device does not support any single-cycled timed loop.

FPGA Target Clock Support

This device supports only top-level FPGA target clock rates that are multiples of 40 MHz, such as 40 MHz, 80 MHz, 120 MHz, and 160 MHz.

C Series Module Properties Dialog Box for the NI 9361 (FPGA Interface)

Right-click an NI 9361 C Series module in the **Project Explorer** window and select **Properties** from the shortcut menu to launch the **C Series Module Properties** dialog box, that includes the following components, which you can use to configure a C Series module.

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. Use this field to assign a descriptive name to the module.
- **Type**—Specifies the type of C Series module. You cannot change this option.
- **Location**—Specifies the slot in the chassis used by the C Series module.
- **Channel**—Specifies the list of counters available in the module, which you can select to configure.
- **Measurement**—Specifies the selected measurement mode of the corresponding counter.
- **Terminals**—Specifies the selected terminal settings of the corresponding counter.

- **Settings**—Specifies the selected configuration of the corresponding counter.
- **Measurement Mode**—Sets the measurement mode of the corresponding counter.

Measurement Mode	Configuration Type	Description
Edge Counting	Initial Count	Sets the initial counter value.
	Active Edge	Sets the active edge of the co unter.
	Pause	Enables or disables the Paus e feature.
	Pause When	Configures the Pause trigger t o Pause When High or Pause When Low.
	HW Reset	Enables or disables the Hard ware Reset.
	Reset Edge	Configures the HW Reset to tr igger on the rising or falling e dge.
	Reset Count	Sets the value the counter res ets to when HW Reset is trigg ered.
	Direction	Sets the count direction to C ount Up, Count Down, or Exte rnally Controlled.
	Count Up When	Sets the counter to Count Up when the external terminal is high or low.
Period	Starting Edge	Configures the counter to sta rt counting on the rising or fa lling edge.
	Sample Rate (Hz)	Specifies the rate at which da ta is being sampled from the counter. This value is used to calculate the Measurement Ti me and Divisor of the counter .

	Maximum Measurable Period (ms)	Specifies the maximum (slowest) period input signal that can be measured.
	Maximum Freq (Hz)	Specifies the maximum input frequency. This value is used to calculate the Measurement Time and Divisor of the counter.
Pulse	Starting Edge	Configures the counter to start counting on the rising or falling edge.
	Maximum Measurable Period (ms)	Specifies the maximum (slowest) period input signal that can be measured.
Pulse Width	Starting Edge	Configures the counter to start counting on the rising or falling edge.
	Maximum Measurable Period (ms)	Specifies the maximum (slowest) period input signal that can be measured.
Two Edge Separation	First Edge	Configures the first edge to either rising or falling.
	Second Edge	Configures the second edge to either rising or falling.
	Maximum Measurable Separation (ms)	Specifies the maximum separation that can be measured between the first input signal and the second input signal.
Quadrature Encoder Position	Initial Position	Sets the initial counter value.
	Decoding Type	Configures the decoding type (x1, x2, or x4).
	Z Index Enable	Enables or disables the usage of the Z terminal.
	Z Index Value	Sets the value that is loaded to the counter when the Z terminal is triggered.
	Z Index Phase	Configures the AB phase in which the Z Index value is load

		ed to the counter when the Z Terminal is triggered.
Two Pulse Encoder	Initial Position	Sets the initial counter value.
	HW Reset	Enables or disables the Hard ware Reset.
	Reset Edge	Configures the HW Reset to tr igger on the rising or falling e dge.
	Reset Position	Sets the value the counter res ets to when HW Reset is trigg ered.
Quadrature Encoder Velocity	Decoding Type	Configures the decoding type (x1, x2, and x4).
	Sample Rate (Hz)	Specifies the rate at which da ta is being sampled from the counter. This value is used to calculate the Measurement Ti me and Divisor of the counter .
	Maximum Measurable Count Period (ms)	Specifies the maximum (slow est) period between encoder input counts that can be mea sured.
	Maximum Count Rate (Hz)	Specifies the maximum coun t rate. This value is used to ca lculate the Measurement Tim e and Divisor of the counter.
Two Pulse Encoder Velocity	Sample Rate (Hz)	Specifies the rate at which da ta is being sampled from the counter. This value is used to calculate the Measurement Ti me and Divisor of the counter .
	Maximum Measurable Count Period (ms)	Specifies the maximum (slow est) period between encoder input counts that can be mea sured.
	Maximum Count Rate (Hz)	Specifies the maximum coun t rate. This value is used to ca

		lculate the Measurement Tim e and Divisor of the counter.

- **Advanced Configuration**—Launches the Advanced Configuration dialog box.

NI 9361 I/O Method Parameters

Refer to the I/O Methods, that includes the following parameters, which you can use to configure the NI 9361 measurement modes.

Note The counters operate based on the module's timebase of 100 MHz. Each timebase tick corresponds to 10 ns.

- **Configure Edge Counting**—Configures the corresponding counter for any edge counting application. The Method Node returns an error if invoked while the module is in running state. The Initial Count and Reset Count are in edges.

Parameters	Description
Terminal	Source input terminal of the counter.
Initial Count	Initial counter value once the counter is arm ed.
Active Edge	Sets the triggering edge of the input signal. Rising indicates the counter would count on every rising edge and vice versa.
Direction	Sets the count direction to either count up, c ount down or to be externally controlled.
Direction Terminal	Configures the external terminal that is used to control the count direction. This needs to be set when Direction is configured to "Exter nally Controlled". If not set, the parameter va lue defaults to DI0 terminal.
External Direction Count Up When	Configures whether the counter would coun t up when the Direction Terminal is 'HIGH' or to count up when the Direction Terminal is 'L OW'. If not set, the parameter value defaults to count up when high.
Reset Enable	Enables or disables Hardware Reset.

Reset Terminal	Configures the reset terminal that is used to reset the counter. This needs to be set when Hardware Reset is enabled. If not set, the parameter value defaults to DI0 terminal.
Reset Count	Sets the count value to load to the counter upon reset. If not set, the parameter value defaults to zero.
Reset Active Edge	Sets the triggering edge of the reset signal. If not set, the parameter value defaults to reset on the rising edge.
Pause Enable	Enables or disables the pause trigger.
Pause Terminal	Configures the pause terminal that is used to pause the counter. This needs to be set when pause trigger is enabled. If not set, the parameter value defaults to DI0 terminal.
Pause When	Configures the pause trigger to either pause the counter when the pause terminal is 'HIGH' or 'LOW'. If not set, the parameter value defaults to pause when high.

- **Configure Edge Counting Simple**—Configures the corresponding counter for simple edge counting. The simple configuration for edge counting sets Direction to Count Up and disables both Reset and Pause. The Method Node returns an error if invoked while the module is in running state. The Initial Count is in edges.

Parameters	Description
Terminal	Source input terminal of the counter.
Initial Count	Initial counter value once the counter is armed.
Active Edge	Sets the triggering edge of the input signal. Rising indicates the counter would count on every rising edge and vice versa.

- **Configure Period**—Configures the corresponding counter for period measurement. The Method Node returns an error if invoked while the module is in running state.

Parameters	Description
Terminal	Source input terminal of the counter.

Starting Edge	Configures the triggering edge of the input signal.
Measurement Time	Configures the amount of time over which to measure and average the period of the input signal. This value is specified in units of counter timebase ticks. Set to 0 to disable the **Measurement Time**, in which case the measurement will be completed using only the **Divisor** setting.
Divisor	Configures the number of periods of the input signal to measure and average to determine the input signal period. Set to 0 to disable the **Divisor**, in which case the measurement will be completed using only the **Measurement Time** setting.
Maximum Measurable Period	Configures the maximum (slowest) period input signal that can be measured. If the actual input signal period is longer than this value, the measurement will timeout and the counter returns a value of 0. This value is specified in units of counter timebase ticks. Set this value to 0 to disable enforcing the maximum period.
	**Note** Setting both **Measurement Time** and **Divisor** to 0 is invalid, and will cause the counter to always return a value of 0.

- **Configure Period Simple**—Configures the corresponding counter for simple period measurement. The simple configuration for period measurement sets **Measurement Time** to 0 and **Divisor** to 1. The Method Node returns an error if invoked while the module is in running state.

Parameters	Description
Terminal	Source input terminal of the counter.
Starting Edge	Configures the triggering edge of the input signal.
Maximum Measurable Period	Configures the maximum (slowest) period input signal that can be measured. If the actua

	l input signal period is longer than this value , the measurement will timeout and the cou nter returns a value of 0. This value is specifi ed in units of counter timebase ticks. Set this value to 0 to disable enforcing the maximum period.

- **Configure Pulse**—Configures the corresponding counter for pulse measurement. The Method Node returns an error if invoked while the module is in running state.

Parameters	Description
Terminal	Source input terminal of the counter.
Starting Edge	Configures the triggering edge of the input si gnal.
Maximum Measurable Period	Configures the maximum (slowest) period in put signal that can be measured. If the actua l input signal period is longer than this value , the measurement will timeout and the cou nter returns a non-zero value for the high pul se and a value of 0 for the low pulse if the act ual signal is high during timeout. The counte r returns a non-zero value for the low pulse a nd a value of 0 for the high pulse if the actual signal is low during timeout. This value is sp ecified in units of counter timebase ticks. Set this value to 0 to disable enforcing the maxi mum period.

- **Configure Pulse Width**—Configures the corresponding counter for pulse width measurement. The Method Node returns an error if invoked while the module is in running state.

Parameters	Description
Terminal	Source input terminal of the counter.
Starting Edge	Configures the triggering edge of the input si gnal.
Maximum Measurable Period	Configures the maximum (slowest) period in put signal that can be measured. If the actua l input signal period is longer than this value , the measurement will timeout and the cou

	nter returns a value of 0. This value is specifi ed in units of counter timebase ticks. Set this value to 0 to disable enforcing the maximum period.

- **Configure Two Edge Separation**—Configures the corresponding counter for two edge separation measurement. The Method Node returns an error if invoked while the module is in running state.

Parameters	Description
First Terminal	First source input terminal of the counter.
First Edge	Configures the triggering edge of the first sig nal.
Second Terminal	Second source input terminal of the counter.
Second Edge	Configures the triggering edge of the second signal.
Maximum Measurable Separation	Configures the maximum separation betwee n the first input signal and the second input signal that can be measured. If the actual in put signal separation is longer than this valu e, the measurement will timeout and the co unter returns a value of 0. This value is specif ied in units of counter timebase ticks. Set thi s value to 0 to disable enforcing the maximu m separation.

- **Configure Quadrature Encoder Position**—Configure the corresponding counter for quadrature encoder measurement. **Z** indexing can be enabled or disabled. The Method Node returns an error if invoked while the module is in running state.

Parameters	Description
A Terminal	**A** input terminal of the counter.
A Invert Polarity	Configures the module to invert the **A** signal.
B Terminal	**B** input terminal of the counter.
B Invert Polarity	Configures the module to invert the **B** signal.
Initial Position	Initial counter value once the counter is arm ed.

Decoding Type	Configures the decoding type to either x1, x2 or x4.
Z Index Enable	Enables or disables the Z Index.
Z Terminal	Configures the Z terminal for the Z index. Th is needs to be set when Z Index is enabled. If not set, the parameter value defaults to DI0 t erminal.
Z Invert Polarity	Configures the module to invert the Z signal. If not set, the parameter value defaults to no t inverting the Z signal.
Z Index Value	Configures the counter value to be loaded w hen the Z Index is triggered. If not set, the pa rameter value defaults to not zero.
Z Index Phase	Configures the Z Index phase in which the Z index would be triggered. If not set, the para meter value defaults to trigger when A signal is low and B signal is low.

- **Configure Two Pulse Encoder**—Configures the corresponding counter for any two pulse encoder measurement. The Method Node returns an error if invoked while the module is in running state. The Initial Position and Reset Position values are in encoder counts.

Parameters	Description
A Terminal	A input terminal of the counter.
A Invert Polarity	Configures the module to invert the A signal.
B Terminal	B input terminal of the counter.
B Invert Polarity	Configures the module to invert the B signal.
Initial Position	Initial counter value once the counter is arm ed.
Reset Enable	Enables or disables Hardware Reset.
Reset Terminal	Configures the reset terminal that is used to reset the counter. This needs to be set when Hardware Reset is enabled. If not set, the par ameter value defaults to DI0 terminal

Reset Position	Sets the count value that would be loaded to the counter upon reset. If not set, the parameter value defaults to zero.
Reset Active Edge	Sets the triggering edge of the reset signal. If not set, the parameter value defaults to reset on rising edge.

- **Configure Two Pulse Encoder Simple**—Configures the corresponding counter for any two pulse encoder measurement. The simple configuration for two pulse encoder measurement disables Reset. The Method Node returns an error if invoked while the module is in running state. The Initial Position value is in encoder counts.

Parameters	Description
A Terminal	**A** input terminal of the counter.
A Invert Polarity	Configures the module to invert the **A** signal.
B Terminal	**B** input terminal of the counter.
B Invert Polarity	Configures the module to invert the **B** signal.
Initial Position	Initial counter value once the counter is armed.

- **Configure Quadrature Encoder Velocity**—Configures the corresponding counter for quadrature encoder velocity measurement. The Method Node returns an error if invoked while the module is in running state.

Parameters	Description
A Terminal	**A** input terminal of the counter.
A Invert Polarity	Configures the module to invert the **A** signal.
B Terminal	**B** input terminal of the counter.
B Invert Polarity	Configures the module to invert the **B** signal.
Decoding Type	Configures the decoding type to either x1, x2 or x4.
Measurement Time	Configures the amount of time over which to measure and average the period of the input signal. This value is specified in units of counter timebase ticks. Set to 0 to disable the **Measurement Time**, in which case the measu

	rement will be completed using only the **Div isor** setting.
Divisor	Configures the number of encoder count per iods to measure and average to determine t he encoder input period (velocity). Set to 0 t o disable the **Divisor**, in which case the mea surement will be completed using only the **Measurement Time** setting.
Maximum Measurable Count Period	Configures the maximum (slowest) period b etween encoder input counts that can be me asured. If the actual time between encoder c ounts is longer than this value, the measure ment will timeout and the counter returns a value of 0. This value is specified in units of c ounter timebase ticks. Set this value to 0 to disable enforcing the maximum period.

Note Setting both **Measurement Time** and **Divisor** to 0 is invalid, and will cause the counter to always return a value of 0.

- **Configure Two Pulse Encoder Velocity**—Configures the corresponding counter for two pulse encoder velocity measurement. The Method Node returns an error if invoked while the module is in running state.

Parameters	Description
A Terminal	**A** input terminal of the counter.
A Invert Polarity	Configures the module to invert the **A** signal.
B Terminal	**B** input terminal of the counter.
B Invert Polarity	Configures the module to invert the **B** signal.
Measurement Time	Configures the amount of time over which to measure and average the period of the input signal. This value is specified in units of coun ter timebase ticks. Set to 0 to disable the **Me asurement Time**, in which case the measu rement will be completed using only the **Div isor** setting.
Divisor	Configures the number of encoder count per iods to measure and average to determine t

	he encoder input period (velocity). Set to 0 t o disable the **Divisor**, in which case the mea surement will be completed using only the **Measurement Time** setting.
Maximum Measurable Count Period	Configures the maximum (slowest) period b etween encoder input counts that can be me asured. If the actual time between encoder c ounts is longer than this value, the measure ment will timeout and the counter returns a value of 0. This value is specified in units of c ounter timebase ticks. Set this value to 0 to disable enforcing the maximum period.

Advanced Configuration Dialog Box (FPGA Interface)

Click the **Advanced Configuration** button on the C Series Module Properties dialog box for the NI 9361 to launch the **Advanced Configuration** dialog box, which you can use to configure the counter input terminals and each digital input line.

- **Counters**—Configures the corresponding counter terminal.
  - Measurement Mode—Displays the measurement mode of the selected counter.
  - Reset Terminals to Default—Reset the terminal settings to the factory defaults.
  - Terminals of the selected counters:
    - For Edge Counting, there are up to 4 terminals per counter (Input, Reset, Direction, and Pause).
    - For Quadrature Encoder Position and Two Pulse Encoder, there are up to 3 terminals per counter (A Input, B Input, and Z or Reset).
    - For Two Edge Separation, there are two terminals per counter (First Input and Second Input).
    - For Quadrature Encoder Velocity and Two Pulse Encoder Velocity, there are two terminals per counter (A Input and B Input).

    - For Period, Pulse, and Pulse Width, there is only one terminal per counter.
- **Digital Inputs**—Configures the corresponding digital inputs lines.
  - Digital Input Channels—Selects the Digital Inputs to configure.
  - Terminal Mode—Configures the terminal mode (Differential, Single-Ended, or Single-Ended with Pull-up) of the selected digital input.
  - Digital Filter—Enables or disables the digital input filter.
  - Minimum Pulse Width (ms)—Configures the minimum pulse width of the digital input filter. Pulses that are shorter than the minimum pulse width will be filtered out (Applies only when Digital Filter is enabled).
  - Threshold (V)—Sets the threshold value for the counter (Applies only to terminals that are not differential).

Synchronizing Multiple NI 9361 Modules (FPGA Interface)

Complete the following steps to synchronize multiple NI 9361 modules that are connected to the same FPGA device.

1. Create the FPGA I/O items with all the I/O channels to be synchronized, within a single FPGA I/O Node. Otherwise, the FPGA I/O Node will not return synchronized data.
2. Configure an FPGA I/O Node with **Start** channels for the NI 9361 modules you want to synchronize.
3. Wire a Boolean constant set to TRUE to each **Start** channel.

Digital Input Modules

Use this book as a reference for the following information:

- FPGA I/O functions, I/O resources, arbitration options, methods, and properties each C Series digital input module supports in FPGA Interface mode
- I/O variables and properties each C Series digital input module supports in Scan Interface mode
- Instructions for using LabVIEW with CompactRIO digital input devices

To view related topics, click the **Locate** button, shown at left, in the toolbar at the top of this window. The **LabVIEW Help** highlights this topic in the **Contents** tab so you can navigate the related topics.

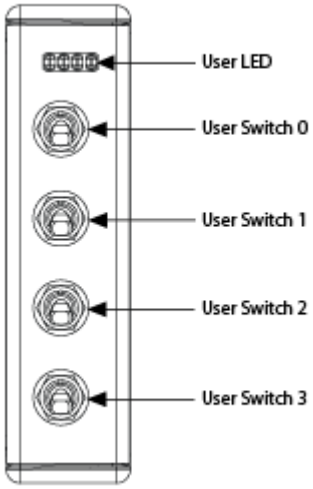
NI 9344

CompactRIO 4-Channel Switch Input and 4-Channel LED Output Module

Software Reference (?)

FPGA Interface

NI 9344 Front Panel



Related Topics

FPGA Interface

NI 9344 (FPGA Interface)

CompactRIO 4-Channel Switch Input and 4-Channel LED Output Module

Find examples

FPGA I/O Node

You can use an FPGA I/O Node, configured for reading and writing, with this device. When you write to an NI 9344 channel, the FPGA I/O Node does not automatically enable the channel for output.

Terminals in Software

Use the FPGA I/O Node to access the following terminals for this device.

Terminal	Description
User LED**x**	LED output channel **x**, where **x** is the number of the channel. The NI 9344 has LED channels 0 to 3.
User Switch x	Switch input channel **x**, where **x** is the number of the channel. The NI 9344 has Switch channels 0 to 3.
User LED 3:0	Digital output port consisting of channels 0 through 3. Channel 3 is returned in the MSB, and channel 0 is returned in the LSB.
User Switch 3:0	Digital input port consisting of channels 0 through 3. Channel 3 is returned in the MSB, and channel 0 is returned in the LSB.

Arbitration

You can configure the arbitration settings for digital output channels of this device in the Advanced Code Generation page of the FPGA I/O Properties dialog box. The default arbitration setting is Never Arbitrate. Digital input channels of this device support only the **Never Arbitrate** option for arbitration. You cannot configure arbitration settings for the digital input channels of this device.

I/O Methods

Use the FPGA I/O Method Node to access the following I/O methods for this device.

Method	Description

Wait on Any Edge	Pauses the execution of the I/O Method Node until the next falling or rising edge of the digital signal. The **Timeout** input specifies in FPGA clock ticks how long the Wait on Any Edge method waits for the next falling or rising edge. A value of 0 causes the method to time out immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.
Wait on Falling Edge	Pauses the execution of the I/O Method Node until the next falling edge of the digital signal. The **Timeout** input specifies in FPGA clock ticks how long the Wait on Falling Edge method waits for the next falling edge. A value of 0 causes the method to time out immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.
Wait on High Level	Pauses the execution of the I/O Method Node until the digital signal is high. The **Timeout** input specifies in FPGA clock ticks how long the Wait on High Level method waits for the next high level. A value of 0 causes the method to time out immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.
Wait on Low Level	Pauses the execution of the I/O Method Node until the digital signal is low. The **Timeout** input specifies in FPGA clock ticks how long the Wait on Low Level method waits for the next low level. A value of 0 causes the method to time out immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.
Wait on Rising Edge	Pauses the execution of the I/O Method Node until the next rising edge of the digital signal. The **Timeout** input specifies in FPGA clock ticks ho

	w long the Wait on Rising Edge method waits for the next rising edge. A value of 0 causes the met hod to time out immediately, a negative value c auses the method to wait indefinitely, and a pos itive value causes the method to wait for that nu mber of clock ticks before timing out.

Module Methods

Use the FPGA I/O Method Node to access the following module methods for this device.

Method	Description
Check Status	Returns a Boolean value that indicates whether the module is ready.  **Note** During the first 2 seconds after you reset the FPGA VI, the error t erminals on this metho d may not correctly rep ort certain types of err ors.

I/O Properties

This device does not support any I/O properties.

Module Properties

Use the FPGA I/O Property Node to access the following module properties for this device.

Property	Description
Module ID	Returns the module ID, 0x77C5.
Serial Number	Returns the unique serial number of the module .
Vendor ID	Returns the NI vendor ID, 0x1093.

Single-Cycle Timed Loop

This device supports the single-cycle Timed Loop. Configure the number of output synchronizing registers for the channels of this device in the Advanced Configuration dialog box. Configure the number of input synchronizing registers for the channels of this device in the Advanced Code Generation page of the FPGA I/O Node Properties dialog box.

When the module is within a single-cycle Timed Loop, it must be ready to perform digital I/O before a loop containing digital I/O starts. Poll the **Ready** output of the Check Status method to determine whether the module is ready. Digital input operations return invalid data if the module is not ready. The module also might ignore or delay digital output operations if it is not ready.

While the module is performing digital I/O within a single-cycle Timed Loop, do not perform property reads, use the Set Line Direction method, or remove the module from the chassis. Doing any of these actions causes the module to be unable to perform digital I/O and the **Ready** output of the Check Status method to return FALSE.

FPGA Target Clock Support

This device supports only top-level FPGA target clock rates and single-cycle Timed Loop clock rates that are multiples of 40 MHz, such as 40 MHz, 80 MHz, 120 MHz, and so on.

C Series Module Properties Dialog Box for the NI 9344 (FPGA Interface)

Right-click an NI 9344 C Series module in the **Project Explorer** window and select **Properties** from the shortcut menu to display this dialog box.

Use this dialog box to configure a C Series module.

This dialog box includes the following components:

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.

- **Module Type**—Specifies the type of C Series module. You cannot change this option.
- **Location**—Specifies a slot in the chassis for the C Series module.

NI 9344 (Scan Interface)

CompactRIO 4-Channel Switch Input and 4-Channel LED Output Module

Module I/O Variables

To use I/O from this module in a VI, drag and drop I/O variables from the **Project Explorer** window to the block diagram of the VI. The I/O variables for the channels read and write Boolean values.

Module Channels

The NI 9344 has the following channels.

Channel	Description
User LED**x**	LED output channel **x**, where **x** is the number of the channel. The NI 9344 has LED channels 0 to 3.
User Switch **x**	Switch input channel **x**, where **x** is the number o f the channel. The NI 9344 has Switch channels 0 to 3.

C Series Module Properties Dialog Box

Use this dialog box to configure the NI 9344. Right-click the NI 9375 in the **Project Explorer** window and select **Properties** to display this dialog box. You can configure the following options.

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.

- **Module Type**—Specifies the type of C Series module. You cannot change this value.
- **Location**—Specifies a slot in the chassis for the C Series module.

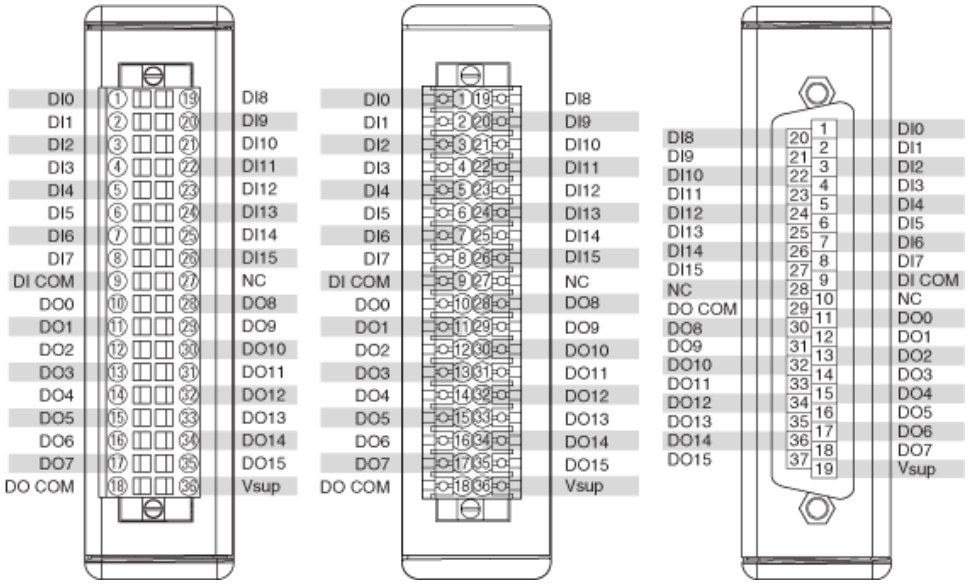
NI 9375

CompactRIO 16-Channel Digital Input and 16-Channel Digital Output

Software Reference (?)

FPGA Interface | Scan Interface

NI 9375 Pinout



Related Topics

FPGA Interface
Avoiding Timing Uncertainty with the NI 9375

NI 9375 (FPGA Interface)

CompactRIO 16-Channel Digital Input and 16-Channel Digital Output

Find NI 9375 examples

FPGA I/O Node

You can use an FPGA I/O Node, configured for reading or writing, with this device.

Terminals in Software

Use the FPGA I/O Node to access the following terminals for this device.

Terminal	Description
DI**x**	Digital input channel **x**, where **x** is the number of the channel. The NI 9375 has DI channels 0 to 15.
DI7:0	Digital port consisting of DI channels 0 through 7. Channel 7 is returned in the MSB, and channel 0 is returned in the LSB.
DI15:8	Digital port consisting of DI channels 8 through 15. Channel 15 is returned in the MSB, and channel 8 is returned in the LSB.
DI15:0	Digital port consisting of DI channels 0 through 15. Channel 15 is returned in the MSB, and channel 0 is returned in the LSB.
DO**x**	Digital output channel **x**, where **x** is the number of the channel. The NI 9375 has DO channels 0 to 15.
DO7:0	Digital port consisting of DO channels 0 through 7. Channel 7 is returned in the MSB, and channel 0 is returned in the LSB.
DO15:8	Digital port consisting of DO channels 8 through 15. Channel 15 is returned in the MSB, and channel 8 is returned in the LSB.
DO15:0	Digital port consisting of DO channels 0 through 15. Channel 15 is returned in the MSB, and channel 0 is returned in the LSB.
	**Caution** DI and DO operations that are run concurrently may exhibit jitter. Access both subsystems using a single I/O Node to avoid jitter in your application. Refer to the Avoiding Timing Uncertainty topic for more information.

Arbitration

This device supports only the Arbitrate if Multiple Requestors Only option for arbitration. You cannot configure arbitration settings for this device.

I/O Methods

This device does not support any I/O methods.

Module Methods

This device does not support any module methods.

I/O Properties

This device does not support any I/O properties.

Module Properties

Use the FPGA I/O Property Node to access the following module properties for this device.

Property	Description
Module ID	Returns the module ID.
Serial Number	Returns the unique serial number of the module .
Vendor ID	Returns the NI vendor ID, 0x1093.

Single-Cycle Timed Loop

This device does not support the single-cycle Timed Loop.

Avoiding Timing Uncertainty with the NI 9375 (FPGA Interface)

Follow these guidelines to avoid introducing timing uncertainty into DI and DO Node calls.

- Use a single I/O Node to access DI and DO operations to ensure proper sequencing.

- Do not perform the following operations concurrently:
  - DI Node call
  - DO Node call

Refer to the NI 9375 Digital Port Input Output VI in the `labview\examples\CompactRIO\Module Specific\NI 9375\NI 9375 Digital Port Input Output\NI 9375 Digital Port Input Output.lvproj` for an example of the recommended way to use the DIO subsystems.

C Series Module Properties Dialog Box for the NI 9375/9411/9421/9422/9423/9425/9426/9435/9436/9437/950x (FPGA Interface)

Right-click an NI 9375, NI 9411, NI 9421, NI 9422, NI 9423, NI 9425, NI 9426, NI 9435, NI 9436, NI 9437, NI 9501, or NI 9505 C Series module in the **Project Explorer** window and select **Properties** from the shortcut menu to display this dialog box.

Use this dialog box to configure a C Series module.

This dialog box includes the following components:

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this option.
- **Location**—Specifies a slot in the chassis for the C Series module.

NI 9375 (Scan Interface)

CompactRIO 16-Channel Digital Input and 16-Channel Digital Output

Module I/O Variables

To use I/O from this module in a VI, drag and drop I/O variables from the **Project Explorer** window to the block diagram of the VI. The I/O variables for the channels read and write Boolean values.

Module Channels

The NI 9375 has the following channels.

Channel	Description
DI**x**	Digital input channel **x**, where **x** is the number of the channel. For the NI 9375, **x** is 0 to 15.
DO**x**	Digital output channel **x**, where **x** is the number of the channel. For the NI 9375, **x** is 0 to 15.

C Series Module Properties Dialog Box

Use this dialog box to configure the NI 9375. Right-click the NI 9375 in the **Project Explorer** window and select **Properties** to display this dialog box. You can configure the following options.

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this value.
- **Location**—Specifies a slot in the chassis for the C Series module.

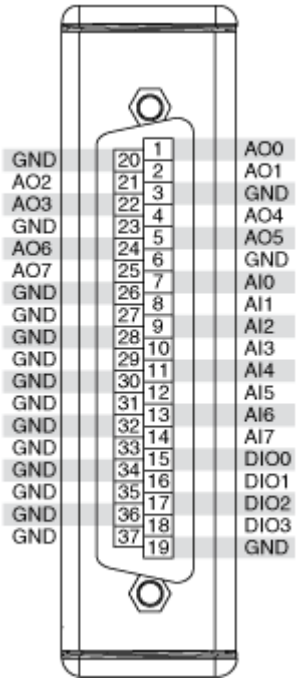
NI 9381

CompactRIO 0 V to 5 V, 12-bit, Multifunction Input/Output Module

Software Reference (?)

FPGA Interface | Scan Interface

NI 9381 Pinout



Running AI and AO Operations Concurrently on the NI 9381

AI and AO operations that are run concurrently may exhibit jitter. Access both subsystems using a single I/O Node to avoid jitter in your application. Refer to the Avoiding Timing Uncertainty topic for more information.

Related Topics

FPGA Interface
Converting and Calibrating CompactRIO Analog Input Values
Detecting Out-of-Range Channels
Avoiding Timing Uncertainty with the NI 9381
Converting Voltage Values to Binary Values for the NI 9381

NI 9381 (FPGA Interface)

CompactRIO 0 V to 5 V, 12-bit, Multifunction Input/Output Module

Find NI 9381 examples

FPGA I/O Node

You can use an FPGA I/O Node, configured for reading and writing, with this device.

Terminal	Description
AI**x**	Analog input channel **x**, where **x** is the number of the channel. The NI 9381 has AI channels 0 to 7.
AO**x**	Analog output channel **x**, where **x** is the number of the channel. The NI 9381 has AO channels 0 to 3.
DIO**x**	Digital input/output channel **x**, where **x** is the number of the channel. The NI 9381 has DIO channels 0 to 3.
DIO3:0	Digital port consisting of channels 0 through 3. Channel 3 is returned in the MSB, and channel 0 is returned in the LSB.

Caution AI and AO operations that are run concurrently may exhibit jitter. Access both subsystems using a single I/O Node to avoid jitter in your application. Refer to the Avoiding Timing Uncertainty topic for more information.

Arbitration

Analog input and analog output channels of this device support only the Arbitrate if Multiple Requestors Only option for arbitration. You cannot configure arbitration settings for analog input and analog output channels of this device.

You can configure the arbitration settings for digital output channels of this device in the Advanced Code Generation page of the FPGA I/O Properties dialog box. The default arbitration setting is Never Arbitrate.

Digital input channels of this device support only the **Never Arbitrate** option for arbitration. You cannot configure arbitration settings for the digital input channels of this device.

I/O Methods

Use the FPGA I/O Method Node to access the following I/O methods for the DIO channels of this device.

Method	Description
Set Output Data	Refer to the FPGA I/O Method Node (FPGA Module) topic for a description of this method. This method is available only when you set the DIO line direction to output. You can set the DIO line direction in the C Series Module Properties dialog box.
Set Output Enable	Sets the line direction of the digital channel or the DIO3:0 digital port. Refer to the FPGA I/O Method Node (FPGA Module) topic for more information on this method. This method can introduce jitter in an analog input or analog output loop. This method is available only when you enable programmable DIO line changes on the module. You can enable programmable DIO line changes on the module in the C Series Module Properties dialog box.
Wait on Any Edge	Pauses the execution of the I/O Method Node until the next falling or rising edge of the digital signal. The **Timeout** input specifies in FPGA clock ticks how long the Wait on Any Edge method waits for the next falling or rising edge. A value of 0 causes the method to time out immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out. **Notes** This method is not available on the DIO3:0 port. For the first two seconds after resetting the F

	PGA VI, the time out wil l not start counting unt il the module is identifi ed.
Wait on Falling Edge	Pauses the execution of the I/O Method Node un til the next falling edge of the digital signal. The **Timeout** input specifies in FPGA clock ticks ho w long the Wait on Falling Edge method waits fo r the next falling edge. A value of 0 causes the m ethod to time out immediately, a negative value causes the method to wait indefinitely, and a po sitive value causes the method to wait for that n umber of clock ticks before timing out.  **Notes** This method is not available on the DI O3:0 port. For the first two secon ds after resetting the F PGA VI, the time out wil l not start counting unt il the module is identifi ed.
Wait on High Level	Pauses the execution of the I/O Method Node un til the digital signal is high. The **Timeout** input specifies in FPGA clock ticks how long the Wait o n High Level method waits for the next high leve l. A value of 0 causes the method to time out im mediately, a negative value causes the method t o wait indefinitely, and a positive value causes t he method to wait for that number of clock ticks before timing out.  **Notes** This method is not available on the DI O3:0 port. For the first two secon ds after resetting the F PGA VI, the time out wil

	l not start counting unt il the module is identifi ed.
Wait on Low Level	Pauses the execution of the I/O Method Node un til the digital signal is low. The **Timeout** input s pecifies in FPGA clock ticks how long the Wait o n Low Level method waits for the next low level. A value of 0 causes the method to time out imm ediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks be fore timing out. **Notes** This method is not available on the DI O3:0 port. For the first two secon ds after resetting the F PGA VI, the time out wil l not start counting unt il the module is identifi ed.
Wait on Rising Edge	Pauses the execution of the I/O Method Node un til the next rising edge of the digital signal. The **Timeout** input specifies in FPGA clock ticks ho w long the Wait on Rising Edge method waits for the next rising edge. A value of 0 causes the met hod to time out immediately, a negative value c auses the method to wait indefinitely, and a pos itive value causes the method to wait for that nu mber of clock ticks before timing out. **Notes** This method is not available on the DI O3:0 port. For the first two secon ds after resetting the F PGA VI, the time out wil l not start counting unt

	il the module is identifi ed.

Module Method

Use the FPGA I/O Method Node to access the following module method for this device.

Method	Description
Check Status	Returns a Boolean value that indicates whether the module is ready.

I/O Properties

Use the FPGA I/O Property Node to access the following I/O properties for AI and AO channels of this device.

Property	Description
LSB Weight	Returns the LSB weight in nV/LSB for the channe l. Use this value to convert and calibrate NI 9381 data if you set the **Calibration Mode** to **Raw** i n the C Series Module Properties dialog box.
Offset	Returns the calibration offset in nV for the chan nel. Use this value to convert and calibrate NI 93 81 data if you set the **Calibration Mode** to **Ra w** in the **C Series Module Properties** dialog b ox.

Module Properties

Use the FPGA I/O Property Node to access the following module properties for this device.

Property	Description
Module ID	Returns the module ID.
Serial Number	Returns the unique serial number of the module .
Vendor ID	Returns the NI vendor ID, 0x1093.

Single-Cycle Timed Loop

This device supports the single-cycle Timed Loop. Configure the number of input synchronizing registers for the channels of this device in the Advanced Code Generation page of the FPGA I/O Node Properties dialog box. Configure the number of output synchronizing registers for the channels of this device in the Advanced Code Generation page of the FPGA I/O Properties dialog box.

This device supports the Number of Synchronizing Registers for Output Data synchronizing register option when used in SCTL output. This option supports the same functionality as the **Number of Synchronizing Registers for Output Data** option described in the Advanced Code Generation FPGA I/O Properties Page (FPGA Module) topic, with the exception that you can use this option only in a single-cycle Timed Loop. You can implement either 0 or 1 synchronizing registers inside the single-cycle Timed Loop, however, if you configure 0 synchronizing registers outside of the single-cycle Timed Loop, the FPGA VI implements 1 synchronizing register by default.

When the device is within a single-cycle Timed Loop, it must be ready to perform digital I/O before a loop containing digital I/O starts. Poll the **Ready** output of the Check Status method to determine whether the module is ready. Digital input operations return invalid data if the module is not ready. The module also might ignore or delay digital output operations if it is not ready.

While the digital is performing digital I/O within a single-cycle Timed Loop, do not perform property reads or remove the module from the chassis. Doing any of these actions causes the module to be unable to perform digital I/O and the **Ready** output of the Check Status method to return FALSE.

FPGA Target Clock Support

This device supports only top-level FPGA target clock rates and single-cycle Timed Loop clock rates that are multiples of 40 MHz, such as 40 MHz, 80 MHz, 120 MHz, and so on.

Avoiding Timing Uncertainty with the NI 9381 (FPGA Interface)

Follow these guidelines to avoid introducing timing uncertainty into AI node, AO Node, DO Node, and Set Output Data method calls. Additionally, failing to follow

these guidelines may result in lost data points for DO Node calls or Set Output Data method calls when either of them are made from inside a single-cycle Timed Loop.

- Use a single I/O Node to access AI and AO operations to ensure proper sequencing.
- Do not run the Set Output Enable method when an AI, AO, or DO subsystems is active.
- Do not perform the following operations concurrently:
  - AI Node call
  - AO Node call
  - Set Output Enable method call
  - Automatic line direction change when a DO call is made under the following conditions:
    - The call is made from outside of a single-cycle Timed Loop.
    - The **Allow programmatic DIO line direction** checkbox is checked in the C Series Module Properties dialog box.
    - The DIO channel is configured as an input at the time when the DO node is called.

Refer to the NI 9381 Advanced IO VI in the `labview\examples\CompactRIO\Module Specific\NI 9381\NI 9381 Advanced IO\NI 9381 Advanced IO.lvproj` for an example of the recommended way to use the AI, AO , and DIO subsystems.

C Series Module Properties Dialog Box for the NI 9381 (FPGA Interface)

Right-click an NI 9381 C Series module in the **Project Explorer** window and select **Properties** from the shortcut menu to display this dialog box.

Use this dialog box to configure a C Series module.

This dialog box includes the following components:

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this option.
- **Location**—Specifies a slot in the chassis for the C Series module.
- **Calibration Mode**—Sets the calibration mode for the C Series module. Select **Calibrated** if you want the FPGA I/O Node to return calibrated, fixed-point data from the module in units of volts. The fixed-point data is unsigned, with a word length of 18 bits and an integer word length of 3 bits for the analog input channels and a word length of 16 bits and an integer word length of 3 bits for the analog output channels. Select **Raw** if you want the FPGA I/O Node to return uncalibrated, binary data from the module. If you select **Raw**, you must convert and calibrate the analog input values in the host VI. The default is **Calibrated**.
- **Channels**—Specifies the channel(s) for which you want to select the direction.
- **Selected Channel(s) Settings**—Specifies the direction for each channel.
- **Hot Swap Behavior (Analog Output)**—Specifies the state of the analog output channels when the C Series module is removed and reinserted with the FPGA VI loaded and running. The power-on output state is the state that a C Series output module is in when power is applied to the module. The default is Last output value.
- **Allow Programmatic DIO Line Direction Change**—Place a checkmark in this checkbox if you want to enable programmable DIO line changes on the module.

Caution Performing a DIO line direction change will affect the timing of any concurrent AI, AO, and DO operations. Refer to the Avoiding Timing Uncertainty topic for more information.

Converting Voltage Values to Binary Values for the NI 9381 (FPGA Interface)

Set the **Calibration Mode** to **Calibrated** in the C Series Module Properties dialog box for the NI 9381 if you want the FPGA I/O Node to accept fixed-point data in units of volts when writing to the module. If you set the **Calibration Mode** to **Raw**, the FPGA I/O Node accepts only binary values when writing to the module. You must convert output voltage values to binary values before you write them to the module. You must convert these values in the host VI.

Using an Equation to Convert Voltage to Binary

You can use the following equation in the host VI to convert the analog output values to binary values:

Binary Value = (**Voltage Value** – **Offset**) ÷ **LSB Weight**

where	**Binary Value** is the value you write to the FPGA I/O Node
	Current Value is the voltage in V that you want the channel to output
	Offset is the value returned by the Offset property
	LSB Weight is the value returned by the LSB Weight property

NI recommends using calibrated values for analog output. To convert calibrated voltage values, use the FPGA I/O Property Node to read the LSB Weight and Offset properties. If you do not want to read the LSB Weight and Offset values from the module, you can convert uncalibrated voltage values by using the following values for **Offset** and **LSB Weight**:

Offset = –5249

LSB Weight = $5.105\ V \div 2^{\textbf{DAC Resolution}}$

where	**DAC Resolution** is the DAC resolution value in the **NI 9381 Operating Instructions and Specifications**.

NI 9381 (Scan Interface)

CompactRIO 0 V to 5 V, 12-bit, Multifunction Input/Output Module

Module I/O Variables

To use I/O from this module in a VI, drag and drop I/O variables from the **Project Explorer** window to the block diagram of the VI. The I/O variables for the AI channels return floating-point data in volts. The I/O variables for the AO channels write floating-point data in volts. The I/O variables for the DIO channels read and write boolean values.

Module Channels

The NI 9381 has the following channels.

Channel	Description
AI**x**	Analog input channel **x**, where **x** is the number of the channel. For the NI 9381, **x** is 0 to 7.
AO**x**	Analog output channel **x**, where **x** is the number of the channel. For the NI 9381, **x** is 0 to 7.
DIO**x**	Digital input/output channel **x**, where **x** is the n umber of the channel. For the NI 9381, **x** is 0 to 3 .

C Series Module Properties Dialog Box

Use this dialog box to configure the NI 9381. Right-click the NI 9381 in the **Project Explorer** window and select **Properties** to display this dialog box. You can configure the following options.

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Type**—Specifies the type of C Series module. You cannot change this value.
- **Location**—Specifies a slot in the chassis for the C Series module.

- **Channels**—Specifies the channel(s) for which you want to configure settings.
- **Direction**—Specifies the initial line direction of the selected channel(s) as input or output.

Note If you are using direct access to read from or write to AI or AO channels of the NI 9381, the conversion time is somewhat longer than 50 µs.

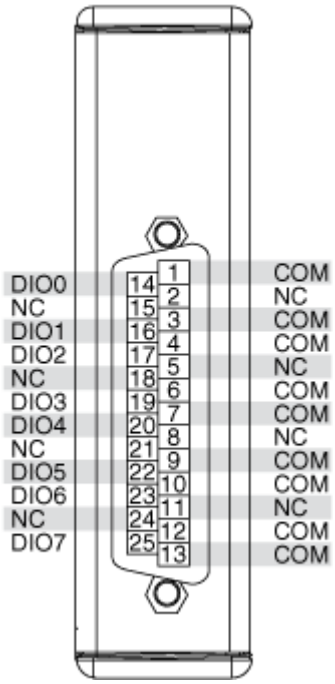
NI 9401

CompactRIO 8-Channel, TTL Digital Input/Output Module

Software Reference (?)

FPGA Interface | Scan Interface

NI 9401 Pinout



Related Topics

FPGA Interface
Configuring the Initial Line Direction for the NI 9401

NI 9401 (FPGA Interface)

CompactRIO 8-Channel, TTL Digital Input/Output Module

Find examples

FPGA I/O Node

You can use an FPGA I/O Node, configured for reading and writing, with this device. When you write to an NI 9401 channel, the FPGA I/O Node does not automatically enable the channel for output.

Terminals in Software

Use the FPGA I/O Node to access the following terminals for this device.

Terminal	Description
DIO**x**	Digital input/output channel **x**, where **x** is the number of the channel. The NI 9401 has DIO channels 0 to 7.
DIO3:0	Digital port consisting of channels 0 through 3. Channel 3 is returned in the MSB, and channel 0 is returned in the LSB.
DIO7:4	Digital port consisting of channels 4 through 7. Channel 7 is returned in the MSB, and channel 4 is returned in the LSB.
DIO7:0	Digital port consisting of channels 0 through 7. Channel 7 is returned in the MSB, and channel 0 is returned in the LSB.

Arbitration

You can configure the arbitration settings for digital output channels of this device in the Advanced Code Generation page of the FPGA I/O Properties dialog box. The default arbitration setting is Never Arbitrate. Digital input channels of this device

support only the **Never Arbitrate** option for arbitration. You cannot configure arbitration settings for the digital input channels of this device.

I/O Methods

Use the FPGA I/O Method Node to access the following I/O methods for this device.

Method	Description
Wait on Any Edge	Pauses the execution of the I/O Method Node until the next falling or rising edge of the digital signal. The **Timeout** input specifies in FPGA clock ticks how long the Wait on Any Edge method waits for the next falling or rising edge. A value of 0 causes the method to time out immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.
Wait on Falling Edge	Pauses the execution of the I/O Method Node until the next falling edge of the digital signal. The **Timeout** input specifies in FPGA clock ticks how long the Wait on Falling Edge method waits for the next falling edge. A value of 0 causes the method to time out immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.
Wait on High Level	Pauses the execution of the I/O Method Node until the digital signal is high. The **Timeout** input specifies in FPGA clock ticks how long the Wait on High Level method waits for the next high level. A value of 0 causes the method to time out immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.
Wait on Low Level	Pauses the execution of the I/O Method Node until the digital signal is low. The **Timeout** input specifies in FPGA clock ticks how long the Wait on Low Level method waits for the next low level.

	A value of 0 causes the method to time out immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.
Wait on Rising Edge	Pauses the execution of the I/O Method Node until the next rising edge of the digital signal. The **Timeout** input specifies in FPGA clock ticks how long the Wait on Rising Edge method waits for the next rising edge. A value of 0 causes the method to time out immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.

Module Methods

Use the FPGA I/O Method Node to access the following module methods for this device.

Method	Description
Check Status	Returns a Boolean value that indicates whether the module is ready.  **Note** During the first 2 seconds after you reset the FPGA VI, the error terminals on this method may not correctly report certain types of errors.
Set Line Direction	Sets the direction of one port to input or output.

I/O Properties

This device does not support any I/O properties.

Module Properties

Use the FPGA I/O Property Node to access the following module properties for this device.

Property	Description
Module ID	Returns the module ID.
Serial Number	Returns the unique serial number of the module .
Vendor ID	Returns the NI vendor ID, 0x1093.

Single-Cycle Timed Loop

This device supports the single-cycle Timed Loop. Configure the number of output synchronizing registers for the channels of this device in the Advanced Configuration dialog box. Configure the number of input synchronizing registers for the channels of this device in the Advanced Code Generation page of the FPGA I/O Node Properties dialog box.

When the module is within a single-cycle Timed Loop, it must be ready to perform digital I/O before a loop containing digital I/O starts. Poll the **Ready** output of the Check Status method to determine whether the module is ready. Digital input operations return invalid data if the module is not ready. The module also might ignore or delay digital output operations if it is not ready.

While the module is performing digital I/O within a single-cycle Timed Loop, do not perform property reads, use the Set Line Direction method, or remove the module from the chassis. Doing any of these actions causes the module to be unable to perform digital I/O and the **Ready** output of the Check Status method to return FALSE.

FPGA Target Clock Support

This device supports only top-level FPGA target clock rates and single-cycle Timed Loop clock rates that are multiples of 40 MHz, such as 40 MHz, 80 MHz, 120 MHz, and so on.

C Series Module Properties Dialog Box for the NI 9401 (FPGA Interface)

Right-click an NI 9401 C Series module in the **Project Explorer** window and select **Properties** from the shortcut menu to display this dialog box.

Use this dialog box to configure a C Series module.

This dialog box includes the following components:

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this option.
- **Location**—Specifies a slot in the chassis for the C Series module.
- **Initial Line Direction**—Sets the initial line direction for each digital port to digital input or digital output. The default is digital input.
- **Advanced**—Launches the Advanced Configuration dialog box.

Configuring the Initial Line Direction for the NI 9401 (FPGA Interface)

Each digital port on the NI 9401 is initially configured as a digital input. You can configure the initial line direction for each port on the NI 9401 at edit time using the C Series Module Properties dialog box. You can programmatically change the line direction for each port at run time using the FPGA I/O Method Node. The execution of an I/O Method Node that is configured with a Set Line Direction method overwrites the value you configured in the **C Series Module Properties** dialog box.

Configuring Line Direction Using the C Series Module Properties Dialog Box

Complete the following steps to configure the line direction of each digital port using the **C Series Module Properties** dialog box.

1. Configure the CompactRIO system, and add an NI 9401.

2. Right-click the NI 9401 in the **Project Explorer** window and select **Properties** from the shortcut menu to display the **C Series Module Properties** dialog box.
3. Select the direction for each port from the **Initial Line Direction** pull-down menus.
4. Click the **OK** button.
5. Select **File»Save All** in the **Project Explorer** window.

Configuring Line Direction Using the FPGA I/O Method Node

Complete the following steps to configure the line direction of each digital port using the FPGA I/O Method Node.

1. Place an FPGA I/O Method Node on the block diagram and configure it for the NI 9401.
2. Click the **Method** section and select the **Set Line Direction** method from the shortcut menu.
3. Right-click each digital port input and select **Create»Control** from the shortcut menu.
4. On the front panel of the VI, select the direction for each port from the digital port pull-down menus.

NI 9401 (Scan Interface)

CompactRIO 8-Channel, TTL Digital Input/Output Module

 Open digital input example

 Open digital output example

Module I/O Variables

To use I/O from this module in a VI, drag and drop I/O variables from the **Project Explorer** window to the block diagram of the VI. The I/O variables for the channels read and write Boolean values.

Module Channels

The NI 9401 has the following channels.

Channel	Description
DIO**x**	Digital input/output channel **x**, where **x** is the n umber of the channel. For the NI 9401, **x** is 0 to 7 .

C Series Module Properties Dialog Box

Use this dialog box to configure the NI 9401. Right-click the NI 9401 in the **Project Explorer** window and select **Properties** to display this dialog box. You can configure the following options.

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this value.
- **Location**—Specifies a slot in the chassis for the C Series module.
- **Initial Line Direction**—Specifies the initial line direction of each four-channel port as input or output.

Specialty Digital Configuration

You can use the Specialty Digital Configuration page of the **C Series Module Properties** dialog box to configure channels of this module for counter input, counter-driven output, pulse-width modulation output, or quadrature input.

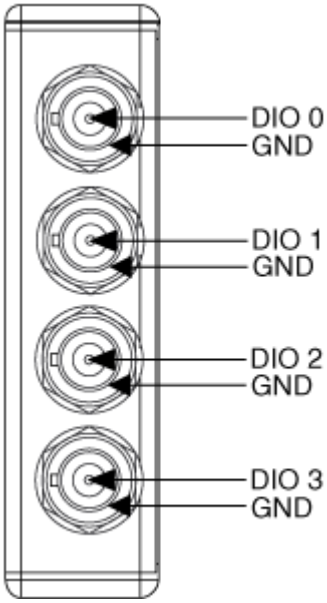
NI 9402

CompactRIO 4-Channel, LVTTL Digital Input/Output Module

Software Reference (?)

FPGA Interface | Scan Interface

NI 9402 Pinout



Related Topics

FPGA Interface
Configuring the Line Direction for the NI 9402

NI 9402 (FPGA Interface)

CompactRIO 4-Channel, LVTTL Digital Input/Output Module

FPGA I/O Node

You can use an FPGA I/O Node, configured for reading and writing, with this device.

Terminals in Software

Use the FPGA I/O Node to access the following terminals for this device.

Terminal	Description

DIO**x**	Digital input/output channel **x**, where **x** is the number of the channel. The NI 9402 has DIO channels 0 to 3.
DIO3:0	Digital port consisting of channels 0 through 3. Channel 3 is returned in the MSB, and channel 0 is returned in the LSB.

Arbitration

You can configure the arbitration settings for digital output channels of this device in the Advanced Code Generation page of the FPGA I/O Properties dialog box. The default arbitration setting is Never Arbitrate. Digital input channels of this device support only the **Never Arbitrate** option for arbitration. You cannot configure arbitration settings for the digital input channels of this device.

I/O Methods

Use the FPGA I/O Method Node to access the following I/O methods for this device.

Method	Description
Set Output Data	Refer to the FPGA I/O Method Node (FPGA Module) topic for a description of this method.
Set Output Enable	Sets the line direction of the digital channel or the DIO3:0 digital port. Refer to the FPGA I/O Method Node (FPGA Module) topic for more information on this method.
Wait on Any Edge	Pauses the execution of the I/O Method Node until the next falling or rising edge of the digital signal. The **Timeout** input specifies in FPGA clock ticks how long the Wait on Any Edge method waits for the next falling or rising edge. A value of 0 causes the method to time out immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.
Wait on Falling Edge	Pauses the execution of the I/O Method Node until the next falling edge of the digital signal. The **Timeout** input specifies in FPGA clock ticks ho

	w long the Wait on Falling Edge method waits fo r the next falling edge. A value of 0 causes the m ethod to time out immediately, a negative value causes the method to wait indefinitely, and a po sitive value causes the method to wait for that n umber of clock ticks before timing out.
Wait on High Level	Pauses the execution of the I/O Method Node un til the digital signal is high. The **Timeout** input specifies in FPGA clock ticks how long the Wait o n High Level method waits for the next high leve l. A value of 0 causes the method to time out im mediately, a negative value causes the method t o wait indefinitely, and a positive value causes t he method to wait for that number of clock ticks before timing out.
Wait on Low Level	Pauses the execution of the I/O Method Node un til the digital signal is low. The **Timeout** input s pecifies in FPGA clock ticks how long the Wait o n Low Level method waits for the next low level. A value of 0 causes the method to time out imm ediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks be fore timing out.
Wait on Rising Edge	Pauses the execution of the I/O Method Node un til the next rising edge of the digital signal. The **Timeout** input specifies in FPGA clock ticks ho w long the Wait on Rising Edge method waits for the next rising edge. A value of 0 causes the met hod to time out immediately, a negative value c auses the method to wait indefinitely, and a pos itive value causes the method to wait for that nu mber of clock ticks before timing out.

Module Method

Use the FPGA I/O Method Node to access the following module method for this device.

Method	Description

Check Status	Returns a Boolean value that indicates whether the module is ready.  **Note** During the first 2 seconds after you reset the FPGA VI, the error terminals on this method may not correctly report certain types of errors.

I/O Properties

This device does not support any I/O properties.

Module Properties

Use the FPGA I/O Property Node to access the following module properties for this device.

Property	Description
Module ID	Returns the module ID.
Serial Number	Returns the unique serial number of the module.
Vendor ID	Returns the NI vendor ID, 0x1093.

Single-Cycle Timed Loop

This device supports the single-cycle Timed Loop. Configure the number of input synchronizing registers for the channels of this device in the Advanced Code Generation page of the FPGA I/O Node Properties dialog box. Configure the number of output synchronizing registers for the channels of this device in the Advanced Code Generation page of the FPGA I/O Properties dialog box.

The NI 9402 supports the following output synchronizing register options:

- **Number of Synchronizing Registers for Output Data when used in SCTL**

- **Number of Synchronizing Registers for Output Enable when used in SCTL**

These two options support the same functionality as the **Number of Synchronizing Registers for Output Data** and **Number of Synchronizing Registers for Output Enable** options described in the Advanced Code Generation FPGA I/O Properties Page (FPGA Module) topic, with the exception that you can use these options only in a single-cycle Timed Loop. You can implement either 0 or 1 synchronizing registers inside the single-cycle Timed Loop, however, if you configure 0 synchronizing registers outside of the single-cycle Timed Loop, the FPGA VI implements 1 synchronizing register by default.

When the module is within a single-cycle Timed Loop, it must be ready to perform digital I/O before a loop containing digital I/O starts. Poll the **Ready** output of the Check Status method to determine whether the module is ready. Digital input operations return invalid data if the module is not ready. The module also might ignore or delay digital output operations if it is not ready.

While the module is performing digital I/O within a single-cycle Timed Loop, do not perform property reads or remove the module from the chassis. Doing any of these actions causes the module to be unable to perform digital I/O and the **Ready** output of the Check Status method to return FALSE.

FPGA Target Clock Support

This device supports only top-level FPGA target clock rates and single-cycle Timed Loop clock rates that are multiples of 40 MHz, such as 40 MHz, 80 MHz, 120 MHz, and so on.

C Series Module Properties Dialog Box for the NI 9402 (FPGA Interface)

Right-click an NI 9402 C Series module in the **Project Explorer** window and select **Properties** from the shortcut menu to display this dialog box.

Use this dialog box to configure a C Series module.

This dialog box includes the following components:

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this option.
- **Location**—Specifies a slot in the chassis for the C Series module.
- **Channels**—Specifies the channel(s) for which you want to select the line direction.
- **Selected Channel(s) Settings**—Specifies the line direction for each channel.
  - **Direction**—Sets the line direction for the selected channel(s) to digital input or digital output. The default is digital input.

Configuring the Line Direction for the NI 9402 (FPGA Interface)

Each digital channel on the NI 9402 is initially configured as a digital input. You can configure the initial line direction for each channel on the NI 9402 at edit time using the C Series Module Properties dialog box. You can programmatically change the line direction for each channel at run time using the FPGA I/O Method Node. The execution of an I/O Method Node that is configured with a Set Output Enable method overwrites the values you configured in the **C Series Module Properties** dialog box. In addition, the execution of an FPGA I/O Node configured for output automatically configures the line for output and overwrites the values you configured in the **C Series Module Properties** dialog box or using the **Set Output Enable** method.

Configuring Line Direction Using the C Series Module Properties Dialog Box

Complete the following steps to set the line direction of channels using the **C Series Module Properties** dialog box.

1. Configure the CompactRIO system, and add an NI 9402.

2. Right-click the NI 9402 in the **Project Explorer** window and select **Properties** from the shortcut menu to display the **C Series Module Properties** dialog box.
3. Select the channel(s) for which you want to configure the line direction from the **Channels** table. You can select more than one channel by holding the <Ctrl> or <Shift> key when selecting channels.
4. Select the direction for the channel(s) from the **Direction** pull-down menu.
5. Click the **OK** button.
6. Select **File»Save All** in the **Project Explorer** window.

Configuring Line Direction of One Channel Using the FPGA I/O Method Node

Complete the following steps to set the line direction of a channel using the FPGA I/O Method Node.

1. Create FPGA I/O items for the channel of the NI 9402 for which you want to configure the line direction.
2. Place an FPGA I/O Method Node on the block diagram and configure it for this channel.
3. Click the **Method** section and select the **Set Output Enable** method from the shortcut menu.
4. Right-click the **Enable** input and select **Create»Control** from the shortcut menu.
5. On the front panel of the VI, click the **Enable** Boolean control to set it to TRUE if you want to set the line direction of the channel to digital output.

Configuring Line Direction of Multiple Channels Using the FPGA I/O Method Node

Complete the following steps to set the line direction of multiple channels using the FPGA I/O Method Node.

1. Create FPGA I/O items for the DIO3:0 digital port of the NI 9402.

2. Place an FPGA I/O Method Node on the block diagram and configure it for the DIO3:0 digital port.
3. Click the **Method** section and select the **Set Output Enable** method from the shortcut menu.
4. Right-click the **Enable** input and select **Create»Control** from the shortcut menu. The **Enable** control appears as an unsigned 8-bit integer. Each bit in the integer represents the line direction of one channel of the NI 9402.
5. On the front panel of the VI, use the **Enable** control to enter the line direction for each channel in the port. Change a bit to 1 to set the line direction of the corresponding channel to digital output. Leave a bit as 0 to set the line direction of the corresponding channel to digital input. Refer to the table below for examples of what to enter in the **Enable** control.

Channel Line Direction Configuration	Enable Control (Floating Point)	Enable Control (Binary)	Enable Control (Hex)
Change all channels to input	0	0000	0x00
Change all channels to output	15	1111	0x0F
Change channel 0 to output	1	0001	0x01

NI 9402 (Scan Interface)

CompactRIO 4-Channel, LVTTL Digital Input/Output Module

Open digital input example

Open digital output example

Module I/O Variables

To use I/O from this module in a VI, drag and drop I/O variables from the **Project Explorer** window to the block diagram of the VI. The I/O variables for the channels read and write Boolean values.

Module Channels

The NI 9402 has the following channels.

Channel	Description
DIO**x**	Digital input/output channel **x**, where **x** is the number of the channel. For the NI 9402, **x** is 0 to 3.

C Series Module Properties Dialog Box

Use this dialog box to configure the NI 9402. Right-click the NI 9402 in the **Project Explorer** window and select **Properties** to display this dialog box. You can configure the following options.

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this value.
- **Location**—Specifies a slot in the chassis for the C Series module.
- **Channels**—Specifies the channel(s) for which you want to configure settings.
- **Direction**—Specifies the initial line direction of the selected channel(s) as input or output.

Specialty Digital Configuration

You can use the Specialty Digital Configuration page of the **C Series Module Properties** dialog box to configure channels of this module for counter input, counter-driven output, pulse-width modulation output, or quadrature input.

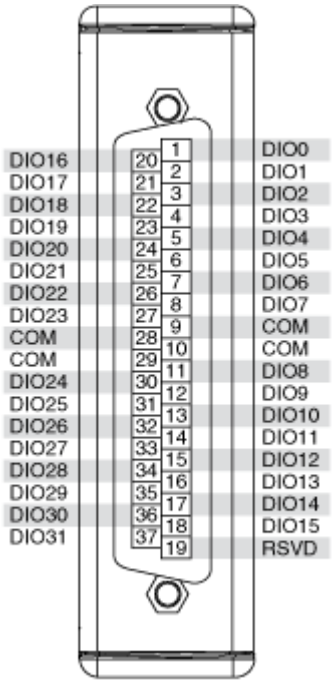
NI 9403

CompactRIO 32-Channel, TTL Digital Input/Output Module

Software Reference (?)

FPGA Interface | Scan Interface

NI 9403 Pinout



Related Topics

FPGA Interface
Configuring the Line Direction for the NI 9403

NI 9403 (FPGA Interface)

CompactRIO 32-Channel, TTL Digital Input/Output Module

FPGA I/O Node

You can use an FPGA I/O Node, configured for reading and writing, with this device.

Terminals in Software

Use the FPGA I/O Node to access the following terminals for this device.

Terminal	Description
DIO**x**	Digital input/output channel **x**, where **x** is the number of the channel. The NI 9403 has DIO channels 0 to 31.
DIO7:0	Digital port consisting of channels 0 through 7. Channel 7 is returned in the MSB, and channel 0 is returned in the LSB.
DIO15:8	Digital port consisting of channels 8 through 15. Channel 15 is returned in the MSB, and channel 8 is returned in the LSB.
DIO23:16	Digital port consisting of channels 16 through 23. Channel 23 is returned in the MSB, and channel 16 is returned in the LSB.
DIO31:24	Digital port consisting of channels 24 through 31. Channel 31 is returned in the MSB, and channel 24 is returned in the LSB.
DIO31:0	Digital port consisting of channels 0 through 31. Channel 31 is returned in the MSB, and channel 0 is returned in the LSB.

Arbitration

This device supports only the Arbitrate if Multiple Requestors Only and Never Arbitrate options for arbitration. The default arbitration setting is **Arbitrate if Multiple Requestors Only**.

If you are sure that the design of the FPGA VI will never allow more than one digital function to execute at the same time, even on different channels, you can place a checkmark in the **Disable Arbitration** checkbox on the C Series Module Properties dialog box to disable arbitration and reduce the amount of FPGA logic used by VIs. If more than one digital function could execute simultaneously in the FPGA VI, leave the box unchecked.

I/O Methods

Use the FPGA I/O Method Node to access the following I/O methods for this device.

Method	Description

Read and Set Output Data	First returns the data read from the digital line or port, then writes data to the line or port without enabling it. You can use the Read and Set Output Data method to optimize performance when performing successive reads and writes on a DIO resource. For the NI 9403, this method is faster than using a read FPGA I/O Node and a Set Output Data method. The data type of the output and input depends on the I/O item. If the I/O item is a digital line, **Data to Set** requires a Boolean data type. If the I/O item is a digital port, **Data to Set** requires a numeric data type.
Set Output Data	Refer to the FPGA I/O Method Node (FPGA Module) topic for a description of this method.
Set Output Enable	Sets the line direction of the digital channel or port. Refer to the FPGA I/O Method Node (FPGA Module) topic for more information on this method.

Module Methods

This device does not support any module methods.

I/O Properties

This device does not support any I/O properties.

Module Properties

Use the FPGA I/O Property Node to access the following module properties for this device.

Property	Description
Module ID	Returns the module ID.
Serial Number	Returns the unique serial number of the module.
Vendor ID	Returns the NI vendor ID, 0x1093.

Single-Cycle Timed Loop

This device does not support the single-cycle Timed Loop.

Hardware Documentation

Refer to the NI 9403 hardware documentation on ni.com/manuals for information about module specifications and how to use the module. Refer to the CompactRIO Related Documentation topic for additional CompactRIO documentation resources.

C Series Module Properties Dialog Box for the NI 9403 (FPGA Interface)

Right-click an NI 9403 C Series module in the **Project Explorer** window and select **Properties** from the shortcut menu to display this dialog box.

Use this dialog box to configure a C Series module.

This dialog box includes the following components:

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this option.
- **Location**—Specifies a slot in the chassis for the C Series module.
- **Channels**—Specifies the channel(s) for which you want to select the line direction.
- **Selected Channel(s) Settings**—Specifies the line direction for each channel.
  - **Direction**—Sets the line direction for the selected channel(s) to digital input or digital output. The default is digital input.
- **Disable Arbitration**—Place a checkmark in this checkbox if you want to change the arbitration setting to Never Arbitrate and reduce the amount of FPGA logic used by VIs. Check this box only if you are sure that the design of

the FPGA VI will never allow more than one digital function to execute at the same time, even on different channels. If more than one digital function could execute simultaneously in the FPGA VI, leave the box unchecked to keep the default Arbitrate if Multiple Requestors Only arbitration setting.

Configuring the Line Direction for the NI 9403 (FPGA Interface)

Each digital channel on the NI 9403 is initially configured as a digital input. You can configure the initial line direction for each channel on the NI 9403 at edit time using the C Series Module Properties dialog box. You can programmatically change the line direction for each channel at run time using the FPGA I/O Method Node. The execution of an I/O Method Node that is configured with a Set Output Enable method overwrites the values you configured in the **C Series Module Properties** dialog box. In addition, the execution of an FPGA I/O Node configured for output automatically configures the line for output and overwrites the values you configured in the **C Series Module Properties** dialog box or using the **Set Output Enable** method.

Configuring Line Direction Using the C Series Module Properties Dialog Box

Complete the following steps to set the line direction of channels using the **C Series Module Properties** dialog box.

1. Configure the CompactRIO system, and add an NI 9403.
2. Right-click the NI 9403 in the **Project Explorer** window and select **Properties** from the shortcut menu to display the **C Series Module Properties** dialog box.
3. Select the channel(s) for which you want to configure the line direction from the **Channels** table. You can select more than one channel by holding the <Ctrl> or <Shift> key when selecting channels.
4. Select the direction for the channel(s) from the **Direction** pull-down menu.
5. Click the **OK** button.
6. Select **File»Save All** in the **Project Explorer** window.

Configuring Line Direction of One Channel Using the FPGA I/O Method Node

Complete the following steps to set the line direction of a channel using the FPGA I/O Method Node.

1. Create FPGA I/O items for the channel of the NI 9403 for which you want to configure the line direction.
2. Place an FPGA I/O Method Node on the block diagram and configure it for this channel.
3. Click the **Method** section and select the **Set Output Enable** method from the shortcut menu.
4. Right-click the **Enable** input and select **Create»Control** from the shortcut menu.
5. On the front panel of the VI, click the **Enable** Boolean control to set it to TRUE if you want to set the line direction of the channel to digital output.

Configuring Line Direction of Multiple Channels Using the FPGA I/O Method Node

Complete the following steps to set the line direction of multiple channels using the FPGA I/O Method Node.

1. Create FPGA I/O items for the digital port of the NI 9403 that contains the channels you want to configure.
2. Place an FPGA I/O Method Node on the block diagram and configure it for this digital port.
3. Click the **Method** section and select the **Set Output Enable** method from the shortcut menu.
4. Right-click the **Enable** input and select **Create»Control** from the shortcut menu. If you configured the FPGA I/O Method Node for the DIO7:0, DIO15:8, DIO23:16, or DIO31:24 digital port, the **Enable** control appears as an unsigned 8-bit integer. If you configured the FPGA I/O Method Node for the DIO31:0 digital port, the **Enable** control appears as an unsigned 32-bit integer. Each bit in the integer represents the line direction of one channel of the NI 9403.

5. On the front panel of the VI, use the **Enable** control to enter the line direction for each channel in the port. Change a bit to 1 to set the line direction of the corresponding channel to digital output. Leave a bit as 0 to set the line direction of the corresponding channel to digital input. Refer to the table below for examples of what to enter in the **Enable** control if you configured the FPGA I/O Method Node for the DIO7:0 digital port.

Channel Line Direction Configuration	Enable Control (Hex)	Enable Control (Binary)
Change all channels to input	0x00	0b00000000
Change all channels to output	0xFF	0b11111111
Change channel 0 to output	0x01	0b00000001
Change channels 0 through 5 to output	0x3F	0b00111111
Change channels 3 and 7 to output	0x88	0b10001000

Refer to the table below for examples of what to enter in the **Enable** control if you configured the FPGA I/O Method Node for the DIO31:0 digital port.

Channel Line Direction Configuration	Enable Control (Hex)	Enable Control (Binary)
Change all channels to input	0x00000000	0b0000000000000000 0000000000000000
Change all channels to output	0xFFFFFFFF	0b1111111111111111 1111111111111111
Change channel 0 to output	0x00000001	0b0000000000000000 0000000000000001
Change channels 0 through 5 to output	0x0000003F	0b0000000000000000 0000000000111111
Change channels 3 and 7 to output	0x00000088	0b0000000000000000 0000000010001000

NI 9403 (Scan Interface)

CompactRIO 32-Channel, TTL Digital Input/Output Module

Open digital input example

Open digital output example

Module I/O Variables

To use I/O from this module in a VI, drag and drop I/O variables from the **Project Explorer** window to the block diagram of the VI. The I/O variables for the channels read and write Boolean values.

Module Channels

The NI 9403 has the following channels.

Channel	Description
DIO**x**	Digital input/output channel **x**, where **x** is the n umber of the channel. For the NI 9403, **x** is 0 to 3 1.

C Series Module Properties Dialog Box

Use this dialog box to configure the NI 9403. Right-click the NI 9403 in the **Project Explorer** window and select **Properties** to display this dialog box. You can configure the following options.

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this value.
- **Location**—Specifies a slot in the chassis for the C Series module.
- **Channels**—Specifies the channel(s) for which you want to configure settings.

- **Initial Line Direction**—Specifies the initial line direction of the selected channel(s) as input or output.

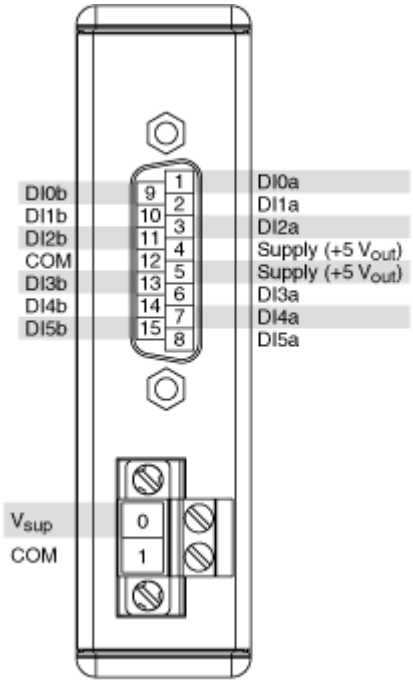
NI 9411

CompactRIO 6-Channel, Differential or TTL Digital Input Module

Software Reference (?)

FPGA Interface | Scan Interface

NI 9411 Pinout



NI 9411 (FPGA Interface)

CompactRIO 6-Channel, Differential or TTL Digital Input Module

FPGA I/O Node

You can use an FPGA I/O Node, configured for reading, with this device.

Terminals in Software

Use the FPGA I/O Node to access the following terminals for this device.

Terminal	Description
DI**x**	Digital input channel **x**, where **x** is the number of the channel. The NI 9411 has DI channels 0 to 5.
DI5:0	Digital port consisting of channels 0 through 5. Channel 5 is returned in bit 5, and channel 0 is returned in bit 0. Bits 6 and 7 return a zero.

Arbitration

This device supports only the Never Arbitrate option for arbitration. You cannot configure arbitration settings for this device.

I/O Methods

Use the FPGA I/O Method Node to access the following I/O methods for this device.

Method	Description
Wait on Any Edge	Pauses the execution of the I/O Method Node until the next falling or rising edge of the digital signal. The **Timeout** input specifies in FPGA clock ticks how long the Wait on Any Edge method waits for the next falling or rising edge. A value of 0 causes the method to time out immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.
Wait on Falling Edge	Pauses the execution of the I/O Method Node until the next falling edge of the digital signal. The **Timeout** input specifies in FPGA clock ticks how long the Wait on Falling Edge method waits for the next falling edge. A value of 0 causes the method to time out immediately, a negative value causes the method to wait indefinitely, and a po

	sitive value causes the method to wait for that number of clock ticks before timing out.
Wait on High Level	Pauses the execution of the I/O Method Node until the digital signal is high. The **Timeout** input specifies in FPGA clock ticks how long the Wait on High Level method waits for the next high level. A value of 0 causes the method to time out immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.
Wait on Low Level	Pauses the execution of the I/O Method Node until the digital signal is low. The **Timeout** input specifies in FPGA clock ticks how long the Wait on Low Level method waits for the next low level. A value of 0 causes the method to time out immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.
Wait on Rising Edge	Pauses the execution of the I/O Method Node until the next rising edge of the digital signal. The **Timeout** input specifies in FPGA clock ticks how long the Wait on Rising Edge method waits for the next rising edge. A value of 0 causes the method to time out immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.

Module Methods

Use the FPGA I/O Method Node to access the following module method for this device.

Method	Description
Check Status	Returns a Boolean value that indicates whether the module is ready. **Note** During the first 2 seconds after you reset

	the FPGA VI, the error terminals on this method may not correctly report certain types of errors.

I/O Properties

This device does not support any I/O properties.

Module Properties

Use the FPGA I/O Property Node to access the following module properties for this device.

Property	Description
Module ID	Returns the module ID.
Serial Number	Returns the unique serial number of the module.
Vendor ID	Returns the NI vendor ID, 0x1093.

Single-Cycle Timed Loop

This device supports the single-cycle Timed Loop. Configure the number of input synchronizing registers for the channels of this device in the Advanced Code Generation page of the FPGA I/O Node Properties dialog box.

When the module is within a single-cycle Timed Loop, it must be ready to perform digital input before a loop containing digital input starts. Poll the **Ready** output of the Check Status method to determine whether the module is ready. Digital input operations return invalid data if the module is not ready.

While the module is performing digital input within a single-cycle Timed Loop, do not perform property reads or remove the module from the chassis. Doing either of these actions causes the module to be unable to perform digital input and the **Ready** output of the Check Status method to return FALSE.

FPGA Target Clock Support

This device supports only top-level FPGA target clock rates and single-cycle Timed Loop clock rates that are multiples of 40 MHz, such as 40 MHz, 80 MHz, 120 MHz, and so on.

NI 9411 (Scan Interface)

CompactRIO 6-Channel, Differential or TTL Digital Input Module

Open example

Module I/O Variables

To use I/O from this module in a VI, drag and drop I/O variables from the **Project Explorer** window to the block diagram of the VI. The I/O variables for the channels return data as Boolean values.

Module Channels

The NI 9411 has the following channels.

Channel	Description
DI**x**	Digital input channel **x**, where **x** is the number of the channel. For the NI 9411, **x** is 0 to 5.

C Series Module Properties Dialog Box

Use this dialog box to configure the NI 9411. Right-click the NI 9411 in the **Project Explorer** window and select **Properties** to display this dialog box. You can configure the following options.

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this value.

- **Location**—Specifies a slot in the chassis for the C Series module.

Specialty Digital Configuration

You can use the Specialty Digital Configuration page of the **C Series Module Properties** dialog box to configure channels of this module for counter input or quadrature input.

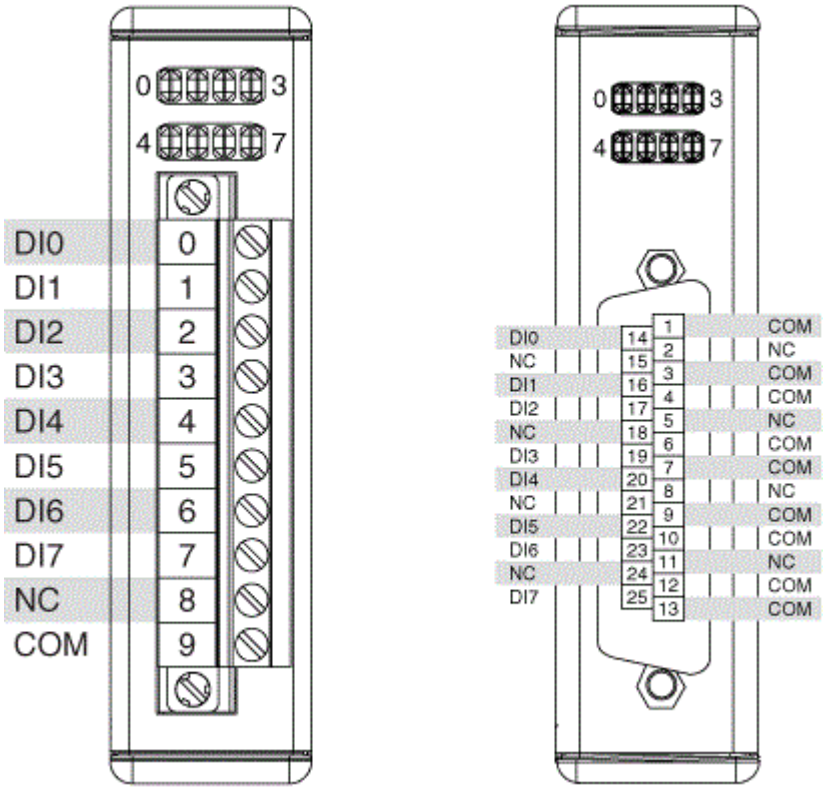
NI 9421

CompactRIO 8-Channel, 24 V, Sinking Digital Input Module

Software Reference (?)

FPGA Interface | Scan Interface

NI 9421 Pinout



NI 9421 (FPGA Interface)

CompactRIO 8-Channel, 24 V, Sinking Digital Input Module

FPGA I/O Node

You can use an FPGA I/O Node, configured for reading, with this device.

Terminals in Software

Use the FPGA I/O Node to access the following terminals for this device.

Terminal	Description
DI**x**	Digital input channel **x**, where **x** is the number of the channel. The NI 9421 has DI channels 0 to 7.
DI7:0	Digital port consisting of channels 0 through 7. Channel 7 is returned in the MSB, and channel 0 is returned in the LSB.

Arbitration

This device supports only the Never Arbitrate option for arbitration. You cannot configure arbitration settings for this device.

I/O Methods

Use the FPGA I/O Method Node to access the following I/O methods for this device.

Method	Description
Wait on Any Edge	Pauses the execution of the I/O Method Node until the next falling or rising edge of the digital signal. The **Timeout** input specifies in FPGA clock ticks how long the Wait on Any Edge method waits for the next falling or rising edge. A value of 0 causes the method to time out immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.

Wait on Falling Edge	Pauses the execution of the I/O Method Node until the next falling edge of the digital signal. The **Timeout** input specifies in FPGA clock ticks how long the Wait on Falling Edge method waits for the next falling edge. A value of 0 causes the method to time out immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.
Wait on High Level	Pauses the execution of the I/O Method Node until the digital signal is high. The **Timeout** input specifies in FPGA clock ticks how long the Wait on High Level method waits for the next high level. A value of 0 causes the method to time out immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.
Wait on Low Level	Pauses the execution of the I/O Method Node until the digital signal is low. The **Timeout** input specifies in FPGA clock ticks how long the Wait on Low Level method waits for the next low level. A value of 0 causes the method to time out immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.
Wait on Rising Edge	Pauses the execution of the I/O Method Node until the next rising edge of the digital signal. The **Timeout** input specifies in FPGA clock ticks how long the Wait on Rising Edge method waits for the next rising edge. A value of 0 causes the method to time out immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.

Module Methods

Use the FPGA I/O Method Node to access the following module method for this device.

Method	Description
Check Status	Returns a Boolean value that indicates whether the module is ready.  **Note** During the first 2 seconds after you reset the FPGA VI, the error terminals on this method may not correctly report certain types of errors.

I/O Properties

This device does not support any I/O properties.

Module Properties

Use the FPGA I/O Property Node to access the following module properties for this device.

Property	Description
Module ID	Returns the module ID.
Serial Number	Returns the unique serial number of the module.
Vendor ID	Returns the NI vendor ID, 0x1093.

Single-Cycle Timed Loop

This device supports the single-cycle Timed Loop. Configure the number of input synchronizing registers for the channels of this device in the Advanced Code Generation page of the FPGA I/O Node Properties dialog box.

When the module is within a single-cycle Timed Loop, it must be ready to perform digital input before a loop containing digital input starts. Poll the **Ready** output of

the Check Status method to determine whether the module is ready. Digital input operations return invalid data if the module is not ready.

While the module is performing digital input within a single-cycle Timed Loop, do not perform property reads or remove the module from the chassis. Doing either of these actions causes the module to be unable to perform digital input and the **Ready** output of the Check Status method to return FALSE.

FPGA Target Clock Support

This device supports only top-level FPGA target clock rates and single-cycle Timed Loop clock rates that are multiples of 40 MHz, such as 40 MHz, 80 MHz, 120 MHz, and so on.

C Series Module Properties Dialog Box for the NI 9375/9411/9421/9422/9423/9425/9426/9435/9436/9437/950x (FPGA Interface)

Right-click an NI 9375, NI 9411, NI 9421, NI 9422, NI 9423, NI 9425, NI 9426, NI 9435, NI 9436, NI 9437, NI 9501, or NI 9505 C Series module in the **Project Explorer** window and select **Properties** from the shortcut menu to display this dialog box.

Use this dialog box to configure a C Series module.

This dialog box includes the following components:

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this option.
- **Location**—Specifies a slot in the chassis for the C Series module.

NI 9421 (Scan Interface)

CompactRIO 8-Channel, 24 V, Sinking Digital Input Module


Open example

Module I/O Variables

To use I/O from this module in a VI, drag and drop I/O variables from the **Project Explorer** window to the block diagram of the VI. The I/O variables for the channels return data as Boolean values.

Module Channels

The NI 9421 has the following channels.

Channel	Description
DI**x**	Digital input channel **x**, where **x** is the number of the channel. For the NI 9421, **x** is 0 to 7.

C Series Module Properties Dialog Box

Use this dialog box to configure the NI 9421. Right-click the NI 9421 in the **Project Explorer** window and select **Properties** to display this dialog box. You can configure the following options.

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this value.
- **Location**—Specifies a slot in the chassis for the C Series module.

Specialty Digital Configuration

You can use the Specialty Digital Configuration page of the **C Series Module Properties** dialog box to configure channels of this module for counter input or quadrature input.

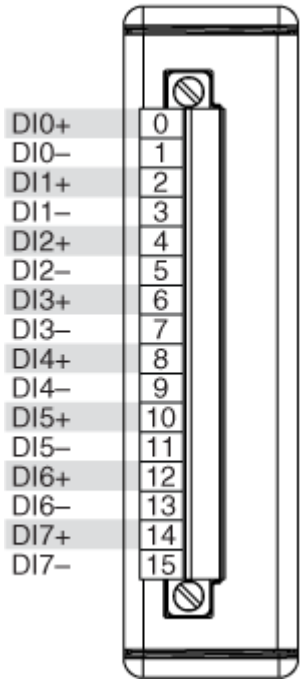
NI 9422

CompactRIO 8-Channel, Differential or TTL Digital Input Module

Software Reference (?)

FPGA Interface | Scan Interface

NI 9422 Pinout



NI 9422 (FPGA Interface)

CompactRIO 8-Channel, 24 V, Sinking/Sourcing Digital Input Module

FPGA I/O Node

You can use an FPGA I/O Node, configured for reading, with this device.

Terminals in Software

Use the FPGA I/O Node to access the following terminals for this device.

Terminal	Description
DI**x**	Digital input channel **x**, where **x** is the number of the channel. The NI 9422 has DI channels 0 to 7.

DI7:0	Digital port consisting of channels 0 through 7. Channel 7 is returned in the MSB, and channel 0 is returned in the LSB.

Arbitration

This device supports only the Never Arbitrate option for arbitration. You cannot configure arbitration settings for this device.

I/O Methods

Use the FPGA I/O Method Node to access the following I/O methods for this device.

Method	Description
Wait on Any Edge	Pauses the execution of the I/O Method Node until the next falling or rising edge of the digital signal. The **Timeout** input specifies in FPGA clock ticks how long the Wait on Any Edge method waits for the next falling or rising edge. A value of 0 causes the method to time out immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.
Wait on Falling Edge	Pauses the execution of the I/O Method Node until the next falling edge of the digital signal. The **Timeout** input specifies in FPGA clock ticks how long the Wait on Falling Edge method waits for the next falling edge. A value of 0 causes the method to time out immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.
Wait on High Level	Pauses the execution of the I/O Method Node until the digital signal is high. The **Timeout** input specifies in FPGA clock ticks how long the Wait on High Level method waits for the next high level. A value of 0 causes the method to time out immediately, a negative value causes the method to wait indefinitely, and a positive value causes t

	he method to wait for that number of clock ticks before timing out.
Wait on Low Level	Pauses the execution of the I/O Method Node until the digital signal is low. The **Timeout** input specifies in FPGA clock ticks how long the Wait on Low Level method waits for the next low level. A value of 0 causes the method to time out immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.
Wait on Rising Edge	Pauses the execution of the I/O Method Node until the next rising edge of the digital signal. The **Timeout** input specifies in FPGA clock ticks how long the Wait on Rising Edge method waits for the next rising edge. A value of 0 causes the method to time out immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.

Module Methods

Use the FPGA I/O Method Node to access the following module method for this device.

Method	Description
Check Status	Returns a Boolean value that indicates whether the module is ready. **Note** During the first 2 seconds after you reset the FPGA VI, the error terminals on this method may not correctly report certain types of errors.

I/O Properties

This device does not support any I/O properties.

Module Properties

Use the FPGA I/O Property Node to access the following module properties for this device.

Property	Description
Module ID	Returns the module ID.
Serial Number	Returns the unique serial number of the module .
Vendor ID	Returns the NI vendor ID, 0x1093.

Single-Cycle Timed Loop

This device supports the single-cycle Timed Loop. Configure the number of input synchronizing registers for the channels of this device in the Advanced Code Generation page of the FPGA I/O Node Properties dialog box.

When the module is within a single-cycle Timed Loop, it must be ready to perform digital input before a loop containing digital input starts. Poll the **Ready** output of the Check Status method to determine whether the module is ready. Digital input operations return invalid data if the module is not ready.

While the module is performing digital input within a single-cycle Timed Loop, do not perform property reads or remove the module from the chassis. Doing either of these actions causes the module to be unable to perform digital input and the **Ready** output of the Check Status method to return FALSE.

FPGA Target Clock Support

This device supports only top-level FPGA target clock rates and single-cycle Timed Loop clock rates that are multiples of 40 MHz, such as 40 MHz, 80 MHz, 120 MHz, and so on.

C Series Module Properties Dialog Box for the NI 9375/9411/9421/9422/9423/9425/9426/9435/9436/9437/950x (FPGA Interface)

Right-click an NI 9375, NI 9411, NI 9421, NI 9422, NI 9423, NI 9425, NI 9426, NI 9435, NI 9436, NI 9437, NI 9501, or NI 9505 C Series module in the **Project Explorer** window and select **Properties** from the shortcut menu to display this dialog box.

Use this dialog box to configure a C Series module.

This dialog box includes the following components:

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this option.
- **Location**—Specifies a slot in the chassis for the C Series module.

NI 9422 (Scan Interface)

CompactRIO 8-Channel, 24 V, Sinking/Sourcing Digital Input Module


Open example

Module I/O Variables

To use I/O from this module in a VI, drag and drop I/O variables from the **Project Explorer** window to the block diagram of the VI. The I/O variables for the channels return data as Boolean values.

Module Channels

The NI 9422 has the following channels.

Channel	Description
DI**x**	Digital input channel **x**, where **x** is the number o f the channel. For the NI 9422, **x** is 0 to 7.

C Series Module Properties Dialog Box

Use this dialog box to configure the NI 9422. Right-click the NI 9422 in the **Project Explorer** window and select **Properties** to display this dialog box. You can configure the following options.

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this value.
- **Location**—Specifies a slot in the chassis for the C Series module.

Specialty Digital Configuration

You can use the Specialty Digital Configuration page of the **C Series Module Properties** dialog box to configure channels of this module for counter input or quadrature input.

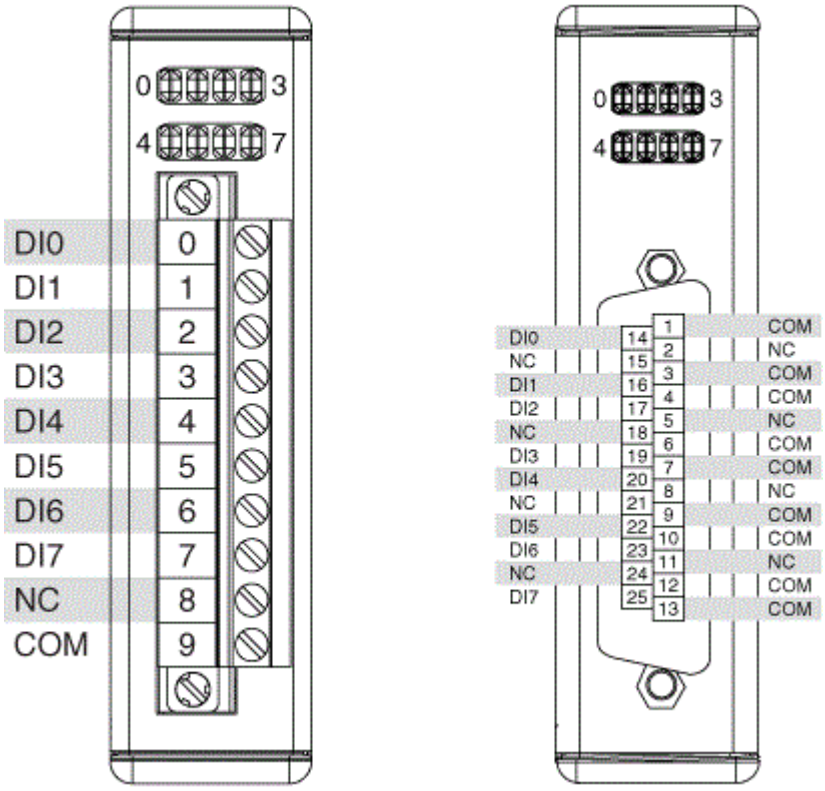
NI 9423

CompactRIO 8-Channel, 24 V, High-Speed Digital Input Module

Software Reference (?)

FPGA Interface | Scan Interface

NI 9423 Pinout



NI 9423 (FPGA Interface)

CompactRIO 8-Channel, 24 V, High-Speed Digital Input Module

FPGA I/O Node

You can use an FPGA I/O Node, configured for reading, with this device.

Terminals in Software

Use the FPGA I/O Node to access the following terminals for this device.

Terminal	Description
DI**x**	Digital input channel **x**, where **x** is the number of the channel. The NI 9423 has DI channels 0 to 7.

DI7:0	Digital port consisting of channels 0 through 7. Channel 7 is returned in the MSB, and channel 0 is returned in the LSB.

Arbitration

This device supports only the Never Arbitrate option for arbitration. You cannot configure arbitration settings for this device.

I/O Methods

Use the FPGA I/O Method Node to access the following I/O methods for this device.

Method	Description
Wait on Any Edge	Pauses the execution of the I/O Method Node until the next falling or rising edge of the digital signal. The **Timeout** input specifies in FPGA clock ticks how long the Wait on Any Edge method waits for the next falling or rising edge. A value of 0 causes the method to time out immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.
Wait on Falling Edge	Pauses the execution of the I/O Method Node until the next falling edge of the digital signal. The **Timeout** input specifies in FPGA clock ticks how long the Wait on Falling Edge method waits for the next falling edge. A value of 0 causes the method to time out immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.
Wait on High Level	Pauses the execution of the I/O Method Node until the digital signal is high. The **Timeout** input specifies in FPGA clock ticks how long the Wait on High Level method waits for the next high level. A value of 0 causes the method to time out immediately, a negative value causes the method to wait indefinitely, and a positive value causes t

	he method to wait for that number of clock ticks before timing out.
Wait on Low Level	Pauses the execution of the I/O Method Node until the digital signal is low. The **Timeout** input specifies in FPGA clock ticks how long the Wait on Low Level method waits for the next low level. A value of 0 causes the method to time out immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.
Wait on Rising Edge	Pauses the execution of the I/O Method Node until the next rising edge of the digital signal. The **Timeout** input specifies in FPGA clock ticks how long the Wait on Rising Edge method waits for the next rising edge. A value of 0 causes the method to time out immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.

Module Methods

Use the FPGA I/O Method Node to access the following module method for this device.

Method	Description
Check Status	Returns a Boolean value that indicates whether the module is ready. **Note** During the first 2 seconds after you reset the FPGA VI, the error terminals on this method may not correctly report certain types of errors.

I/O Properties

This device does not support any I/O properties.

Module Properties

Use the FPGA I/O Property Node to access the following module properties for this device.

Property	Description
Module ID	Returns the module ID.
Serial Number	Returns the unique serial number of the module .
Vendor ID	Returns the NI vendor ID, 0x1093.

Single-Cycle Timed Loop

This device supports the single-cycle Timed Loop. Configure the number of input synchronizing registers for the channels of this device in the Advanced Code Generation page of the FPGA I/O Node Properties dialog box.

When the module is within a single-cycle Timed Loop, it must be ready to perform digital input before a loop containing digital input starts. Poll the **Ready** output of the Check Status method to determine whether the module is ready. Digital input operations return invalid data if the module is not ready.

While the module is performing digital input within a single-cycle Timed Loop, do not perform property reads or remove the module from the chassis. Doing either of these actions causes the module to be unable to perform digital input and the **Ready** output of the Check Status method to return FALSE.

FPGA Target Clock Support

This device supports only top-level FPGA target clock rates and single-cycle Timed Loop clock rates that are multiples of 40 MHz, such as 40 MHz, 80 MHz, 120 MHz, and so on.

C Series Module Properties Dialog Box for the NI 9375/9411/9421/9422/9423/9425/9426/9435/9436/9437/950x (FPGA Interface)

Right-click an NI 9375, NI 9411, NI 9421, NI 9422, NI 9423, NI 9425, NI 9426, NI 9435, NI 9436, NI 9437, NI 9501, or NI 9505 C Series module in the **Project Explorer** window and select **Properties** from the shortcut menu to display this dialog box.

Use this dialog box to configure a C Series module.

This dialog box includes the following components:

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this option.
- **Location**—Specifies a slot in the chassis for the C Series module.

NI 9423 (Scan Interface)

CompactRIO 8-Channel, 24 V, High-Speed Digital Input Module


Open example

Module I/O Variables

To use I/O from this module in a VI, drag and drop I/O variables from the **Project Explorer** window to the block diagram of the VI. The I/O variables for the channels return data as Boolean values.

Module Channels

The NI 9423 has the following channels.

Channel	Description
DI**x**	Digital input channel **x**, where **x** is the number o f the channel. For the NI 9423, **x** is 0 to 7.

C Series Module Properties Dialog Box

Use this dialog box to configure the NI 9423. Right-click the NI 9423 in the **Project Explorer** window and select **Properties** to display this dialog box. You can configure the following options.

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this value.
- **Location**—Specifies a slot in the chassis for the C Series module.

Specialty Digital Configuration

You can use the Specialty Digital Configuration page of the **C Series Module Properties** dialog box to configure channels of this module for counter input or quadrature input.

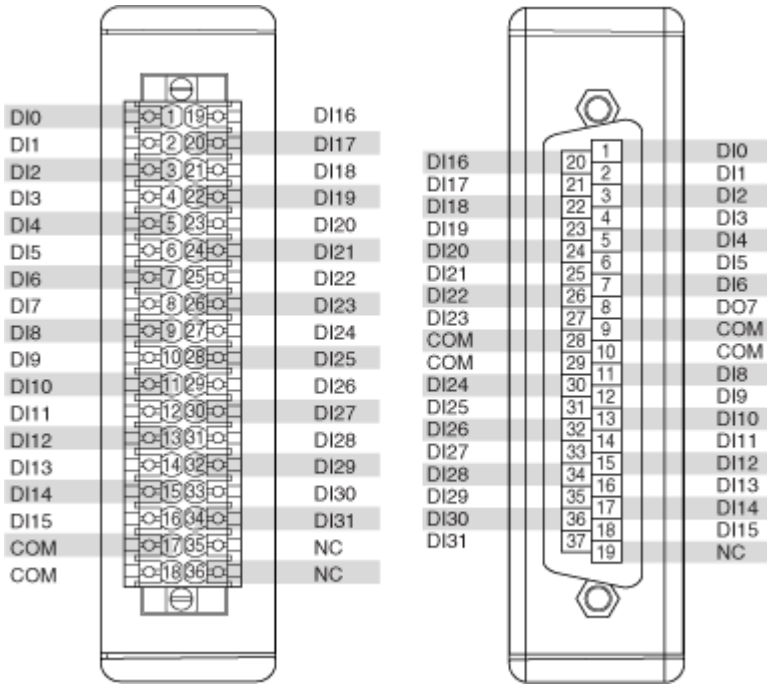
NI 9425

CompactRIO 32-Channel, 24 V, Sinking Digital Input Module

Software Reference (?)

FPGA Interface | Scan Interface

NI 9425 Pinout



NI 9425 (FPGA Interface)

CompactRIO 32-Channel, 24 V, Sinking Digital Input Module

FPGA I/O Node

You can use an FPGA I/O Node, configured for reading, with this device.

Terminals in Software

Use the FPGA I/O Node to access the following terminals for this device.

Terminal	Description
DI**x**	Digital input channel **x**, where **x** is the number of the channel. The NI 9425 has DI channels 0 to 31.
DI7:0	Digital port consisting of channels 0 through 7. Channel 7 is returned in the MSB, and channel 0 is returned in the LSB.

DI15:8	Digital port consisting of channels 8 through 15. Channel 15 is returned in the MSB, and channel 8 is returned in the LSB.
DI23:16	Digital port consisting of channels 16 through 23. Channel 23 is returned in the MSB, and channel 16 is returned in the LSB.
DI31:24	Digital port consisting of channels 24 through 31. Channel 31 is returned in the MSB, and channel 24 is returned in the LSB.
DI31:0	Digital port consisting of channels 0 through 31. Channel 31 is returned in the MSB, and channel 0 is returned in the LSB.

Arbitration

This device supports only the Arbitrate if Multiple Requestors Only option for arbitration. You cannot configure arbitration settings for this device.

Methods

This device does not support any methods.

I/O Properties

This device does not support any I/O properties.

Module Properties

Use the FPGA I/O Property Node to access the following module properties for this device.

Property	Description
Module ID	Returns the module ID.
Serial Number	Returns the unique serial number of the module.
Vendor ID	Returns the NI vendor ID, 0x1093.

Single-Cycle Timed Loop

This device does not support the single-cycle Timed Loop.

C Series Module Properties Dialog Box for the NI 9375/9411/9421/9422/9423/9425/9426/9435/9436/9437/950x (FPGA Interface)

Right-click an NI 9375, NI 9411, NI 9421, NI 9422, NI 9423, NI 9425, NI 9426, NI 9435, NI 9436, NI 9437, NI 9501, or NI 9505 C Series module in the **Project Explorer** window and select **Properties** from the shortcut menu to display this dialog box.

Use this dialog box to configure a C Series module.

This dialog box includes the following components:

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this option.
- **Location**—Specifies a slot in the chassis for the C Series module.

NI 9425 (Scan Interface)

CompactRIO 32-Channel, 24 V, Sinking Digital Input Module


Open example

Module I/O Variables

To use I/O from this module in a VI, drag and drop I/O variables from the **Project Explorer** window to the block diagram of the VI. The I/O variables for the channels return data as Boolean values.

Module Channels

The NI 9425 has the following channels.

Channel	Description
DI**x**	Digital input channel **x**, where **x** is the number of the channel. For the NI 9425, **x** is 0 to 31.

C Series Module Properties Dialog Box

Use this dialog box to configure the NI 9425. Right-click the NI 9425 in the **Project Explorer** window and select **Properties** to display this dialog box. You can configure the following options.

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this value.
- **Location**—Specifies a slot in the chassis for the C Series module.

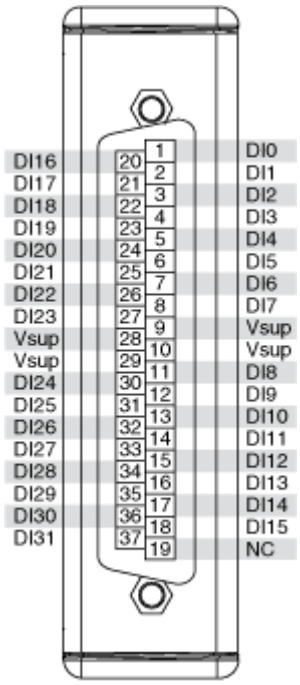
NI 9426

CompactRIO 32-Channel, 24 V, Sourcing Digital Input Module

Software Reference (?)

FPGA Interface | Scan Interface

NI 9426 Pinout



NI 9426 (FPGA Interface)

CompactRIO 32-Channel, 24 V, Sourcing Digital Input Module

FPGA I/O Node

You can use an FPGA I/O Node, configured for reading, with this device.

Terminals in Software

Use the FPGA I/O Node to access the following terminals for this device.

Terminal	Description
DI**x**	Digital input channel **x**, where **x** is the number of the channel. The NI 9426 has DI channels 0 to 31.
DI7:0	Digital port consisting of channels 0 through 7. Channel 7 is returned in the MSB, and channel 0 is returned in the LSB.

DI15:8	Digital port consisting of channels 8 through 15. Channel 15 is returned in the MSB, and channel 8 is returned in the LSB.
DI23:16	Digital port consisting of channels 16 through 23. Channel 23 is returned in the MSB, and channel 16 is returned in the LSB.
DI31:24	Digital port consisting of channels 24 through 31. Channel 31 is returned in the MSB, and channel 24 is returned in the LSB.
DI31:0	Digital port consisting of channels 0 through 31. Channel 31 is returned in the MSB, and channel 0 is returned in the LSB.

Arbitration

This device supports only the Arbitrate if Multiple Requestors Only option for arbitration. You cannot configure arbitration settings for this device.

Methods

This device does not support any methods.

I/O Properties

This device does not support any I/O properties.

Module Properties

Use the FPGA I/O Property Node to access the following module properties for this device.

Property	Description
Module ID	Returns the module ID.
Serial Number	Returns the unique serial number of the module.
Vendor ID	Returns the NI vendor ID, 0x1093.

Single-Cycle Timed Loop

This device does not support the single-cycle Timed Loop.

C Series Module Properties Dialog Box for the NI 9375/9411/9421/9422/9423/9425/9426/9435/9436/9437/950x (FPGA Interface)

Right-click an NI 9375, NI 9411, NI 9421, NI 9422, NI 9423, NI 9425, NI 9426, NI 9435, NI 9436, NI 9437, NI 9501, or NI 9505 C Series module in the **Project Explorer** window and select **Properties** from the shortcut menu to display this dialog box.

Use this dialog box to configure a C Series module.

This dialog box includes the following components:

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this option.
- **Location**—Specifies a slot in the chassis for the C Series module.

NI 9426 (Scan Interface)

CompactRIO 32-Channel, 24 V, Sourcing Digital Input Module


Open example

Module I/O Variables

To use I/O from this module in a VI, drag and drop I/O variables from the **Project Explorer** window to the block diagram of the VI. The I/O variables for the channels return data as Boolean values.

Module Channels

The NI 9426 has the following channels.

Channel	Description
DI**x**	Digital input channel **x**, where **x** is the number of the channel. For the NI 9426, **x** is 0 to 31.

C Series Module Properties Dialog Box

Use this dialog box to configure the NI 9426. Right-click the NI 9426 in the **Project Explorer** window and select **Properties** to display this dialog box. You can configure the following options.

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this value.
- **Location**—Specifies a slot in the chassis for the C Series module.

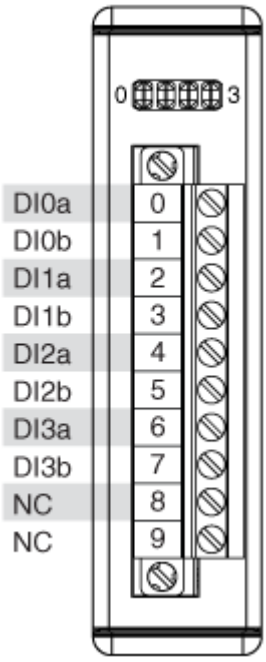
NI 9435

CompactRIO 4-Channel, AC/DC Universal Digital Input Module

Software Reference (?)

FPGA Interface | Scan Interface

NI 9435 Pinout



NI 9435 (FPGA Interface)

CompactRIO 4-Channel, AC/DC Universal Digital Input Module

FPGA I/O Node

You can use an FPGA I/O Node, configured for reading, with this device.

Terminals in Software

Use the FPGA I/O Node to access the following terminals for this device.

Terminal	Description
DI**x**	Digital input channel **x**, where **x** is the number of the channel. The NI 9435 has DI channels 0 to 3.
DI3:0	Digital port consisting of channels 0 through 3. Channel 3 is returned in bit 3, and channel 0 is returned in bit 0. Bits 4 through 7 return a zero.

Arbitration

This device supports only the Never Arbitrate option for arbitration. You cannot configure arbitration settings for this device.

I/O Methods

Use the FPGA I/O Method Node to access the following I/O methods for this device.

Method	Description
Wait on Any Edge	Pauses the execution of the I/O Method Node until the next falling or rising edge of the digital signal. The **Timeout** input specifies in FPGA clock ticks how long the Wait on Any Edge method waits for the next falling or rising edge. A value of 0 causes the method to time out immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.
Wait on Falling Edge	Pauses the execution of the I/O Method Node until the next falling edge of the digital signal. The **Timeout** input specifies in FPGA clock ticks how long the Wait on Falling Edge method waits for the next falling edge. A value of 0 causes the method to time out immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.
Wait on High Level	Pauses the execution of the I/O Method Node until the digital signal is high. The **Timeout** input specifies in FPGA clock ticks how long the Wait on High Level method waits for the next high level. A value of 0 causes the method to time out immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.
Wait on Low Level	Pauses the execution of the I/O Method Node until the digital signal is low. The **Timeout** input s

	pecifies in FPGA clock ticks how long the Wait o n Low Level method waits for the next low level. A value of 0 causes the method to time out imm ediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks be fore timing out.
Wait on Rising Edge	Pauses the execution of the I/O Method Node un til the next rising edge of the digital signal. The **Timeout** input specifies in FPGA clock ticks ho w long the Wait on Rising Edge method waits for the next rising edge. A value of 0 causes the met hod to time out immediately, a negative value c auses the method to wait indefinitely, and a pos itive value causes the method to wait for that nu mber of clock ticks before timing out.

Module Methods

Use the FPGA I/O Method Node to access the following module method for this device.

Method	Description
Check Status	Returns a Boolean value that indicates whether the module is ready.  **Note** During the first 2 seconds after you reset the FPGA VI, the error t erminals on this metho d may not correctly rep ort certain types of err ors.

I/O Properties

This device does not support any I/O properties.

Module Properties

Use the FPGA I/O Property Node to access the following module properties for this device.

Property	Description
Module ID	Returns the module ID.
Serial Number	Returns the unique serial number of the module .
Vendor ID	Returns the NI vendor ID, 0x1093.

Single-Cycle Timed Loop

This device supports the single-cycle Timed Loop. Configure the number of input synchronizing registers for the channels of this device in the Advanced Code Generation page of the FPGA I/O Node Properties dialog box.

When the module is within a single-cycle Timed Loop, it must be ready to perform digital input before a loop containing digital input starts. Poll the **Ready** output of the Check Status method to determine whether the module is ready. Digital input operations return invalid data if the module is not ready.

While the module is performing digital input within a single-cycle Timed Loop, do not perform property reads or remove the module from the chassis. Doing either of these actions causes the module to be unable to perform digital input and the **Ready** output of the Check Status method to return FALSE.

FPGA Target Clock Support

This device supports only top-level FPGA target clock rates and single-cycle Timed Loop clock rates that are multiples of 40 MHz, such as 40 MHz, 80 MHz, 120 MHz, and so on.

C Series Module Properties Dialog Box for the NI 9375/9411/9421/9422/9423/9425/9426/9435/9436/9437/950x (FPGA Interface)

Right-click an NI 9375, NI 9411, NI 9421, NI 9422, NI 9423, NI 9425, NI 9426, NI 9435, NI 9436, NI 9437, NI 9501, or NI 9505 C Series module in the **Project Explorer** window and select **Properties** from the shortcut menu to display this dialog box.

Use this dialog box to configure a C Series module.

This dialog box includes the following components:

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this option.
- **Location**—Specifies a slot in the chassis for the C Series module.

NI 9435 (Scan Interface)

CompactRIO 4-Channel, AC/DC Universal Digital Input Module


Open example

Module I/O Variables

To use I/O from this module in a VI, drag and drop I/O variables from the **Project Explorer** window to the block diagram of the VI. The I/O variables for the channels return data as Boolean values.

Module Channels

The NI 9435 has the following channels.

Channel	Description
DI**x**	Digital input channel **x**, where **x** is the number o f the channel. For the NI 9435, **x** is 0 to 3.

C Series Module Properties Dialog Box

Use this dialog box to configure the NI 9435. Right-click the NI 9435 in the **Project Explorer** window and select **Properties** to display this dialog box. You can configure the following options.

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this value.
- **Location**—Specifies a slot in the chassis for the C Series module.

Specialty Digital Configuration

You can use the Specialty Digital Configuration page of the **C Series Module Properties** dialog box to configure channels of this module for counter input or quadrature input.

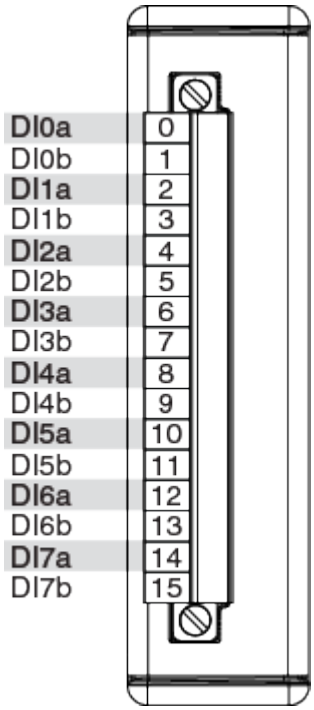
NI 9436

CompactRIO 8 DI, ±100 VDC to ±250 VDC/100 VAC to 250 VAC, Sinking/Sourcing, 10 ms Input Module

Software Reference (?)

FPGA Interface

NI 9436 Pinout



NI 9436 (FPGA Interface)

CompactRIO 8 DI, ±100 VDC to ±250 VDC/100 VAC to 250 VAC, Sinking/Sourcing, 10 ms Input Module

FPGA I/O Node

You can use an FPGA I/O Node, configured for reading, with this device.

Terminals in Software

Use the FPGA I/O Node to access the following terminals for this device.

Terminal	Description
DI**x**	Digital input channel **x**, where **x** is the number of the channel. The NI 9436 has DI channels 0 to 7.
DI7:0	Digital port consisting of channels 0 through 7. Channel 7 is returned in the MSB, and channel 0 is returned in the LSB.

Arbitration

This device supports only the Never Arbitrate option for arbitration. You cannot configure arbitration settings for this device.

I/O Methods

Use the FPGA I/O Method Node to access the following I/O methods for this device.

Method	Description
Wait on Any Edge	Pauses the execution of the I/O Method Node until the next falling or rising edge of the digital signal. The **Timeout** input specifies in FPGA clock ticks how long the Wait on Any Edge method waits for the next falling or rising edge. A value of 0 causes the method to time out immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.
Wait on Falling Edge	Pauses the execution of the I/O Method Node until the next falling edge of the digital signal. The **Timeout** input specifies in FPGA clock ticks how long the Wait on Falling Edge method waits for the next falling edge. A value of 0 causes the method to time out immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.
Wait on High Level	Pauses the execution of the I/O Method Node until the digital signal is high. The **Timeout** input specifies in FPGA clock ticks how long the Wait on High Level method waits for the next high level. A value of 0 causes the method to time out immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.
Wait on Low Level	Pauses the execution of the I/O Method Node until the digital signal is low. The **Timeout** input s

	pecifies in FPGA clock ticks how long the Wait o n Low Level method waits for the next low level. A value of 0 causes the method to time out imm ediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks be fore timing out.
Wait on Rising Edge	Pauses the execution of the I/O Method Node un til the next rising edge of the digital signal. The **Timeout** input specifies in FPGA clock ticks ho w long the Wait on Rising Edge method waits for the next rising edge. A value of 0 causes the met hod to time out immediately, a negative value c auses the method to wait indefinitely, and a pos itive value causes the method to wait for that nu mber of clock ticks before timing out.

Module Methods

Use the FPGA I/O Method Node to access the following module method for this device.

Method	Description
Check Status	Returns a Boolean value that indicates whether the module is ready. **Note** During the first 2 seconds after you reset the FPGA VI, the error t erminals on this metho d may not correctly rep ort certain types of err ors.

I/O Properties

This device does not support any I/O properties.

Module Properties

Use the FPGA I/O Property Node to access the following module properties for this device.

Property	Description
Module ID	Returns the module ID.
Serial Number	Returns the unique serial number of the module .
Vendor ID	Returns the NI vendor ID, 0x1093.

Single-Cycle Timed Loop

This device supports the single-cycle Timed Loop. Configure the number of input synchronizing registers for the channels of this device in the Advanced Code Generation page of the FPGA I/O Node Properties dialog box.

When the module is within a single-cycle Timed Loop, it must be ready to perform digital input before a loop containing digital input starts. Poll the **Ready** output of the Check Status method to determine whether the module is ready. Digital input operations return invalid data if the module is not ready.

While the module is performing digital input within a single-cycle Timed Loop, do not perform property reads or remove the module from the chassis. Doing either of these actions causes the module to be unable to perform digital input and the **Ready** output of the Check Status method to return FALSE.

FPGA Target Clock Support

This device supports only top-level FPGA target clock rates and single-cycle Timed Loop clock rates that are multiples of 40 MHz, such as 40 MHz, 80 MHz, 120 MHz, and so on.

C Series Module Properties Dialog Box for the NI 9375/9411/9421/9422/9423/9425/9426/9435/9436/9437/950x (FPGA Interface)

Right-click an NI 9375, NI 9411, NI 9421, NI 9422, NI 9423, NI 9425, NI 9426, NI 9435, NI 9436, NI 9437, NI 9501, or NI 9505 C Series module in the **Project Explorer** window and select **Properties** from the shortcut menu to display this dialog box.

Use this dialog box to configure a C Series module.

This dialog box includes the following components:

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this option.
- **Location**—Specifies a slot in the chassis for the C Series module.

NI 9436 (Scan Interface)

CompactRIO 8 DI, ±100 VDC to ±250 VDC/100 VAC to 250 VAC, Sinking/Sourcing, 10 ms Input Module

Module I/O Variables

To use I/O from this module in a VI, drag and drop I/O variables from the **Project Explorer** window to the block diagram of the VI. The I/O variables for the channels read and write Boolean values.

Module Channels

The NI 9436 has the following channels.

Channel	Description
DI**x**	Digital input channel **x**, where **x** is the number of the channel. The NI 9436 has DI channels 0 to 7.

C Series Module Properties Dialog Box

Use this dialog box to configure the NI 9436. Right-click the NI 9436 in the **Project Explorer** window and select **Properties** to display this dialog box. You can configure the following options.

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this value.
- **Location**—Specifies a slot in the chassis for the C Series module.

Specialty Digital Configuration

You can use the Specialty Digital Configuration page of the **C Series Module Properties** dialog box to configure channels of this module for counter input or quadrature input.

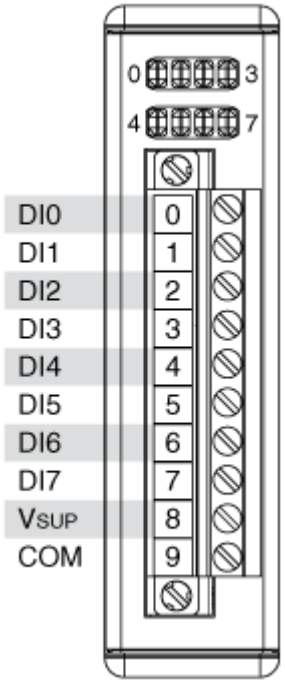
NI 9437

CompactRIO 8-Channel, 250 V, Sinking Digital Input Module

Software Reference (?)

FPGA Interface

NI 9437 Pinout



NI 9437 (FPGA Interface)

CompactRIO 8-Channel, 250 V, Sinking Digital Input Module

FPGA I/O Node

You can use an FPGA I/O Node, configured for reading, with this device.

Terminals in Software

Use the FPGA I/O Node to access the following terminals for this device.

Terminal	Description
DI**x**	Digital input channel **x**, where **x** is the number of the channel. The NI 9437 has DI channels 0 to 7.
DI7:0	Digital port consisting of channels 0 through 7. Channel 7 is returned in the MSB, and channel 0 is returned in the LSB.

Arbitration

This device supports only the Never Arbitrate option for arbitration. You cannot configure arbitration settings for this device.

I/O Methods

Use the FPGA I/O Method Node to access the following I/O methods for this device.

Method	Description
Wait on Any Edge	Pauses the execution of the I/O Method Node until the next falling or rising edge of the digital signal. The **Timeout** input specifies in FPGA clock ticks how long the Wait on Any Edge method waits for the next falling or rising edge. A value of 0 causes the method to time out immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.
Wait on Falling Edge	Pauses the execution of the I/O Method Node until the next falling edge of the digital signal. The **Timeout** input specifies in FPGA clock ticks how long the Wait on Falling Edge method waits for the next falling edge. A value of 0 causes the method to time out immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.
Wait on High Level	Pauses the execution of the I/O Method Node until the digital signal is high. The **Timeout** input specifies in FPGA clock ticks how long the Wait on High Level method waits for the next high level. A value of 0 causes the method to time out immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.
Wait on Low Level	Pauses the execution of the I/O Method Node until the digital signal is low. The **Timeout** input s

	pecifies in FPGA clock ticks how long the Wait o n Low Level method waits for the next low level. A value of 0 causes the method to time out imm ediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks be fore timing out.
Wait on Rising Edge	Pauses the execution of the I/O Method Node un til the next rising edge of the digital signal. The **Timeout** input specifies in FPGA clock ticks ho w long the Wait on Rising Edge method waits for the next rising edge. A value of 0 causes the met hod to time out immediately, a negative value c auses the method to wait indefinitely, and a pos itive value causes the method to wait for that nu mber of clock ticks before timing out.

Module Methods

Use the FPGA I/O Method Node to access the following module method for this device.

Method	Description
Check Status	Returns a Boolean value that indicates whether the module is ready.  **Note** During the first 2 seconds after you reset the FPGA VI, the error t erminals on this metho d may not correctly rep ort certain types of err ors.

I/O Properties

This device does not support any I/O properties.

Module Properties

Use the FPGA I/O Property Node to access the following module properties for this device.

Property	Description
Module ID	Returns the module ID.
Serial Number	Returns the unique serial number of the module .
Vendor ID	Returns the NI vendor ID, 0x1093.

Single-Cycle Timed Loop

This device supports the single-cycle Timed Loop. Configure the number of input synchronizing registers for the channels of this device in the Advanced Code Generation page of the FPGA I/O Node Properties dialog box.

When the module is within a single-cycle Timed Loop, it must be ready to perform digital input before a loop containing digital input starts. Poll the **Ready** output of the Check Status method to determine whether the module is ready. Digital input operations return invalid data if the module is not ready.

While the module is performing digital input within a single-cycle Timed Loop, do not perform property reads or remove the module from the chassis. Doing either of these actions causes the module to be unable to perform digital input and the **Ready** output of the Check Status method to return FALSE.

FPGA Target Clock Support

This device supports only top-level FPGA target clock rates and single-cycle Timed Loop clock rates that are multiples of 40 MHz, such as 40 MHz, 80 MHz, 120 MHz, and so on.

C Series Module Properties Dialog Box for the NI 9375/9411/9421/9422/9423/9425/9426/9435/9436/9437/950x (FPGA Interface)

Right-click an NI 9375, NI 9411, NI 9421, NI 9422, NI 9423, NI 9425, NI 9426, NI 9435, NI 9436, NI 9437, NI 9501, or NI 9505 C Series module in the **Project Explorer** window and select **Properties** from the shortcut menu to display this dialog box.

Use this dialog box to configure a C Series module.

This dialog box includes the following components:

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this option.
- **Location**—Specifies a slot in the chassis for the C Series module.

NI 9437 (Scan Interface)

CompactRIO 8-Channel, 250 V, Sinking Digital Input Module

Module I/O Variables

To use I/O from this module in a VI, drag and drop I/O variables from the **Project Explorer** window to the block diagram of the VI. The I/O variables for the channels return calibrated floating-point data in volts.

Module Channels

The NI 9437 has the following channels.

Channel	Description
DI**x**	Digital input channel **x**, where **x** is the number of the channel. The NI 9437 has DI channels 0 to 7.

C Series Module Properties Dialog Box

Use this dialog box to configure the NI 9437. Right-click the NI 9437 in the **Project Explorer** window and select **Properties** to display this dialog box. You can configure the following options.

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this value.
- **Location**—Specifies a slot in the chassis for the C Series module.

Digital Output Modules

Use this book as a reference for the following information:

- FPGA I/O functions, I/O resources, arbitration options, methods, and properties each C Series digital output module supports in FPGA Interface mode
- I/O variables and properties each C Series digital output module supports in Scan Interface mode
- Instructions for using LabVIEW with CompactRIO digital output devices

To view related topics, click the **Locate** button, shown at left, in the toolbar at the top of this window. The **LabVIEW Help** highlights this topic in the **Contents** tab so you can navigate the related topics.

Advanced Configuration Dialog Box (FPGA Interface)

Click the **Advanced** button on the C Series Module Properties dialog box for the NI 9401, NI 9472, NI 9474, NI 9475, NI 9481, or NI 9485 to display this dialog box.

Use this dialog box to configure the number of output synchronizing registers for each DO channel in a single-cycle Timed Loop.

This dialog box includes the following components:

- **Channels**—Select the channel for which you want to configure the number of output synchronizing registers.
- **Channel Configuration**—Specifies the number of synchronizing registers between the DO channel executing on the FPGA target and the FPGA target hardware interface. The FPGA target hardware interface might be a physical I/O connector on the device or a connection to a section of the FPGA that contains circuitry designed by NI. Each synchronizing register executes in one clock cycle.

Caution Select **0** only if you also use the IP Integration Node and the code contains its own synchronization registers.

  - **0**—Specifies that the FPGA VI uses no synchronizing registers. Do not select this option for most FPGA Module applications.

Note If you select **0** for digital output resources in a single-cycle Timed Loop, you create a combinatorial circuit between the two resources. The combinatorial circuit might cause glitches on the output signal.

  - **1**—Specifies that the FPGA VI uses one synchronizing register between the DO channel and the FPGA target hardware interface.

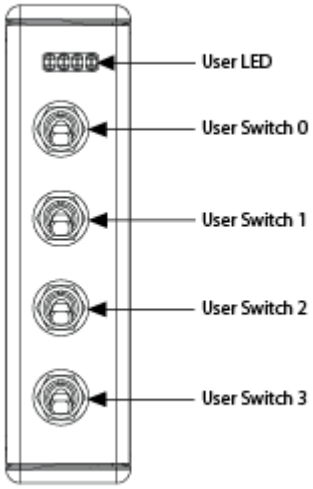
NI 9344

CompactRIO 4-Channel Switch Input and 4-Channel LED Output Module

Software Reference (?)

FPGA Interface

NI 9344 Front Panel



Related Topics

FPGA Interface

NI 9344 (FPGA Interface)

CompactRIO 4-Channel Switch Input and 4-Channel LED Output Module

Find examples

FPGA I/O Node

You can use an FPGA I/O Node, configured for reading and writing, with this device. When you write to an NI 9344 channel, the FPGA I/O Node does not automatically enable the channel for output.

Terminals in Software

Use the FPGA I/O Node to access the following terminals for this device.

Terminal	Description

User LED**x**	LED output channel **x**, where **x** is the number of the channel. The NI 9344 has LED channels 0 to 3.
User Switch x	Switch input channel **x**, where **x** is the number o f the channel. The NI 9344 has Switch channels 0 to 3.
User LED 3:0	Digital output port consisting of channels 0 thro ugh 3. Channel 3 is returned in the MSB, and cha nnel 0 is returned in the LSB.
User Switch 3:0	Digital input port consisting of channels 0 throu gh 3. Channel 3 is returned in the MSB, and chan nel 0 is returned in the LSB.

Arbitration

You can configure the arbitration settings for digital output channels of this device in the Advanced Code Generation page of the FPGA I/O Properties dialog box. The default arbitration setting is Never Arbitrate. Digital input channels of this device support only the **Never Arbitrate** option for arbitration. You cannot configure arbitration settings for the digital input channels of this device.

I/O Methods

Use the FPGA I/O Method Node to access the following I/O methods for this device.

Method	Description
Wait on Any Edge	Pauses the execution of the I/O Method Node un til the next falling or rising edge of the digital sig nal. The **Timeout** input specifies in FPGA clock ticks how long the Wait on Any Edge method wa its for the next falling or rising edge. A value of 0 causes the method to time out immediately, a n egative value causes the method to wait indefini tely, and a positive value causes the method to wait for that number of clock ticks before timing out.
Wait on Falling Edge	Pauses the execution of the I/O Method Node un til the next falling edge of the digital signal. The **Timeout** input specifies in FPGA clock ticks ho

	w long the Wait on Falling Edge method waits fo r the next falling edge. A value of 0 causes the m ethod to time out immediately, a negative value causes the method to wait indefinitely, and a po sitive value causes the method to wait for that n umber of clock ticks before timing out.
Wait on High Level	Pauses the execution of the I/O Method Node un til the digital signal is high. The **Timeout** input specifies in FPGA clock ticks how long the Wait o n High Level method waits for the next high leve l. A value of 0 causes the method to time out im mediately, a negative value causes the method t o wait indefinitely, and a positive value causes t he method to wait for that number of clock ticks before timing out.
Wait on Low Level	Pauses the execution of the I/O Method Node un til the digital signal is low. The **Timeout** input s pecifies in FPGA clock ticks how long the Wait o n Low Level method waits for the next low level. A value of 0 causes the method to time out imm ediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks be fore timing out.
Wait on Rising Edge	Pauses the execution of the I/O Method Node un til the next rising edge of the digital signal. The **Timeout** input specifies in FPGA clock ticks ho w long the Wait on Rising Edge method waits for the next rising edge. A value of 0 causes the met hod to time out immediately, a negative value c auses the method to wait indefinitely, and a pos itive value causes the method to wait for that nu mber of clock ticks before timing out.

Module Methods

Use the FPGA I/O Method Node to access the following module methods for this device.

Method	Description

Check Status	Returns a Boolean value that indicates whether the module is ready.  **Note** During the first 2 seconds after you reset the FPGA VI, the error terminals on this method may not correctly report certain types of errors.

I/O Properties

This device does not support any I/O properties.

Module Properties

Use the FPGA I/O Property Node to access the following module properties for this device.

Property	Description
Module ID	Returns the module ID, 0x77C5.
Serial Number	Returns the unique serial number of the module.
Vendor ID	Returns the NI vendor ID, 0x1093.

Single-Cycle Timed Loop

This device supports the single-cycle Timed Loop. Configure the number of output synchronizing registers for the channels of this device in the Advanced Configuration dialog box. Configure the number of input synchronizing registers for the channels of this device in the Advanced Code Generation page of the FPGA I/O Node Properties dialog box.

When the module is within a single-cycle Timed Loop, it must be ready to perform digital I/O before a loop containing digital I/O starts. Poll the **Ready** output of the Check Status method to determine whether the module is ready. Digital input operations return invalid data if the module is not ready. The module also might ignore or delay digital output operations if it is not ready.

While the module is performing digital I/O within a single-cycle Timed Loop, do not perform property reads, use the Set Line Direction method, or remove the module from the chassis. Doing any of these actions causes the module to be unable to perform digital I/O and the **Ready** output of the Check Status method to return FALSE.

FPGA Target Clock Support

This device supports only top-level FPGA target clock rates and single-cycle Timed Loop clock rates that are multiples of 40 MHz, such as 40 MHz, 80 MHz, 120 MHz, and so on.

C Series Module Properties Dialog Box for the NI 9344 (FPGA Interface)

Right-click an NI 9344 C Series module in the **Project Explorer** window and select **Properties** from the shortcut menu to display this dialog box.

Use this dialog box to configure a C Series module.

This dialog box includes the following components:

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this option.
- **Location**—Specifies a slot in the chassis for the C Series module.

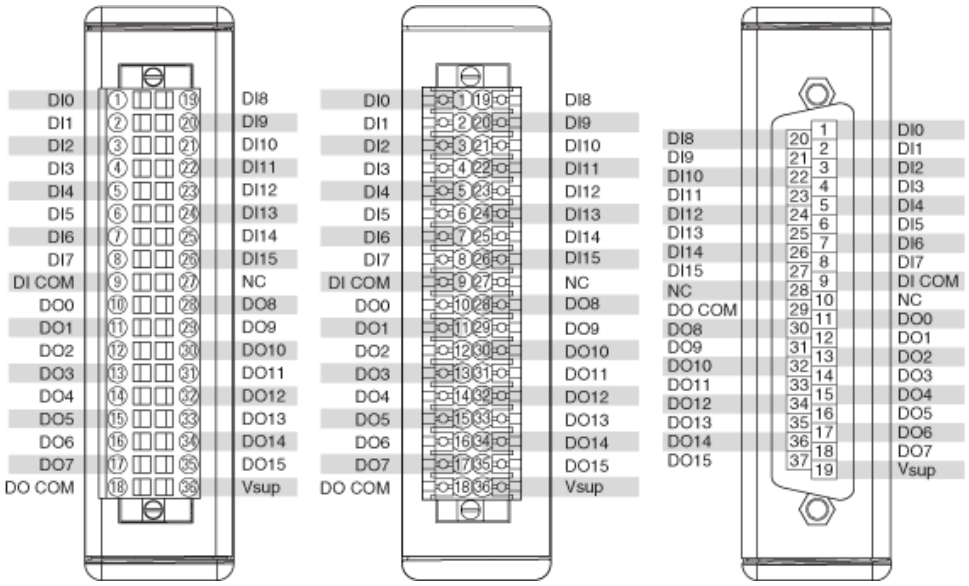
NI 9375

CompactRIO 16-Channel Digital Input and 16-Channel Digital Output

Software Reference (?)

FPGA Interface | Scan Interface

NI 9375 Pinout



Related Topics

FPGA Interface
Avoiding Timing Uncertainty with the NI 9375

NI 9375 (FPGA Interface)

CompactRIO 16-Channel Digital Input and 16-Channel Digital Output

Find NI 9375 examples

FPGA I/O Node

You can use an FPGA I/O Node, configured for reading or writing, with this device.

Terminals in Software

Use the FPGA I/O Node to access the following terminals for this device.

Terminal	Description
DI**x**	Digital input channel **x**, where **x** is the number of the channel. The NI 9375 has DI channels 0 to 15.

DI7:0	Digital port consisting of DI channels 0 through 7. Channel 7 is returned in the MSB, and channel 0 is returned in the LSB.
DI15:8	Digital port consisting of DI channels 8 through 15. Channel 15 is returned in the MSB, and channel 8 is returned in the LSB.
DI15:0	Digital port consisting of DI channels 0 through 15. Channel 15 is returned in the MSB, and channel 0 is returned in the LSB.
DO**x**	Digital output channel **x**, where **x** is the number of the channel. The NI 9375 has DO channels 0 to 15.
DO7:0	Digital port consisting of DO channels 0 through 7. Channel 7 is returned in the MSB, and channel 0 is returned in the LSB.
DO15:8	Digital port consisting of DO channels 8 through 15. Channel 15 is returned in the MSB, and channel 8 is returned in the LSB.
DO15:0	Digital port consisting of DO channels 0 through 15. Channel 15 is returned in the MSB, and channel 0 is returned in the LSB.

Caution DI and DO operations that are run concurrently may exhibit jitter. Access both subsystems using a single I/O Node to avoid jitter in your application. Refer to the Avoiding Timing Uncertainty topic for more information.

Arbitration

This device supports only the Arbitrate if Multiple Requestors Only option for arbitration. You cannot configure arbitration settings for this device.

I/O Methods

This device does not support any I/O methods.

Module Methods

This device does not support any module methods.

I/O Properties

This device does not support any I/O properties.

Module Properties

Use the FPGA I/O Property Node to access the following module properties for this device.

Property	Description
Module ID	Returns the module ID.
Serial Number	Returns the unique serial number of the module .
Vendor ID	Returns the NI vendor ID, 0x1093.

Single-Cycle Timed Loop

This device does not support the single-cycle Timed Loop.

Avoiding Timing Uncertainty with the NI 9375 (FPGA Interface)

Follow these guidelines to avoid introducing timing uncertainty into DI and DO Node calls.

- Use a single I/O Node to access DI and DO operations to ensure proper sequencing.
- Do not perform the following operations concurrently:
  - DI Node call
  - DO Node call

Refer to the NI 9375 Digital Port Input Output VI in the `labview\examples\CompactRIO\Module Specific\NI 9375\NI 9375 Digital Port Input Output\NI 9375 Digital Port Input Output.lvproj` for an example of the recommended way to use the DIO subsystems.

C Series Module Properties Dialog Box for the NI 9375/9411/9421/9422/9423/9425/9426/9435/9436/9437/950x (FPGA Interface)

Right-click an NI 9375, NI 9411, NI 9421, NI 9422, NI 9423, NI 9425, NI 9426, NI 9435, NI 9436, NI 9437, NI 9501, or NI 9505 C Series module in the **Project Explorer** window and select **Properties** from the shortcut menu to display this dialog box.

Use this dialog box to configure a C Series module.

This dialog box includes the following components:

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this option.
- **Location**—Specifies a slot in the chassis for the C Series module.

NI 9375 (Scan Interface)

CompactRIO 16-Channel Digital Input and 16-Channel Digital Output

Module I/O Variables

To use I/O from this module in a VI, drag and drop I/O variables from the **Project Explorer** window to the block diagram of the VI. The I/O variables for the channels read and write Boolean values.

Module Channels

The NI 9375 has the following channels.

Channel	Description
DI**x**	Digital input channel **x**, where **x** is the number o f the channel. For the NI 9375, **x** is 0 to 15.
DO**x**	Digital output channel **x**, where **x** is the number of the channel. For the NI 9375, **x** is 0 to 15.

C Series Module Properties Dialog Box

Use this dialog box to configure the NI 9375. Right-click the NI 9375 in the **Project Explorer** window and select **Properties** to display this dialog box. You can configure the following options.

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this value.
- **Location**—Specifies a slot in the chassis for the C Series module.

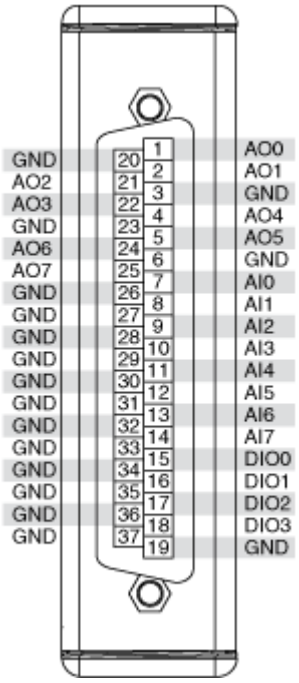
NI 9381

CompactRIO 0 V to 5 V, 12-bit, Multifunction Input/Output Module

Software Reference (?)

FPGA Interface | Scan Interface

NI 9381 Pinout



Running AI and AO Operations Concurrently on the NI 9381

AI and AO operations that are run concurrently may exhibit jitter. Access both subsystems using a single I/O Node to avoid jitter in your application. Refer to the Avoiding Timing Uncertainty topic for more information.

Related Topics

FPGA Interface
Converting and Calibrating CompactRIO Analog Input Values
Detecting Out-of-Range Channels
Avoiding Timing Uncertainty with the NI 9381
Converting Voltage Values to Binary Values for the NI 9381

NI 9381 (FPGA Interface)

CompactRIO 0 V to 5 V, 12-bit, Multifunction Input/Output Module

Find NI 9381 examples

FPGA I/O Node

You can use an FPGA I/O Node, configured for reading and writing, with this device.

Terminal	Description
AI**x**	Analog input channel **x**, where **x** is the number of the channel. The NI 9381 has AI channels 0 to 7.
AO**x**	Analog output channel **x**, where **x** is the number of the channel. The NI 9381 has AO channels 0 to 3.
DIO**x**	Digital input/output channel **x**, where **x** is the number of the channel. The NI 9381 has DIO channels 0 to 3.
DIO3:0	Digital port consisting of channels 0 through 3. Channel 3 is returned in the MSB, and channel 0 is returned in the LSB.

Caution AI and AO operations that are run concurrently may exhibit jitter. Access both subsystems using a single I/O Node to avoid jitter in your application. Refer to the Avoiding Timing Uncertainty topic for more information.

Arbitration

Analog input and analog output channels of this device support only the Arbitrate if Multiple Requestors Only option for arbitration. You cannot configure arbitration settings for analog input and analog output channels of this device.

You can configure the arbitration settings for digital output channels of this device in the Advanced Code Generation page of the FPGA I/O Properties dialog box. The default arbitration setting is Never Arbitrate.

Digital input channels of this device support only the **Never Arbitrate** option for arbitration. You cannot configure arbitration settings for the digital input channels of this device.

I/O Methods

Use the FPGA I/O Method Node to access the following I/O methods for the DIO channels of this device.

Method	Description
Set Output Data	Refer to the FPGA I/O Method Node (FPGA Module) topic for a description of this method. This method is available only when you set the DIO line direction to output. You can set the DIO line direction in the C Series Module Properties dialog box.
Set Output Enable	Sets the line direction of the digital channel or the DIO3:0 digital port. Refer to the FPGA I/O Method Node (FPGA Module) topic for more information on this method. This method can introduce jitter in an analog input or analog output loop. This method is available only when you enable programmable DIO line changes on the module. You can enable programmable DIO line changes on the module in the C Series Module Properties dialog box.
Wait on Any Edge	Pauses the execution of the I/O Method Node until the next falling or rising edge of the digital signal. The **Timeout** input specifies in FPGA clock ticks how long the Wait on Any Edge method waits for the next falling or rising edge. A value of 0 causes the method to time out immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out. **Notes** This method is not available on the DIO3:0 port. For the first two seconds after resetting the F

	PGA VI, the time out will not start counting until the module is identified.
Wait on Falling Edge	Pauses the execution of the I/O Method Node until the next falling edge of the digital signal. The **Timeout** input specifies in FPGA clock ticks how long the Wait on Falling Edge method waits for the next falling edge. A value of 0 causes the method to time out immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out. **Notes** This method is not available on the DIO3:0 port. For the first two seconds after resetting the FPGA VI, the time out will not start counting until the module is identified.
Wait on High Level	Pauses the execution of the I/O Method Node until the digital signal is high. The **Timeout** input specifies in FPGA clock ticks how long the Wait on High Level method waits for the next high level. A value of 0 causes the method to time out immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out. **Notes** This method is not available on the DIO3:0 port. For the first two seconds after resetting the FPGA VI, the time out will

	l not start counting unt il the module is identifi ed.
Wait on Low Level	Pauses the execution of the I/O Method Node un til the digital signal is low. The **Timeout** input s pecifies in FPGA clock ticks how long the Wait o n Low Level method waits for the next low level. A value of 0 causes the method to time out imm ediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks be fore timing out. **Notes** This method is not available on the DI O3:0 port. For the first two secon ds after resetting the F PGA VI, the time out wil l not start counting unt il the module is identifi ed.
Wait on Rising Edge	Pauses the execution of the I/O Method Node un til the next rising edge of the digital signal. The **Timeout** input specifies in FPGA clock ticks ho w long the Wait on Rising Edge method waits for the next rising edge. A value of 0 causes the met hod to time out immediately, a negative value c auses the method to wait indefinitely, and a pos itive value causes the method to wait for that nu mber of clock ticks before timing out. **Notes** This method is not available on the DI O3:0 port. For the first two secon ds after resetting the F PGA VI, the time out wil l not start counting unt

	il the module is identifi ed.

Module Method

Use the FPGA I/O Method Node to access the following module method for this device.

Method	Description
Check Status	Returns a Boolean value that indicates whether the module is ready.

I/O Properties

Use the FPGA I/O Property Node to access the following I/O properties for AI and AO channels of this device.

Property	Description
LSB Weight	Returns the LSB weight in nV/LSB for the channe l. Use this value to convert and calibrate NI 9381 data if you set the **Calibration Mode** to **Raw** i n the C Series Module Properties dialog box.
Offset	Returns the calibration offset in nV for the chan nel. Use this value to convert and calibrate NI 93 81 data if you set the **Calibration Mode** to **Ra w** in the **C Series Module Properties** dialog b ox.

Module Properties

Use the FPGA I/O Property Node to access the following module properties for this device.

Property	Description
Module ID	Returns the module ID.
Serial Number	Returns the unique serial number of the module .
Vendor ID	Returns the NI vendor ID, 0x1093.

Single-Cycle Timed Loop

This device supports the single-cycle Timed Loop. Configure the number of input synchronizing registers for the channels of this device in the Advanced Code Generation page of the FPGA I/O Node Properties dialog box. Configure the number of output synchronizing registers for the channels of this device in the Advanced Code Generation page of the FPGA I/O Properties dialog box.

This device supports the Number of Synchronizing Registers for Output Data synchronizing register option when used in SCTL output. This option supports the same functionality as the **Number of Synchronizing Registers for Output Data** option described in the Advanced Code Generation FPGA I/O Properties Page (FPGA Module) topic, with the exception that you can use this option only in a single-cycle Timed Loop. You can implement either 0 or 1 synchronizing registers inside the single-cycle Timed Loop, however, if you configure 0 synchronizing registers outside of the single-cycle Timed Loop, the FPGA VI implements 1 synchronizing register by default.

When the device is within a single-cycle Timed Loop, it must be ready to perform digital I/O before a loop containing digital I/O starts. Poll the **Ready** output of the Check Status method to determine whether the module is ready. Digital input operations return invalid data if the module is not ready. The module also might ignore or delay digital output operations if it is not ready.

While the digital is performing digital I/O within a single-cycle Timed Loop, do not perform property reads or remove the module from the chassis. Doing any of these actions causes the module to be unable to perform digital I/O and the **Ready** output of the Check Status method to return FALSE.

FPGA Target Clock Support

This device supports only top-level FPGA target clock rates and single-cycle Timed Loop clock rates that are multiples of 40 MHz, such as 40 MHz, 80 MHz, 120 MHz, and so on.

Avoiding Timing Uncertainty with the NI 9381 (FPGA Interface)

Follow these guidelines to avoid introducing timing uncertainty into AI node, AO Node, DO Node, and Set Output Data method calls. Additionally, failing to follow

these guidelines may result in lost data points for DO Node calls or Set Output Data method calls when either of them are made from inside a single-cycle Timed Loop.

- Use a single I/O Node to access AI and AO operations to ensure proper sequencing.
- Do not run the Set Output Enable method when an AI, AO, or DO subsystems is active.
- Do not perform the following operations concurrently:
  - AI Node call
  - AO Node call
  - Set Output Enable method call
  - Automatic line direction change when a DO call is made under the following conditions:
    - The call is made from outside of a single-cycle Timed Loop.
    - The **Allow programmatic DIO line direction** checkbox is checked in the C Series Module Properties dialog box.
    - The DIO channel is configured as an input at the time when the DO node is called.

Refer to the NI 9381 Advanced IO VI in the `labview\examples\CompactRIO\Module Specific\NI 9381\NI 9381 Advanced IO\NI 9381 Advanced IO.lvproj` for an example of the recommended way to use the AI, AO , and DIO subsystems.

C Series Module Properties Dialog Box for the NI 9381 (FPGA Interface)

Right-click an NI 9381 C Series module in the **Project Explorer** window and select **Properties** from the shortcut menu to display this dialog box.

Use this dialog box to configure a C Series module.

This dialog box includes the following components:

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this option.
- **Location**—Specifies a slot in the chassis for the C Series module.
- **Calibration Mode**—Sets the calibration mode for the C Series module. Select **Calibrated** if you want the FPGA I/O Node to return calibrated, fixed-point data from the module in units of volts. The fixed-point data is unsigned, with a word length of 18 bits and an integer word length of 3 bits for the analog input channels and a word length of 16 bits and an integer word length of 3 bits for the analog output channels. Select **Raw** if you want the FPGA I/O Node to return uncalibrated, binary data from the module. If you select **Raw**, you must convert and calibrate the analog input values in the host VI. The default is **Calibrated**.
- **Channels**—Specifies the channel(s) for which you want to select the direction.
- **Selected Channel(s) Settings**—Specifies the direction for each channel.
- **Hot Swap Behavior (Analog Output)**—Specifies the state of the analog output channels when the C Series module is removed and reinserted with the FPGA VI loaded and running. The power-on output state is the state that a C Series output module is in when power is applied to the module. The default is Last output value.
- **Allow Programmatic DIO Line Direction Change**—Place a checkmark in this checkbox if you want to enable programmable DIO line changes on the module.

Caution Performing a DIO line direction change will affect the timing of any concurrent AI, AO, and DO operations. Refer to the Avoiding Timing Uncertainty topic for more information.

Converting Voltage Values to Binary Values for the NI 9381 (FPGA Interface)

Set the **Calibration Mode** to **Calibrated** in the C Series Module Properties dialog box for the NI 9381 if you want the FPGA I/O Node to accept fixed-point data in units of volts when writing to the module. If you set the **Calibration Mode** to **Raw**, the FPGA I/O Node accepts only binary values when writing to the module. You must convert output voltage values to binary values before you write them to the module. You must convert these values in the host VI.

Using an Equation to Convert Voltage to Binary

You can use the following equation in the host VI to convert the analog output values to binary values:

Binary Value = (**Voltage Value** – **Offset**) ÷ **LSB Weight**

where	**Binary Value** is the value you write to the FPGA I/O Node
	Current Value is the voltage in V that you want the channel to output
	Offset is the value returned by the Offset property
	LSB Weight is the value returned by the LSB Weight property

NI recommends using calibrated values for analog output. To convert calibrated voltage values, use the FPGA I/O Property Node to read the LSB Weight and Offset properties. If you do not want to read the LSB Weight and Offset values from the module, you can convert uncalibrated voltage values by using the following values for **Offset** and **LSB Weight**:

Offset = –5249

LSB Weight = $5.105\ V \div 2^{\textbf{DAC Resolution}}$

where	**DAC Resolution** is the DAC resolution value in the **NI 9381 Operating Instructions and Specifications**.

NI 9381 (Scan Interface)

CompactRIO 0 V to 5 V, 12-bit, Multifunction Input/Output Module

Module I/O Variables

To use I/O from this module in a VI, drag and drop I/O variables from the **Project Explorer** window to the block diagram of the VI. The I/O variables for the AI channels return floating-point data in volts. The I/O variables for the AO channels write floating-point data in volts. The I/O variables for the DIO channels read and write boolean values.

Module Channels

The NI 9381 has the following channels.

Channel	Description
AI**x**	Analog input channel **x**, where **x** is the number of the channel. For the NI 9381, **x** is 0 to 7.
AO**x**	Analog output channel **x**, where **x** is the number of the channel. For the NI 9381, **x** is 0 to 7.
DIO**x**	Digital input/output channel **x**, where **x** is the n umber of the channel. For the NI 9381, **x** is 0 to 3 .

C Series Module Properties Dialog Box

Use this dialog box to configure the NI 9381. Right-click the NI 9381 in the **Project Explorer** window and select **Properties** to display this dialog box. You can configure the following options.

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Type**—Specifies the type of C Series module. You cannot change this value.
- **Location**—Specifies a slot in the chassis for the C Series module.

- **Channels**—Specifies the channel(s) for which you want to configure settings.
- **Direction**—Specifies the initial line direction of the selected channel(s) as input or output.

Note If you are using direct access to read from or write to AI or AO channels of the NI 9381, the conversion time is somewhat longer than 50 µs.

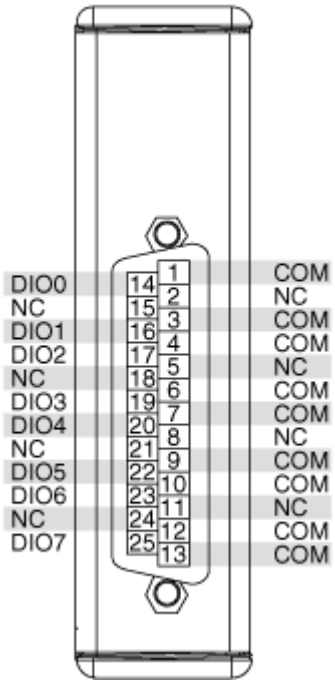
NI 9401

CompactRIO 8-Channel, TTL Digital Input/Output Module

Software Reference (?)

FPGA Interface | Scan Interface

NI 9401 Pinout



Related Topics

FPGA Interface
Configuring the Initial Line Direction for the NI 9401

NI 9401 (FPGA Interface)

CompactRIO 8-Channel, TTL Digital Input/Output Module

Find examples

FPGA I/O Node

You can use an FPGA I/O Node, configured for reading and writing, with this device. When you write to an NI 9401 channel, the FPGA I/O Node does not automatically enable the channel for output.

Terminals in Software

Use the FPGA I/O Node to access the following terminals for this device.

Terminal	Description
DIO**x**	Digital input/output channel **x**, where **x** is the number of the channel. The NI 9401 has DIO channels 0 to 7.
DIO3:0	Digital port consisting of channels 0 through 3. Channel 3 is returned in the MSB, and channel 0 is returned in the LSB.
DIO7:4	Digital port consisting of channels 4 through 7. Channel 7 is returned in the MSB, and channel 4 is returned in the LSB.
DIO7:0	Digital port consisting of channels 0 through 7. Channel 7 is returned in the MSB, and channel 0 is returned in the LSB.

Arbitration

You can configure the arbitration settings for digital output channels of this device in the Advanced Code Generation page of the FPGA I/O Properties dialog box. The default arbitration setting is Never Arbitrate. Digital input channels of this device

support only the **Never Arbitrate** option for arbitration. You cannot configure arbitration settings for the digital input channels of this device.

I/O Methods

Use the FPGA I/O Method Node to access the following I/O methods for this device.

Method	Description
Wait on Any Edge	Pauses the execution of the I/O Method Node until the next falling or rising edge of the digital signal. The **Timeout** input specifies in FPGA clock ticks how long the Wait on Any Edge method waits for the next falling or rising edge. A value of 0 causes the method to time out immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.
Wait on Falling Edge	Pauses the execution of the I/O Method Node until the next falling edge of the digital signal. The **Timeout** input specifies in FPGA clock ticks how long the Wait on Falling Edge method waits for the next falling edge. A value of 0 causes the method to time out immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.
Wait on High Level	Pauses the execution of the I/O Method Node until the digital signal is high. The **Timeout** input specifies in FPGA clock ticks how long the Wait on High Level method waits for the next high level. A value of 0 causes the method to time out immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.
Wait on Low Level	Pauses the execution of the I/O Method Node until the digital signal is low. The **Timeout** input specifies in FPGA clock ticks how long the Wait on Low Level method waits for the next low level.

	A value of 0 causes the method to time out immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.
Wait on Rising Edge	Pauses the execution of the I/O Method Node until the next rising edge of the digital signal. The **Timeout** input specifies in FPGA clock ticks how long the Wait on Rising Edge method waits for the next rising edge. A value of 0 causes the method to time out immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.

Module Methods

Use the FPGA I/O Method Node to access the following module methods for this device.

Method	Description
Check Status	Returns a Boolean value that indicates whether the module is ready.  **Note** During the first 2 seconds after you reset the FPGA VI, the error terminals on this method may not correctly report certain types of errors.
Set Line Direction	Sets the direction of one port to input or output.

I/O Properties

This device does not support any I/O properties.

Module Properties

Use the FPGA I/O Property Node to access the following module properties for this device.

Property	Description
Module ID	Returns the module ID.
Serial Number	Returns the unique serial number of the module .
Vendor ID	Returns the NI vendor ID, 0x1093.

Single-Cycle Timed Loop

This device supports the single-cycle Timed Loop. Configure the number of output synchronizing registers for the channels of this device in the Advanced Configuration dialog box. Configure the number of input synchronizing registers for the channels of this device in the Advanced Code Generation page of the FPGA I/O Node Properties dialog box.

When the module is within a single-cycle Timed Loop, it must be ready to perform digital I/O before a loop containing digital I/O starts. Poll the **Ready** output of the Check Status method to determine whether the module is ready. Digital input operations return invalid data if the module is not ready. The module also might ignore or delay digital output operations if it is not ready.

While the module is performing digital I/O within a single-cycle Timed Loop, do not perform property reads, use the Set Line Direction method, or remove the module from the chassis. Doing any of these actions causes the module to be unable to perform digital I/O and the **Ready** output of the Check Status method to return FALSE.

FPGA Target Clock Support

This device supports only top-level FPGA target clock rates and single-cycle Timed Loop clock rates that are multiples of 40 MHz, such as 40 MHz, 80 MHz, 120 MHz, and so on.

C Series Module Properties Dialog Box for the NI 9401 (FPGA Interface)

Right-click an NI 9401 C Series module in the **Project Explorer** window and select **Properties** from the shortcut menu to display this dialog box.

Use this dialog box to configure a C Series module.

This dialog box includes the following components:

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this option.
- **Location**—Specifies a slot in the chassis for the C Series module.
- **Initial Line Direction**—Sets the initial line direction for each digital port to digital input or digital output. The default is digital input.
- **Advanced**—Launches the Advanced Configuration dialog box.

Configuring the Initial Line Direction for the NI 9401 (FPGA Interface)

Each digital port on the NI 9401 is initially configured as a digital input. You can configure the initial line direction for each port on the NI 9401 at edit time using the C Series Module Properties dialog box. You can programmatically change the line direction for each port at run time using the FPGA I/O Method Node. The execution of an I/O Method Node that is configured with a Set Line Direction method overwrites the value you configured in the **C Series Module Properties** dialog box.

Configuring Line Direction Using the C Series Module Properties Dialog Box

Complete the following steps to configure the line direction of each digital port using the **C Series Module Properties** dialog box.

1. Configure the CompactRIO system, and add an NI 9401.

2. Right-click the NI 9401 in the **Project Explorer** window and select **Properties** from the shortcut menu to display the **C Series Module Properties** dialog box.
3. Select the direction for each port from the **Initial Line Direction** pull-down menus.
4. Click the **OK** button.
5. Select **File»Save All** in the **Project Explorer** window.

Configuring Line Direction Using the FPGA I/O Method Node

Complete the following steps to configure the line direction of each digital port using the FPGA I/O Method Node.

1. Place an FPGA I/O Method Node on the block diagram and configure it for the NI 9401.
2. Click the **Method** section and select the **Set Line Direction** method from the shortcut menu.
3. Right-click each digital port input and select **Create»Control** from the shortcut menu.
4. On the front panel of the VI, select the direction for each port from the digital port pull-down menus.

NI 9401 (Scan Interface)

CompactRIO 8-Channel, TTL Digital Input/Output Module

 Open digital input example

 Open digital output example

Module I/O Variables

To use I/O from this module in a VI, drag and drop I/O variables from the **Project Explorer** window to the block diagram of the VI. The I/O variables for the channels read and write Boolean values.

Module Channels

The NI 9401 has the following channels.

Channel	Description
DIO**x**	Digital input/output channel **x**, where **x** is the n umber of the channel. For the NI 9401, **x** is 0 to 7 .

C Series Module Properties Dialog Box

Use this dialog box to configure the NI 9401. Right-click the NI 9401 in the **Project Explorer** window and select **Properties** to display this dialog box. You can configure the following options.

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this value.
- **Location**—Specifies a slot in the chassis for the C Series module.
- **Initial Line Direction**—Specifies the initial line direction of each four-channel port as input or output.

Specialty Digital Configuration

You can use the Specialty Digital Configuration page of the **C Series Module Properties** dialog box to configure channels of this module for counter input, counter-driven output, pulse-width modulation output, or quadrature input.

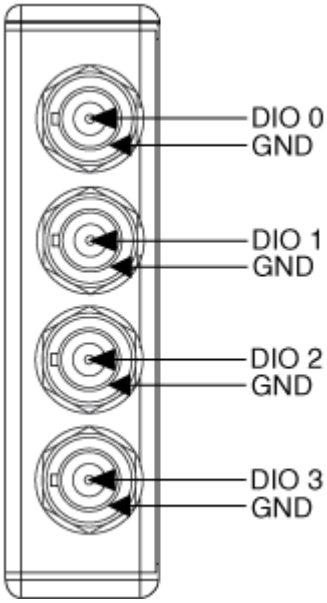
NI 9402

CompactRIO 4-Channel, LVTTL Digital Input/Output Module

Software Reference (?)

FPGA Interface | Scan Interface

NI 9402 Pinout



Related Topics

FPGA Interface
Configuring the Line Direction for the NI 9402

NI 9402 (FPGA Interface)

CompactRIO 4-Channel, LVTTL Digital Input/Output Module

FPGA I/O Node

You can use an FPGA I/O Node, configured for reading and writing, with this device.

Terminals in Software

Use the FPGA I/O Node to access the following terminals for this device.

Terminal	Description

DIO**x**	Digital input/output channel **x**, where **x** is the number of the channel. The NI 9402 has DIO channels 0 to 3.
DIO3:0	Digital port consisting of channels 0 through 3. Channel 3 is returned in the MSB, and channel 0 is returned in the LSB.

Arbitration

You can configure the arbitration settings for digital output channels of this device in the Advanced Code Generation page of the FPGA I/O Properties dialog box. The default arbitration setting is Never Arbitrate. Digital input channels of this device support only the **Never Arbitrate** option for arbitration. You cannot configure arbitration settings for the digital input channels of this device.

I/O Methods

Use the FPGA I/O Method Node to access the following I/O methods for this device.

Method	Description
Set Output Data	Refer to the FPGA I/O Method Node (FPGA Module) topic for a description of this method.
Set Output Enable	Sets the line direction of the digital channel or the DIO3:0 digital port. Refer to the FPGA I/O Method Node (FPGA Module) topic for more information on this method.
Wait on Any Edge	Pauses the execution of the I/O Method Node until the next falling or rising edge of the digital signal. The **Timeout** input specifies in FPGA clock ticks how long the Wait on Any Edge method waits for the next falling or rising edge. A value of 0 causes the method to time out immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.
Wait on Falling Edge	Pauses the execution of the I/O Method Node until the next falling edge of the digital signal. The **Timeout** input specifies in FPGA clock ticks ho

	w long the Wait on Falling Edge method waits fo r the next falling edge. A value of 0 causes the m ethod to time out immediately, a negative value causes the method to wait indefinitely, and a po sitive value causes the method to wait for that n umber of clock ticks before timing out.
Wait on High Level	Pauses the execution of the I/O Method Node un til the digital signal is high. The **Timeout** input specifies in FPGA clock ticks how long the Wait o n High Level method waits for the next high leve l. A value of 0 causes the method to time out im mediately, a negative value causes the method t o wait indefinitely, and a positive value causes t he method to wait for that number of clock ticks before timing out.
Wait on Low Level	Pauses the execution of the I/O Method Node un til the digital signal is low. The **Timeout** input s pecifies in FPGA clock ticks how long the Wait o n Low Level method waits for the next low level. A value of 0 causes the method to time out imm ediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks be fore timing out.
Wait on Rising Edge	Pauses the execution of the I/O Method Node un til the next rising edge of the digital signal. The **Timeout** input specifies in FPGA clock ticks ho w long the Wait on Rising Edge method waits for the next rising edge. A value of 0 causes the met hod to time out immediately, a negative value c auses the method to wait indefinitely, and a pos itive value causes the method to wait for that nu mber of clock ticks before timing out.

Module Method

Use the FPGA I/O Method Node to access the following module method for this device.

Method	Description

Check Status	Returns a Boolean value that indicates whether the module is ready.  **Note** During the first 2 seconds after you reset the FPGA VI, the error terminals on this method may not correctly report certain types of errors.

I/O Properties

This device does not support any I/O properties.

Module Properties

Use the FPGA I/O Property Node to access the following module properties for this device.

Property	Description
Module ID	Returns the module ID.
Serial Number	Returns the unique serial number of the module.
Vendor ID	Returns the NI vendor ID, 0x1093.

Single-Cycle Timed Loop

This device supports the single-cycle Timed Loop. Configure the number of input synchronizing registers for the channels of this device in the Advanced Code Generation page of the FPGA I/O Node Properties dialog box. Configure the number of output synchronizing registers for the channels of this device in the Advanced Code Generation page of the FPGA I/O Properties dialog box.

The NI 9402 supports the following output synchronizing register options:

- **Number of Synchronizing Registers for Output Data when used in SCTL**

- **Number of Synchronizing Registers for Output Enable when used in SCTL**

These two options support the same functionality as the **Number of Synchronizing Registers for Output Data** and **Number of Synchronizing Registers for Output Enable** options described in the Advanced Code Generation FPGA I/O Properties Page (FPGA Module) topic, with the exception that you can use these options only in a single-cycle Timed Loop. You can implement either 0 or 1 synchronizing registers inside the single-cycle Timed Loop, however, if you configure 0 synchronizing registers outside of the single-cycle Timed Loop, the FPGA VI implements 1 synchronizing register by default.

When the module is within a single-cycle Timed Loop, it must be ready to perform digital I/O before a loop containing digital I/O starts. Poll the **Ready** output of the Check Status method to determine whether the module is ready. Digital input operations return invalid data if the module is not ready. The module also might ignore or delay digital output operations if it is not ready.

While the module is performing digital I/O within a single-cycle Timed Loop, do not perform property reads or remove the module from the chassis. Doing any of these actions causes the module to be unable to perform digital I/O and the **Ready** output of the Check Status method to return FALSE.

FPGA Target Clock Support

This device supports only top-level FPGA target clock rates and single-cycle Timed Loop clock rates that are multiples of 40 MHz, such as 40 MHz, 80 MHz, 120 MHz, and so on.

C Series Module Properties Dialog Box for the NI 9402 (FPGA Interface)

Right-click an NI 9402 C Series module in the **Project Explorer** window and select **Properties** from the shortcut menu to display this dialog box.

Use this dialog box to configure a C Series module.

This dialog box includes the following components:

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this option.
- **Location**—Specifies a slot in the chassis for the C Series module.
- **Channels**—Specifies the channel(s) for which you want to select the line direction.
- **Selected Channel(s) Settings**—Specifies the line direction for each channel.
  - **Direction**—Sets the line direction for the selected channel(s) to digital input or digital output. The default is digital input.

Configuring the Line Direction for the NI 9402 (FPGA Interface)

Each digital channel on the NI 9402 is initially configured as a digital input. You can configure the initial line direction for each channel on the NI 9402 at edit time using the C Series Module Properties dialog box. You can programmatically change the line direction for each channel at run time using the FPGA I/O Method Node. The execution of an I/O Method Node that is configured with a Set Output Enable method overwrites the values you configured in the **C Series Module Properties** dialog box. In addition, the execution of an FPGA I/O Node configured for output automatically configures the line for output and overwrites the values you configured in the **C Series Module Properties** dialog box or using the **Set Output Enable** method.

Configuring Line Direction Using the C Series Module Properties Dialog Box

Complete the following steps to set the line direction of channels using the **C Series Module Properties** dialog box.

1. Configure the CompactRIO system, and add an NI 9402.

2. Right-click the NI 9402 in the **Project Explorer** window and select **Properties** from the shortcut menu to display the **C Series Module Properties** dialog box.
3. Select the channel(s) for which you want to configure the line direction from the **Channels** table. You can select more than one channel by holding the <Ctrl> or <Shift> key when selecting channels.
4. Select the direction for the channel(s) from the **Direction** pull-down menu.
5. Click the **OK** button.
6. Select **File»Save All** in the **Project Explorer** window.

Configuring Line Direction of One Channel Using the FPGA I/O Method Node

Complete the following steps to set the line direction of a channel using the FPGA I/O Method Node.

1. Create FPGA I/O items for the channel of the NI 9402 for which you want to configure the line direction.
2. Place an FPGA I/O Method Node on the block diagram and configure it for this channel.
3. Click the **Method** section and select the **Set Output Enable** method from the shortcut menu.
4. Right-click the **Enable** input and select **Create»Control** from the shortcut menu.
5. On the front panel of the VI, click the **Enable** Boolean control to set it to TRUE if you want to set the line direction of the channel to digital output.

Configuring Line Direction of Multiple Channels Using the FPGA I/O Method Node

Complete the following steps to set the line direction of multiple channels using the FPGA I/O Method Node.

1. Create FPGA I/O items for the DIO3:0 digital port of the NI 9402.

2. Place an FPGA I/O Method Node on the block diagram and configure it for the DIO3:0 digital port.
3. Click the **Method** section and select the **Set Output Enable** method from the shortcut menu.
4. Right-click the **Enable** input and select **Create»Control** from the shortcut menu. The **Enable** control appears as an unsigned 8-bit integer. Each bit in the integer represents the line direction of one channel of the NI 9402.
5. On the front panel of the VI, use the **Enable** control to enter the line direction for each channel in the port. Change a bit to 1 to set the line direction of the corresponding channel to digital output. Leave a bit as 0 to set the line direction of the corresponding channel to digital input. Refer to the table below for examples of what to enter in the **Enable** control.

Channel Line Direction Configuration	Enable Control (Floating Point)	Enable Control (Binary)	Enable Control (Hex)
Change all channels to input	0	0000	0x00
Change all channels to output	15	1111	0x0F
Change channel 0 to output	1	0001	0x01

NI 9402 (Scan Interface)

CompactRIO 4-Channel, LVTTL Digital Input/Output Module

Open digital input example

Open digital output example

Module I/O Variables

To use I/O from this module in a VI, drag and drop I/O variables from the **Project Explorer** window to the block diagram of the VI. The I/O variables for the channels read and write Boolean values.

Module Channels

The NI 9402 has the following channels.

Channel	Description
DIO**x**	Digital input/output channel **x**, where **x** is the number of the channel. For the NI 9402, **x** is 0 to 3.

C Series Module Properties Dialog Box

Use this dialog box to configure the NI 9402. Right-click the NI 9402 in the **Project Explorer** window and select **Properties** to display this dialog box. You can configure the following options.

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this value.
- **Location**—Specifies a slot in the chassis for the C Series module.
- **Channels**—Specifies the channel(s) for which you want to configure settings.
- **Direction**—Specifies the initial line direction of the selected channel(s) as input or output.

Specialty Digital Configuration

You can use the Specialty Digital Configuration page of the **C Series Module Properties** dialog box to configure channels of this module for counter input, counter-driven output, pulse-width modulation output, or quadrature input.

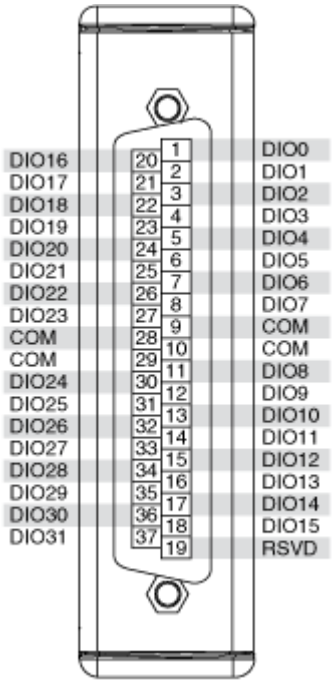
NI 9403

CompactRIO 32-Channel, TTL Digital Input/Output Module

Software Reference (?)

FPGA Interface | Scan Interface

NI 9403 Pinout



Related Topics

FPGA Interface
Configuring the Line Direction for the NI 9403

NI 9403 (FPGA Interface)

CompactRIO 32-Channel, TTL Digital Input/Output Module

FPGA I/O Node

You can use an FPGA I/O Node, configured for reading and writing, with this device.

Terminals in Software

Use the FPGA I/O Node to access the following terminals for this device.

Terminal	Description
DIO**x**	Digital input/output channel **x**, where **x** is the number of the channel. The NI 9403 has DIO channels 0 to 31.
DIO7:0	Digital port consisting of channels 0 through 7. Channel 7 is returned in the MSB, and channel 0 is returned in the LSB.
DIO15:8	Digital port consisting of channels 8 through 15. Channel 15 is returned in the MSB, and channel 8 is returned in the LSB.
DIO23:16	Digital port consisting of channels 16 through 23. Channel 23 is returned in the MSB, and channel 16 is returned in the LSB.
DIO31:24	Digital port consisting of channels 24 through 31. Channel 31 is returned in the MSB, and channel 24 is returned in the LSB.
DIO31:0	Digital port consisting of channels 0 through 31. Channel 31 is returned in the MSB, and channel 0 is returned in the LSB.

Arbitration

This device supports only the Arbitrate if Multiple Requestors Only and Never Arbitrate options for arbitration. The default arbitration setting is **Arbitrate if Multiple Requestors Only**.

If you are sure that the design of the FPGA VI will never allow more than one digital function to execute at the same time, even on different channels, you can place a checkmark in the **Disable Arbitration** checkbox on the C Series Module Properties dialog box to disable arbitration and reduce the amount of FPGA logic used by VIs. If more than one digital function could execute simultaneously in the FPGA VI, leave the box unchecked.

I/O Methods

Use the FPGA I/O Method Node to access the following I/O methods for this device.

Method	Description

Read and Set Output Data	First returns the data read from the digital line or port, then writes data to the line or port without enabling it. You can use the Read and Set Output Data method to optimize performance when performing successive reads and writes on a DIO resource. For the NI 9403, this method is faster than using a read FPGA I/O Node and a Set Output Data method. The data type of the output and input depends on the I/O item. If the I/O item is a digital line, **Data to Set** requires a Boolean data type. If the I/O item is a digital port, **Data to Set** requires a numeric data type.
Set Output Data	Refer to the FPGA I/O Method Node (FPGA Module) topic for a description of this method.
Set Output Enable	Sets the line direction of the digital channel or port. Refer to the FPGA I/O Method Node (FPGA Module) topic for more information on this method.

Module Methods

This device does not support any module methods.

I/O Properties

This device does not support any I/O properties.

Module Properties

Use the FPGA I/O Property Node to access the following module properties for this device.

Property	Description
Module ID	Returns the module ID.
Serial Number	Returns the unique serial number of the module.
Vendor ID	Returns the NI vendor ID, 0x1093.

Single-Cycle Timed Loop

This device does not support the single-cycle Timed Loop.

Hardware Documentation

Refer to the NI 9403 hardware documentation on ni.com/manuals for information about module specifications and how to use the module. Refer to the CompactRIO Related Documentation topic for additional CompactRIO documentation resources.

C Series Module Properties Dialog Box for the NI 9403 (FPGA Interface)

Right-click an NI 9403 C Series module in the **Project Explorer** window and select **Properties** from the shortcut menu to display this dialog box.

Use this dialog box to configure a C Series module.

This dialog box includes the following components:

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this option.
- **Location**—Specifies a slot in the chassis for the C Series module.
- **Channels**—Specifies the channel(s) for which you want to select the line direction.
- **Selected Channel(s) Settings**—Specifies the line direction for each channel.
  - **Direction**—Sets the line direction for the selected channel(s) to digital input or digital output. The default is digital input.
- **Disable Arbitration**—Place a checkmark in this checkbox if you want to change the arbitration setting to Never Arbitrate and reduce the amount of FPGA logic used by VIs. Check this box only if you are sure that the design of

the FPGA VI will never allow more than one digital function to execute at the same time, even on different channels. If more than one digital function could execute simultaneously in the FPGA VI, leave the box unchecked to keep the default Arbitrate if Multiple Requestors Only arbitration setting.

Configuring the Line Direction for the NI 9403 (FPGA Interface)

Each digital channel on the NI 9403 is initially configured as a digital input. You can configure the initial line direction for each channel on the NI 9403 at edit time using the C Series Module Properties dialog box. You can programmatically change the line direction for each channel at run time using the FPGA I/O Method Node. The execution of an I/O Method Node that is configured with a Set Output Enable method overwrites the values you configured in the **C Series Module Properties** dialog box. In addition, the execution of an FPGA I/O Node configured for output automatically configures the line for output and overwrites the values you configured in the **C Series Module Properties** dialog box or using the **Set Output Enable** method.

Configuring Line Direction Using the C Series Module Properties Dialog Box

Complete the following steps to set the line direction of channels using the **C Series Module Properties** dialog box.

1. Configure the CompactRIO system, and add an NI 9403.
2. Right-click the NI 9403 in the **Project Explorer** window and select **Properties** from the shortcut menu to display the **C Series Module Properties** dialog box.
3. Select the channel(s) for which you want to configure the line direction from the **Channels** table. You can select more than one channel by holding the <Ctrl> or <Shift> key when selecting channels.
4. Select the direction for the channel(s) from the **Direction** pull-down menu.
5. Click the **OK** button.
6. Select **File»Save All** in the **Project Explorer** window.

Configuring Line Direction of One Channel Using the FPGA I/O Method Node

Complete the following steps to set the line direction of a channel using the FPGA I/O Method Node.

1. Create FPGA I/O items for the channel of the NI 9403 for which you want to configure the line direction.
2. Place an FPGA I/O Method Node on the block diagram and configure it for this channel.
3. Click the **Method** section and select the **Set Output Enable** method from the shortcut menu.
4. Right-click the **Enable** input and select **Create»Control** from the shortcut menu.
5. On the front panel of the VI, click the **Enable** Boolean control to set it to TRUE if you want to set the line direction of the channel to digital output.

Configuring Line Direction of Multiple Channels Using the FPGA I/O Method Node

Complete the following steps to set the line direction of multiple channels using the FPGA I/O Method Node.

1. Create FPGA I/O items for the digital port of the NI 9403 that contains the channels you want to configure.
2. Place an FPGA I/O Method Node on the block diagram and configure it for this digital port.
3. Click the **Method** section and select the **Set Output Enable** method from the shortcut menu.
4. Right-click the **Enable** input and select **Create»Control** from the shortcut menu. If you configured the FPGA I/O Method Node for the DIO7:0, DIO15:8, DIO23:16, or DIO31:24 digital port, the **Enable** control appears as an unsigned 8-bit integer. If you configured the FPGA I/O Method Node for the DIO31:0 digital port, the **Enable** control appears as an unsigned 32-bit integer. Each bit in the integer represents the line direction of one channel of the NI 9403.

5. On the front panel of the VI, use the **Enable** control to enter the line direction for each channel in the port. Change a bit to 1 to set the line direction of the corresponding channel to digital output. Leave a bit as 0 to set the line direction of the corresponding channel to digital input. Refer to the table below for examples of what to enter in the **Enable** control if you configured the FPGA I/O Method Node for the DIO7:0 digital port.

Channel Line Direction Configuration	Enable Control (Hex)	Enable Control (Binary)
Change all channels to input	0x00	0b00000000
Change all channels to output	0xFF	0b11111111
Change channel 0 to output	0x01	0b00000001
Change channels 0 through 5 to output	0x3F	0b00111111
Change channels 3 and 7 to output	0x88	0b10001000

Refer to the table below for examples of what to enter in the **Enable** control if you configured the FPGA I/O Method Node for the DIO31:0 digital port.

Channel Line Direction Configuration	Enable Control (Hex)	Enable Control (Binary)
Change all channels to input	0x00000000	0b0000000000000000 0000000000000000
Change all channels to output	0xFFFFFFFF	0b1111111111111111 1111111111111111
Change channel 0 to output	0x00000001	0b0000000000000000 0000000000000001
Change channels 0 through 5 to output	0x0000003F	0b0000000000000000 0000000000111111
Change channels 3 and 7 to output	0x00000088	0b0000000000000000 0000000010001000

NI 9403 (Scan Interface)

CompactRIO 32-Channel, TTL Digital Input/Output Module

Open digital input example

Open digital output example

Module I/O Variables

To use I/O from this module in a VI, drag and drop I/O variables from the **Project Explorer** window to the block diagram of the VI. The I/O variables for the channels read and write Boolean values.

Module Channels

The NI 9403 has the following channels.

Channel	Description
DIO**x**	Digital input/output channel **x**, where **x** is the n umber of the channel. For the NI 9403, **x** is 0 to 3 1.

C Series Module Properties Dialog Box

Use this dialog box to configure the NI 9403. Right-click the NI 9403 in the **Project Explorer** window and select **Properties** to display this dialog box. You can configure the following options.

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this value.
- **Location**—Specifies a slot in the chassis for the C Series module.
- **Channels**—Specifies the channel(s) for which you want to configure settings.

- **Initial Line Direction**—Specifies the initial line direction of the selected channel(s) as input or output.

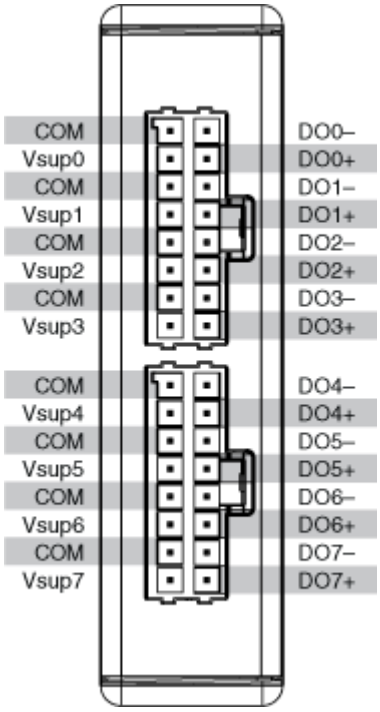
NI 9470

CompactRIO 8-Channel Digital Output Module with Current Readback

Software Reference (?)

FPGA Interface

NI 9470 Pinout



NI 9470 (FPGA Interface)

CompactRIO 8-Channel Digital Output Module with Current Readback

FPGA I/O Node

You can use an FPGA I/O Node, configured for reading, with this device.

Terminals in Software

Use the FPGA I/O Node to access the following terminals for this device.

Terminal	Description
CH**x**	Output setpoint for channel **x**, where **x** is the number of the channel. The NI 9470 has channels 0 to 7. The output setpoint depends on the Output Mode setting for the channel. Open Loop Mode supports output setpoints from 0% to 100%. Closed Loop Mode support output setpoints from 0 A to 3.999 A.
Start	Channel that controls when the NI 9470 starts outputting PWM and acquiring readback data. If TRUE is written to the **Start** channel, the NI 9470 starts outputting PWM and acquiring readback data. The DO**x** that have been enabled will be reset to 0 V every time this I/O node is executed. When the NI 9470 is outputting PWM and acquiring readback data, you must write TRUE to the **Stop** channel before you can access properties. If FALSE is written to the **Start** channel, no operation is performed.
Stop	Channel that controls when the NI 9470 stops outputting PWM and acquiring readback data. If TRUE is written to the **Stop** channel, the NI 9470 stops outputting PWM and acquiring readback data. When the NI 9470 is outputting PWM and acquiring readback data, you must write TRUE to the **Stop** channel before you can access properties. If FALSE is written to the **Stop** channel, no operation is performed.
AverageCurrent	Average current readback. Readback is functional after issuing a **Start** and depends on channel enable. If channel is not enabled, the current reading will be 0. Represented as -4 A to 3.999 A.
DutyCycle	Duty cycle readback. Readback is functional after issuing a **Start** and is independent of channel enable. Represented as 0% to 100%.

Voltage	Channel voltage readback. Readback is functional after issuing a **Start** and is independent of the channel enable. Voltage is represented as 0 V to 40 V. Voltage readback nodes run at a constant data rate independent of the channel PWM frequencies and should not be placed in the same loop as the other NI 9470 I/O nodes.

Arbitration

This device supports only the Arbitrate if Multiple Requestors Only option for arbitration. You cannot configure arbitration settings for this device.

I/O Methods

Use the FPGA I/O Method Node to access the following I/O methods for this device.

Method	Description
Set Channel Enable	Enables or disables each channel. All channels are disabled and DO**x** outputs are tristate when the module powers on. You can execute the **Set Channel Enable** method before or after **Start**. To turn on the channels before acquisition, execute the method before **Start**. If the method is executed before **Start**, the channel will be enabled or disabled immediately, and the DO**x** output will output 0 V. If the method is executed after **Start**, the channel will be enabled or disabled on the next write sequence. ▪ To **Enable** a channel, wire a Boolean constant set to TRUE. ▪ To **Disable** a channel, wire a Boolean constant set to FALSE.

Module Methods

Use the FPGA I/O Method Node to access the following module methods for this device.

Method	Description
Check Output Status	Returns Booleans for each channel that indicates whether the module reported an over temperature fault or any channel reported a power supply fault or overcurrent fault during the last time the FPGA I/O Node communicated with the module. When the FPGA I/O Node communicates with the module, the FPGA VI samples the states of the module and channels and overwrites the previous output status with the latest state of the module and channels. ▪ **Module Over Temperature**—Returns a Boolean value. A value of TRUE indicates that the module exceeded its temperature rating. When a Module Over Temperature occurs, all enabled channels will be disabled, and their respective DO**x** outputs will drive to 0 V. Use the **Set Channel Enable** I/O Method after the over temperature fault condition is removed to re-enable the channel without stopping the task, and the latched status will clear. ▪ **Power Supply Fault**—Returns an array of Boolean values. A value of TRUE in any index indicates that a power fault has been detected after the last status read on the channel with the same number as the index. A value of FALSE indicates that no power fault was detected on that channel after the last status read. When a Power Supply Fault occurs, the channel with the same number as the index will be disabled, and DO**x** will drive to 0 V. Use the **Set Channel Enable** I/O Method after the Power Supply Fault condition is removed to re-enable the channel without stopping the task, and the latched status will clear. ▪ **Channel Overcurrent**—Returns an array of Boolean values. A value of TRUE in any index indicates that the channel with t

	he same number as the index exceeded th e current limit after the last status read. A value of FALSE indicates that the channel did not exceed the current limit after the l ast status read. When a Channel Overcurr ent fault occurs, the channel with the sam e number as the index will be disabled, an d DO**x** will drive to 0 V. Use the **Set Chan nel Enable** I/O Method after the Channel Overcurrent fault condition is removed to re-enable the channel without stopping t he task, and the latched status will clear.
Read Module Temperature	Reads the average measured temperature on th e module. ▪ **Module Temperature**—Returns the module temperature. Temperature readb ack is functional after issuing **Start**. Repre sented as -40 °C to 125 °C

I/O Properties

Use the FPGA I/O Property Node to access the following I/O properties for this device. You must configure all channel properties before starting acquisition. Changing the properties during acquisition will not work.

Property	Description
Output Mode	Sets the channel to operate in either open loop mode (duty cycle setpoint) or closed loop mode (average current setpoint).
PWM Divisor	Configures the channel PWM frequency as a divi sor of the module's overall data rate. Divisor val ues range from 1 to 511. **Note** A divisor value o f 1 is only supported w hen the data rate is set to 2,000 S/s or 2,048 S/ s.

Proportional Gain	Configures the proportional gain (**duty cycle %**/Amps) coefficient of the closed loop PID control.  **Note** This property only applies to channels configured to Closed Loop Mode (Average Current Setpoint).
Integral Gain	Configures the integral gain (**duty cycle %**/Amps) coefficient of the closed loop PID control.  **Note** This property only applies to channels configured to Closed Loop Mode (Average Current Setpoint).
Derivative gain	Configures the derivative gain (**duty cycle %**/Amps) coefficient of the closed loop PID control.  **Note** This property only applies to channels configured to Closed Loop Mode (Average Current Setpoint).
Dither Amplitude	Configures the channel dither amplitude. The value depends on the output mode to which the channel is set. In open loop mode, the peak amplitude is duty cycle (percentage) with a range of 0% to 100%. In closed loop mode, the peak amplitude (amps) is current with a range of 0 A to 3.999 A.  **Note** In closed loop mode, dither performance depends on the PID response.
Dither Divisor	Configures the channel dither frequency as a divisor of the channel's PWM frequency. Divisor values range from 4 to 4,095.

	Note In closed loop mode, dither performance depends on the PID response.

Module Properties

Use the FPGA I/O Property Node to access the following module properties for this device.

Property	Description
Data Rate	Sets the overall data rate. All I/O will be synchronized to this rate. You must configure the data rate before starting acquisition. There are four data rates based on the master timebase source: 12.8 MHz OCLK: 3.200 kS/s; 3.125 kS/s; 2.560 kS/s; 2.000 kS/s 13.1072 MHz OCLK: 3.277 kS/s; 3.200 kS/s; 2.621 kS/s; 2.048 kS/s
Module ID	Returns the module ID, 0x7A59.
Serial Number	Returns the unique serial number of the module.
Vendor ID	Returns the NI vendor ID, 0x1093.

Single-Cycle Timed Loop

This device does not support the single-cycle Timed Loop.

Example

Refer to `LabVIEW\examples\CompactRIO\Module Specific\NI 9470\NI 9470 Getting Started.lvproj` for an example on getting started with this module.

C Series Module Properties Dialog Box for the NI 9470 (FPGA Interface)

Right-click an NI 9470 C Series module in the **Project Explorer** window and select **Properties** from the shortcut menu to display this dialog box.

Use this dialog box to configure a C Series module.

This dialog box includes the following components:

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this option.
- **Location**—Specifies a slot in the chassis for the C Series module.
- **Master Timebase Source**—Specifies the master timebase source that the module uses.
- **Export Onboard Clock**—Place a checkmark in this checkbox if you want to make this module accessible as a master timebase source to other modules.
- **Data Rate**—Specifies the rate at which the module acquires data.
- **Channel Configuration**—Launches the channel configuration dialog box to configure the channel settings.

Configuring Channels on the NI 9470 (FPGA Interface)

Complete the following steps to configure the channels of the NI 9470.

1. Right-click an NI 9470 C Series module in the **Project Explorer** window and select **Properties** from the shortcut menu to display this dialog box.
2. Click the **Channel Configuration** button to open the Channel Configuration dialog box.
3. Select a channel to configure.
4. Configure the following settings.

- **Output Mode**—Specifies the output mode for the selected channel.
  - **Duty Cycle**—Sets the channel to open loop mode without any internal control mechanism. You will have to implement your own control loop in your application.
  - **Average Current**—Sets the channel to closed loop mode using an internal PID control loop. This PID control executes based on the PID coefficients.
- **PWM Divisor**—Specifies the PWM divisor value for the selected channel. Each channel runs based on the PWM frequency, which is derived by the formula **Data Rate** ÷ **PWM Divisor**. Supported values range 2 to 511. You can only set the PWM Divisor to a value of 1 if the data rate is set to 2,000 S/s or 2,048 S/s.
- **PID Response**—Specifies the PID response for the selected channel. This option is only available if the channel's **Output Mode** is set to **Average Current**.
  - **Slow**—The proportional, integral, and derivative gain coefficients are pre-set to provide a slow PID response speed. The output current will arrive at the intended setpoint at a slower rate.
  - **Medium**—The proportional, integral, and derivative gain coefficients are pre-set to provide a medium PID response speed. The output current will arrive at the intended setpoint at a moderate rate.
  - **Fast**—The proportional, integral, and derivative gain coefficients are pre-set to provide a fast PID response speed. The output current will arrive at the intended setpoint at a faster rate.
  - **Custom**—Customize your own PID response by entering your own **Proportional Gain**, **Integral Gain**, and **Derivative Gain**.
    - **Proportional Gain**—Specifies the proportional gain coefficient for the selected channel. Specified in units of **(duty cycle %)** ÷ Amps.
    - **Integral Gain**—Specifies the integral gain coefficient for the selected channel. Specified in units of **(duty cycle %)** ÷ Amps.

- **Derivative Gain**—Specifies the derivative gain coefficient for the selected channel. Specified in units of **(duty cycle %)** ÷ Amps.

- **Dither Amplitude**—Specifies the dither amplitude for the selected channel. Represents the dither peak amplitude for the channel. You can disable dither by setting this parameter to 0. The range depends on which **Output Mode** the channel is set.

Output Mode	Range
Duty Cycle	0% to 100%
Average Current	0 A to 3.999 A

- **Dither Divisor**—Specifies the Dither Divisor for the selected channel, which controls the dither frequency. Dither frequency is derived using the formula **PWM Frequency** ÷ **Dither Divisor**.

5. Click **OK** to close the Channel Configuration dialog box.
6. Click **OK** to close the Module Properties Dialog Box.

Synchronizing the NI 9470 with Other Modules (FPGA Interface)

You can synchronize the NI 9470 with other modules that are connected to the same FPGA device if your application meets the following requirements:

- The modules must use the same master timebase source
- The modules must start acquisition mode at the same time
- Each channel of the NI 9470 must be in its own FPGA I/O Node residing in its own loop.

You must create FPGA I/O items for the module before you can configure the items using the FPGA I/O Node. Develop the FPGA VI to meet the guidelines described in the following table.

For delta-sigma modules, you will need to synchronize multiple sample rates.

Guideline	Details
Share a master timebase source	Configure the modules to share master timebase source.

Start the synchronized acquisition	▪ Configure an FPGA I/O Node with **Start** channels for the module you want to synchronize. ▪ Wire a Boolean constant set to TRUE to each **Start** channel. ▪ Ensure that all **Start** channels are in the same FPGA I/O Node. The data will not be synchronized if they are not.
Acquire data from synchronized modules	▪ Create separate loops for each channel of the NI 9470 that runs at a different data rate. Channels that are configured to run at the same data rate can either be in the same loop or be in a separate loop. ▪ For channels that are configured to run at different data rates, configure an FPGA I/O Node in each loop. For channels that are configured to run at the same data rate, you can either configure one FPGA I/O Node for the all the channels or configure an FPGA I/O Node for each channel. If you place channels that are configured for different data rates in the same loop, LabVIEW returns an overrun warning, error 65539, from the FPGA I/O Node for the AI channels and an underflow warning, error 65676, from the FPGA I/O Node for the AO channels. ▪ A delay occurs before the FPGA I/O Node returns the first data point. The length of the delay depends on the data rate and the PWM Divisor for each NI 9470 channel. ▪ Refer to Synchronizing Multiple Modules (FPGA Interface) for how to synchronize other DSA modules that are synchronized with the NI 9470.
Understand the maximum sample rate when synchronizing multiple modules	—

Equation for synchronizing multiple sample rates

12.8 MHz OCLK	13.1072 MHz OCLK	Time to First Channel Sample(s)
3.200 kS/s	3.277 kS/s	(14,472,838 + 4,000 * **n**) * (**Master Timebase Period** ± 1 **Master Timebase Period**)
3.125 kS/s	3.200 kS/s	(14,472,838 + 4,096 * **n**) * (**Master Timebase Period** ± 1 **Master Timebase Period**)
2.560 KS/s	2.621 KS/s	(14,472,838 + 5,000 * **n**) * (**Master Timebase Period** ± 1 **Master Timebase Period**)
2.000 KS/s	2.048 KS/s	(14,473,006 + 6,400 * **n**) * (**Master Timebase Period** ± 1 **Master Timebase Period**)

Notes:
Master Timebase Period = period of the internal or external clock that the module uses (1/12.8 MHz or 1/13.072 MHz).
n = channel PWN divisor. Refer to the PWM Divisor I/O Property for valid values of **n** for each data rate divisor option.
Only data rates of 3.125 kS/s or 2.000 kS/s with 12.8 MHz OCLK or 3.200 kS/s or 2.048 kS/s with 13.1072 MHz OCLK are compatible with other DSA modules for synchronizing multiple modules.
The formulas above apply to each individual channel of the NI 9470 based on each channel's PWM divisor.

Related Topics

Synchronizing Multiple Modules (FPGA Interface)

Configuring the Master Timebase Source for a Module

Understanding the Maximum Sample Rate when Synchronizing Multiple Modules (FPGA Interface)

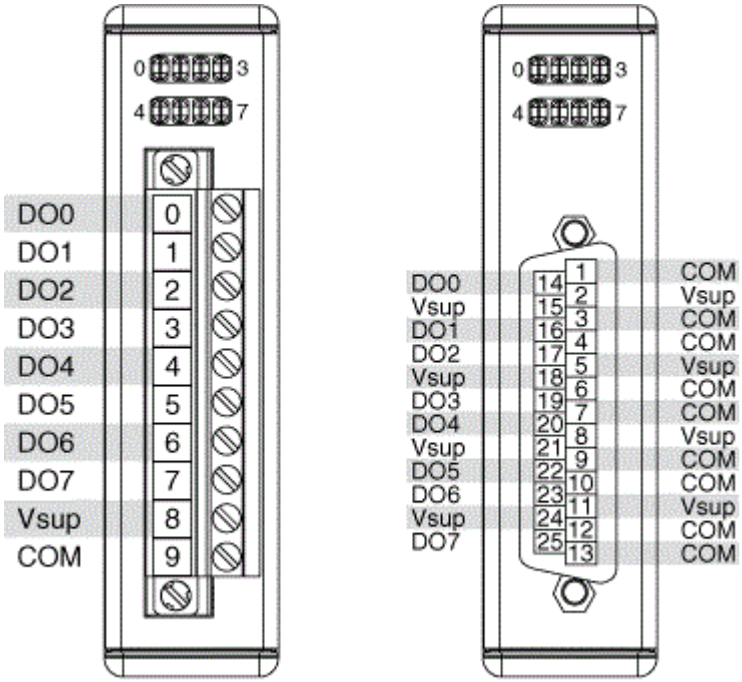
NI 9472

CompactRIO 8-Channel, 24 V, Sourcing Digital Output Module

Software Reference (?)

FPGA Interface | Scan Interface

NI 9472 Pinout



NI 9472 (FPGA Interface)

CompactRIO 8-Channel, 24 V, Sourcing Digital Output Module

FPGA I/O Node

You can use an FPGA I/O Node, configured for writing, with this device.

Terminals in Software

Use the FPGA I/O Node to access the following terminals for this device.

Terminal	Description
DO**x**	Digital output channel **x**, where **x** is the number of the channel. The NI 9472 has DO channels 0 to 7.

DO7:0	Digital port consisting of channels 0 through 7. Channel 7 is returned in the MSB, and channel 0 is returned in the LSB.

Arbitration

You can configure the arbitration settings for the channels of this device in the Advanced Code Generation page of the FPGA I/O Properties dialog box. The default arbitration setting is Never Arbitrate.

I/O Methods

This device does not support any I/O methods.

Module Methods

Use the FPGA I/O Method Node to access the following module method for this device.

Method	Description
Check Status	Returns a Boolean value that indicates whether the module is ready. **Note** During the first 2 seconds after you reset the FPGA VI, the error terminals on this method may not correctly report certain types of errors.

I/O Properties

This device does not support any I/O properties.

Module Properties

Use the FPGA I/O Property Node to access the following module properties for this device.

Property	Description
Module ID	Returns the module ID.
Serial Number	Returns the unique serial number of the module .
Vendor ID	Returns the NI vendor ID, 0x1093.

Single-Cycle Timed Loop

This device supports the single-cycle Timed Loop. Configure the number of output synchronizing registers for the channels of this device in the Advanced Configuration dialog box.

When the module is within a single-cycle Timed Loop, it must be ready to perform digital output before a loop containing digital output starts. Poll the **Ready** output of the Check Status method to determine whether the module is ready. The module might ignore or delay digital output operations if it is not ready.

While the module is performing digital output within a single-cycle Timed Loop, do not perform property reads or remove the module from the chassis. Doing either of these actions causes the module to be unable to perform digital output and the **Ready** output of the Check Status method to return FALSE.

FPGA Target Clock Support

This device supports only top-level FPGA target clock rates and single-cycle Timed Loop clock rates that are multiples of 40 MHz, such as 40 MHz, 80 MHz, 120 MHz, and so on.

C Series Module Properties Dialog Box for the NI 9472/9474/9475/9481/9482/9485 (FPGA Interface)

Right-click an NI 9472, NI 9474, NI 9475, NI 9481, NI 9482, or NI 9485 C Series module in the **Project Explorer** window and select **Properties** from the shortcut menu to display this dialog box.

Use this dialog box to configure a C Series module.

This dialog box includes the following components:

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this option.
- **Location**—Specifies a slot in the chassis for the C Series module.
- **Advanced**—Launches the Advanced Configuration dialog box.

NI 9472 (Scan Interface)

CompactRIO 8-Channel, 24 V, Sourcing Digital Output Module


Open example

Module I/O Variables

To use I/O from this module in a VI, drag and drop I/O variables from the **Project Explorer** window to the block diagram of the VI. The I/O variables write Boolean values to the channels.

Module Channels

The NI 9472 has the following channels.

Channel	Description
DO**x**	Digital output channel **x**, where **x** is the number of the channel. For the NI 9472, **x** is 0 to 7.

C Series Module Properties Dialog Box

Use this dialog box to configure the NI 9472. Right-click the NI 9472 in the **Project Explorer** window and select **Properties** to display this dialog box. You can configure the following options.

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module

based on the slot number. You can use this field to give the module a descriptive name.

- **Module Type**—Specifies the type of C Series module. You cannot change this value.
- **Location**—Specifies a slot in the chassis for the C Series module.

Specialty Digital Configuration

You can use the Specialty Digital Configuration page of the **C Series Module Properties** dialog box to configure channels of this module for counter-driven output or pulse-width modulation output.

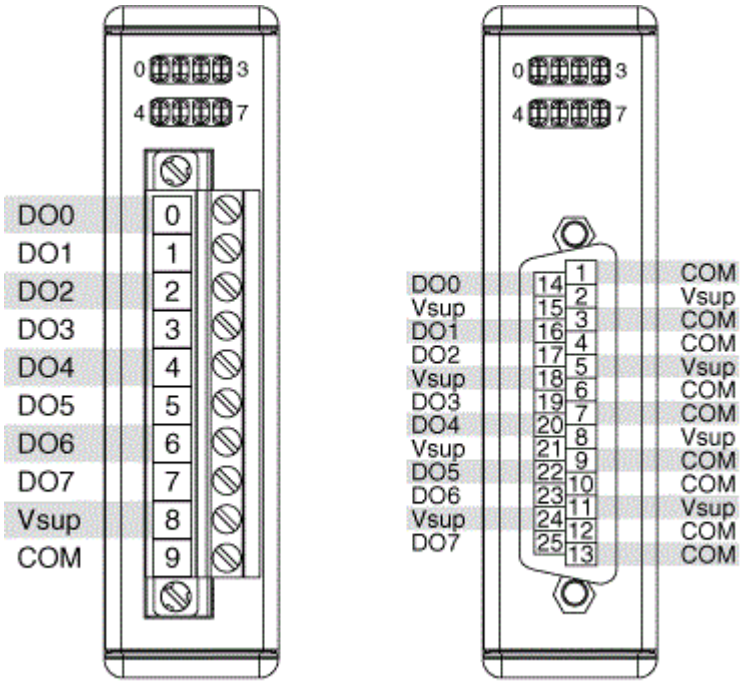
NI 9474

CompactRIO 8-Channel, 24 V, High-Speed, Sourcing Digital Output Module

Software Reference (?)

FPGA Interface | Scan Interface

NI 9474 Pinout



NI 9474 (FPGA Interface)

CompactRIO 8-Channel, 24 V, High-Speed, Sourcing Digital Output Module

FPGA I/O Node

You can use an FPGA I/O Node, configured for writing, with this device.

Terminals in Software

Use the FPGA I/O Node to access the following terminals for this device.

Terminal	Description
DO**x**	Digital output channel **x**, where **x** is the number of the channel. The NI 9474 has DO channels 0 t o 7.
DO7:0	Digital port consisting of channels 0 through 7. Channel 7 is returned in the MSB, and channel 0 is returned in the LSB.

Arbitration

You can configure the arbitration settings for the channels of this device in the Advanced Code Generation page of the FPGA I/O Properties dialog box. The default arbitration setting is Never Arbitrate.

I/O Methods

This device does not support any I/O methods.

Module Methods

Use the FPGA I/O Method Node to access the following module method for this device.

Method	Description
Check Status	Returns a Boolean value that indicates whether the module is ready.

	Note During the first 2 seconds after you reset the FPGA VI, the error terminals on this method may not correctly report certain types of errors.

I/O Properties

This device does not support any I/O properties.

Module Properties

Use the FPGA I/O Property Node to access the following module properties for this device.

Property	Description
Module ID	Returns the module ID.
Serial Number	Returns the unique serial number of the module.
Vendor ID	Returns the NI vendor ID, 0x1093.

Single-Cycle Timed Loop

This device supports the single-cycle Timed Loop. Configure the number of output synchronizing registers for the channels of this device in the Advanced Configuration dialog box.

When the module is within a single-cycle Timed Loop, it must be ready to perform digital output before a loop containing digital output starts. Poll the **Ready** output of the Check Status method to determine whether the module is ready. The module might ignore or delay digital output operations if it is not ready.

While the module is performing digital output within a single-cycle Timed Loop, do not perform property reads or remove the module from the chassis. Doing either of these actions causes the module to be unable to perform digital output and the **Ready** output of the Check Status method to return FALSE.

FPGA Target Clock Support

This device supports only top-level FPGA target clock rates and single-cycle Timed Loop clock rates that are multiples of 40 MHz, such as 40 MHz, 80 MHz, 120 MHz, and so on.

C Series Module Properties Dialog Box for the NI 9472/9474/9475/9481/9482/9485 (FPGA Interface)

Right-click an NI 9472, NI 9474, NI 9475, NI 9481, NI 9482, or NI 9485 C Series module in the **Project Explorer** window and select **Properties** from the shortcut menu to display this dialog box.

Use this dialog box to configure a C Series module.

This dialog box includes the following components:

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this option.
- **Location**—Specifies a slot in the chassis for the C Series module.
- **Advanced**—Launches the Advanced Configuration dialog box.

NI 9474 (Scan Interface)

CompactRIO 8-Channel, 24 V, High-Speed, Sourcing Digital Output Module


Open example

Module I/O Variables

To use I/O from this module in a VI, drag and drop I/O variables from the **Project Explorer** window to the block diagram of the VI. The I/O variables write Boolean values to the channels.

Module Channels

The NI 9474 has the following channels.

Channel	Description
DO**x**	Digital output channel **x**, where **x** is the number of the channel. For the NI 9474, **x** is 0 to 7.

C Series Module Properties Dialog Box

Use this dialog box to configure the NI 9474. Right-click the NI 9474 in the **Project Explorer** window and select **Properties** to display this dialog box. You can configure the following options.

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this value.
- **Location**—Specifies a slot in the chassis for the C Series module.

Specialty Digital Configuration

You can use the Specialty Digital Configuration page of the **C Series Module Properties** dialog box to configure channels of this module for counter-driven output or pulse-width modulation output.

NI 9475

CompactRIO 8-Channel, 60 V, High-Speed, Sourcing Digital Output Module

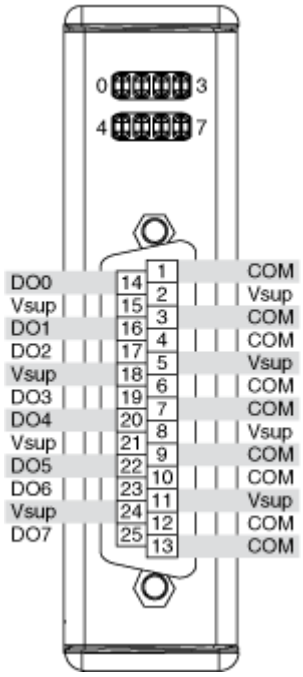
Software Reference (?)

FPGA Interface | Scan Interface

NI 9475

CompactRIO 8-Channel, 60 V, High-Speed, Sourcing Digital Output Module

NI 9475 Pinout



NI 9475 (FPGA Interface)

CompactRIO 8-Channel, 60 V, High-Speed, Sourcing Digital Output Module

FPGA I/O Node

You can use an FPGA I/O Node, configured for writing, with this device.

Terminals in Software

Use the FPGA I/O Node to access the following terminals for this device.

Terminal	Description
DO**x**	Digital output channel **x**, where **x** is the number of the channel. The NI 9475 has DO channels 0 t o 7.

DO7:0	Digital port consisting of channels 0 through 7. Channel 7 is returned in the MSB, and channel 0 is returned in the LSB.

Arbitration

You can configure the arbitration settings for the channels of this device in the Advanced Code Generation page of the FPGA I/O Properties dialog box. The default arbitration setting is Never Arbitrate.

I/O Methods

This device does not support any I/O methods.

Module Methods

Use the FPGA I/O Method Node to access the following module method for this device.

Method	Description
Check Status	Returns a Boolean value that indicates whether the module is ready.  **Note** During the first 2 seconds after you reset the FPGA VI, the error terminals on this method may not correctly report certain types of errors.

I/O Properties

This device does not support any I/O properties.

Module Properties

Use the FPGA I/O Property Node to access the following module properties for this device.

Property	Description
Module ID	Returns the module ID.
Serial Number	Returns the unique serial number of the module .
Vendor ID	Returns the NI vendor ID, 0x1093.

Single-Cycle Timed Loop

This device supports the single-cycle Timed Loop. Configure the number of output synchronizing registers for the channels of this device in the Advanced Configuration dialog box.

When the module is within a single-cycle Timed Loop, it must be ready to perform digital output before a loop containing digital output starts. Poll the **Ready** output of the Check Status method to determine whether the module is ready. The module might ignore or delay digital output operations if it is not ready.

While the module is performing digital output within a single-cycle Timed Loop, do not perform property reads or remove the module from the chassis. Doing either of these actions causes the module to be unable to perform digital output and the **Ready** output of the Check Status method to return FALSE.

FPGA Target Clock Support

This device supports only top-level FPGA target clock rates and single-cycle Timed Loop clock rates that are multiples of 40 MHz, such as 40 MHz, 80 MHz, 120 MHz, and so on.

C Series Module Properties Dialog Box for the NI 9472/9474/9475/9481/9482/9485 (FPGA Interface)

Right-click an NI 9472, NI 9474, NI 9475, NI 9481, NI 9482, or NI 9485 C Series module in the **Project Explorer** window and select **Properties** from the shortcut menu to display this dialog box.

Use this dialog box to configure a C Series module.

This dialog box includes the following components:

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this option.
- **Location**—Specifies a slot in the chassis for the C Series module.
- **Advanced**—Launches the Advanced Configuration dialog box.

NI 9475 (Scan Interface)

CompactRIO 8-Channel, 60 V, High-Speed, Sourcing Digital Output Module


Open example

Module I/O Variables

To use I/O from this module in a VI, drag and drop I/O variables from the **Project Explorer** window to the block diagram of the VI. The I/O variables write Boolean values to the channels.

Module Channels

The NI 9475 has the following channels.

Channel	Description
DO**x**	Digital output channel **x**, where **x** is the number of the channel. For the NI 9475, **x** is 0 to 7.

C Series Module Properties Dialog Box

Use this dialog box to configure the NI 9475. Right-click the NI 9475 in the **Project Explorer** window and select **Properties** to display this dialog box. You can configure the following options.

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module

based on the slot number. You can use this field to give the module a descriptive name.

- **Module Type**—Specifies the type of C Series module. You cannot change this value.
- **Location**—Specifies a slot in the chassis for the C Series module.

Specialty Digital Configuration

You can use the Specialty Digital Configuration page of the **C Series Module Properties** dialog box to configure channels of this module for counter-driven output or pulse-width modulation output.

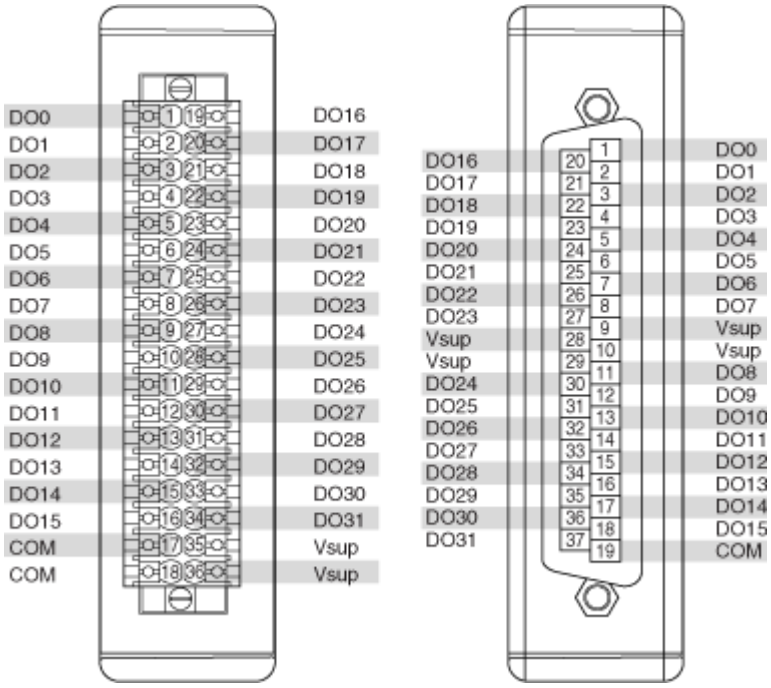
NI 9476

36 V, 32-Channel (Sourcing Output), 500 µs C Series Digital Module

Software Reference (?)

FPGA Interface | Scan Interface

NI 9476 Pinout



NI 9476 (FPGA Interface)

36 V, 32-Channel (Sourcing Output), 500 µs C Series Digital Module

Open example Find related examples

FPGA I/O Node

You can use an FPGA I/O Node, configured for writing, with this device.

Terminals in Software

Use the FPGA I/O Node to access the following terminals for this device.

Terminal	Description
DO**x**	Digital output channel **x**, where **x** is the number of the channel. The NI 9476 has DO channels 0 to 31.
DO7:0	Digital port consisting of channels 0 through 7. Channel 7 is returned in the MSB, and channel 0 is returned in the LSB.
DO15:8	Digital port consisting of channels 8 through 15. Channel 15 is returned in the MSB, and channel 8 is returned in the LSB.
DO23:16	Digital port consisting of channels 16 through 23. Channel 23 is returned in the MSB, and channel 16 is returned in the LSB.
DO31:24	Digital port consisting of channels 24 through 31. Channel 31 is returned in the MSB, and channel 24 is returned in the LSB.
DO31:0	Digital port consisting of channels 0 through 31. Channel 31 is returned in the MSB, and channel 0 is returned in the LSB.

Arbitration

This device supports only the Arbitrate if Multiple Requestors Only and Never Arbitrate options for arbitration. The default arbitration setting is **Arbitrate if Multiple Requestors Only**.

If you are sure that the design of the FPGA VI will never allow more than one digital function to execute at the same time, even on different channels, you can place a checkmark in the **Disable Arbitration** checkbox on the C Series Module Properties dialog box to disable arbitration and reduce the amount of FPGA logic used by VIs. If more than one digital function could execute simultaneously in the FPGA VI, leave the box unchecked.

I/O Methods

This device does not support any I/O methods.

Module Methods

Use the FPGA I/O Method Node to access the following module method for this device.

Method	Description
Check Output Status	Returns Booleans that indicate whether any channel reported an overcurrent fault during the last time the FPGA I/O Node communicated with the module. When the FPGA I/O Node communicates with the module, the FPGA VI samples the states of the channels and overwrites the previous output status with the latest state of the channels. ▪ **Force Status Read**—When the value of this input is FALSE, the method returns the cached status information from the last status read. When the value is TRUE, the method gets the current status information from the module. Forcing a status read can introduce jitter into a digital output loop. ▪ **Any Overcurrent**—Returns a Boolean value. A value of TRUE indicates an overcurrent condition on at least one channel. ▪ **Channel Overcurrent**—Returns an array of Boolean values. A value of TRUE in any index indicates that the channel sharin

	g a number with that index is in an overcu rrent condition.

I/O Properties

This device does not support any I/O properties.

Module Properties

Use the FPGA I/O Property Node to access the following module properties for this device.

Property	Description
Module ID	Returns the module ID.
Serial Number	Returns the unique serial number of the module .
Vendor ID	Returns the NI vendor ID, 0x1093.

Single-Cycle Timed Loop

This device does not support the single-cycle Timed Loop.

C Series Module Properties Dialog Box for the NI 9476/9477 (FPGA Interface)

Right-click an NI 9476 or NI 9477 C Series module in the **Project Explorer** window and select **Properties** from the shortcut menu to display this dialog box.

Use this dialog box to configure a C Series module.

This dialog box includes the following components:

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this option.
- **Location**—Specifies a slot in the chassis for the C Series module.

- **Disable Arbitration**—Place a checkmark in this checkbox if you want to change the arbitration setting to Never Arbitrate and reduce the amount of FPGA logic used by VIs. Check this box only if you are sure that the design of the FPGA VI will never allow more than one digital output function to execute at the same time, even on different channels. If more than one digital output function could execute simultaneously in the FPGA VI, leave the box unchecked to keep the default Arbitrate if Multiple Requestors Only arbitration setting.

NI 9476 (Scan Interface)

36 V, 32-Channel (Sourcing Output), 500 µs C Series Digital Module


Open example

Module I/O Variables

To use I/O from this module in a VI, drag and drop I/O variables from the **Project Explorer** window to the block diagram of the VI. The I/O variables write Boolean values to the channels.

Module Channels

The NI 9476 has the following channels.

Channel	Description
DO**x**	Digital output channel **x**, where **x** is the number of the channel. For the NI 9476, **x** is 0 to 31.

Module-Specific Errors

The NI 9476 can return the following module-specific errors.

Error Code	Description
65548	One or more channels are in overcurrent or over voltage protection mode. Check the terminals fo r any fault condition that could be causing an ou t-of-range voltage or current on the channels.

C Series Module Properties Dialog Box

Use this dialog box to configure the NI 9476. Right-click the NI 9476 in the **Project Explorer** window and select **Properties** to display this dialog box. You can configure the following options.

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this value.
- **Location**—Specifies a slot in the chassis for the C Series module.

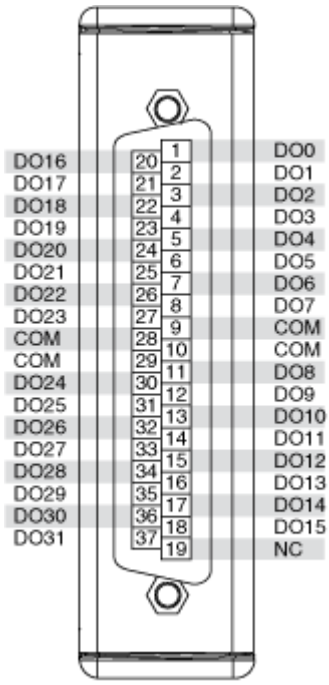
NI 9477

CompactRIO 32-Channel, 5–60 V, Sinking Digital Output Module

Software Reference (?)

FPGA Interface | Scan Interface

NI 9477 Pinout



NI 9477 (FPGA Interface)

CompactRIO 32-Channel, 5–60 V, Sinking Digital Output Module

FPGA I/O Node

You can use an FPGA I/O Node, configured for writing, with this device.

Terminals in Software

Use the FPGA I/O Node to access the following terminals for this device.

Terminal	Description
DO**x**	Digital output channel **x**, where **x** is the number of the channel. The NI 9477 has DO channels 0 t o 31.
DO7:0	Digital port consisting of channels 0 through 7. Channel 7 is returned in the MSB, and channel 0 is returned in the LSB.

DO15:8	Digital port consisting of channels 8 through 15. Channel 15 is returned in the MSB, and channel 8 is returned in the LSB.
DO23:16	Digital port consisting of channels 16 through 23. Channel 23 is returned in the MSB, and channel 16 is returned in the LSB.
DO31:24	Digital port consisting of channels 24 through 31. Channel 31 is returned in the MSB, and channel 24 is returned in the LSB.
DO31:0	Digital port consisting of channels 0 through 31. Channel 31 is returned in the MSB, and channel 0 is returned in the LSB.

Arbitration

This device supports only the Arbitrate if Multiple Requestors Only and Never Arbitrate options for arbitration. The default arbitration setting is **Arbitrate if Multiple Requestors Only**.

If you are sure that the design of the FPGA VI will never allow more than one digital function to execute at the same time, even on different channels, you can place a checkmark in the **Disable Arbitration** checkbox on the C Series Module Properties dialog box to disable arbitration and reduce the amount of FPGA logic used by VIs. If more than one digital function could execute simultaneously in the FPGA VI, leave the box unchecked.

Methods

This device does not support any methods.

I/O Properties

This device does not support any I/O properties.

Module Properties

Use the FPGA I/O Property Node to access the following module properties for this device.

Property	Description
Module ID	Returns the module ID.
Serial Number	Returns the unique serial number of the module .
Vendor ID	Returns the NI vendor ID, 0x1093.

Single-Cycle Timed Loop

This device does not support the single-cycle Timed Loop.

C Series Module Properties Dialog Box for the NI 9476/9477 (FPGA Interface)

Right-click an NI 9476 or NI 9477 C Series module in the **Project Explorer** window and select **Properties** from the shortcut menu to display this dialog box.

Use this dialog box to configure a C Series module.

This dialog box includes the following components:

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this option.
- **Location**—Specifies a slot in the chassis for the C Series module.
- **Disable Arbitration**—Place a checkmark in this checkbox if you want to change the arbitration setting to Never Arbitrate and reduce the amount of FPGA logic used by VIs. Check this box only if you are sure that the design of the FPGA VI will never allow more than one digital output function to execute at the same time, even on different channels. If more than one digital output function could execute simultaneously in the FPGA VI, leave the box unchecked to keep the default Arbitrate if Multiple Requestors Only arbitration setting.

NI 9477 (Scan Interface)

CompactRIO 32-Channel, 5–60 V, Sinking Digital Output Module

Open example

Module I/O Variables

To use I/O from this module in a VI, drag and drop I/O variables from the **Project Explorer** window to the block diagram of the VI. The I/O variables write Boolean values to the channels.

Module Channels

The NI 9477 has the following channels.

Channel	Description
DO**x**	Digital output channel **x**, where **x** is the number of the channel. For the NI 9477, **x** is 0 to 31.

C Series Module Properties Dialog Box

Use this dialog box to configure the NI 9477. Right-click the NI 9477 in the **Project Explorer** window and select **Properties** to display this dialog box. You can configure the following options.

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this value.
- **Location**—Specifies a slot in the chassis for the C Series module.

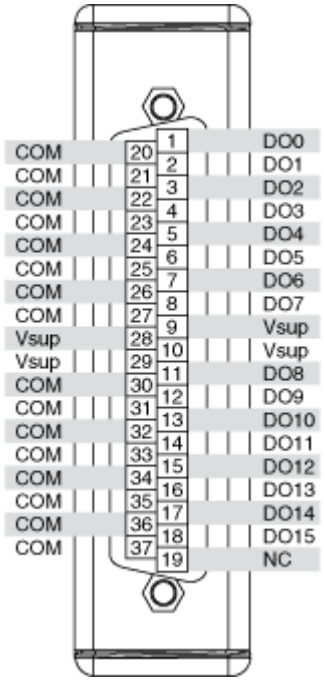
NI 9478

CompactRIO 16-Channel, 0–50 V Sinking Digital Output Module with Programmable Current Limits

Software Reference (?)

FPGA Interface | Scan Interface

NI 9478 Pinout



Related Topics

FPGA Interface
Configuring Current Limits for the NI 9478

NI 9478 (FPGA Interface)

CompactRIO 16-Channel, 0–50 V Sinking Digital Output Module with Programmable Current Limits

Open example Find related examples

FPGA I/O Node

You can use an FPGA I/O Node, configured for writing, with this device.

Terminals in Software

Use the FPGA I/O Node to access the following terminals for this device.

Terminal	Description
DO**x**	Digital output channel **x**, where **x** is the number of the channel. The NI 9478 has DO channels 0 t o 15.
DO7:0	Digital port consisting of channels 0 through 7. Channel 7 is returned in the MSB, and channel 0 is returned in the LSB.
DO15:8	Digital port consisting of channels 8 through 15. Channel 15 is returned in the MSB, and channel 8 is returned in the LSB.
DO15:0	Digital port consisting of channels 0 through 15. Channel 15 is returned in the MSB, and channel 0 is returned in the LSB.

Arbitration

This device supports only the Arbitrate if Multiple Requestors Only option for arbitration. You cannot configure arbitration settings for this device.

I/O Methods

This device does not support any I/O methods.

Module Methods

Use the FPGA I/O Method Node to access the following module method for this device.

Method	Description
Check Output Status	Returns Booleans that indicate whether the mo dule reported an overtemp fault or any channel reported an overcurrent fault during the last tim e the FPGA I/O Node communicated with the m odule. When the FPGA I/O Node communicates with the module, the FPGA VI samples the states of the module and channels and overwrites the

	previous output status with the latest state of the module and channels. ▪ **Limit Selection**—Specifies which current limit status information the module reads. Select **Active Limit** if you want the **Channel Overcurrent** output to return TRUE for any channels that exceed the current limit threshold specified for the active current limit for that channel. Select **Limit A** to return TRUE for any channels that exceed the current limit threshold specified for Current Limit A. Select **Limit B** to return TRUE for any channels that exceed the current limit threshold specified for Current Limit B. ▪ **Module Overtemp**—Returns a Boolean value. A value of TRUE indicates that the module exceeded its temperature rating. ▪ **Channel Overcurrent**—Returns an array of Boolean values. A value of TRUE in any index indicates that the channel sharing a number with that index exceeded the current limit, as specified by the **Limit Selection** input, after the last status read. A value of FALSE indicates that the channel did not exceed the current limit after the last status read.

I/O Properties

This device does not support any I/O properties.

Module Properties

Use the FPGA I/O Property Node to access the following module properties for this device.

Property	Description

Active Current Limit	Sets the active current limit for each channel. The value in an index of the input array controls the active current limit for the channel sharing a number with that index. Select **No Change** if you do not want to modify the active current limit for the channel at run time. Select **Limit A** if you want to set the active current limit for the channel to Current Limit A. Select **Limit B** if you want to set the active current limit for the channel to Current Limit B. Select **No Limit** if you want the channel to have no current limit.
Current Limit A	Sets the current limit threshold for Current Limit A in binary values. You can use the following equation to calculate the binary value from amperes: **Binary Value** = (**Current Value** / 5.12 A) × 256 The range of valid current limit values is 0–5.1 A, which corresponds to binary values 0–255.
Current Limit B	Sets the current limit threshold for Current Limit B in binary values. You can use the following equation to calculate the binary value from amperes: **Binary Value** = (**Current Value** / 5.12 A) × 256 The range of valid current limit values is 0–5.1 A, which corresponds to binary values 0–255.
Module ID	Returns the module ID.
Overcurrent Refresh Period	Sets the time in µs it takes a channel to automatically recover if the channel exceeds its active current limit threshold. Values 2–255 enable overcurrent refresh and specify the time in tens of µs. For example, a value of 3 sets an overcurrent refresh period of 30 µs. A value of 0 disables overcurrent refresh so the channel remains disabled after exceeding its active current limit until you write to the channel using an FPGA I/O Node. A value of 1 is not supported and sets an overcurrent refresh period of 20 µs.
Serial Number	Returns the unique serial number of the module.
Vendor ID	Returns the NI vendor ID, 0x1093.

Single-Cycle Timed Loop

This device does not support the single-cycle Timed Loop.

C Series Module Properties Dialog Box for the NI 9478 (FPGA Interface)

Right-click an NI 9478 C Series module in the **Project Explorer** window and select **Properties** from the shortcut menu to display this dialog box.

Use this dialog box to configure a C Series module.

This dialog box includes the following components:

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this option.
- **Location**—Specifies a slot in the chassis for the C Series module.
- **Channels**—Specifies the channel(s) for which you want to select the active current limit.
- **Selected Channel(s) Settings**—Specifies the active current limit for each channel.
  - **Active Limit**—Sets the active current limit for the selected channel(s). Select **Limit A** if you want to set the active current limit for the channel(s) to Current Limit A. Select **Limit B** if you want to set the active current limit for the channel(s) to Current Limit B. Select **No Limit** if you want the channel(s) to have no current limit.
- **Module Settings**—Specifies the current limit threshold settings for the module.
  - **Current Limit A**—Sets the current limit threshold for Current Limit A in amperes. Valid values are 0–5.1 A.

- **Current Limit B**—Sets the current limit threshold for Current Limit B in amperes. Valid values are 0–5.1 A.
- **Enable Overcurrent Refresh**—Place a checkmark in this checkbox if you want to enable a channel to automatically recover if the channel exceeds its active current limit threshold. If overcurrent refresh is disabled, the channel remains off after an overcurrent condition until you write to the channel using an FPGA I/O Node.
- **Overcurrent Refresh Period**—Sets the time in µs it takes a channel to automatically recover if the channel exceeds its active current limit threshold. Valid values are 20–2550 µs. This option is available only if you select **Enable Overcurrent Refresh**.

Configuring Current Limits for the NI 9478 (FPGA Interface)

You can configure the active current limit for each channel and the current limit thresholds at edit time using the C Series Module Properties dialog box. You can programmatically change these settings at run time using the FPGA I/O Property Node. The execution of an I/O Property Node that is configured with a **Current Limit** property overwrites the value you configured in the **C Series Module Properties** dialog box.

Configuring Current Limits Using the C Series Module Properties Dialog Box

Complete the following steps to configure the active current limit for each channel and the current limit thresholds for the NI 9478 using the **C Series Module Properties** dialog box.

1. Configure the CompactRIO system, and add an NI 9478.
2. Right-click the NI 9478 in the **Project Explorer** window and select **Properties** from the shortcut menu to display the **C Series Module Properties** dialog box.
3. Select the channel(s) for which you want to configure the active current limit from the **Channels** table. You can select more than one channel by holding the <Ctrl> or <Shift> key when selecting channels.

4. Select the active current limit for the channel(s) from the **Active Limit** pull-down menu.
5. Enter a value between 0 and 5.1 in the **Current Limit** text box that corresponds to the active current limit for the selected channel(s).
6. Place a checkmark in the **Enable Overcurrent Refresh** checkbox and set the time in the **Overcurrent Refresh Period** text box if you want to enable a channel to automatically recover if the channel exceeds its active current limit threshold.
7. Click the **OK** button.
8. Select **File»Save All** in the **Project Explorer** window.

Configuring Current Limits Using the FPGA I/O Property Node

Complete the following steps to configure the active current limit for each channel and the current limit thresholds using the FPGA I/O Property Node.

1. Place three FPGA I/O Property Nodes on the block diagram and configure them for the NI 9478.
2. Click the **Property** section on the first Property Node and select the **Active Current Limit** property from the shortcut menu.
3. Right-click the **Active Current Limit** input and select **Create»Control** from the shortcut menu.
4. On the front panel of the VI, select the active current limit for each channel from the **Active Current Limit** array.
5. Click the **Property** section on the second Property Node and select the **Current Limit A** property from the shortcut menu.
6. Right-click the **Current Limit A** input and select **Create»Control** from the shortcut menu.
7. Click the **Property** section on the third Property Node and select the **Current Limit B** property from the shortcut menu.
8. Right-click the **Current Limit B** input and select **Create»Control** from the shortcut menu.

9. On the front panel of the VI, enter binary values in the **Current Limit** controls to set the current limit thresholds. You can use the following equation in the host VI to calculate the binary value from amperes:
Binary Value = (**Current Value** / 5.12 A) × 256

NI 9478 (Scan Interface)

CompactRIO 16-Channel, 0–50 V Sinking Digital Output Module with Programmable Current Limits


Open example

Module I/O Variables

To use I/O from this module in a VI, drag and drop I/O variables from the **Project Explorer** window to the block diagram of the VI. The I/O variables write Boolean values to the channels.

Module Channels

The NI 9478 has the following channels.

Channel	Description
DO**x**	Digital output channel **x**, where **x** is the number of the channel. For the NI 9478, **x** is 0 to 15.

Module-Specific Errors

The NI 9478 can return the following module-specific errors.

Error Code	Description
65548	One or more channels are in overcurrent or over voltage protection mode. Check the terminals for any fault condition that could be causing an out-of-range voltage or current on the channels.
65571	Serial module over-temperature error: An over-temperature error has occurred since the last time the module was accessed. Check for fault conditions or extraneous voltages on the I/O port.

C Series Module Properties Dialog Box

Use this dialog box to configure the NI 9478. Right-click the NI 9478 in the **Project Explorer** window and select **Properties** to display this dialog box. You can configure the following options.

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this value.
- **Location**—Specifies a slot in the chassis for the C Series module.
- **Channels**—Specifies the channels for which you want to configure an active current limit.
- **Active Limit**—Specifies the current limit for the selected channel(s). You can select **Limit A**, **Limit B**, or **No Limit**.
- **Current Limit A**—Specifies one of two current limit values in amps for channels on the module. You can enter a value from 0 to 5.1.
- **Current Limit B**—Specifies one of two current limit values in amps for channels on the module. You can enter a value from 0 to 5.1.
- **Enable Overcurrent Refresh**—If you check this box, a channel that exceeds the current limit automatically recovers after a specified amount of time, the overcurrent refresh period. If you leave this box unchecked, a channel that exceeds the current limit remains disabled until you write to it.
- **Overcurrent Refresh Period**—Specifies the time in µs it takes a channel to automatically recover after exceeding the current limit. You can enter a value from 20 to 2,550.

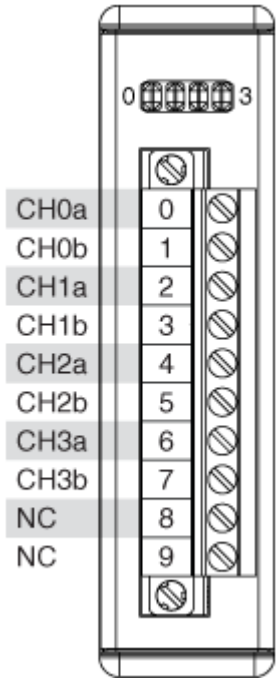
NI 9481

CompactRIO 4-Channel, Form A Electromechanical Relay Module

Software Reference (?)

FPGA Interface | Scan Interface

NI 9481 Pinout



NI 9481 (FPGA Interface)

CompactRIO 4-Channel, Form A Electromechanical Relay Module

FPGA I/O Node

You can use an FPGA I/O Node, configured for writing, with this device.

Terminals in Software

Use the FPGA I/O Node to access the following terminals for this device.

Terminal	Description
CH**x**	channel **x**, where **x** is the number of the channel . The NI 9481 has channels 0 to 3.

CH3:0	Digital port consisting of channels 0 through 3. Channel 3 is returned in bit 3, and channel 0 is r eturned in bit 0.

Arbitration

You can configure the arbitration settings for the channels of this device in the Advanced Code Generation page of the FPGA I/O Properties dialog box. The default arbitration setting is Never Arbitrate.

I/O Methods

This device does not support any I/O methods.

Module Methods

Use the FPGA I/O Method Node to access the following module method for this device.

Method	Description
Check Status	Returns a Boolean value that indicates whether the module is ready.  **Note** During the first 2 seconds after you reset the FPGA VI, the error t erminals on this metho d may not correctly rep ort certain types of err ors.

I/O Properties

This device does not support any I/O properties.

Module Properties

Use the FPGA I/O Property Node to access the following module properties for this device.

Property	Description
Module ID	Returns the module ID.
Serial Number	Returns the unique serial number of the module .
Vendor ID	Returns the NI vendor ID, 0x1093.

Single-Cycle Timed Loop

This device supports the single-cycle Timed Loop. Configure the number of output synchronizing registers for the channels of this device in the Advanced Configuration dialog box.

When the module is within a single-cycle Timed Loop, it must be ready to perform digital output before a loop containing digital output starts. Poll the **Ready** output of the Check Status method to determine whether the module is ready. The module might ignore or delay digital output operations if it is not ready.

While the module is performing digital output within a single-cycle Timed Loop, do not perform property reads or remove the module from the chassis. Doing either of these actions causes the module to be unable to perform digital output and the **Ready** output of the Check Status method to return FALSE.

FPGA Target Clock Support

This device supports only top-level FPGA target clock rates and single-cycle Timed Loop clock rates that are multiples of 40 MHz, such as 40 MHz, 80 MHz, 120 MHz, and so on.

C Series Module Properties Dialog Box for the NI 9472/9474/9475/9481/9482/9485 (FPGA Interface)

Right-click an NI 9472, NI 9474, NI 9475, NI 9481, NI 9482, or NI 9485 C Series module in the **Project Explorer** window and select **Properties** from the shortcut menu to display this dialog box.

Use this dialog box to configure a C Series module.

This dialog box includes the following components:

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this option.
- **Location**—Specifies a slot in the chassis for the C Series module.
- **Advanced**—Launches the Advanced Configuration dialog box.

NI 9481 (Scan Interface)

CompactRIO 4-Channel, Form A Electromechanical Relay Module


Open example

Module I/O Variables

To use I/O from this module in a VI, drag and drop I/O variables from the **Project Explorer** window to the block diagram of the VI. The I/O variables write Boolean values to the channels.

Module Channels

The NI 9481 has the following channels.

Channel	Description
DO**x**	Digital output channel **x**, where **x** is the number of the channel. For the NI 9481, **x** is 0 to 3.

C Series Module Properties Dialog Box

Use this dialog box to configure the NI 9481. Right-click the NI 9481 in the **Project Explorer** window and select **Properties** to display this dialog box. You can configure the following options.

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module

based on the slot number. You can use this field to give the module a descriptive name.

- **Module Type**—Specifies the type of C Series module. You cannot change this value.
- **Location**—Specifies a slot in the chassis for the C Series module.

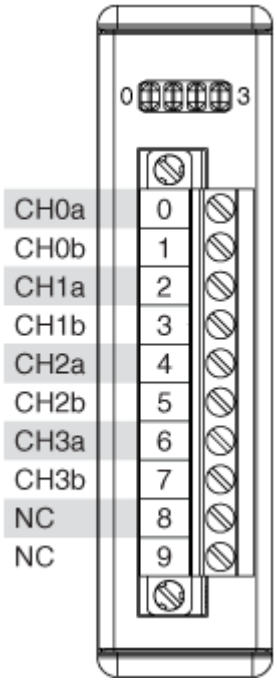
NI 9482

CompactRIO 4-Channel, Form A Electromechanical Relay Module

Software Reference (?)

FPGA Interface | Scan Interface

NI 9482 Pinout



NI 9482 (FPGA Interface)

CompactRIO 4-Channel, Form A Electromechanical Relay Module

FPGA I/O Node

You can use an FPGA I/O Node, configured for writing, with this device.

Terminals in Software

Use the FPGA I/O Node to access the following terminals for this device.

Terminal	Description
CH**x**	channel **x**, where **x** is the number of the channel . The NI 9482 has channels 0 to 3.
CH3:0	Digital port consisting of channels 0 through 3. Channel 3 is returned in bit 3, and channel 0 is r eturned in bit 0.

Arbitration

You can configure the arbitration settings for the channels of this device in the Advanced Code Generation page of the FPGA I/O Properties dialog box. The default arbitration setting is Never Arbitrate.

I/O Methods

This device does not support any I/O methods.

Module Methods

Use the FPGA I/O Method Node to access the following module method for this device.

Method	Description
Check Status	Returns a Boolean value that indicates whether the module is ready. **Note** During the first 2 seconds after you reset the FPGA VI, the error t erminals on this metho d may not correctly rep

	ort certain types of err ors.

I/O Properties

This device does not support any I/O properties.

Module Properties

Use the FPGA I/O Property Node to access the following module properties for this device.

Property	Description
Module ID	Returns the module ID.
Serial Number	Returns the unique serial number of the module .
Vendor ID	Returns the NI vendor ID, 0x1093.

Single-Cycle Timed Loop

This device supports the single-cycle Timed Loop. Configure the number of output synchronizing registers for the channels of this device in the Advanced Configuration dialog box.

When the module is within a single-cycle Timed Loop, it must be ready to perform digital output before a loop containing digital output starts. Poll the **Ready** output of the Check Status method to determine whether the module is ready. The module might ignore or delay digital output operations if it is not ready.

While the module is performing digital output within a single-cycle Timed Loop, do not perform property reads or remove the module from the chassis. Doing either of these actions causes the module to be unable to perform digital output and the **Ready** output of the Check Status method to return FALSE.

FPGA Target Clock Support

This device supports only top-level FPGA target clock rates and single-cycle Timed Loop clock rates that are multiples of 40 MHz, such as 40 MHz, 80 MHz, 120 MHz, and so on.

C Series Module Properties Dialog Box for the NI 9472/9474/9475/9481/9482/9485 (FPGA Interface)

Right-click an NI 9472, NI 9474, NI 9475, NI 9481, NI 9482, or NI 9485 C Series module in the **Project Explorer** window and select **Properties** from the shortcut menu to display this dialog box.

Use this dialog box to configure a C Series module.

This dialog box includes the following components:

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this option.
- **Location**—Specifies a slot in the chassis for the C Series module.
- **Advanced**—Launches the Advanced Configuration dialog box.

NI 9482 (Scan Interface)

CompactRIO 4-Channel, Form A Electromechanical Relay Module


Open example

Module I/O Variables

To use I/O from this module in a VI, drag and drop I/O variables from the **Project Explorer** window to the block diagram of the VI. The I/O variables write Boolean values to the channels.

Module Channels

The NI 9482 has the following channels.

Channel	Description
DO**x**	Digital output channel **x**, where **x** is the number of the channel. For the NI 9482, **x** is 0 to 3.

C Series Module Properties Dialog Box

Use this dialog box to configure the NI 9482. Right-click the NI 9482 in the **Project Explorer** window and select **Properties** to display this dialog box. You can configure the following options.

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this value.
- **Location**—Specifies a slot in the chassis for the C Series module.

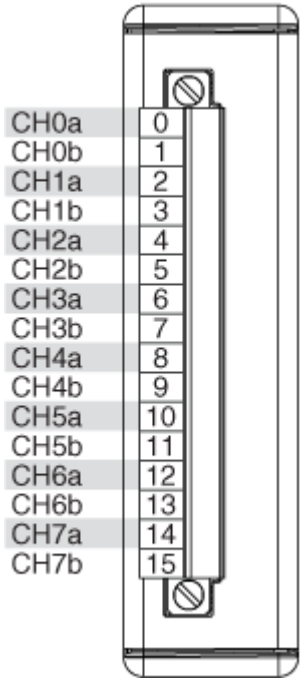
NI 9485

CompactRIO 8-Channel, Solid-State Relay (SSR) Module

Software Reference (?)

FPGA Interface | Scan Interface

NI 9485 Pinout



NI 9485 (FPGA Interface)

CompactRIO 8-Channel, Solid-State Relay (SSR) Module

FPGA I/O Node

You can use an FPGA I/O Node, configured for writing, with this device.

Terminals in Software

Use the FPGA I/O Node to access the following terminals for this device.

Terminal	Description
CH**x**	channel **x**, where **x** is the number of the channel . The NI 9485 has channels 0 to 7.
CH7:0	Digital port consisting of channels 0 through 7. Channel 7 is returned in the MSB, and channel 0 is returned in the LSB.

Arbitration

You can configure the arbitration settings for the channels of this device in the Advanced Code Generation page of the FPGA I/O Properties dialog box. The default arbitration setting is Never Arbitrate.

I/O Methods

This device does not support any I/O methods.

Module Methods

Use the FPGA I/O Method Node to access the following module method for this device.

Method	Description
Check Status	Returns a Boolean value that indicates whether the module is ready. **Note** During the first 2 seconds after you reset the FPGA VI, the error terminals on this method may not correctly report certain types of errors.

I/O Properties

This device does not support any I/O properties.

Module Properties

Use the FPGA I/O Property Node to access the following module properties for this device.

Property	Description
Module ID	Returns the module ID.

Serial Number	Returns the unique serial number of the module .
Vendor ID	Returns the NI vendor ID, 0x1093.

Single-Cycle Timed Loop

This device supports the single-cycle Timed Loop. Configure the number of output synchronizing registers for the channels of this device in the Advanced Configuration dialog box.

When the module is within a single-cycle Timed Loop, it must be ready to perform digital output before a loop containing digital output starts. Poll the **Ready** output of the Check Status method to determine whether the module is ready. The module might ignore or delay digital output operations if it is not ready.

While the module is performing digital output within a single-cycle Timed Loop, do not perform property reads or remove the module from the chassis. Doing either of these actions causes the module to be unable to perform digital output and the **Ready** output of the Check Status method to return FALSE.

FPGA Target Clock Support

This device supports only top-level FPGA target clock rates and single-cycle Timed Loop clock rates that are multiples of 40 MHz, such as 40 MHz, 80 MHz, 120 MHz, and so on.

C Series Module Properties Dialog Box for the NI 9472/9474/9475/9481/9482/9485 (FPGA Interface)

Right-click an NI 9472, NI 9474, NI 9475, NI 9481, NI 9482, or NI 9485 C Series module in the **Project Explorer** window and select **Properties** from the shortcut menu to display this dialog box.

Use this dialog box to configure a C Series module.

This dialog box includes the following components:

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module

based on the slot number. You can use this field to give the module a descriptive name.

- **Module Type**—Specifies the type of C Series module. You cannot change this option.
- **Location**—Specifies a slot in the chassis for the C Series module.
- **Advanced**—Launches the Advanced Configuration dialog box.

NI 9485 (Scan Interface)

CompactRIO 8-Channel, Solid-State Relay (SSR) Module

 Open example

Module I/O Variables

To use I/O from this module in a VI, drag and drop I/O variables from the **Project Explorer** window to the block diagram of the VI. The I/O variables write Boolean values to the channels.

Module Channels

The NI 9485 has the following channels.

Channel	Description
DO**x**	Digital output channel **x**, where **x** is the number of the channel. For the NI 9485, **x** is 0 to 7.

C Series Module Properties Dialog Box

Use this dialog box to configure the NI 9485. Right-click the NI 9485 in the **Project Explorer** window and select **Properties** to display this dialog box. You can configure the following options.

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.

- **Module Type**—Specifies the type of C Series module. You cannot change this value.
- **Location**—Specifies a slot in the chassis for the C Series module.

Functional Safety Modules

Use this book as a reference for the following information:

- I/O variables and properties each C Series functional safety module supports in Scan Interface mode.
- Instructions for using LabVIEW with CompactRIO functional safety devices

To view related topics, click the **Locate** button, shown at left, in the toolbar at the top of this window. The **LabVIEW Help** highlights this topic in the **Contents** tab so you can navigate the related topics.

NI 9350

8-Channel 24 V Sinking DI, 8-Channel 24 V Sourcing DO SIL 3 Capable C Series Functional Safety Module

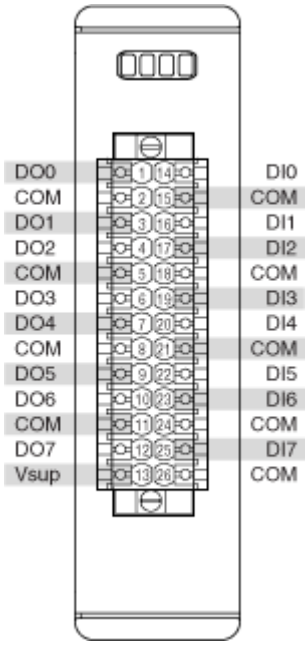
Software Reference (?)

Scan Interface

C Series Functional Safety Manual (?)

C Series Functional Safety Manual

NI 9350 Pinout



NI 9350 (Scan Interface)

8-Channel 24 V Sinking DI, 8-Channel 24 V Sourcing DO SIL 3 Capable C Series Functional Safety Module

Module I/O Variables

To use I/O from this module in a VI, drag and drop I/O variables from the **Project Explorer** window to the block diagram of the VI.

- **Digital input**—reads the Boolean state of that channel.
- **Digital output**—reads the Boolean state of that channel. When the User Program sets the channel to passthrough, the User Program will use the value in the output scan buffer. When the channel is not set to passthroughin the User Program, the User Program ignores the value in the output scan buffer.
- **State machine variable**—reads the Boolean value of that variable in the User Program.
- **User LED0**—reads the Boolean value of the LED in the User Program.

Module Channels

The NI 9350 has the following channels.

Channel	Description
DI**x**	Digital input channel **x**, where **x** is the number o f the channel. For the NI 9350, **x** is 0 to 7.
DO**x**	Digital output channel **x**, where **x** is the number of the channel. For the NI 9350, **x** is 0 to 7.
Var**x**	State machine variable **x**, where **x** is the number of the variable. For the NI 9350, **x** is 0 to 23.
User LED0	User-configurable LED

C Series Module Properties Dialog Box

Use this dialog box to configure the NI 9350. Right-click the NI 9350 in the **Project Explorer** window and select **Properties** to display this dialog box. You can configure the following options.

- **Name**—Indicates the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Indicates the type of C Series module. You cannot change this value.
- **Location**—Indicates a slot in the chassis for the C Series module.
- **Read Module Information**—Reads the Build Number and Program GUID of the current User Program installed on the C Series module.
- **Build Number**—Indicates the build number of the current User Program installed on the C Series module.
- **Program GUID**—Indicates the program GUID of the current User Program installed on the C Series module.
- **Mode**—Indicates the current operating mode of the C Series module.
  - Power Up—Indicates module is powering up.

- Unprogrammed—Indicates User Program is not written to the C Series module.
- User Program Download—Indicates the User Program is downloading to the C Series module.
- Module Firmware Download—Indicates firmware is downloading to the C Series module.
- Verification—Indicates User Program has successfully downloaded. Requires user verification.
- Operational—Indicates C Series module is running the User Program.
- Reserved—Indicates C Series module is in Reserved mode.
- Fail-safe—Indicates User Program has detected a fault that triggered Fail-safe mode. User must address fault and cycle power to return the C Series module to Operational mode.

- **Change Mode to X**—Updates C Series module from Verification mode to Operational mode or from Operational mode to Verification mode.
- **Path to New User Program**—Specifies the file path of the User Program selected for download.
- **Build Number**—Indicates the build number of the User Program selected for download.
- **Program GUID in New Program**—Indicates the program GUID of the User Program selected for download.
- **Download**—Downloads the selected User Program to the C Series module.

Module Methods

Use the Invoke Node to access the following module properties for this device.

Method	Description
Check Channel Status	Returns Boolean arrays that indicate the channel status, including various faults. The index number in the array corresponds to the channel number on the module, so that index 0 indicates the channel status for DI0 or DO0.

	The following parameters are available: ▪ DO Internal Readback—Indicates whether the DO signal is high or low. ▪ DO Channel Overcurrent Fault—Indicates an overcurrent fault has been detected. ▪ DO Channel Open Circuit Fault—Indicates an open circuit fault has been detected. ▪ DI Channel Discrepancy Fault—Indicates a discrepancy fault has been detected. ▪ Channel Test Pulse Fault—Indicates a test pulse fault has been detected. ▪ Channel Readback Fault—Indicates a readback fault has been detected.
Check Module Status	Returns the module status, including digital output values and various faults. The following parameters are available: ▪ Mode—Returns an enum value that reads the operating mode of the NI 9350. ▪ Power Up—Indicates module is powering up. ▪ Unprogrammed—Indicates User Program is not written to the C Series module. ▪ User Program Download—Indicates the User Program is downloading to the C Series module. ▪ Module Firmware Download—Indicates firmware is downloading to the C Series module. ▪ Verification—Indicates User Program has successfully downloaded. Requires user verification. ▪ Operational—Indicates C Series module is running the User Program.

	▪ Reserved—Indicates C Series module is in Reserved mode. ▪ Fail-safe—Indicates User Program has detected a fault that triggered Fail-safe mode. User must address fault and cycle power to return the C Series module to Operational mode. ▪ User Program Running—Returns Boolean value to indicate the status of the User Program. ▪ Internal Fault—Returns Boolean value to indicate whether an internal fault has been detected. ▪ Temperature Fault—Returns Boolean value to indicate whether a temperature fault has been detected. ▪ Power Supply Fault—Returns Boolean value to indicate whether a power supply fault has been detected.
Start Program	Starts the User Program.
Set Mode	Sets the operating mode for the NI 9350 as an enum value. Valid values are Operational or Verification.
Read Current State	Returns an array of U8 values. The array index corresponds to the state machine number in the User Program and the U8 value indicates the current state of that state machine. Refer to the report.log file generated by the Functional Safety Editor to index the state machines and identify the state number.

Module Properties

Use the Property Node to access the following module properties for this device.

Property	Description
Firmware Version Number	Returns U32 value to indicate the version of the module firmware.

User Program GUID	Returns a string to indicate the GUID assigned to the User Program.
User Program Version Number	Returns U32 value to indicate the build number of the User Program.

NI 9351

4-Channel 0-20 mA 16-bit AI, 4-Channel 24 V Sinking DI, 4-Channel 24 V Sourcing DO SIL 3 Capable C Series Functional Safety Module

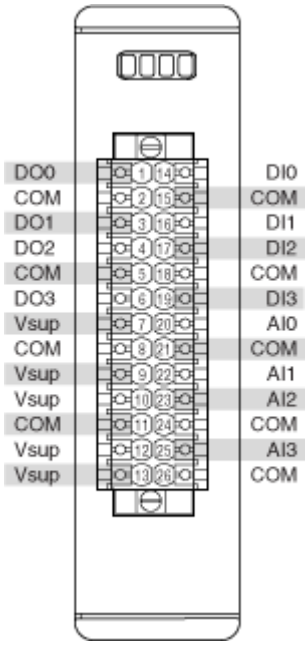
Software Reference (?)

Scan Interface

C Series Functional Safety Manual (?)

C Series Functional Safety Manual

NI 9351 Pinout



NI 9351 (Scan Interface)

4-Channel 0-20 mA 16-bit AI, 4-Channel 24 V Sinking DI, 4-Channel 24 V Sourcing DO SIL 3 Capable C Series Functional Safety Module

Module I/O Variables

To use I/O from this module in a VI, drag and drop I/O variables from the **Project Explorer** window to the block diagram of the VI.

- **Analog input**—reads the analog signal of that channel.
- **Digital input**—reads the Boolean state of that channel.
- **Digital output**—reads the Boolean state of that channel. Writes a Boolean value to the output scan buffer. When the channel is set to passthrough in the User Program, the User Program will use the value in the output scan buffer. When the channel is not set to passthrough in the User Program, the User Program ignores the value in the output scan buffer.
- **State machine variable**—reads the Boolean value of that variable in the User Program.
- **User LED0**—reads the Boolean value of the LED set by the User Program.

Module Channels

The NI 9351 has the following channels.

Channel	Description
AI**x**	Analog input channel **x**, where **x** is the number of the channel. For the NI 9351, **x** is 0 to 3.
DI**x**	Digital input channel **x**, where **x** is the number o f the channel. For the NI 9351, **x** is 0 to 3.
DO**x**	Digital output channel **x**, where **x** is the number of the channel. For the NI 9351, **x** is 0 to 3.
Var**x**	State machine variable **x**, where **x** is the number of the variable. For the NI 9351, **x** is 0 to 23.
User LED0	User-configurable LED

C Series Module Properties Dialog Box

Use this dialog box to configure the NI 9351. Right-click the NI 9351 in the **Project Explorer** window and select **Properties** to display this dialog box. You can configure the following options.

- **Name**—Indicates the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Indicates the type of C Series module. You cannot change this value.
- **Location**—Indicates a slot in the chassis for the C Series module.
- **Read Module Information**—Reads the Build Number and Program GUID of the current User Program installed on the C Series module.
- **Build Number**—Indicates the build number of the current User Program installed on the C Series module.
- **Program GUID**—Indicates the program GUID of the current User Program installed on the C Series module.
- **Mode**—Indicates the current operating mode of the C Series module.
  - Power Up—Indicates module is powering up.
  - Unprogrammed—Indicates User Program is not written to the C Series module.
  - User Program Download—Indicates the User Program is downloading to the C Series module.
  - Module Firmware Download—Indicates firmware is downloading to the C Series module.
  - Verification—Indicates User Program has successfully downloaded. Requires user verification.
  - Operational—Indicates C Series module is running the User Program.
  - Reserved—Indicates C Series module is in Reserved mode.

- Fail-safe—Indicates User Program has detected a fault that triggered Fail-safe mode. User must address fault and cycle power to return the C Series module to Operational mode.

- **Change Mode to X**—Updates C Series module from Verification mode to Operational mode or from Operational mode to Verification mode.
- **Path to New User Program**—Specifies the file path of the User Program selected for download.
- **Build Number**—Indicates the build number of the User Program selected for download.
- **Program GUID in New Program**—Indicates the program GUID of the User Program selected for download.
- **Download**—Downloads the selected User Program to the C Series module.

Module Methods

Use the Invoke Node to access the following module properties for this device.

Method	Description
Check Channel Status	Returns Boolean arrays that indicate the channel status, including various faults. The index number in the array corresponds to the channel number on the module, so that index 0 indicates the channel status for DI0, DO0, or AI0. The following parameters are available: ▪ DO Internal Readback—Indicates whether the DO signal is high or low. ▪ DO Channel Overcurrent Fault—Indicates an overcurrent fault has been detected. ▪ DO Channel Open Circuit Fault—Indicates an open circuit fault has been detected. ▪ DI Channel Discrepancy Fault—Indicates a discrepancy fault has been detected. ▪ Channel Test Pulse Fault—Indicates a test pulse fault has been detected.

	▪ Channel Readback Fault—Indicates a readback fault has been detected. ▪ AI Discrepancy Fault—Indicates a discrepancy fault has been detected. ▪ AI Overcurrent Fault—Indicates a overcurrent fault has been detected. ▪ AI Discrepancy Warning—Indicates which AI channel in a 2oo3 configuration is out of discrepancy range.
Check Module Status	Returns the module status, including digital output values and various faults. The following parameters are available: ▪ Mode—Returns an enum value that reads the operating mode of the NI 9351. ▪ Power Up—Indicates module is powering up. ▪ Unprogrammed—Indicates User Program is not written to the C Series module. ▪ User Program Download—Indicates the User Program is downloading to the C Series module. ▪ Module Firmware Download—Indicates firmware is downloading to the C Series module. ▪ Verification—Indicates User Program has successfully downloaded. Requires user verification. ▪ Operational—Indicates C Series module is running the User Program. ▪ Reserved—Indicates C Series module is in Reserved mode. ▪ Fail-safe—Indicates User Program has detected a fault that triggered Fail-safe mode. User must address fault and cy

	cle power to return the C Series module to Operational mode. ▪ User Program Running—Returns Boole an value to indicate the status of the User Program. ▪ Internal Fault—Returns Boolean value t o indicate whether an internal fault has be en detected. ▪ Temperature Fault—Returns Boolean v alue to indicate whether a temperature fa ult has been detected. ▪ Power Supply Fault—Returns Boolean value to indicate whether a power supply fault has been detected.
Start Program	Starts the User Program.
Set Mode	Sets the operating mode for the NI 9351 as an e num value. Valid values are Operational or Verifi cation.
Read Current State	Returns an array of U8 values. The array index c orresponds to the state machine number in the User Program and the U8 value indicates the cur rent state of that state machine. Refer to the rep ort.log file generated by the Functional Safety E ditor to index the state machines and identify th e state number.

Module Properties

Use the Property Node to access the following module properties for this device.

Property	Description
Firmware Version Number	Returns U32 value to indicate the version of the module firmware.
User Program GUID	Returns a string to indicate the GUID assigned to the User Program.
User Program Version Number	Returns U32 value to indicate the build number of the User Program.

Modular Instruments Modules

Use this book as a reference for information about which FPGA I/O functions, I/O resources, arbitration options, methods, and properties each C Series modular instruments module supports in FPGA Programming mode.

To view related topics, click the **Locate** button, shown at left, in the toolbar at the top of this window. The **LabVIEW Help** highlights this topic in the **Contents** tab so you can navigate the related topics.

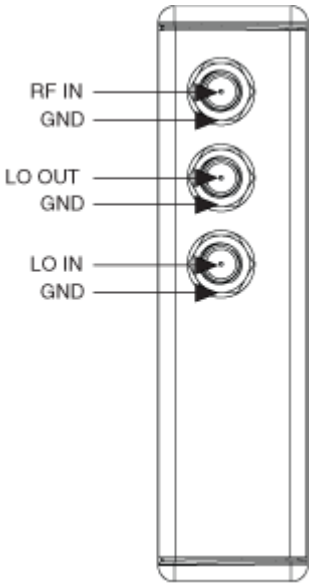
NI 9770

CompactRIO 30 kHz to 100 MHz, 50 Ω, AC Coupled RF Receiver Module

Software Reference (?)

FPGA Interface

NI 9770 Pinout



Related Topics

FPGA Interface
Acquiring Data from a Module (FPGA Interface)
Configuring the Master Timebase Source for a Module (FPGA Interface)
Configuring the Data Rate for a Module (FPGA Interface)
Synchronizing Multiple NI 9770 Modules
Understanding Loop Timing (FPGA Interface)

NI 9770 (FPGA Interface)

30 kHz to 100 MHz, 50 Ω, AC Coupled RF Receiver Module

Open example Find related examples

FPGA I/O Node

You can use an FPGA I/O Node, configured for reading, with this device.

Terminals in Software

Use the FPGA I/O Node to access the following terminals for this device.

Terminal	Description
RF In/I	Returns the I data that comes from the RF IN connector. The I and Q data from each module must be accessed from within the same FPGA I/O Node. Do not access I and Q data on multiple modules in the same FPGA I/O Node if the modules are not synchronized or do not use the same data rate.
RF In/Q	Returns the Q data that comes from the RF IN connector. The I and Q data from each module must be accessed from within the same FPGA I/O Node. Do not access I and Q data on multiple modules in the same FPGA I/O Node if the modules are not synchronized or do not use the same data rate.

Onboard Clock	Provides access to the onboard clock in LabVIEW. The onboard clock frequency is 12.288 MHz. Use the FPGA I/O Node in a single-cycle Timed Loop to access this channel. You must export the **Onboard Clock** of the module to access this channel.
Start	Channel that controls when the module starts acquiring IQ data. If you write TRUE to the **Start** channel, the module starts acquiring data. When the module is acquiring data, you must write TRUE to the **Stop** channel before you can access properties for this module. If you write FALSE to the **Start** channel, no operation is performed. Refer to the NI 9770 Getting Started VI in the `labview\examples\CompactRIO\Module Specific\NI 9770\NI 9770 Getting Started\NI 9770 Getting Started.lvproj` directory for an example of using the **Start** and **Stop** channels.
Stop	Channel that controls when the module stops acquiring data. If you write TRUE to the **Stop** channel, the module stops acquiring data. When the module is acquiring data, you must write TRUE to the **Stop** channel before you can access properties for the module. If you write FALSE to the **Stop** channel, no operation is performed. Refer to the NI 9770 Getting Started VI in the `labview\examples\CompactRIO\Module Specific\NI 9770\NI 9770 Getting Started\NI 9770 Getting Started.lvproj` directory for an example of using the **Start** and **Stop** channels.

Arbitration

This device supports only the Arbitrate if Multiple Requestors Only option for arbitration. You cannot configure arbitration settings for this device.

I/O Methods

This device does not support any I/O methods.

Module Methods

Use the FPGA I/O Method Node to access the following module methods for this device.

Method	Description
Configure RF In	Configures the RF center frequency of the module and input signal reference level. ▪ **Center Frequency**—Specifies in Hz the desired RF center frequency that the module should tune to. ▪ **Reference Level**—Specifies in dBm the expected total power of the RF input signal. ▪ **LO Source**—Optional parameter that specifies the source of the LO signal that the module uses for RF downconversion. Options are **Internal** or **LO In**. When **Internal**, the module uses the internal LO signal that originates from within the module. When **LO In**, the module uses the signal that is connected to the LO IN connector on the module. ▪ **LO In Frequency**—Optional parameter that specifies the frequency in Hz of the signal connected to the LO IN connector on the module. When you set the **LO Source** to **LO In**, you must connect a signal to the LO IN connector on the module and us

	e this parameter to specify the frequency of that signal. ▪ **Downconverter Gain**—Returns the n et signal gain in dB of the RF downconvert er. Use this parameter to scale the IQ data to the proper power level, as seen at the R F IN connector on the module. **Note** Refer to the N I 9770 Getting Starte d VI in `labview\e xamples\Compa ctRIO\Module Specific\NI 97 70\NI 9770 Ge tting Started \NI 9770 Gett ing Started.l vproj` for an exam ple of how to use Do wnconverter Gain t o scale the IQ data.
Check Cached Status	Returns the following status information that re ports whether various conditions occurred on th e module since the last execution of the **Check Cached Status** method: ▪ **IQ Data Overflow**—Returns a Boolean value. A value of TRUE indicates that the R F input subsystem tried to acquire a signal that is larger in amplitude than the ADC ca n accurately measure using the current ha rdware gain configuration. This problem may result from using a reference level th at is too low for the supplied input signal. ▪ **LO PLL Unlocked**—Returns a Boolean value. A value of TRUE indicates that the L O PLL is in an unlocked state. The LO PLL must be locked in order to ensure that cor rect data is acquired from the module.

	▪ **Sample Clock PLL Unlocked**—Returns a Boolean value. A value of TRUE indicates that the sample clock PLL is in an unlocked state. When synchronizing multiple modules, the sample clock PLL must be locked in order to ensure that the modules are synchronized properly.

I/O Properties

This device does not support any I/O properties.

Module Properties

Use the FPGA I/O Property Node to access the following module properties for this device.

Property	Description
Data Rate	Sets the rate at which the module acquires IQ data.
Peak RF In Power	Returns the peak signal power level in dBm that was measured at the RF IN connector across the full RF frequency range of the module. The peak is cleared when this property is read.  **Note** This value only updates while the module is acquiring IQ data. When the acquisition stops, this property returns the last measured peak signal power level.
LO Out Enabled	When set to TRUE, the module drives the LO signal to the LO OUT connector on the module. This property is used to share the LO signal across multiple NI 9770 modules. This property cannot be set to FALSE when the **LO Source** is set to **LO In**. The module always dr

	ives LO OUT when using an external LO signal o n the LO IN connector on the module.
Downconverter Gain	Returns the net signal gain in dB of the RF down converter. Use this parameter to scale the IQ dat a to the proper power level, as seen at the RF IN connector on the module.  **Note** Refer to the NI 9 770 Getting Started VI i n `labview\exampl es\CompactRIO\M odule Specific\N I 9770\NI 9770 Getting Started \NI 9770 Gettin g Started.lvpro j` for an example of ho w to use Downconvert er Gain to scale the IQ data.
RF Attenuation	Configures the amount of RF attenuation in dB t hat is applied to the input signal. The valid para meter range is 0 dB to 30 dB. You can read or wri te to this property. If you write to this property, you must read Downconverter Gain again.
IF Attenuation	Configures the amount of IF attenuation in dB t hat is applied to the input signal. The valid para meter range is 0 dB to 30 dB. You can read or wri te to this property. If you write to this property, you must read Downconverter Gain again.
Module ID	Returns the Module ID, 0x7827.
Serial Number	Returns the unique serial number of the module .
Vendor ID	Returns the NI vendor ID, 0x1093.

Single-Cycle Timed Loop

You can use the **Onboard Clock** channel in the single-cycle Timed Loop. You cannot use the other channels on the NI 9770 with the single-cycle Timed Loop.

Refer to the Understanding Loop Timing (FPGA Interface) topic for information about loop timing for this module.

C Series Module Properties Dialog Box for the NI 9770 (FPGA Interface)

Right-click an NI 9770 C Series module in the **Project Explorer** window and select **Properties** from the shortcut menu to display this dialog box.

Use this dialog box to configure a C Series module.

This dialog box includes the following components:

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this option.
- **Location**—Specifies a slot in the chassis for the C Series module.
- **Master Timebase Source**—Specifies the master timebase source used by the module.
- **Export Onboard Clock**—Place a checkmark in this checkbox if you want to make this module accessible as a master timebase source to other modules.
- **Data Rate**—Specifies the rate at which the module acquires data.
- **Center Frequency (Hz)**—Specifies the RF center frequency at which the module acquires data.
- **Reference Level (dBm)**—Specifies the expected total power in dBm of the RF input signal.

Synchronizing Multiple NI 9770 Modules (FPGA Interface)

You can synchronize multiple NI 9770 modules that are connected to the same FPGA device if your application meets the following requirements:

- The modules must use the same master timebase source

- The modules must start acquisition mode at the same time
- A single FPGA I/O Node function must read the synchronous data

You must create FPGA I/O items for the NI 9770 before you can configure the items using the FPGA I/O Node. Develop the FPGA VI to meet the guidelines described in this topic.

Note The NI 9770 does not support synchronization with other non-NI 9770 modules.

Sharing a Master Timebase Source

Configure the modules to share the same master timebase source.

Sharing the LO Signal

You can share a local oscillator (LO) signal between a master module and one or more slave modules to enable a repeatable phase relationship between the master module and the slave modules.

Complete the following steps to configure the modules to share the same LO signal.

1. Designate one module as the master module, which will drive its LO signal to a slave module.
2. Connect the LO OUT terminal on the master module to the LO IN terminal on the slave module.

Notes

- You can add multiple slave modules in a daisy-chain configuration by connecting the LO OUT terminal of one slave module to the LO IN terminal of the next slave module.
- Add 50 Ω termination to the LO OUT terminal of the last slave module in the chain.

3. Configure the master module to export its LO signal on the LO OUT terminal by setting the **LO Out Enabled** property of the master module to TRUE.
4. Read the **LO Frequency** property of the master module. This value is used to configure the frequency of the LO IN signal on the slave module.
5. Configure the slave module to import its LO signal from the LO IN connector. Use the **Configure RF In** method of the slave module to set the following values:

Parameter	Value
LO Source	LO In
LO In Frequency	The value returned by the **LO Frequency** property of the master module

Starting the Synchronized Acquisition

Configure an FPGA I/O Node with **Start** channels for the NI 9770 modules you want to synchronize and wire a Boolean constant set to TRUE to each **Start** channel.

Note Ensure that all I/O channels are in the same FPGA I/O Node. Otherwise, the FPGA I/O Node will not return synchronized data.

Acquiring Data from Synchronized NI 9770 Modules with the Same Data Rate

Configure an FPGA I/O Node with all of the channels from which you want to synchronously sample.

Note Ensure that all I/O channels are in the same FPGA I/O Node. Otherwise, the FPGA I/O Node will not return synchronized data.

Refer to the Synchronizing NI 9770 Modules (FPGA) VI in the `labview\examples\CompactRIO\Module Specific\NI 9770\NI 9770 Multi-Module Synchronization\NI 9770 Multi-Module Synchronization.lvproj` for an example of synchronizing multiple modules with the same data rate.

Acquiring Data from Synchronized NI 9770 Modules with Different Data Rates

If you synchronize NI 9770 modules that are configured for different data rates, create a separate loop for each data rate in the FPGA VI. In each loop, configure an FPGA I/O Node with all of the channels that are configured for the data rate of that loop. If you place NI 9770 channels that are configured for different data rates in the same loop, LabVIEW returns an overrun warning from the FPGA I/O Node (error 65539) when you run the VI. There is a delay before the FPGA I/O Node returns the first data point. The length of the delay depends on the data rate of the NI 9770.

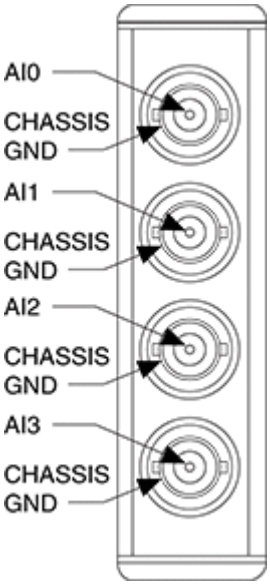
NI 9775

CompactRIO 4-Ch, ±10 V, 20 MS/s, 14-Bit Digitizer

Software Reference (?)

FPGA Interface

NI 9775 Pinout



Related Topics

FPGA Interface
NI 9775 Acquisition Modes
Acquiring Data from a Module (FPGA Interface)
Configuring the Master Timebase Source for a Module (FPGA Interface)
Configuring the Data Rate for a Module (FPGA Interface)
Synchronizing Multiple Modules
Understanding Loop Timing (FPGA Interface)

NI 9775 (FPGA Interface)

CompactRIO 4-Ch, ±10 V, 20 MS/s, 14-Bit Digitizer

Open example

Find related examples

FPGA I/O Node

You can use an FPGA I/O Node, configured for reading, with this device.

Note You can synchronize an NI 9775 module with other modules that have a selectable timebase source.

Note You can only use the 12.8 MHz exported clock of the NI 9469 as the reference clock of the NI 9775. You cannot use the 13.1072 MHz clock with the NI 9775.

Note You can only use another NI 9775 or the NI 9469 configured to export its clock as the reference clock for the NI 9775.

Terminals in Software

Use the FPGA I/O Node to access the following terminals for this device.

Terminal	Description
AI**x**	Analog input channel x, where x is the number of the channel. The NI 9775 has AI channels 0 to 3.

	 **Caution** Do not access AI channels on multiple modules from the same FPGA I/O Node if the modules are not synchronized or do not use the same data rate.
Reference Clock	Gives access to the reference clock in the LabVIEW block diagram. Export the onboard clock of the NI 9775 and use the FPGA I/O Node in a single-cycle timed loop to access this channel.
Start	Controls when the NI 9775 starts acquiring data.
Stop	Controls when the NI 9775 stops acquiring data. When the 9775 is acquiring data, you must write TRUE to this channel before you can access properties of the module.

Arbitration

This device supports only the Arbitrate if Multiple Requestors Only option for arbitration. You cannot configure arbitration settings for this device.

I/O Methods

This device does not support any I/O methods.

Module Methods

Use the FPGA I/O Method Node to access the following module methods for this device.

Method	Description
Fetch Record Data	Fetches the next available sample from each channel in the Triggered Records. Updates the number of remaining elements of the current record, and the number of remaining records. This method cannot be executed at the same time as the AI**x** I/O node or any of the Trigger Record Method Nodes.

	▪ **Records Remaining**—Indicates the number of records available to be fetched from the module. ▪ **Elements Remaining**—Indicates the number of samples available to be fetched from the current record. ▪ **Timeout**—Specifies the minimum number of ticks the Method Node waits before timing out. The Method Node times out if the data is not yet available to access. Set this parameter to -1 if you want the Method Node to wait indefinitely.
Trigger Record on HW Event	Triggers a record event whenever a hardware event occurs on a single channel. Any hardware event that occurs outside of this execution will be lost. Once there are no more records available to trigger, you cannot send any more triggers. ▪ **AI Channel**—Specifies which input channel the hardware event will come from. ▪ **Trigger Slope**—Specifies the slope direction of the hardware event. Can be either "Positive" or "Negative". ▪ **Trigger Level**—Specifies the voltage level used to trigger a record. ▪ **Hysteresis Value**—Specifies the hysteresis value for the trigger. If the Trigger Slope is positive, the Hysteresis Value will be below the Trigger Level. If the Trigger Slope is negative, the Hysteresis Value will be above the Trigger Level. ▪ **Timeout**—Specifies the minimum number of ticks the Method Node waits before timing out. The Method Node times out if the module cannot be triggered or if the hardware event condition has not been met. Set this parameter to -1 if you want the Method Node to wait indefinitely. The har

	dware event may be missed if timeout is s et to a small number of ticks.
Trigger Record On HW Event (Multiple Sources)	Triggers a record event whenever a hardware ev ent occurs on any channel. Any hardware event that occurs outside of this execution will be lost. Once there are no more records available to trig ger, you cannot send any more triggers. ▪ **Trigger Configuration**—Specifies the trigger configurations for each channel. E ach of these contains the following chann els: Enable, Trigger Slope, Trigger Level, a nd Hysteresis Value. ▪ **Timeout**—Specifies the minimum num ber of ticks the Method Node waits before timing out. The Method Node times out if the module cannot be triggered or if the h ardware event condition has not been me t. Set this parameter to -1 if you want the Method Node to wait indefinitely. The har dware event may be missed if timeout is s et to a small number of ticks.
Trigger Record	Signals the module to trigger a record. Once the re are no more records available to trigger, you c an not send any more triggers. ▪ **Timeout**—Specifies the minimum num ber of ticks the Method Node waits before timing out. The Method Node times out if the module cannot be triggered. Set this p arameter to -1 if you want the Method No de to wait until the module can trigger. Se t this parameter to 0 if you want the Meth od Node to trigger immediately if there is not already already a record being acquire d.

I/O Properties

Use the FPGA I/O Property Node to access the following I/O properties for this device.

Property	Description
Enable Analog Filter	Changes the configuration of the analog filter
LSB Weight (High-Resolution)	Returns the LSB weight in nV/LSB.
LSB Weight (High-Speed, Analog Filter Disabled)	Returns the LSB weight in nV/LSB.
LSB Weight (High-Speed, Analog Filter Enabled)	Returns the LSB weight in nV/LSB.
Offset (High-Resolution)	Returns the calibration offset in µV.
Offset (High-Speed, Analog Filter Disabled)	Returns the calibration offset in µV.
Offset (High-Speed, Analog Filter Enabled)	Returns the calibration offset in µV.

Module Properties

Use the FPGA I/O Property Node to access the following module properties for this device.

Property	Description
Module ID	Returns the Module ID, 0x7889.
Serial Number	Returns the unique serial number of the module .
Vendor ID	Returns the NI vendor ID, 0x1093.
Record Data Rate	Specifies the rate at which the module acquires data for the Record Acquisition.
Record Pre-Trigger Samples	Specifies the number of acquired samples prior to the trigger of a record.
Continuous Data Rate	Specifies the rate at which the module acquires data in continuous mode.
Records Available to Fetch	Returns the number of records available to fetch in the module.
Records Available to Trigger	Returns the number of records available to trigg er in memory.
Total Record Samples	Specifies the number of samples per record.

Timing Mode	Changes the module configuration between High-Speed and High-Resolution

Single-Cycle Timed Loop

This device does not support the single-cycle Timed Loop.

C Series Module Properties Dialog Box for the NI 9775 (FPGA Interface)

Right-click an NI 9775 C Series module in the **Project Explorer** window and select **Properties** from the shortcut menu to display this dialog box.

Use this dialog box to configure a C Series module.

This dialog box includes the following components:

- **Name**—Specifies the name of the C Series module, which appears in the **Project Explorer** window. LabVIEW assigns a default name to the module based on the slot number. You can use this field to give the module a descriptive name.
- **Module Type**—Specifies the type of C Series module. You cannot change this option.
- **Location**—Specifies a slot in the chassis for the C Series module.
- **Calibration Mode**—Sets the calibration mode for the C Series module. Can be either "Calibrated" or "Raw."
- **Reference Clock Source**—Specifies the master timebase source used by the module.
- **Export Reference Clock**—Place a checkmark in this checkbox if you want to make this module accessible as a master timebase source to other modules.
- **Record Data Rate**—Specifies the rate at which the module acquires data for the Record Acquisition.
- **Record Pre-Trigger Samples**—Sets the number of acquired samples prior to the trigger of a record.

- **Record Samples**—Specifies the number of samples per record. The maximum number of record samples depend on the number of channels enabled.
- **Continuous Data Rate**—Specifies the rate at which the module acquires data in continuous mode. The maximum data rate depends on the number of channels enabled.
- **Channel Configuration**— Enables or disables each channel. Also sets the analog filter configuration for each channel.
- **Timing Mode**—Changes the module configuration between high-speed and high-resolution.
- **Maximum Number of Records**—Indicates the maximum number of records that can be potentially triggered based on the number of channels enabled and the record samples.
- **Reference Trigger Source**—Specifies the master trigger source used by this module. The default value is "Same as Ref Clock," which will set the trigger source for this module to the same as the reference clock source. You can configure a different reference trigger source as the reference clock source.
- **Export Reference Trigger**—Allows you to select this module as a reference trigger source for other modules. This checkbox will not appear if the reference trigger source is set to "Same as Ref Clock."

NI 9775 Acquisition Modes (FPGA Interface)

The NI 9775 has three different acquisition modes: continuous mode, record mode, and advanced mode.

Continuous Mode

In continuous mode, the NI 9775 transfers real-time data to the chassis at an aggregate rate of 4MS/s across all channels. The NI 9775 will default to continuous mode after executing the Start I/O Node. You can configure the data rate through the Module Property **Continuous Data Rate**. The maximum value of the data rate varies based on the configuration, and can be found in the device datasheet at ni.com/manuals.

Implementing Continuous Mode

1. Configure the **Timing Mode**, **Continuous Data Rate** and **Analog Filter Configuration**.
2. Run the **Start** I/O Node.
3. Run the **AIx** I/O Node as many times as needed.
4. Run the **Stop** I/O Node.

Open example (continuous mode)

Record Mode

In record mode, the NI 9775 stores samples into onboard memory at up to 20 MS/s then transfers the data to the chassis at a slower rate. The start of the data collection is based on a trigger signal sent to the device. This signal can be digital or analog. The collected data is stored in the buffer until the entire acquisition is restarted.

Implementing Record Mode

1. Configure the **Timing Mode**, **Record Data Rate**, **Record Samples**, **Record Pre-Trigger Samples**, and **Analog Configuration**.
2. Run the **Start** I/O Node.
3. Trigger a record using any of the following nodes: **Trigger Record**, **Trigger Record on HW Event**, or **Trigger Record on HW Event (Multiple Sources)**.
4. Run the **Fetch Record Data** Method Node until there are no more samples available to fetch.
5. Run the **Stop** I/O Node.

Open example (record mode)

Advanced Mode

In advanced mode, the NI 9775 combines the functionality of continuous mode and record mode to enable more complex triggering. Advanced mode can use live data

from continuous mode to trigger a faster collection rate using record mode. This can be used for applications such as pattern detection or frequency triggering, and gives you more advanced triggering options.

Implementing Advanced Mode

1. Configure **Timing Mode**, **Record Data Rate**, **Record Samples**, **Record Pre-Trigger Samples**, **Analog Filter Configuration**, and **Continuous Data Rate**.
2. Run the **Start** I/O Node.
3. Use the **AIx** I/O Node to build a custom trigger condition.
4. Trigger on the custom trigger condition using any Trigger Record Method Node for as many times as needed, up to the number of available records.
5. Run the **Fetch Record Data** Method Node until there are no more samples available to fetch.
6. Run the **Stop** I/O Node.

 Open example (advanced mode)