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PCI-6052

NI 6052E Family Specifications

This document lists the I/O terminal summary and specifications for the devices that make up the NI 6052E family of devices. This family includes the following devices:

- NI DAQPad-6052E
- NI PCI-6052E
- NI PXI-6052E

I/O Terminal Summary



Note With NI-DAQmx, National Instruments revised its terminal names so they are easier to understand and more consistent among NI hardware and software products. The revised terminal names used in this document are usually similar to the names they replace. For a complete list of Traditional NI-DAQ (Legacy) terminal names and their NI-DAQmx equivalents, refer to *Terminal Name Equivalents* of the *E Series Help*.

Table 1. I/O Terminals

Terminal Name	Terminal Type and Direction	Impedance Input/Output	Protection (V) On/Off	Source (mA at V)	Sink (mA at V)	Rise Time (ns)	Bias
AI <0..15>	AI	100 G Ω in parallel with 100 pF	$\pm 25/15$	—	—	—	± 200 pA
AI SENSE, AI SENSE 2	AI	100 G Ω in parallel with 100 pF	$\pm 25/15$	—	—	—	± 200 pA
AI GND	—	—	—	—	—	—	—
AO 0	AO	0.1 Ω	Short-circuit to ground	5 at 10	5 at -10	20 V/ μ s	—
AO 1	AO	0.1 Ω	Short-circuit to ground	5 at 10	5 at -10	20 V/ μ s	—
AO EXT REF	AI	10 k Ω	$\pm 25/15$	—	—	—	—
AO GND	—	—	—	—	—	—	—
D GND	—	—	—	—	—	—	—
+5 V	—	0.1 Ω	Short-circuit to ground	1 A at 5	—	—	—

Table 1. I/O Terminals (Continued)

Terminal Name	Terminal Type and Direction	Impedance Input/ Output	Protection (V) On/Off	Source (mA at V)	Sink (mA at V)	Rise Time (ns)	Bias
P0.<0..7>	DIO	—	$V_{CC} + 0.5$	13 at $(V_{CC} - 0.4)$	24 at 0.4	1.1	50 k Ω pu
AI HOLD COMP	DO	—	—	3.5 at $(V_{CC} - 0.4)$	5 at 0.4	1.5	50 k Ω pu
EXT STROBE*	DO	—	—	3.5 at $(V_{CC} - 0.4)$	5 at 0.4	1.5	50 k Ω pu
PFI 0/ (AI START TRIG)	AI/DIO	10 k Ω	$V_{CC} + 0.5/\pm 35$	3.5 at $(V_{CC} - 0.4)$	5 at 0.4	1.5	9 k Ω pu, 10 k Ω pd
PFI 1/ (AI REF TRIG)	DIO	—	$V_{CC} + 0.5$	3.5 at $(V_{CC} - 0.4)$	5 at 0.4	1.5	50 k Ω pu
PFI 2/ (AI CONV CLK)*	DIO	—	$V_{CC} + 0.5$	3.5 at $(V_{CC} - 0.4)$	5 at 0.4	1.5	50 k Ω pu
PFI 3/ CTR 1 SOURCE	DIO	—	$V_{CC} + 0.5$	3.5 at $(V_{CC} - 0.4)$	5 at 0.4	1.5	50 k Ω pu
PFI 4/CTR 1 GATE	DIO	—	$V_{CC} + 0.5$	3.5 at $(V_{CC} - 0.4)$	5 at 0.4	1.5	50 k Ω pu
CTR 1 OUT	DO	—	—	3.5 at $(V_{CC} - 0.4)$	5 at 0.4	1.5	50 k Ω pu
PFI 5/ (AO SAMP CLK)*	DIO	—	$V_{CC} + 0.5$	3.5 at $(V_{CC} - 0.4)$	5 at 0.4	1.5	50 k Ω pu
PFI 6/ (AO START TRIG)	DIO	—	$V_{CC} + 0.5$	3.5 at $(V_{CC} - 0.4)$	5 at 0.4	1.5	50 k Ω pu
PFI 7/ (AI SAMP CLK)	DIO	—	$V_{CC} + 0.5$	3.5 at $(V_{CC} - 0.4)$	5 at 0.4	1.5	50 k Ω pu
PFI 8/ CTR 0 SOURCE	DIO	—	$V_{CC} + 0.5$	3.5 at $(V_{CC} - 0.4)$	5 at 0.4	1.5	50 k Ω pu
PFI 9/CTR 0 GATE	DIO	—	$V_{CC} + 0.5$	3.5 at $(V_{CC} - 0.4)$	5 at 0.4	1.5	50 k Ω pu
CTR 0 OUT	DO	—	—	3.5 at $(V_{CC} - 0.4)$	5 at 0.4	1.5	50 k Ω pu
FREQ OUT	DO	—	—	3.5 at $(V_{CC} - 0.4)$	5 at 0.4	1.5	50 k Ω pu

* Indicates active low.

AI = Analog Input

DIO = Digital Input/Output

pd = pull-down

AO = Analog Output

DO = Digital Output

pu = pull-up

AI/DIO = Analog Input/Digital Input/Output

Note: The tolerance on the 50 k Ω pull-up and pull-down resistors is large. Actual value may range between 17 k Ω and 100 k Ω .

Specifications

The following specifications are typical at 25 °C unless otherwise noted.

Analog Input

Input Characteristics

Number of channels 16 single-ended or
8 differential
(software-selectable
per channel)

Type of A/D converter (ADC)..... Successive
approximation

Resolution 16 bits, 1 in 65,536

Max sampling rate 333 kS/s guaranteed

Input signal ranges

Range (Software-Selectable)	Input Range	
	Bipolar	Unipolar
20 V	±10 V	—
10 V	±5 V	0 to 10 V
5 V	±2.5 V	0 to 5 V
2 V	±1 V	0 to 2 V
1 V	±500 mV	0 to 1 V
500 mV	±250 mV	0 to 500 mV
200 mV	±100 mV	0 to 200 mV
100 mV	±50 mV	0 to 100 mV

Input coupling DC

Max working voltage
(signal + common-mode)..... Each input should remain
within ± 11 V of ground.

Overvoltage protection

 Powered on ± 25 V

 Powered off ± 15 V

Inputs protected..... AI <0..15>, AI SENSE

FIFO buffer size 512 samples (S)

DMA (PCI and PXI only)

 Channels 3

 Data sources/destinations Analog input, analog
output, counter/timer 0,
or counter/timer 1

Data transfers Direct memory access
(DMA), interrupts,
programmed I/O

DMA modes Scatter-gather

Configuration memory size 512 words

Transfer Characteristics

Relative accuracy ± 1.5 LSB typ,
 ± 3.0 LSB max

Differential nonlinearity (DNL)..... ± 0.5 LSB typ,
 ± 1.0 LSB max

No missing codes 16 bits, guaranteed

Offset error

 Pregain error after calibration..... ± 1.0 μ V max

 Pregain error before
calibration ± 2.6 mV max

 Postgain error after calibration ... ± 76 μ V

 Postgain error before
calibration ± 82 mV

Gain error (relative to calibration reference)

 After calibration (gain = 1)..... ± 30.5 ppm of reading
max

 Before calibration $\pm 22,000$ ppm of reading
max

Gain $\neq 1$ with gain error
adjusted to 0 at gain = 1 ± 200 ppm of reading max

Amplifier Characteristics

Input impedance

 Normal powered on 100 G Ω in parallel
with 100 pF

 Powered off 820 Ω min

Overload 820 Ω min

Input bias current ± 200 pA

Input offset current ± 100 pA

Common-mode rejection ratio (CMRR), DC to 60 Hz

Range	Bipolar	Unipolar
20 V	92 dB	—
10 V	97 dB	97 dB
5 V	101 dB	101 dB
2 V	104 dB	104 dB
100 mV to 1 V	105 dB	105 dB

Dynamic Characteristics

Bandwidth

 Small signal (-3 dB) 480 kHz

 Large signal (1% THD) 500 kHz

Dynamic range

 Gain 0.5 to 5 87 dB, ± 10 V input

 Gain 10 83 dB

Settling time for full-scale step

Full-Scale Step Accuracy*	Settling Time
± 6 LSB	3 μ s max
± 4 LSB	4 μ s max
± 2 LSB	5 μ s max, gain 0.5 to 10 10 μ s max, gain 20 to 50 10 μ s typ, gain 100
± 1 LSB	10 μ s max, gain 0.5 to 2 15 μ s max, gain 5 to 10 15 μ s typ, gain 20 to 100
* Settling times are valid for source impedances < 1 k Ω . Refer to <i>Multichannel Scanning Considerations</i> of the <i>E Series Help</i> for more information.	

System noise (LSB_{rms}, including quantization)

Range	Bipolar	Unipolar
2 to 20 V	0.95	0.95
1 V	1.1	1.1
500 mV	1.3	1.3
200 mV	2.7	2.7
100 mV	5.0	5.0

Crosstalk (DC to 100 kHz)

Adjacent channels-75 dB

All other channels-90 dB

Stability

Recommended warm-up time15 minutes

Offset temperature coefficient

Pregain±4 µV/°C

Bipolar postgain±120 µV/°C

Unipolar postgain.....±30 µV/°C

Gain temperature coefficient±17 ppm/°C

Onboard calibration reference

Level5.000 V (±1.0 mV),
(over full operating
temperature, actual value
stored in EEPROM)

Temperature coefficient±0.6 ppm/°C max

Long-term stability±6 ppm/√1,000 h

Analog Output

Output Characteristics

Number of channels.....2 voltage

Resolution.....16 bits, 1 in 65,536

Max update rate333 kS/s

Type of D/A converter (DAC)Double-buffered,
multiplying

FIFO buffer size2,048 Samples (S)

Data transfers.....DMA, interrupts,
programmed I/O

DMA modesScatter-gather

Accuracy Information

Nominal Range (V)		Absolute Accuracy					Absolute Accuracy at Full Scale (mV)
Positive Full Scale	Negative Full Scale	% of Reading			Offset (μV)	Temp Drift (°/°C)	
		24 Hours	90 Days	1 Year			
10	−10	0.0044	0.0052	0.0061	798	0.0001	1.405
10	0	0.0044	0.0052	0.0061	569	0.0001	1.176

Note: Accuracies are valid for measurements following an internal E Series calibration. Averaged numbers assume dithering and averaging of 100 single-channel readings. Measurement accuracies are listed for operational temperatures within $\pm 1^{\circ}\text{C}$ of internal calibration temperature and $\pm 10^{\circ}\text{C}$ of external or factory-calibration temperature. NI recommends a one-year calibration interval. The Absolute Accuracy at Full Scale calculations were performed for a maximum range input voltage (for example, 10 V for the $\pm 10\text{ V}$ range) after one year, assuming 100 points of averaged data. Go to ni.com/info and enter info code `rdspec` for example calculations.

Transfer Characteristics

Relative accuracy, or integral nonlinearity (INL)

After calibration ± 0.35 LSB typ,
 ± 1.0 LSB max

Before calibration ± 4 LSB max

DNL

After calibration ± 0.5 LSB typ,
 ± 1.0 LSB max

Before calibration ± 3 LSB max

Monotonicity 16 bits, guaranteed
after calibration

Offset error

After calibration $\pm 305\ \mu\text{V}$ max

Before calibration $\pm 17\text{ mV}$ max

Gain error (relative to internal reference)

After calibration ± 30.5 ppm of output max

Before calibration $\pm 9,000$ ppm of output
max

Gain error

(relative to external reference) $+0\%$ to $+0.5\%$ of output
max, not adjustable

Voltage Output

Ranges $\pm 10\text{ V}$, 0 to 10 V,
 $\pm \text{AO EXT REF}$,
0 V to AO EXT REF
(software-selectable)

Output coupling DC

Output impedance $0.1\ \Omega$ max

Current drive $\pm 5\text{ mA}$ max

Protection Short-circuit to ground

Power-on state 0 V ($\pm 20\text{ mV}$)

External reference input

Range $\pm 11\text{ V}$

Overvoltage protection

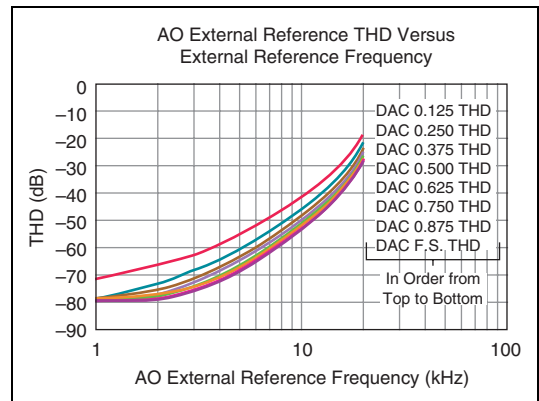
Powered on $\pm 25\text{ V}$

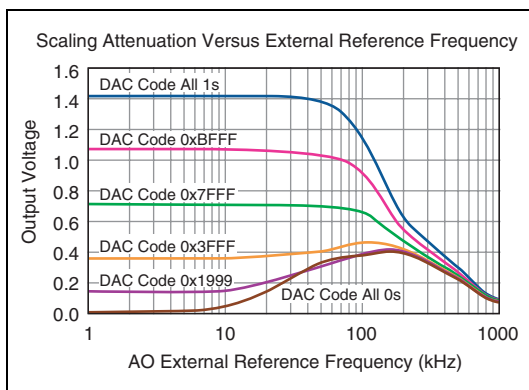
Powered off $\pm 15\text{ V}$

Input impedance $10\text{ k}\Omega$

Bandwidth (-3 dB) 3 kHz

Slew rate $0.3\text{ V}/\mu\text{s}$





Dynamic Characteristics

Settling time for full-scale step3.5 μ s to ± 1.0 LSB accuracy

Settling time for half-scale step.....3.0 μ s to ± 1.0 LSB accuracy

Slew rate15 V/ μ s

Noise.....60 μ V_{rms},
DC to 1 MHz

Glitch energy (at mid-scale transition)

Magnitude10 mV

Duration1 μ s

Stability

Offset temperature coefficient..... ± 35 μ V/ $^{\circ}$ C

Gain temperature coefficient

Internal reference ± 6.5 ppm/ $^{\circ}$ C

External reference ± 5 ppm/ $^{\circ}$ C

Onboard calibration reference

Level5.000 V (± 1.0 mV),
(over full operating
temperature, actual value
stored in EEPROM)

Temperature coefficient ± 0.6 ppm/ $^{\circ}$ C max

Long-term stability ± 6 ppm/ $\sqrt{1,000}$ h

Digital I/O

Number of channels 8 input/output

Compatibility 5 V TTL/CMOS

Digital logic levels on P0.<0..7>

Level	Min	Max
Input low voltage	0 V	0.8 V
Input high voltage	2.0 V	5.0 V
Input low current ($V_{in} = 0$ V)	—	-320 μ A
Input high current ($V_{in} = 5$ V)	—	10 μ A
Output low voltage ($I_{OL} = 24$ mA)	—	0.4 V
Output high voltage ($I_{OH} = -13$ mA)	4.35 V	—

Power-on state..... Input (high-impedance)

Data transfers Programmed I/O

Max transfer rate 50 kwords/s,
system-dependent

Constant sustainable rate 1 to 10 kwords/s, typ

Timing I/O

Number of channels

Up/down counter/timers 2

Frequency scaler..... 1

Resolution

Up/down counter/timers 24 bits

Frequency scaler..... 4 bits

Compatibility 5 V TTL/CMOS

Digital logic levels

Level	Min	Max
Input low voltage	0.0 V	0.8 V
Input high voltage	2.0 V	5.0 V
Output low voltage ($I_{out} = 5$ mA)	—	0.4 V
Output high voltage ($I_{out} = -3.5$ mA)	4.35 V	—

Base clocks available

Up/down counter/timers 20 MHz, 100 kHz

Frequency scaler..... 10 MHz, 100 kHz

Base clock accuracy $\pm 0.01\%$

Max external source frequency	
Up/down counter/timers	20 MHz
External source selections	PFI <0..9>, RTSI <0..6>, analog trigger, software-selectable
External gate selections	PFI <0..9>, RTSI <0..6>, analog trigger, software-selectable
Min source pulse duration	10 ns in edge-detect mode
Min gate pulse duration	10 ns in edge-detect mode
Data transfers	
PCI/PXI up/down counter/timer	DMA (scatter-gather), interrupts, programmed I/O
DAQPad up/down counter/timer	Interrupts, programmed I/O
Frequency scaler	Programmed I/O

Triggers

Analog Trigger

Purpose	
Analog input	Start, reference, and pause trigger, sample clock
Analog output	Start and pause trigger, sample clock
Counter/timers	Source, gate
Source	AI <0..15>, PFI 0/AI START TRIG
Level	
Internal	±Full-scale
External	±10 V
Slope	Positive or negative (software-selectable)
Resolution	12 bits, 1 in 4,096
Hysteresis	Programmable
Bandwidth (–3 dB)	
Internal	700 kHz
External	700 kHz
External input (PFI 0/AI START TRIG)	
Impedance	10 kΩ
Coupling	DC

Protection	
When configured as a digital signal	–0.5 to VCC + 0.5 V
When configured as an analog trigger signal or disabled	±35 V
Powered off	±35 V
Accuracy	±1.0% of full-scale range max

Digital Trigger

Purpose	
Analog input	Start, reference, and pause trigger, sample clock
Analog output	Start and pause trigger, sample clock
Counter/timers	Source, gate
Source	PFI <0..9>, RTSI <0..6>
Compatibility	5 V TTL
Response	Rising or falling edge
Pulse width	10 ns min

RTSI

Trigger lines	
NI PCI-6052E	7
NI DAQPad-6052E	4
Clock line	1

PXI Trigger Bus (PXI Only)

Trigger lines	6
Star trigger	1

Calibration

Recommended warm-up time	15 minutes
Calibration interval	1 year
Onboard calibration	
reference level	5,000 V (±3.5 mV), (over full operating temperature, actual value stored in EEPROM)
Temperature coefficient	±0.6 ppm/°C max
Long-term stability	±6.0 ppm/√1,000 h

Bus Interface

NI PCI/PXI-6052E	Master, slave
NI DAQPad-6052E	Master, slave, asynchronous, 400 Mb/s

Power Requirement

Power available at I/O connector+4.65 VDC to
+5.25 VDC at 1 A

NI PCI/PXI-6052E +5 VDC ($\pm 5\%$)	1.3 A (does not include current drawn from 5 V fuse on I/O connector)
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NI DAQPad-6052E 9–24 VDC	20 W
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Physical

Dimensions (not including connectors)

NI PCI-6052E	17.5 cm $\times$ 10.6 cm (6.9 in. $\times$ 4.2 in.)
NI PXI-6052E	16 cm $\times$ 10 cm (6.3 in. $\times$ 3.9 in.)
NI DAQPad-6052E	30.7 cm $\times$ 25.4 cm $\times$ 4.3 cm (12.1 in. $\times$ 10 in. $\times$ 1.7 in.)

Weight

NI PCI-6052E	160 g (5.6 oz)
NI PXI-6052E	206 g (7.2 oz)
NI DAQPad-6052E	1951 g (4 lb 4.8 oz)

I/O connector

NI PCI/PXI-6052E	68-pin male SCSI-II type
NI DAQPad-6052E	68-pin male SCSI-II type, or 15 BNCs and 30 removable screw terminals

Maximum Working Voltage

Maximum working voltage refers to the signal voltage plus the common-mode voltage.

Channel-to-earth	11 V, Installation Category I
Channel-to-channel	11 V, Installation Category I

Environmental

Operating temperature	0 to 55 °C
Storage temperature	–20 to 70 °C
Relative humidity	10 to 90%, noncondensing

Maximum altitude..... 2,000 m

Pollution Degree
(indoor use only)..... 2

Safety

NI PCI/PXI-6052E

The NI PCI/PXI-6052E devices meet the requirements of the following standards for safety and electrical equipment for measurement, control, and laboratory use:

- IEC 61010-1, EN 61010-1
- UL 61010-1
- CAN/CSA-C22.2 No. 61010.1



Note For UL and other safety certifications, refer to the product label, or visit ni.com/certification, search by model number or product line, and click the appropriate link in the Certification column.

NI DAQPad-6052E

The NI DAQPad-6052E devices meet the requirements of the following standards for safety and electrical equipment for measurement, control, and laboratory use:

- IEC 60950-1, EN 60950-1
- UL 60950-1
- CAN/CSA-C22.2 No. 60950-1



Note For UL and other safety certifications, refer to the product label, or visit ni.com/certification, search by model number or product line, and click the appropriate link in the Certification column.

Electromagnetic Compatibility

Emissions	EN 55011 Class A at 10 m FCC Part 15A above 1 GHz
Immunity	EN 61326:1997 A2:2001, Table 1

CE, C-Tick, and FCC Part 15 (Class A) Compliant



Note For EMC compliance, operate this device with shielded cabling.

CE Compliance

This product meets the essential requirements of applicable European Directives, as amended for CE marking, as follows:

Low-Voltage Directive (safety) 73/23/EEC

Electromagnetic Compatibility

Directive (EMC) 89/336/EEC



Note Refer to the Declaration of Conformity (DoC) for this product for any additional regulatory compliance information. To obtain the DoC for this product, visit ni.com/certification, search by model number or product line, and click the appropriate link in the Certification column.

AI 8	34	68	AI 0
AI 1	33	67	AI GND
AI GND	32	66	AI 9
AI 10	31	65	AI 2
AI 3	30	64	AI GND
AI GND	29	63	AI 11
AI 4	28	62	AI SENSE
AI GND	27	61	AI 12
AI 13	26	60	AI 5
AI 6	25	59	AI GND
AI GND	24	58	AI 14
AI 15	23	57	AI 7
AO 0	22	56	AI GND
AO 1	21	55	AO GND
AO EXT REF	20	54	AO GND
P0.4	19	53	D GND
D GND	18	52	P0.0
P0.1	17	51	P0.5
P0.6	16	50	D GND
D GND	15	49	P0.2
+5 V	14	48	P0.7
D GND	13	47	P0.3
D GND	12	46	AI HOLD COMP
PFI 0/AI START TRIG	11	45	EXT STROBE
PFI 1/AI REF TRIG	10	44	D GND
D GND	9	43	PFI 2/AI CONV CLK
+5 V	8	42	PFI 3/CTR 1 SRC
D GND	7	41	PFI 4/CTR 1 GATE
PFI 5/AO SAMP CLK	6	40	CTR 1 OUT
PFI 6/AO START TRIG	5	39	D GND
D GND	4	38	PFI 7/AI SAMP CLK
PFI 9/CTR 0 GATE	3	37	PFI 8/CTR 0 SRC
CTR 0 OUT	2	36	D GND
FREQ OUT	1	35	D GND

Figure 1. NI PCI/PXI-6052E Pinout

PFI 9	2	1	P0.7
PFI 8	4	3	P0.6
PFI 7	6	5	P0.5
PFI 6	8	7	P0.4
PFI 5	10	9	P0.3
PFI 4	12	11	P0.2
PFI 3	14	13	P0.1
PFI 2	16	15	P0.0
PFI 1	18	17	CTR 1 OUT
D GND	20	19	D GND
USER 2	22	21	USER 1
FREQ OUT	24	23	AI HOLD COMP
+5 V	26	25	EXT STROBE
+5 V	28	27	AI SENSE
D GND	30	29	AI GND

Figure 2. NI DAQPad-6052E BNC Pinout