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USER MANUAL

NI PCIe-7857

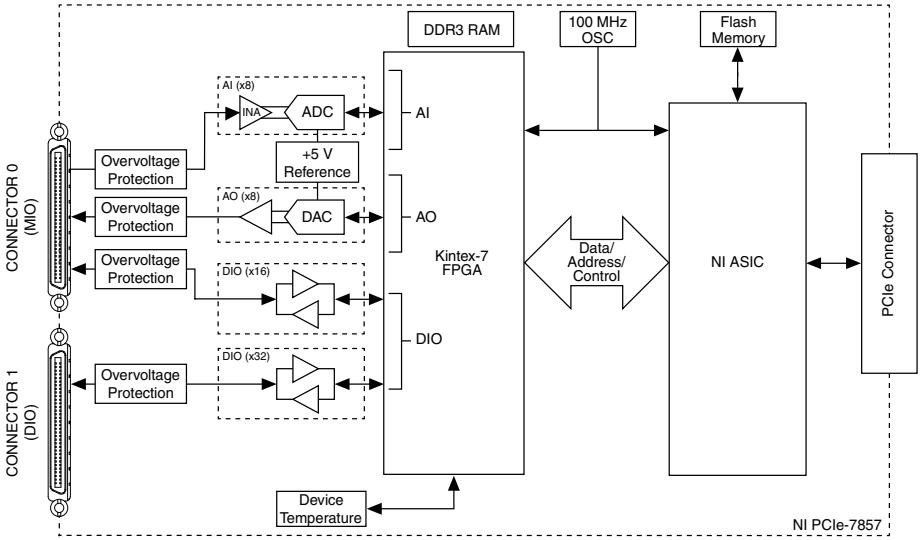
R Series Digital I/O Module for PCI Express, 8 AI, 8 AO, 48 DIO, 1 MS/s AI, 512 MB DRAM, Kintex-7 160T FPGA

This document provides compliance, pinout, connectivity, mounting, and power information for the PCIe-7857.

Hardware Overview

The following high-level block diagram represents the PCIe-7857.

Figure 1. PCIe-7857 Block Diagram



Pinout

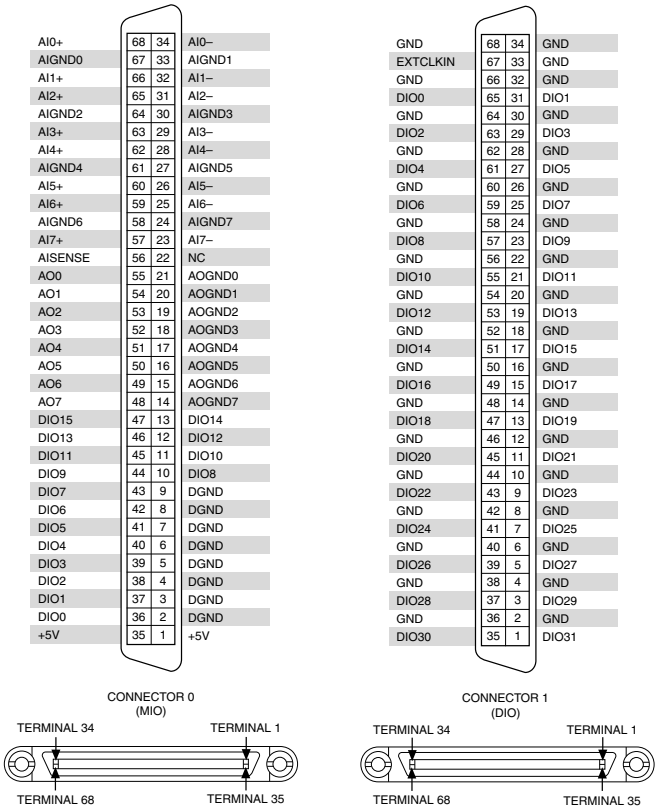


Table 1. PCIe-7857 Signal Descriptions

Signal	Description
AI+	Positive analog input signal connection
AI-	Negative analog input signal connection
AISENSE	Reference connection for NRSE measurements
AIGND	Ground reference for the analog input signal
AO	Analog output signal connection
AOGND	Ground reference for the analog output signal

Table 1. PCIe-7857 Signal Descriptions (Continued)

Signal	Description
DIO	Digital input/output signal connection
DGND	Ground reference for the digital signal
EXTCLKIN	External clock input source that can be used for source synchronous acquisitions. The provided clock source must be stable and glitch-free.
GND	Ground connection
Supply (+5 V_{out})	5 V power output connection for external devices
NC	No connection

The PCIe-7857 is protected from overvoltage and overcurrent conditions.

Note Refer to the device specifications, available at *ni.com/manuals* for more information.

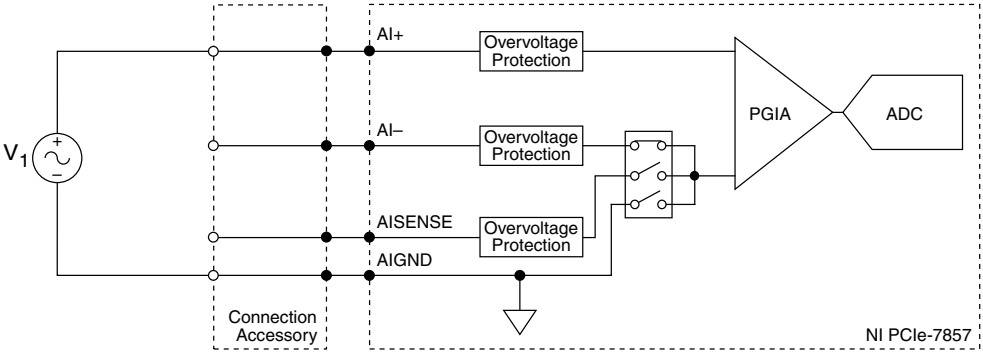
Analog Input

The PCIe-7857 provides connections for eight AI channels. Each channel has an AI+ pin, AI- pin, and AIGND pin to which you can connect both single-ended or differential voltage signals. Use the AISENSE pin to connect non-referenced single-ended signals.

Connecting Single-Ended Voltage Signals

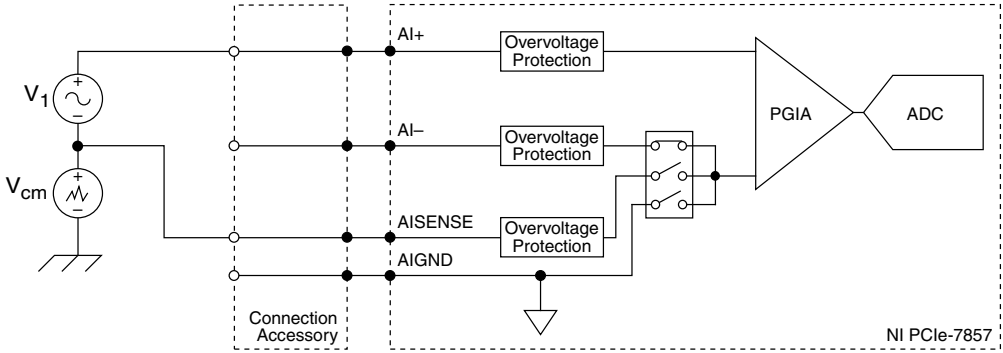
To connect referenced single-ended voltage signals to the PCIe-7857, you must connect the voltage ground signal to AI GND in order to keep the common-mode voltage in the specified range.

Figure 2. Connecting Referenced Single-Ended Signals to the PCIe-7857



To connect non-referenced single-ended voltage signals to the PCIe-7857, you must connect the voltage ground signal to AI SENSE in order to keep the common-mode voltage in the specified range.

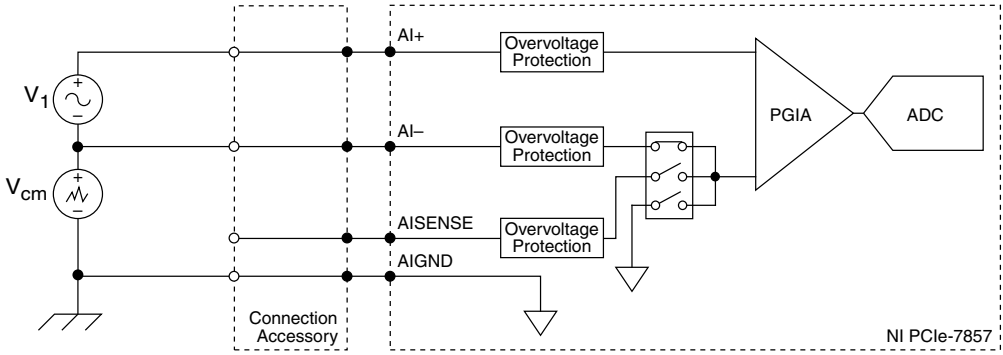
Figure 3. Connecting Non-Referenced Single-Ended Signals to the PCIe-7857



Connecting Differential Voltage Signals

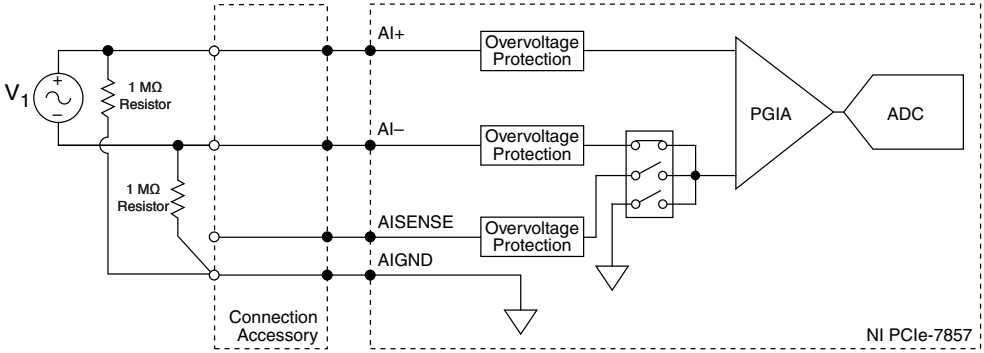
You can connect grounded or floating differential signal sources to the PCIe-7857. Connect the positive voltage signal to the AI+ and the negative voltage signal to AI-. To connect grounded differential signals to the PCIe-7857, you must also connect the signal reference to AI GND.

Figure 4. Connecting Grounded Differential Signals to the PCIe-7857



To connect floating differential signals to the PCIe-7857, you must connect the negative and positive signals to AI GND through 1 MΩ resistors to keep the voltage within the common-mode voltage range. If the voltage source is outside the common-mode voltage range, the PCIe-7857 does not read data accurately.

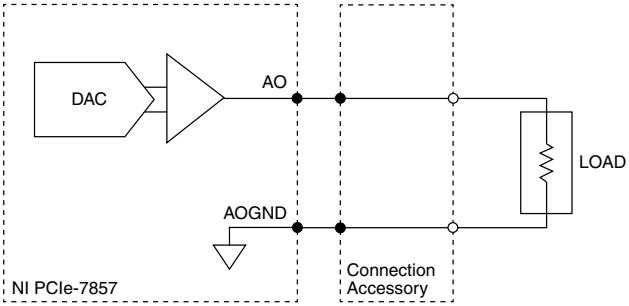
Figure 5. Connecting Floating Differential Signals to the PCIe-7857



Analog Output

The PCIe-7857 provides connections for eight analog output channels. Each channel has an AO pin and AOGND pin to which you can connect a load.

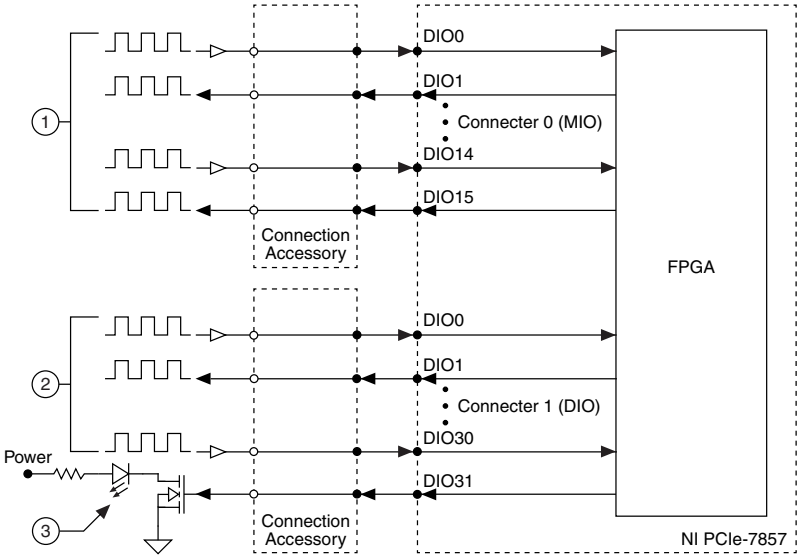
Figure 6. Connecting a Load



Digital I/O

The NI PCIe-7857 provides connections for 48 digital input/output (DIO) channels. Connector 0 contains 16 low-speed channels that can run up to 10 MHz signal frequencies. Connector 1 contains 32 high-speed DIO channels that can run up to 80 MHz signal frequencies and support external clock source. Each connector has selectable logic levels that you can configure as 1.2 V, 1.5 V, 1.8 V, 2.5 V, or 3.3 V. You can configure each channel as input or output.

Figure 7. Connecting to the DIO Channels



1. Low-speed signal frequencies up to 10 MHz with logic levels configured as 1.2 V, 1.5 V, 1.8 V, 2.5 V, or 3.3 V.
2. High-speed signal frequencies up to 80 MHz with logic levels configured as 1.2 V, 1.5 V, 1.8 V, 2.5 V, or 3.3 V.
3. LED

The DIO channels have overvoltage and undervoltage protection as well as over current protection. Refer to the device specifications on *ni.com/manuals* for more information about the maximum voltage and current.

When the system powers on, the DIO channels are set as input low with pull-down resistors. To set another power-on state, you can configure the NI PCIe-7857 to load a VI when the system powers on. The VI can then set the DIO lines to any power-on state.

All the high-speed DIO channels on Connector 1 are routed with a 50 Ω characteristic trace impedance. Route all external circuitry with a similar impedance to ensure best signal quality. NI recommends performing signal integrity measurements to test the affect of signal routing with the cable and connection accessory for your application.

Field Wiring Considerations

Environmental noise can seriously affect the measurement accuracy of the device if you do not take proper care when running signal wire between signal sources and the device. The following recommendations mainly apply to AI signal routing to the device, as well as signal routing in general.

Take the following precautions to minimize noise pickup and maximize measurement accuracy:

- Use differential AI connections to reject common-mode noise.
- Use individually shielded, twisted-pair wires to connect AI signals to the device. With this type of wire, the signal attached to the positive and negative inputs are twisted together and then covered with a shield. You then connect this shield only at one point to the signal source ground. This kind of connection is required for signals traveling through areas with large magnetic fields or high electromagnetic interference.
- Route signals to the device carefully. Keep cabling away from noise sources, such as video monitors and analog signals.

Use the following recommendations for all signal connections to the NI PCIe-7857:

- Separate NI PCIe-7857 signal lines from high-current or high-voltage lines. These lines can induce currents in or voltages on the NI PCIe-7857 signal lines if they run in parallel paths at a close distance. To reduce the magnetic coupling between lines, separate them by a reasonable distance if they run in parallel or run the lines at right angles to each other.
- Do not run signal lines through conduits that also contain power lines.
- Protect signal lines from magnetic fields caused by electric motors, welding equipment, breakers, or transformers by running them through special metal conduits.
- To minimize signal-to-signal skew within each digital channel, maintain signal lines' length within 1 inch of difference.

+5 V Power Source

Use the +5 V terminals on the I/O connector supply +5 V referenced to DGND to power external circuitry.

Caution Never connect the +5 V power terminals to analog or digital ground or any other voltage source on the NI PCIe-7857 or any other device. Doing so can damage the device and the computer. National Instruments is not liable for damage resulting from such a connection.

The power rating is 4.75 to 5.1 V DC at 0.5 A.

On-board Flash Memory

The PCIe-7857 includes a flash memory on-board, allowing users to store their FPGA bitfile in the flash memory with NI MAX. The user FPGA bitfile will be loaded from the flash memory after a system power cycle. For more information on downloading a bitfile to NI FPGA target, visit *ni.com/info* and enter the Info Code `dwnbitfile`.

Monitoring the Device Temperature

You can monitor the device temperature through the onboard temperature sensor of the PCIe-7857 using an FPGA I/O Node. After adding an FPGA I/O Node to the block diagram,

click the element section of the node, and select Device Temperature. The return value is in increments of 0.25 °C. For more details, refer to the NI PCIe-7857 Reference topic in LabVIEW Help.

Worldwide Support and Services

The NI website is your complete resource for technical support. At *ni.com/support*, you have access to everything from troubleshooting and application development self-help resources to email and phone assistance from NI Application Engineers.

Visit *ni.com/services* for information about the services NI offers.

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378052A-03 November 5, 2018