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**PXI-5404**

## SPECIFICATIONS

# PXI-5404

100 MHz Bandwidth, 12-Bit PXI Waveform Generator

## Contents

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## Conditions

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Specifications are valid under the following conditions unless otherwise noted:

- Ambient temperature range of 0 °C to 50 °C
- Output voltage amplitudes with a 50 Ω load
- SINE out voltage amplitude of 2 V<sub>pk-pk</sub> with a 50 Ω load
- CLOCK out level of 5 V
- External calibration performed between 18 °C and 28 °C

Typical specifications were determined on a small sampling of PXI-5404 waveform generators.

# CH 0 Outputs

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Both CH 0 outputs generate the same frequency simultaneously.

|                   |                   |
|-------------------|-------------------|
| Number of outputs | 1 sine<br>1 clock |
|-------------------|-------------------|

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## CH 0 SINE Out

---

|  |   |
|--|---|
| Connector type   | SMB male  |
| Frequency range  | 9 kHz to 105 MHz  |
| Frequency resolution   | 1.07 $\mu$ Hz   |
| Phase range  | 0° to 359.978°  |
| Phase resolution   | 16,384 steps including endpoints ( $\sim 0.022^\circ$ ) |
| Output impedance <sup>1</sup>  | 50 $\Omega$ , nominal                                   |
| Output protection  | 10 V RMS  |
| Sample rate  | 300 MS/s  |
| Amplitude range  |   |
| Open load  | 4 V pk-pk to 2 V pk-pk                                  |
| 50 $\Omega$ load   | 2 V pk-pk to 1 V pk-pk                                  |
| Amplitude resolution <sup>2</sup>  | 2,048 steps including endpoints                         |
| Amplitude accuracy (50 kHz)  | $\pm 1\%$   |
| Amplitude passband flatness (relative to the amplitude at 50 kHz) <sup>3</sup> | $\pm 0.2$ dB  |
| Vertical resolution (open load)  |   |
| 4 V pk-pk  | 12 bits   |
| 2 V pk-pk  | 11 bits   |
| Bandwidth (0.2 dB) <sup>4</sup>  | 105 MHz   |
| Filter   | Analog, 7-pole elliptical                               |

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<sup>1</sup> VSWR 2:1. Spans 9 kHz to 105 MHz.

<sup>2</sup> Steps are  $\sim 977$   $\mu$ V with an open load and  $\sim 489$   $\mu$ V with a 50  $\Omega$  load.

<sup>3</sup> 9 kHz  $< f < 105$  MHz. At 15 °C to 50 °C.

<sup>4</sup> At 15 °C to 50 °C.

**Table 1.** Signal to Noise and Distortion (SINAD)<sup>5</sup>

| Frequency | SINAD (dB), Typical |
|-----------|---------------------|
| 1 MHz     | +51                 |
| 10 MHz    | +48                 |
| 20 MHz    | +45                 |
| 50 MHz    | +42                 |
| 100 MHz   | +42                 |

**Table 2.** Spurious-Free Dynamic Range (SFDR) with Harmonics<sup>5</sup>

| Frequency | SFDR with Harmonics (dBc), Typical |
|-----------|------------------------------------|
| 1 MHz     | -55                                |
| 10 MHz    | -54                                |
| 20 MHz    | -49                                |
| 50 MHz    | -45                                |
| 100 MHz   | -53                                |

**Table 3.** Total Harmonic Distortion (THD)<sup>6</sup>

| Frequency | THD (dB), Typical |
|-----------|-------------------|
| 1 MHz     | -50               |
| 10 MHz    | -47               |
| 20 MHz    | -40               |
| 50 MHz    | -35               |
| 100 MHz   | -30               |

Average noise density<sup>7</sup>0.126  $\mu\text{V RMS}/\sqrt{\text{Hz}}$   
-125 dBm/Hz<sup>5</sup> Amplitude set to 1.8 Vpk-pk (~ -1 dBFS). Spans 9 kHz to 150 MHz.<sup>6</sup> Amplitude set to 1.8 Vpk-pk (~ -1 dBFS). Includes the 2nd through the 6th harmonics.<sup>7</sup> Integrated from 9 kHz to 150 MHz.

# CH 0 CLOCK Out

|                               |   |
|-------------------------------|---|
| Connector type                | SMB male                                    |
| Frequency range               | DC to 105 MHz                               |
| Frequency resolution          | 1.07 $\mu$ Hz                               |
| Phase range                   | 0° to 359.978°                              |
| Phase resolution              | 16,384 steps including endpoints (~ 0.022°) |
| Output impedance <sup>8</sup> | 50 $\Omega$ , nominal                       |
| Output protection             | +8 V to -4 V                                |

**Table 4.** Output Current (Source or Sink)

| Voltage Level | Current (mA), Typical |
|---------------|-----------------------|
| 5.0 V         | 120                   |
| 3.3 V         | 72                    |
| 1.8 V         | 48                    |

**Table 5.** Amplitude (Open Load)

| Voltage Level | Amplitude (V) |         |         |         |
|---------------|---------------|---------|---------|---------|
|               | VOL           |         | VOH     |         |
|               | Minimum       | Maximum | Minimum | Maximum |
| 5.0 V         | -0.10         | 0.40    | 4.00    | 5.30    |
| 3.3 V         |               |         | 2.60    | 3.70    |
| 1.8 V         |               |         | 1.40    | 2.20    |

<sup>8</sup> VSWR 1.7:1. Spans DC to 105 MHz.

**Table 6.** Amplitude (50  $\Omega$  Load)<sup>9</sup>

| Voltage Level | Amplitude (V) |         |         |         |
|---------------|---------------|---------|---------|---------|
|               | VOL           |         | VOH     |         |
|               | Minimum       | Maximum | Minimum | Maximum |
| 5.0 V         | -0.10         | 0.20    | 2.00    | 2.65    |
| 3.3 V         |               |         | 1.30    | 1.85    |
| 1.8 V         |               |         | 0.70    | 1.10    |

Rise/fall time (50  $\Omega$  load)

4 ns

Duty cycle range

25% to 75%

Duty cycle accuracy<sup>10</sup>

30% to 70%

 $\pm 2\%$ , typical

25% and 75%

 $\pm 4\%$ , typical

## PFI 0 I/O

Connector type

SMB male

Direction

Bidirectional

Frequency range

DC to 20 MHz

Input signal

Destinations

 PXI\_Trig <0..7> (backplane connector)  
 REF OUT (front panel connector)  
 Start Trigger

Input resistance

1 k $\Omega$   $\pm$  1%

Input protection

+8 V to -4 V

VIH

2.0 V

VIL

0.8 V

<sup>9</sup> If the CH 0 CLOCK out signal is terminated into a 50  $\Omega$  load, the voltage levels are divided by two.

<sup>10</sup> Spans 1.07  $\mu$ Hz to 60 MHz. SINE out at maximum amplitude.

## Output signal

|                                |  |
|--------------------------------|--|
| Sources                        | PXI_CLK10 (backplane connector)<br>Sample Timebase Clock (60 MHz) divided by $N$ ( $3 \leq N \leq 255$ )<br>REF IN (front panel connector)<br>PXI_Trig <0..7> (backplane connector)<br>PXI Star Trigger (backplane connector)<br>CH 0 CLOCK out (front panel connector)<br>Software Trigger<br>Start Trigger |
| Output impedance <sup>11</sup> | 50 $\Omega \pm 5\%$  |
| Output protection              | +6 V to -1 V   |
| Minimum VOH                    |  |
| Open load                      | 4.0 V  |
| 50 $\Omega$ load               | 2.0 V  |
| Maximum VOL                    |  |
| Open load                      | 0.4 V  |
| 50 $\Omega$ load               | 0.2 V  |
| Rise/fall time                 | 4 ns   |

## REF IN

|  |  |
|--|--|
| Connector type                                 | SMB male   |
| Frequency range                                |  |
| Phase-Locked Loop (PLL) Reference destination  | 1 MHz to 20 MHz  |
| All other destinations (besides PLL Reference) | 200 kHz to 30 MHz  |
| Destinations                                   | PLL Reference<br>REF OUT (front panel connector)<br>PFI 0 (front panel connector)<br>PXI_TRIG <0..7> (backplane connector) |
| Input impedance                                | 1 k $\Omega \pm 1\%$   |
| Input protection (sine or square wave)         | 12 V pk-pk $\pm$ 5 V DC  |

<sup>11</sup> Spans DC to 20 MHz.

|                                 |                           |
|---------------------------------|---------------------------|
| Amplitude (sine or square wave) | 300 mV pk-pk to 5 V pk-pk |
| Input coupling                  | AC                        |

## REF OUT

|                                   |   |
|-----------------------------------|---|
| Connector type                    | SMB male  |
| Frequency range                   | DC to 20 MHz  |
| Sources                           | PXI_CLK10 (backplane connector)<br>Sample Timebase Clock (60 MHz) divided by $N$ ( $3 \leq N \leq 255$ )<br>REF IN (front panel connector)<br>PXI_Trig <0..7> (backplane connector)<br>PXI Star Trigger (backplane connector)<br>CH 0 CLOCK out (front panel connector)<br>PFI 0 (front panel connector)<br>Software Trigger<br>Start Trigger |
| Output impedance <sup>12</sup>    | 50 $\Omega \pm 5\%$   |
| Output protection                 | +6 V to -1 V  |
| VOH                               |   |
| Open load                         | 4.0 V   |
| 50 $\Omega$ load                  | 2.0 V   |
| VOL                               |   |
| Open load                         | 0.4 V   |
| 50 $\Omega$ load                  | 0.2 V   |
| Rise/fall time (50 $\Omega$ load) | 4 ns  |

## Start Trigger

|         |   |
|---------|---|
| Sources | PFI 0 (front panel connector)<br>PXI_Trig<0..7> (backplane connector)<br>PXI Star Trigger (backplane connector)<br>Software<br>Immediate (Does not wait for a trigger.) <sup>13</sup> |
| Mode    | Continuous  |

<sup>12</sup> Spans DC to 20 MHz.

<sup>13</sup> The default is Immediate.



|                              |                      |
|------------------------------|----------------------|
| Trigger detection            | Edge (rising)        |
| Minimum pulse width          | 10 ns                |
| Trigger to SINE output delay | 250 $\mu$ s, typical |

## Sample Clock

|   |             |
|---|-------------|
| Frequency                                 | 300 MS/s    |
| Average phase noise density <sup>14</sup> | -112 dBc/Hz |

## Phase-Locked Loop (PLL) Reference

|                         |   |
|-------------------------|---|
| Sources                 | PXI_CLK10 (backplane connector)<br>REF IN (front panel connector)<br>PXI_TRIG <0..7> (backplane connector)<br>None (The PLL is not used.) <sup>15</sup> |
| Frequency accuracy      | When using the PLL, the frequency accuracy of the PXI-5404 is solely dependent on the frequency accuracy of the PLL Reference source.                   |
| Lock time               | 200 ms, typical   |
| Frequencies             | 3 MHz to 20 MHz in 1 MHz increments   |
| Frequency locking range | $\pm$ 50 ppm  |
| Duty cycle range        | 30% to 70%  |

## Internal Clock

|                                   |  |
|-----------------------------------|--|
| Clock source                      | The clock circuitry of the PXI-5404 can either be locked to a reference signal using the PLL or use an onboard frequency reference, specifically the Internal Clock. |
| Frequency accuracy <sup>16</sup>  | $\pm$ 25 ppm, maximum<br>$\pm$ 11 ppm, typical   |
| Frequency temperature coefficient | $\pm$ 0.4 ppm/ $^{\circ}$ C  |

<sup>14</sup> SINE out set to 10 MHz. Offset of 10 kHz  $\pm$  500 Hz. PLL Reference set to REF IN.

<sup>15</sup> The default is None. Refer to [Internal Clock](#) for more information.

<sup>16</sup> At 18  $^{\circ}$ C to 28  $^{\circ}$ C.

# External Calibration

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|                      |  |
|----------------------|--|
| Calibration interval | Specifications valid within one year of external calibration |
| Warm-up time         | 15 minutes   |

---

## Power<sup>17</sup>

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|             |        |
|-------------|--------|
| +3.3 V rail | 1 A    |
| +5 V rail   | 550 mA |
| +12 V rail  | 180 mA |
| -12 V rail  | 50 mA  |

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## Environment

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|                       |                 |
|-----------------------|-----------------|
| Operating temperature | 0 °C to 50 °C   |
| Storage temperature   | -20 °C to 70 °C |

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## Physical

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|            |  |
|------------|--|
| Dimensions | 3U, one-slot, PXI/cPCI module<br>21.6 cm × 2.0 cm × 13.0 cm<br>(8.5 in. × 0.8 in. × 5.1 in.) |
| Weight     | 175 g (6.1 oz)   |

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# Compliance and Certifications

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## Safety

This product is designed to meet the requirements of the following electrical equipment safety standards for measurement, control, and laboratory use:

- IEC 61010-1, EN 61010-1
- UL 61010-1, CSA C22.2 No. 61010-1



**Note** For UL and other safety certifications, refer to the product label or the [Online Product Certification](#) section.

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<sup>17</sup> With SINE out, CLOCK out, and REF OUT generating maximum amplitude waveforms into 50 Ω loads.

# Electromagnetic Compatibility

This product meets the requirements of the following EMC standards for electrical equipment for measurement, control, and laboratory use:

- EN 61326-1 (IEC 61326-1): Class A emissions; Basic immunity
- EN 55011 (CISPR 11): Group 1, Class A emissions
- AS/NZS CISPR 11: Group 1, Class A emissions
- FCC 47 CFR Part 15B: Class A emissions
- ICES-001: Class A emissions



**Note** In the United States (per FCC 47 CFR), Class A equipment is intended for use in commercial, light-industrial, and heavy-industrial locations. In Europe, Canada, Australia, and New Zealand (per CISPR 11), Class A equipment is intended for use only in heavy-industrial locations.



**Note** Group 1 equipment (per CISPR 11) is any industrial, scientific, or medical equipment that does not intentionally generate radio frequency energy for the treatment of material or inspection/analysis purposes.



**Note** For EMC declarations and certifications, refer to the [Online Product Certification](#) section.

## CE Compliance

This product meets the essential requirements of applicable European Directives, as follows:

- 2014/35/EU; Low-Voltage Directive (safety)
- 2014/30/EU; Electromagnetic Compatibility Directive (EMC)

## Online Product Certification

Refer to the product Declaration of Conformity (DoC) for additional regulatory compliance information. To obtain product certifications and the DoC for this product, visit [ni.com/certification](https://ni.com/certification), search by model number or product line, and click the appropriate link in the Certification column.

## Environmental Management

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