NI PXI/PCI-6561/6562 Specifications

100/200 MHz Digital Waveform Generator/Analyzer

このドキュメントには、日本語ページも含まれています。

This document provides the specifications for the NI PXI/PCI-6561 (NI 6561) and the NI PXI/PCI-6562 (NI 6562), collectively called the NI 656*x*.

Typical values are representative of an average unit operating at room temperature. Specifications are subject to change without notice. For the most recent NI 656*x* specifications, visit `ni.com/manuals`.

To access the NI 656*x* documentation, including the *NI Digital Waveform Generator/Analyzer Getting Started Guide*, which contains functional descriptions of the NI 656*x* signals, navigate to **Start»All Programs» National Instruments»NI-HSDIO»Documentation**.

Caution If the NI 656*x* has been in use, it may exceed safe handling temperatures and cause burns. Allow the NI 656*x* to cool before removing it from the chassis.

Contents

NATIONAL INSTRUMENTS

Channel Specifications

<table>
<tr><th>Specification</th><th colspan="4">Value</th><th>Comments</th></tr>
<tr><td>Number of data channels</td><td colspan="4">16</td><td>—</td></tr>
<tr><td rowspan="3">Direction control of data channels</td><td colspan="2">Single Data Rate (SDR)</td><td colspan="2">Double Data Rate (DDR)</td><td rowspan="3">Using SDR, data is clocked using the rising or falling edge of the Sample clock. Using DDR, data is clocked using both edges of the Sample clock.</td></tr>
<tr><td rowspan="2">Data<0..15></td><td rowspan="2">Per channel</td><td>Data<0..7></td><td>Dedicated for data generation</td></tr>
<tr><td>Data<8..15></td><td>Dedicated for data acquisition</td></tr>
<tr><td>Number of Programmable Function Interface (PFI) channels</td><td colspan="4">4</td><td>Refer to the Waveform Specifications section for more details.</td></tr>
<tr><td>Direction control of PFI channels</td><td colspan="4">Per channel</td><td>—</td></tr>
<tr><td>Number of clock terminals</td><td colspan="4">3 input
3 output</td><td>Refer to the Timing Specifications section for more details.</td></tr>
</table>

Generation Channels (Data, DDC CLK OUT, and PFI <0..3>)

Specification	Value									Comments
Generation voltage families	**Data<0..15>, PFI <1..2>, DDC CLK OUT LVDS**			**DDC CLK OUT LVPECL**			**PFI 0**		**PFI 3**	—
	LVDS			LVPECL			LVCMOS		LVDS or LVCMOS (software selectable)	
Generation voltage levels (LVDS)	**Offset (V_{os})**						**Differential Voltage (V_{od})**			Into 100 Ω differential load, TIA/EIA-644 compliant
	Min	**Typ**	**Max**				**Min**	**Typ**	**Max**	
	1.125 V	1.220 V	1.375 V				247 mV	305 mV	454 mV	
Generation voltage levels (LVCMOS)	**Low Voltage Levels**						**High Voltage Levels**			—
	Max						**Min**			
	0.2 V						2.8 V			
Generation voltage levels (LVPECL)	**Single Ended Output High**						**Single Ended Output Low**			Into open load.
	Min			**Max**			**Min**		**Max**	
	2.16 V			2.50 V			1.38 V		1.72 V	
Output impedance	**LVDS**						**LVCMOS/LVPECL**			Nominal
	100 Ω differential						50 Ω series			
Data channel driver enable/disable control	Per channel									Software-selectable
Channel power-on state	Drivers disabled, 100 Ω differential impedance Data channels have a weak pull-up resistor (300 kΩ), internal to the I/0 buffer, to 3.3 V. This internal pull-up resistor is a fail-safe mechanism intended to set a known state when the receiver circuit is not being driven.									PFI 3 powers up in LVDS mode.
Output protection	Each channel can indefinitely sustain a short to any voltage between 0 and 5 V and is protected from up to 12 kV ESD.									—

Acquisition Channels (Data, STROBE, and PFI <0..3>)

<table>
<tr><th>Specification</th><th colspan="3">Value</th><th>Comments</th></tr>
<tr><td rowspan="2">Acquisition voltage families</td><td>Data <0..15>, PFI <1..2> and STROBE</td><td>PFI 0</td><td>PFI 3</td><td rowspan="2">—</td></tr>
<tr><td>LVDS</td><td>LVCMOS</td><td>LVDS or LVCMOS (software-selectable)</td></tr>
<tr><td rowspan="3">Acquisition voltage levels (LVDS)</td><td colspan="2">Voltage Threshold</td><td colspan="2">Voltage Range</td><td rowspan="3">TIA/EIA-644 compliant</td></tr>
<tr><td>Max[1]</td><td>Min</td><td>Max</td></tr>
<tr><td>±50 mV</td><td>0 V</td><td>2.4 V</td></tr>
<tr><td rowspan="3">Acquisition voltage levels (LVCMOS)</td><td colspan="2">Low Voltage Threshold</td><td colspan="2">High Voltage Threshold</td><td rowspan="3">—</td></tr>
<tr><td colspan="2">Max</td><td colspan="2">Min</td></tr>
<tr><td colspan="2">0.8 V</td><td colspan="2">2 V</td></tr>
<tr><td rowspan="3">Input impedance</td><td colspan="2">LVDS</td><td colspan="2">LVCMOS</td><td rowspan="3">PFI 3 powers up in LVDS mode.</td></tr>
<tr><td colspan="2">100 Ω differential</td><td colspan="2">10 kΩ</td></tr>
<tr><td colspan="4">Data channels have a weak pull-up resistor (300 kΩ), internal to the I/O buffer, to 3.3 V. This internal pull-up resistor is a fail-safe mechanism intended to set a known state when the receiver circuit is not being driven.</td></tr>
<tr><td>Input protection</td><td colspan="3">Each channel can indefinitely sustain a short to any voltage between 0 and 5 V and is protected from up to 12 kV ESD.</td><td>—</td></tr>
<tr><td colspan="5">[1] The device under test must supply more than 50 mV of differential voltage.</td></tr>
</table>

Timing Specifications

Sample Clock

Specification	Value	Comments
Sample clock sources	1. On Board Clock (internal voltage-controlled crystal oscillator (VCXO) with divider) 2. CLK IN (SMB jack connector) 3. PXI_STAR (PXI backplane—PXI only) 4. STROBE (Digital Data & Control (DDC) connector; acquisition only)	—
On Board Clock frequency range	**NI 6561**: 48 Hz to 100 MHz Configurable to 200 MHz/*N*; $2 \le N \le 4{,}194{,}304$ **NI 6562**: 48 Hz to 200 MHz Configurable to 200 MHz/*N*; $1 \le N \le 4{,}194{,}304$	—
CLK IN frequency range	**NI 6561**: 20 kHz to 100 MHz **NI 6562**: 20 kHz to 200 MHz	Refer to the *CLK IN (SMB Jack Connector)* section for restrictions based on waveform type.
PXI_STAR frequency range (PXI only)	48 Hz to 70 MHz	Refer to the *PXI_STAR (PXI Backplane)* section.
STROBE frequency range	**NI 6561**: 48 Hz to 100 MHz **NI 6562**: 48 Hz to 200 MHz	Refer to the *STROBE (DDC Connector)* section.

<table>
<tr><th>Specification</th><th colspan="2">Value</th><th>Comments</th></tr>
<tr><td>Sample clock relative delay adjustment range</td><td colspan="2">0 to 1 Sample clock period</td><td rowspan="2">You can apply a delay or phase adjustment to the On Board Clock to align multiple devices.</td></tr>
<tr><td>Sample clock relative delay adjustment resolution</td><td colspan="2">10 ps</td></tr>
<tr><td>Exported Sample clock destinations</td><td colspan="2">1. DDC CLK OUT (DDC connector)
Note: Selecting DDC CLK OUT in software will export the internal Sample clock to the DDC CLK OUT LVDS and DDC CLK OUT LVPECL terminals.
2. CLK OUT (SMB jack connector)</td><td>Internal Sample clocks with sources other than STROBE can be exported.</td></tr>
<tr><td rowspan="3">Exported Sample clock delay</td><td>Frequency Range</td><td>Delay Range</td><td rowspan="3">Supported for clock frequencies ≥25 MHz</td></tr>
<tr><td>25 to <50 MHz</td><td>0.0 to 1.0 Sample clock periods;
Refer to Figure 1, Valid Data Position Delay Ranges, for more information.</td></tr>
<tr><td>50 MHz to max clock frequency</td><td>0.0 to 1.0 Sample clock periods</td></tr>
<tr><td>Exported Sample clock delay resolution (δ_C)</td><td colspan="2">1/256 of Sample clock period or 60 ps, whichever is greater</td><td>Supported for clock frequencies ≥25 MHz</td></tr>
<tr><td rowspan="2">Exported Sample clock jitter</td><td>Period Jitter</td><td>Cycle-to-Cycle Jitter</td><td rowspan="2">Typical; using On Board Clock</td></tr>
<tr><td>19 ps_{rms}</td><td>29 ps_{rms}</td></tr>
<tr><td>Exported Sample clock transition time</td><td colspan="2">1 ns</td><td>—</td></tr>
<tr><td>Exported Sample clock duty cycle</td><td colspan="2">47 to 53%</td><td>—</td></tr>
</table>

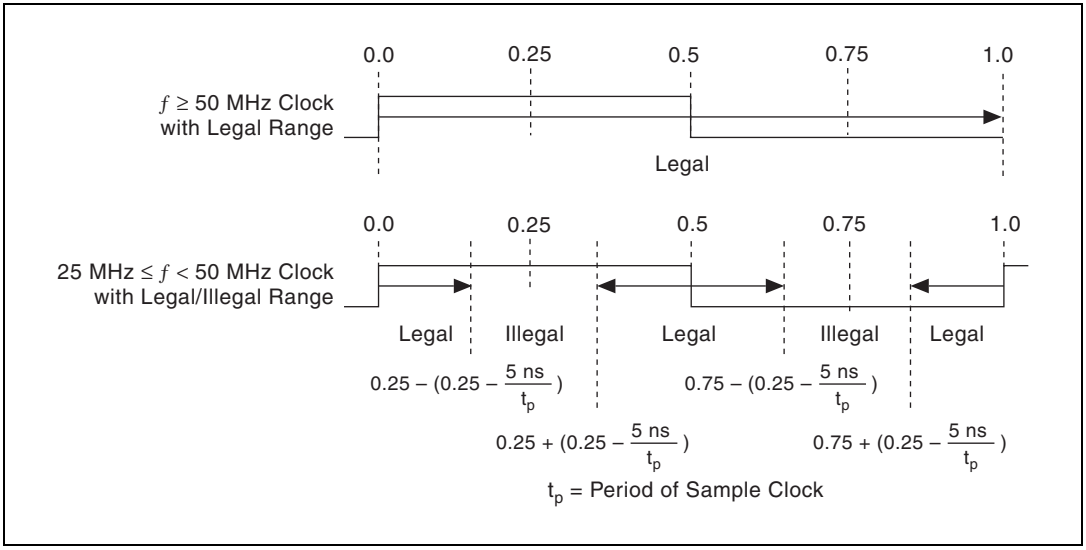


Figure 1. Valid Data Position Delay Ranges

Generation Timing (Data, DDC CLK OUT, and PFI <0..3> Channels)

Specification	Value				Comments
Data channel-to-channel skew	**Typical**		**Max**		Across all data channels and PFI <1..2>
	±215 ps		±500 ps		
Maximum data channel toggle rate	**Single Data Rate (SDR)**		**Double Data Rate (DDR)**		—
	NI 6561	**NI 6562**	**NI 6561**	**NI 6562**	
	50 MHz	100 MHz	100 MHz	200 MHz	
Data position modes	Rising edge, Falling edge, or Delayed				Relative to Sample clock

Specification	Value		Comments
Generation data delay (δ_G)	**Frequency Range**	**Delay Range**	Supported for clock frequencies ≥25 MHz
	25 to 50 MHz	0.0 to 1.0 Sample clock periods; Refer to Figure 1, *Valid Data Position Delay Ranges*, for more information.	
	50 MHz to max clock frequency	0.0 to 1.0 Sample clock periods	
Generation data delay resolution (δ_G)	1/256 of Sample clock period or 60 ps, whichever is greater		Supported for clock frequencies ≥25 MHz

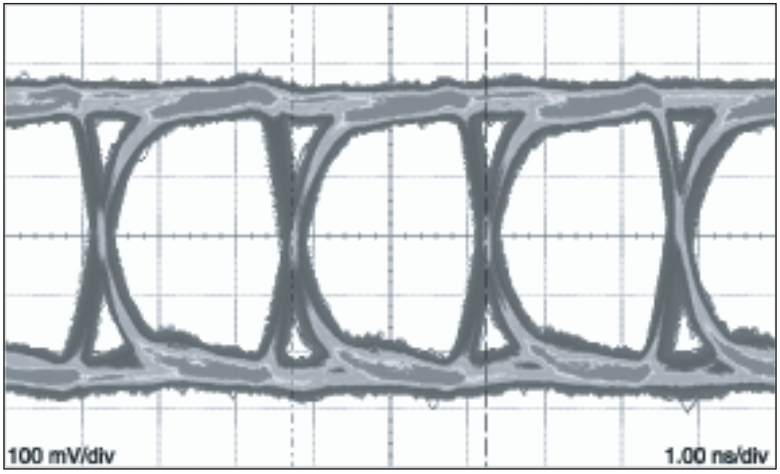


Figure 2. Eye Diagram[1]

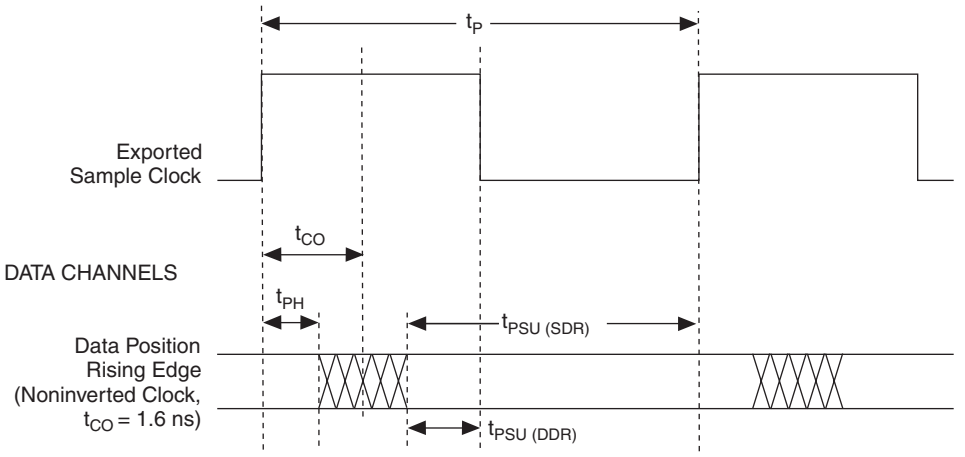
[1] This eye diagram was captured on DIO 0 (200 MHz clock rate in DDR mode) at room temperature into 100 Ω differential terminating resistance.

<table>
<tr><th>Specification</th><th colspan="4">Value</th><th>Comments</th></tr>
<tr><td>Data transition time</td><td colspan="4">1 ns maximum
Transition time could be as fast as 610 ps.</td><td>20 to 80% transitions.</td></tr>
<tr><td rowspan="2">PFI transition time</td><td>PFI 0</td><td>PFI <1..2></td><td>PFI 3 (LVCMOS)</td><td>PFI 3 (LVDS)</td><td rowspan="2">Typical.
20 to 80% transitions.</td></tr>
<tr><td>6 ns</td><td>2.5 ns</td><td>6 ns</td><td>4.2 ns</td></tr>
<tr><td>Exported Sample clock offset (t_{CO})</td><td colspan="4">1.6 ns</td><td>Refer to Figure 3, Generation Provided Setup and Hold Times Timing Diagram.</td></tr>
<tr><td>Time delay from internal Sample clock to DDC Connector (t_{SCDDC})</td><td colspan="4">5.8 ns</td><td>Typical.</td></tr>
<tr><td rowspan="2">Exported Sample clock offset to selectable PFI</td><td colspan="2">LVDS (t_{CPD})</td><td colspan="2">LVCMOS (t_{CPS})</td><td rowspan="2">Typical.</td></tr>
<tr><td colspan="2">2 ns</td><td colspan="2">3.45 ns</td></tr>
<tr><td rowspan="2">Generation provided setup and hold times</td><td colspan="2">Minimum Provided Setup Time (t_{SUP})</td><td colspan="2">Minimum Provided Hold Time (t_{HP})</td><td rowspan="2">Exported Sample clock mode set to Noninverted.</td></tr>
<tr><td colspan="2">t_p – 2.2 ns</td><td colspan="2">1.1 ns</td></tr>
<tr><td colspan="6">Compare the setup and hold times from the datasheet of your device under test (DUT) to the values in the preceding table. The provided setup and hold times must be greater than the setup and hold times required for the DUT. If you require more setup time, configure your exported Sample clock mode as Inverted and/or delay your data relative to the Sample clock.

Refer to Figure 3, Generation Provided Setup and Hold Times Timing Diagram, for a diagram illustrating the relationship between the exported Sample clock mode and the provided setup and hold times.

Notes: This table assumes the Data Position is set to the rising edge of the Sample clock and that the Sample clock is exported to the DDC connector.

This table includes worst-case effects of channel-to-channel skew, inter-symbol interference, and jitter.</td></tr>
</table>



$t_P = \frac{1}{f}$ = Period of Sample Clock

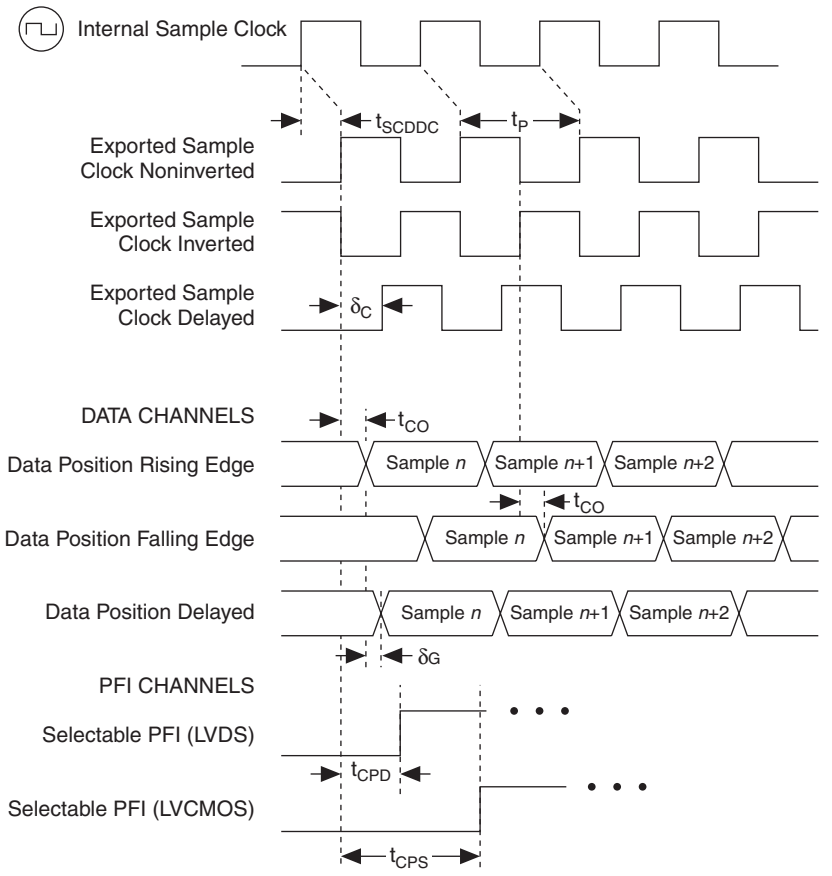
t_{PH} = Minimum Provided Hold Time

t_{PSU} = Minimum Provided Setup Time; SDR = Single Data Rate, DDR = Double Data Rate

t_{CO} = Exported Sample Clock Offset

Note: At 25 MHz and higher, STROBE duty cycle is corrected to 50%.

Figure 3. Generation Provided Setup and Hold Times Timing Diagram



t_{SCDDC} = Time Delay from Sample Clock (Internal) to DDC Connector Exported Sample Clock

$0 \le \delta_C \le 1$: Exported Sample Clock Delay (Fraction of t_P)

$0 \le \delta_G \le 1$: Pattern Generation Data Delay (Fraction of t_P)

$t_P = \frac{1}{f}$ = Period of Sample Clock

t_{CO} = Exported Sample Clock Offset

t_{CPD} = Exported Sample Clock to Selectable PFI Offset (LVDS)

t_{CPS} = Exported Sample Clock to Selectable PFI Offset (LVCMOS)

Figure 4. Generation Timing Diagram[1]

[1] SDR mode generation shown.

Acquisition Timing (Data, STROBE, and PFI <0..3> Channels)

Specification	Value				Comments
Channel-to-channel skew	$f \geq 25$ MHz		$f < 25$ MHz		Across all data channels and PFI<1..2>
	Typ	Max	Typ	Max	
	±330 ps	±600 ps	±600 ps	±1.2 ns	
Data position modes	Rising edge, Falling edge, or Delayed				Relative to Sample clock
Setup time to STROBE (t_{SUS})	$f \geq 25$ MHz = 1.1 ns $f < 25$ MHz = 1.8 ns **Note**: At 25 MHz and higher, STROBE duty cycle is corrected to 50% while maintaining rising edge placement.				Maximum; includes maximum data channel-to-channel skew
Hold time to STROBE (t_{HS})	$f \geq 25$ MHz = 0.8 ns $f < 25$ MHz = 2.1 ns **Note**: At 25 MHz and higher, STROBE duty cycle is corrected to 50% while maintaining rising edge placement.				Maximum; includes maximum data channel-to-channel skew
Time delay from DDC connector data to internal Sample clock (t_{DDCSC})	$f \geq 25$ MHz = 5.6 ns $f < 25$ MHz = 6.6 ns				Typical
Setup time to Sample clock (t_{SUSC})	$f \geq 25$ MHz = 0.9 ns $f < 25$ MHz = 1.9 ns				Does not include data channel-to-channel skew, t_{DDCSC}, or t_{SCDDC}
Hold time to Sample clock (t_{HSC})	$f \geq 25$ MHz = –0.4 ns $f < 25$ MHz = –0.6 ns				Does not include data channel-to-channel skew, t_{DDCSC}, or t_{SCDDC}

Specification	Value		Comments
Acquisition data delay (δ_A)	**Frequency Range**	**Delay Range**	Supported for clock frequencies ≥25 MHz
	25 to <50 MHz	0.0 to 1.0 Sample clock periods; Refer to Figure 1, *Valid Data Position Delay Ranges*, for more information.	
	50 MHz to max clock frequency	0.0 to 1.0 Sample clock period	
Acquisition data delay resolution (δ_A)	1/256 of Sample clock period or 60 ps, whichever is greater		Supported for clock frequencies ≥25 MHz

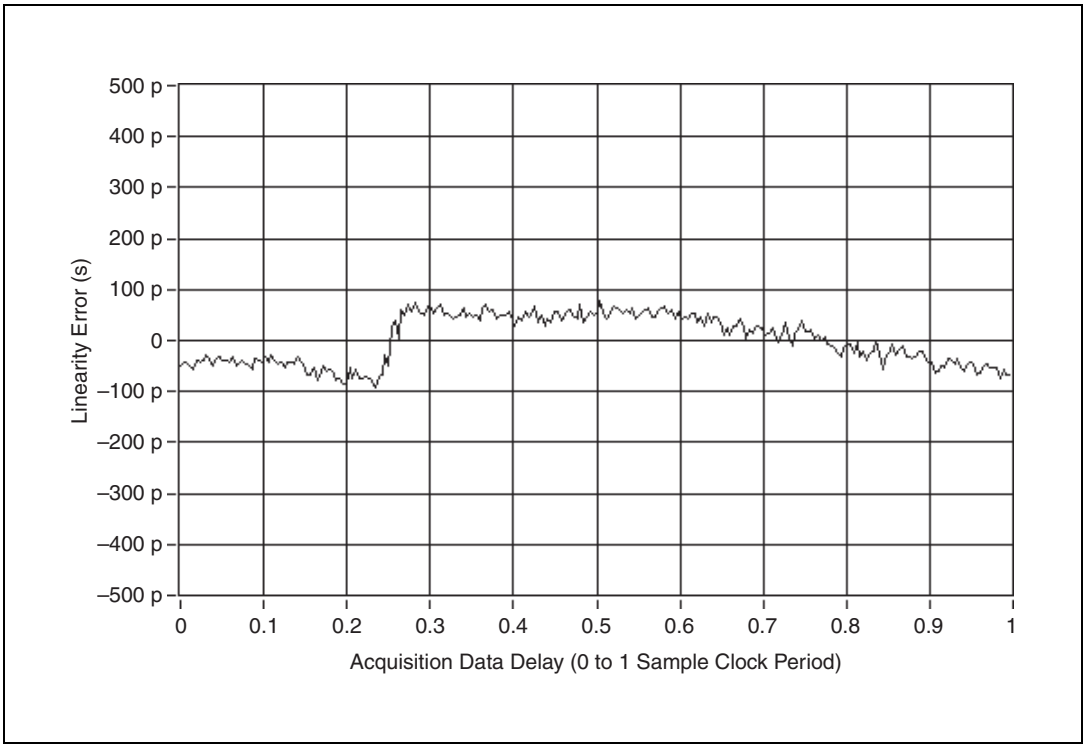
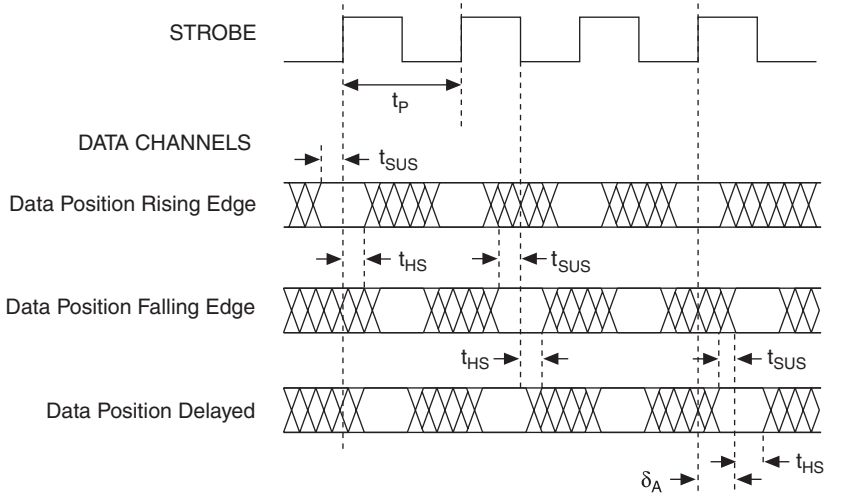


Figure 5. Acquisition Data Delay Normalized Linearity



t_{SUS} = Set-up Time to STROBE

t_{HS} = Hold Time from STROBE

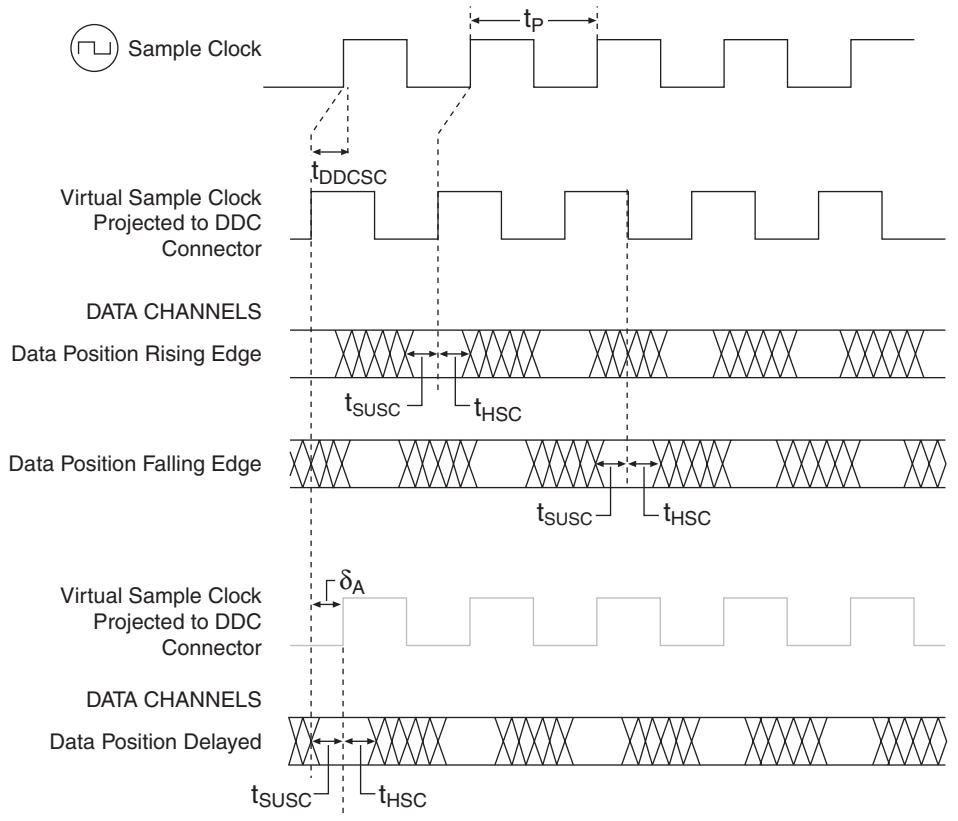
$0 \leq \delta_A \leq 1$: Pattern Acquisition Data Delay (fraction of tP)

$t_P = \frac{1}{f}$ = Period of Sample Clock

Note: At 25 MHz and higher, STROBE duty cycle is corrected to 50% while maintaining rising edge placement.

Figure 6. Acquisition Timing Diagram Using STROBE as the Sample Clock[1]

[1] SDR mode acquisition shown.



t_{DDCSC} : Time Delay from DDC Connector to Internal Sample Clock

$0 \leq \delta_A \leq 1$: Pattern Acquisition Data Delay (fraction of t_P)

$t_P = \frac{1}{f}$ = Period of Sample Clock

t_{SUSC} = Set-Up Time to Sample Clock

t_{HSC} = Hold Time to Sample Clock

Figure 7. Acquisition Timing Diagram with Sample Clock Sources Other than STROBE[1]

[1] SDR mode acquisition shown.

CLK IN (SMB Jack Connector)

Specification	Value				Comments
Direction	Input into device				—
Destinations	1. Reference clock (for the phase lock loop (PLL)) 2. Sample clock				—
Input coupling	AC				—
Input protection	±10 VDC				—
Input impedance	50 Ω (default) or 1 kΩ				Software-selectable
Minimum detectable pulse width	2 ns				—
Clock requirements	Clock must be continuous.				—
As Sample Clock					
External Sample clock range	**Square Waves**				—
	Voltage range	0.65 to 5.0 V_{pp}			
	Frequency range	**NI 6561**: 20 kHz to 100 MHz			
		NI 6562: 20 kHz to 200 MHz			
	Duty cycle range	f < 50 MHz: 25 to 75% f ≥ 50 MHz: 40 to 60%			
	Sine Waves				
	Voltage range	0.65 to 5.0 V_{pp}	1.0 to 5.0 V_{pp}	2.0 to 5.0 V_{pp}	
	Frequency range	**NI 6561**: 5.5 to 100 MHz	**NI 6561**: 3.5 to 100 MHz	**NI 6561**: 1.8 to 100 MHz	
		NI 6562: 5.5 to 200 MHz	**NI 6562**: 3.5 to 200 MHz	**NI 6562**: 1.8 to 200 MHz	

Specification	Value	Comments
As Reference Clock		
Reference clock frequency range	10 MHz ±50 ppm	—
Reference clock voltage range	0.65 to 5.0 V_{pp}	—
Reference clock duty cycle	25 to 75%	—

STROBE (DDC Connector)

Specification	Value	Comments
Direction	Input into device	—
Destinations	Sample clock (acquisition only)	—
STROBE frequency range	**NI 6561**: 48 Hz to 100 MHz **NI 6562**: 48 Hz to 200 MHz	—
STROBE duty cycle range	**NI 6561**: 25 to 75% for clock frequencies <50 MHz **NI 6562**: 40 to 60% for clock frequencies ≥50 MHz 25 to 75% for clock frequencies <50 MHz	—
Minimum detectable pulse width	2 ns	—
Clock requirements	Clock must be continuous.	—
Input impedance	100 Ω differential Data channels have a weak pull-up resistor (300 kΩ), internal to the I/O buffer, to 3.3 V. This internal pull-up resistor is a fail-safe mechanism intended to set a known state when the receiver circuit is not being driven.	—

PXI_STAR (PXI Backplane)

Specification	Value	Comments
Direction	Input into device	—
Destinations	1. Sample clock 2. Start trigger 3. Reference trigger (acquisition sessions only) 4. Advance trigger (acquisition sessions only) 5. Pause trigger (generation sessions only) 6. Script trigger <0..3> (generation sessions only)	—
PXI_STAR frequency range	48 Hz to 70 MHz	—
Clock requirements	Clock must be continuous.	—

CLK OUT (SMB Jack Connector)

Specification	Value	Comments
Direction	Output from device	—
Sources	1. Sample clock (excluding STROBE) 2. Reference clock (PLL)	—
Output impedance	50 Ω nominal	—
Voltage families	LVCMOS	—
Maximum drive current	32 mA	—

DDC CLK OUT LVDS (DDC Connector)

Specification	Value						Comments
Direction	Output from device						—
Sources	Sample clock **Note**: Exporting the internal Sample clock to DDC CLK OUT in software will export the internal Sample clock to the DDC CLK OUT LVDS and DDC CLK OUT LVPECL terminals.						STROBE cannot be routed to DDC CLK OUT.
Voltage families	LVDS						—
Voltage levels	**Offset (V_{os})**			**Differential Voltage (V_{od})**			Into 100 Ω differential load, TIA/EIA-644 compliant
	Min	**Typ**	**Max**	**Min**	**Typ**	**Max**	
	1.125 V	1.220 V	1.375 V	247 mV	305 mV	454 mV	
Transition time	1 ns						—
Output impedance	100 Ω differential						—
Output protection	This terminal can indefinitely sustain a short to any voltage between 0 and 5 V and is protected from up to 15 kV ESD.						—

DDC CLK OUT LVPECL (DDC Connector)

Specification	Value				Comments
Direction	Output from device				—
Source	Sample clock **Note**: Exporting the internal Sample clock to DDC CLK OUT in software will export the internal Sample clock to the DDC CLK OUT LVDS and DDC CLK OUT LVPECL terminals.				STROBE cannot be routed to DDC CLK OUT.
Voltage families	LVPECL				—
Voltage levels	**Single-Ended Output High**		**Single-Ended Output Low**		Into open load
	Min	**Max**	**Min**	**Max**	
	2.16 V	2.50 V	1.38 V	1.72 V	

Specification	Value	Comments
Transition time	1 ns	—
Output impedance	50 Ω source series nominal	Series impedance on each polarity
Output protection	This terminal can indefinitely sustain a short to any voltage between 0 and 5 V and is protected from up to 15 kV ESD.	—

Reference Clock (PLL)

Specification	Value	Comments
Reference clock sources	1. PXI_CLK10 (PXI backplane—PXI only) 2. RTSI 7 (PCI only) 3. CLK IN (SMB jack connector) 4. None (onboard clock source not locked to a reference)	Provides the reference frequency for the phase lock loop
Lock time	400 ms	Typical
Reference clock frequencies	10 MHz ±50 ppm	—
Reference clock duty cycle range	25 to 75%	—
Reference clock destinations	CLK OUT (SMB jack connector)	—

Waveform Specifications

Memory and Scripting

Specification	Value			Comments
Memory architecture	The NI 656*x* uses the Synchronization and Memory Core (SMC) technology in which waveforms and instructions share onboard memory. Parameters such as number of script instructions, maximum number of waveforms in memory, and number of samples (S) available for waveform storage are flexible and user-defined.			Refer to the *Onboard Memory* section in the *NI Digital Waveform Generator/ Analyzer Help* for more information.
Onboard memory size	2 Mbit/channel (for generation sessions) 2 Mbit/channel (for acquisition sessions)	16 Mbit/channel (for generation sessions) 16 Mbit/channel (for acquisition sessions)	128 Mbit/channel (for generation sessions) 128 Mbit/channel (for acquisition sessions)	Maximum limit for generation sessions assumes no scripting instructions. Onboard memory size doubles with 8-bit data width (DDR mode).
Generation modes	**Single-waveform mode**: Generate a single waveform once, *n* times, or continuously.			—
	Scripted mode: Generate a simple or complex sequence of waveforms. Use scripts to describe the waveforms to be generated, the order in which the waveforms are generated, how many times the waveforms are generated, and how the device responds to Script triggers.			

<table>
<tr><th>Specification</th><th colspan="3">Value</th><th>Comments</th></tr>
<tr><td rowspan="6">Generation minimum waveform size</td><td rowspan="2">Configuration</td><td colspan="2">Sample Rate</td><td rowspan="6">Sample rate dependent. Increasing sample rate increases minimum waveform size requirement.
For information on these configurations, refer to Common Scripting Use Cases in the NI Digital Waveform Generator/ Analyzer Help.</td></tr>
<tr><td>200 MHz (NI 6562 only)</td><td>100 MHz</td></tr>
<tr><td>Single waveform</td><td>4 S</td><td>4 S</td></tr>
<tr><td>Continuous waveform</td><td>64 S</td><td>32 S</td></tr>
<tr><td>Stepped sequence</td><td>256 S</td><td>128 S</td></tr>
<tr><td>Burst sequence</td><td>1,024 S</td><td>512 S</td></tr>
<tr><td colspan="3">Note: Waveform quantum and block size double when using 8-bit data width (DDR mode).</td></tr>
<tr><td>Generation finite repeat count</td><td colspan="3">1 to 16,777,216</td><td>—</td></tr>
<tr><td>Generation waveform quantum</td><td colspan="3">Waveform size must be an integer multiple of 4 S.
Note: Waveform quantum and block size double when using 8-bit data width (DDR mode).</td><td>Regardless of waveform size, NI-HSDIO allocates waveforms into block sizes of 64 S of physical memory.</td></tr>
<tr><td>Acquisition minimum record size</td><td colspan="3">1 S</td><td>Regardless of waveform size, NI-HSDIO allocates at least 128 bytes for a record.</td></tr>
<tr><td>Acquisition record quantum</td><td colspan="3">1 S</td><td>—</td></tr>
</table>

Specification	Value	Comments
Acquisition maximum number of records	2,147,483,647	The maximum value varies based on the memory size of your device and memory consumed by saved scripts.
Acquisition number of pre-Reference trigger samples	0 up to full record	—
Acquisition number of post-Reference trigger samples	0 up to full record	—

Triggers (Inputs to the NI 656*x*)

Specification	Value	Comments
Trigger types	1. Start trigger 2. Pause trigger 3. Script trigger <0..3> (generation sessions only) 4. Reference trigger (acquisition sessions only) 5. Advance trigger (acquisition sessions only)	—
Sources	1. PFI 0 (SMB jack connector) 2. PFI <1..3> (DDC connector) 3. PXI_TRIG<0..7> (PXI backplane—PXI only)/ RTSI<0..7> (RTSI bus—PCI only) 4. PXI_STAR (PXI backplane—PXI only) 5. Pattern match (acquisition sessions only) 6. Software (user function call) 7. Disabled (do not wait for a trigger)	—

<table>
<tr><th>Specification</th><th>Value</th><th>Comments</th></tr>
<tr><td>Trigger detection</td><td>1. Start trigger (edge detection: rising or falling)
2. Pause trigger (level detection: high or low)
3. Script trigger <0..3> (edge detection: rising or falling; level detection: high or low)
4. Reference trigger (edge detection: rising or falling)
5. Advance trigger (edge detection: rising or falling)</td><td>—</td></tr>
<tr><td rowspan="2">Minimum required trigger pulse width</td><td>Generation Triggers</td><td>Acquisition Triggers</td><td></td></tr>
<tr><td>30 ns</td><td>Acquisition triggers must meet setup and hold time requirements.
For triggers synchronous to STROBE, triggers must meet setup and hold requirements. For asynchronous triggers, pulse width must be larger than the greater of 30 ns or Clock Period + Setup + Hold</td><td>—</td></tr>
<tr><td rowspan="2">Trigger rearm time</td><td>Start to Reference Trigger</td><td>Start to Advance Trigger</td><td>Reference to Reference Trigger</td><td rowspan="2">—</td></tr>
<tr><td>85 S, typical;
96 S, maximum</td><td>220 S, typical;
230 S, maximum</td><td>210 S, typical;
230 S, maximum</td></tr>
<tr><td>Destinations</td><td>1. PFI 0 (SMB jack connectors)
2. PFI <1..3> (DDC connector)
3. PXI_TRIG<0..6> (PXI backplane—PXI only)/ RTSI<0..6> (RTSI bus—PCI only)</td><td>Each trigger can be routed to any destination except the Pause trigger. The Pause trigger cannot be exported for acquisition sessions.</td></tr>
</table>

Specification	Value		Comments
Delay from Pause trigger to Pause state	**Generation Sessions**	**Acquisition Sessions**	Use the Data Active event during generation to determine when the NI 656*x* enters the Pause state.
	31 Sample clock periods + 90 ns	Synchronous to the data	
Delay from trigger to digital data output	34 Sample clock periods + 85 ns		—

Events (Generated from the NI 656*x*)

Specification	Value	Comments
Event type	1. Marker <0..3> (generation sessions only) 2. Data Active event (generation sessions only) 3. Ready for Start event 4. Ready for Advance event (acquisition sessions only) 5. End of record event (acquisition sessions only)	—
Destinations	1. PFI 0 (SMB jack connectors) 2. PFI <1..3> (DDC connector) 3. PXI_TRIG<0..6> (PXI backplane—PXI only)/ RTSI<0..6> (RTSI bus—PCI only)	Each event can be routed to any destination, except the Data Active event. The Data Active event can only be routed to the PFI channels.
Marker time resolution (placement)	Markers must be placed at an integer multiple of 4 S.	Marker time resolution doubles with 8-bit data width (DDR mode).

Miscellaneous

Specification	Value	Comments
Warm-up time	15 minutes	—
On Board Clock characteristics (valid when PLL reference source is set to None)		
Frequency accuracy	±100 ppm	Typical
Temperature stability	±30 ppm	Typical
Aging	±5 ppm first year	Typical

Power

Specification	Value		Comments
	PXI	PCI	
+3.3 VDC	1.8 A	1.7 A	All values refer to maximum power.
+5 VDC	1.0 A	1.1 A	
+12 VDC	0.4 A	0.4 A	
–12 VDC	0.05 A	0.05 A	
Total power	16.4 W	16.5 W	

Software

Specification	Value	Comments
Driver software	NI-HSDIO driver software 1.3 or later. NI-HSDIO allows you to configure and control the NI 656*x*. NI-HSDIO provides application interfaces for many development environments. NI-HSDIO follows IVI application programming interface (API) guidelines.	—
Application software	NI-HSDIO provides programming interfaces for the following application development environments: • National Instruments LabVIEW 7.0 or later • National Instruments LabWindows™/CVI™ 6.0 or later • Microsoft Visual C/C++ 6.0 or later	—
Test panel	National Instruments Measurement & Automation Explorer (MAX) provides test panels with basic acquisition and generation functionality for the NI 656*x*. MAX is included on the NI-HSDIO driver CD.	—

Environment

Note To ensure that the NI 656*x* cools effectively, follow the guidelines in the *Maintain Forced Air Cooling Note to Users* included with the NI 656*x*. The NI 656*x* is intended for indoor use only.

Specification	Value	Comments
Operating temperature	**PXI**: 0 to +55 ºC in all NI PXI chassis except the following: 0 to +45 ºC when installed in an NI PXI-1000/B and NI PXI-101*X* chassis (Meets IEC 60068-2-1 and IEC 60068-2-2.) **PCI**: 0 to +45 ºC	—
Storage temperature	–20 to 70 ºC	—
Operating relative humidity	10 to 90% relative humidity, noncondensing (Meets IEC 60068-2-56)	—
Storage relative humidity	5 to 95% relative humidity, noncondensing (Meets IEC 60068-2-56)	—
Operating shock	30 g, half-sine, 11 ms pulse (Meets IEC 60068-2-27. Test profile developed in accordance with MIL-PRF-28800F.)	—
Storage shock	50 g, half-size, 11 ms pulse (Meets IEC 60068-2-27. Test profile developed in accordance with MIL-PRF-28800F.)	—
Operating vibration	5 to 500 Hz, 0.31 g_{rms} (Meets IEC 60068-2-64.)	—
Storage vibration	5 to 500 Hz, 2.46 g_{rms} (Meets IEC 60068-2-64. Test profile exceeds requirements of MIL-PRF-28800F, Class 3.)	—
Maximum altitude	0 to 2,000 m above sea level (at 25 ºC ambient temperature)	—
Pollution Degree	2	—

Safety, Electromagnetic Compatibility, and CE Compliance

Specification	Value	Comments
Safety	The NI 656*x* meets the requirements of the following standards of safety for electrical equipment for measurement, control, and laboratory use: • IEC 61010-1, EN 61010-1 • UL 61010-1, CSA 61010-1	For UL and other safety certifications, refer to the product label or to `ni.com`.
Emissions	EN 55011 Class A at 10 m FCC Part 15A above 1 GHz	—
Immunity	EN 61326:1997 + A2:2001, Table 1	—
EMC/EMI	CE, C-Tick, and FCC Part 15 (Class A) Compliant	—
This product meets the essential requirements of applicable European Directives, as amended for CE marking, as follows:		
Low-Voltage Directive (safety)	73/23/EEC	—
Electro-magnetic Compatibility Directive (EMC)	89/336/EEC	—
For EMC compliance, operate this device with shielded cabling. In addition, filler panels must be installed. Refer to the Declaration of Conformity (DoC) for this product for any additional regulatory compliance information. To obtain the DoC for this product, visit `ni.com/certification`, search by model number or product line, and click the appropriate link in the Certification column.		

Physical Specifications

Specification	Value		Comments
Dimensions	**PXI**: 3U, One Slot, PXI/cPCI Module 21.6 × 2.0 × 13.0 cm (8.5 × 0.8 × 5.1 in) **PCI**: 12.6 × 35.5 cm (4.96 × 13.9 in.)		—
Weight	**PXI**: 340 g (12 oz) **PCI**: 410 g (14.5 oz)		—
Front Panel Connectors			
Label	**Function(s)**	**Connector Type**	—
CLK IN	External Sample clock, external PLL reference input	SMB jack connector	—
PFI 0	Events, triggers	SMB jack connector	—
CLK OUT	Exported Sample clock, exported Reference clock	SMB jack connector	—
DIGITAL DATA & CONTROL	Digital data channels, exported Sample clock, STROBE, events, triggers	12X InfiniBand connector	—
	Note: The NI SHB12X-B12X LVDS cable (192344-01) is a pass-through cable. When designing a custom fixture, notice that the cable pinout is reversed from that of the NI 656x. For example, the NI 656x generates DIO 0 on pin 14. This signal connects to pin 60 at the cable end. Refer to the *NI Digital Waveform Generator/Analyzer Getting Started Guide* or the *NI Digital Waveform Generator/Analyzer Help* for more pinout information.		

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