SPECIFICATIONS

PXI-6561

100 MHz, 16-Channel PXI Digital Waveform Instrument

These specifications apply to the PXI-6561 with 2 MBit, 16 MBit, and 128 MBit of memory per channel.

Hot Surface If the PXI-6561 has been in use, it may exceed safe handling temperatures and cause burns. Allow the PXI-6561 to cool before removing it from the chassis.

Note All values were obtained using a 1 m cable (SHC68-C68-D4 recommended). Performance specifications are not guaranteed when using longer cables.

Contents

NATIONAL INSTRUMENTS

Definitions

Warranted specifications describe the performance of a model under stated operating conditions and are covered by the model warranty.

The following characteristic specifications describe values that are relevant to the use of the model under stated operating conditions but are not covered by the model warranty.

- *Typical* specifications describe the performance met by a majority of models.
- *Nominal* specifications describe an attribute that is based on design, conformance testing, or supplemental testing.

Conditions

Typical values are representative of an average unit operating at room temperature.

Channels

Data	
Number of channels	16
Direction control, Single Data Rate (SDR)[1]	Per channel
Direction control, Double Data Rate (DDR)	
Data <0..7>	Data generation
Data <8..15>	Data acquisition
Programmable Function Interface (PFI)	
Number of channels	4
Direction control	Per channel

[1] Using SDR, data is clocked using the rising or falling edge of the Sample clock. Using DDR, data is clocked using both edges of the Sample clock.

Clock terminals	
Input	3
Output	3

Generation Channels

Channels	Data DDC CLK OUT PFI <0..3>
Voltage families	
Data <0..15>, PFI <1..2>, DDC CLK OUT LVDS	LVDS
DDC CLK OUT LVPECL	LVPECL
PFI 0	LVCMOS
PFI 3	Software-selectable: LVDS or LVCMOS

Table 1. Voltage Levels

LVDS[2]		LVCMOS		LVPECL[3]	
Offset (V_{os})	**Differential Voltage (V_{od})**	**Low**	**High**	**Single Ended Output Low**	**Single Ended Output High**
1.125 V, min	247 mV, min	0.2 V, max	2.8 V, min	1.38 V, min	2.16 V, min
1.220 V, typ	305 mV, typ	—	—	1.72 V, max	2.50 V, max
1.375 V, max	454 mV, max	—	—	—	—

Output impedance	
LVDS	100 Ω differential, nominal
LVCMOS/LVPECL	50 Ω series, nominal
Data channel driver enable/disable control	Software-selectable: per channel
Channel power-on state[4]	Drivers disabled, 100 Ω differential impedance PFI 3: LVDS mode

[2] Into 100 Ω differential load, TIA/EIA-644 compliant.
[3] Into open load.
[4] Data channels have a weak pull-up resistor (300 kΩ), internal to the I/O buffer, to 3.3 V. This internal pull-up resistor is a fail-safe mechanism intended to set a known state when the receiver circuit is not being driven.

Output protection, per channel	
Range	0 V to 5 V
Duration	Indefinite
ESD	Up to 12 kV

Acquisition Channels

Channels	Data STROBE PFI <0..3>
Voltage families	
Data <0..15>, PFI <1..2>, and STROBE	LVDS
PFI 0	LVCMOS
PFI 3	Software-selectable: LVDS or LVCMOS
Voltage levels (LVDS)[5]	
Voltage threshold[6]	±50 mV, maximum
Voltage range	0 V, minimum 2.4 V, maximum
Voltage levels (LVCMOS)	
Low voltage threshold	0.8 V, maximum
High voltage threshold	2 V, minimum
Input impedance[7]	
LVDS	100 Ω differential
LVCMOS	10 kΩ
Input protection, per channel	
Range	0 V to 5 V
Duration	Indefinite
ESD	Up to 12 kV

[5] TIA/EIA-644 compliant.
[6] The device under test must supply more than 50 mV of differential voltage.
[7] Data channels have a weak pull-up resistor (300 kΩ), internal to the I/O buffer, to 3.3 V. This internal pull-up resistor is a fail-safe mechanism intended to set a known state when the receiver circuit is not being driven. PFI 3 powers up in LVDS mode.

Timing

Sample Clock

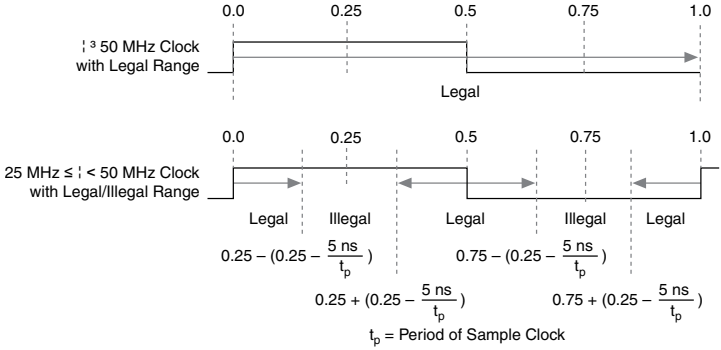
Sources	1. On Board clock (internal voltage-controlled crystal oscillator [VCXO] with divider) 2. CLK IN (SMB jack connector) 3. PXI_STAR (PXI backplane) 4. STROBE (DDC connector; acquisition only)
Frequency range	
On Board clock	48 Hz to 100 MHz, Configurable to 200 MHz/*N;* $2 \leq N \leq 4{,}194{,}304$
CLK IN	20 kHz to 100 MHz
PXI_STAR	48 Hz to 70 MHz
STROBE	48 Hz to 100 MHz
Relative delay adjustment[8]	
Range	0 to 1 Sample clock periods
Resolution	10 ps
Exported Sample clock	
Destinations[9]	1. DDC CLK OUT (DDC connector) 2. CLK OUT (SMB jack connector)
Delay, for clock frequencies ≥25 MHz	
Range	0.0 to 1.0 Sample clock periods[10]
Resolution (δ_C)	1/256 of Sample clock period or 60 ps, whichever is greater
Jitter, using On Board clock	
Period	19 ps_{rms}, typical
Cycle-to-cycle	29 ps_{rms}, typical
Transition time	1 ns
Duty cycle	47% to 53%

[8] You can apply a delay or phase adjustment to the On Board clock to align multiple devices.

[9] Internal Sample clocks with sources other than STROBE can be exported. Selecting DDC CLK OUT in software exports the internal Sample clock to the DDC CLK OUT LVDS and DDC CLK OUT LVPECL terminals.

[10] Refer to the *Valid Data Position Delay Ranges* figure for more information.

Figure 1. Valid Data Position Delay Ranges

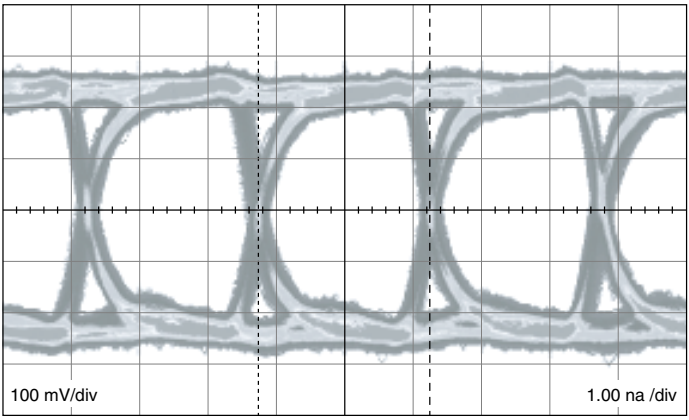


Generation Timing

Channels	Data DDC CLK OUT PFI <0..3>
Data channel-to-channel skew[11]	±215 ps, typical ±500 ps, maximum
Maximum data channel toggle rate	
SDR	50 MHz
DDR	100 MHz
Data position modes	Sample clock rising edge Sample clock falling edge Delay from Sample clock rising edge
Generation data delay (δ_G), for clock frequencies ≥25 MHz	
Range	0.0 to 1.0 Sample clock periods
Resolution	1/256 of Sample clock period or 60 ps, whichever is greater

[11] Across all data channels and PFI <1..2>

Figure 2. Eye Diagram



Note This eye diagram was captured on DIO 0 (200 MHz clock rate in DDR mode) at room temperature into 100 Ω differential terminating resistance.

Transition time (20% to 80% transitions)	
Data channels	610 ps, minimum 1 ns, maximum
PFI channels	
PFI 0	6 ns, typical
PFI <1..2>	2.5 ns, typical
PFI 3 (LVCMOS)	6 ns, typical
PFI 3 (LVDS)	4.2 ns, typical
Exported Sample clock	
Offset (t_{CO})[12]	1.6 ns
Offset to selectable PFI	
LVDS (t_{CPD})	2 ns, typical
LVCMOS (t_{CPS})	3.45 ns, typical
Time delay (from internal Sample clock) to DDC connector (t_{SCDDC})	5.8 ns, typical

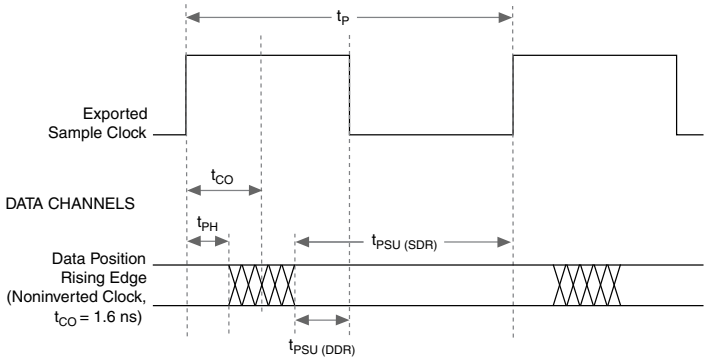
[12] Refer to the *Generation Provided Setup and Hold Times Timing Diagram* figure.

Minimum generation provided setup and hold times[13]	
Setup time (t_{SUP})	t_p - 2.2 ns
Hold time (t_{HP})	1.1 ns

Compare the setup and hold times from the datasheet of the of your device under test (DUT) to the values in the preceding specifications. The provided setup and hold times must be greater than the setup and hold times required for the DUT. If you require more setup time, configure your exported Sample clock mode as Inverted and/or delay your data relative to the Sample clock.

Note The *Transition time* and *Sample clock* specification values assume that the Data Position is set to the rising edge of the Sample clock and that the Sample clock is exported to the DDC connector. These values include the worst-case effects of channel-to-channel skew, inter-symbol interference, and jitter.

Figure 3. Generation Provided Setup and Hold Times Timing Diagram



$t_P = \frac{1}{i}$ = Period of Sample Clock

t_{PH} = Minimum Provided Hold Time

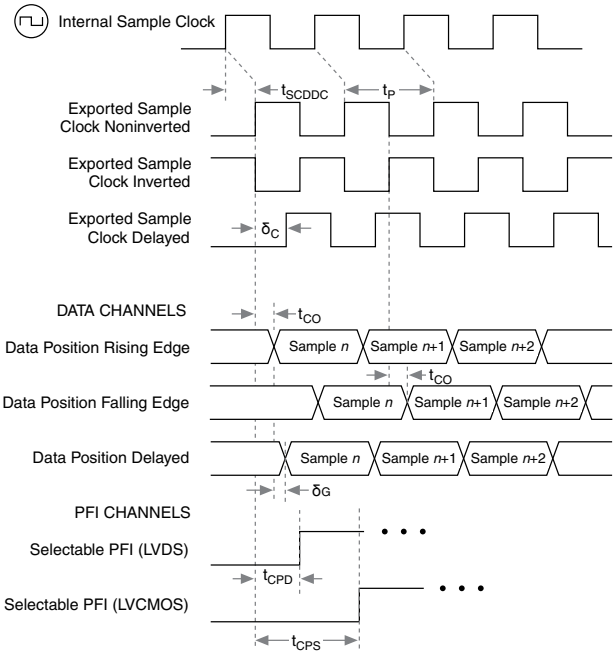
t_{PSU} = Minimum Provided Setup Time; SDR = Single Data Rate, DDR = Double Data Rate

t_{CO} = Exported Sample Clock Offset

Note: At 25 MHz and higher, STROBE duty cycle is corrected to 50%.

[13] Exported Sample clock mode set to Noninverted.

Figure 4. Generation Timing Diagram



t_{SCDDC} = Time Delay from Sample Clock (Internal) to DDC Connector Exported Sample Clock

$0 \le \delta_C \le 1$: Exported Sample Clock Delay (Fraction of t_P)

$0 \le \delta_G \le 1$: Pattern Generation Data Delay (Fraction of t_P)

$t_P = \frac{1}{i}$ = Period of Sample Clock

t_{CO} = Exported Sample Clock Offset

t_{CPD} = Exported Sample Clock to Selectable PFI Offset (LVDS)

t_{CPS} = Exported Sample Clock to Selectable PFI Offset (LVCMOS)

Note SDR mode acquisition shown.

Acquisition Timing

Channels	Data STROBE PFI <0..3>
Channel-to-channel skew[14]	
f < 25 MHz	±600 ps, typical ±1.2 ns, maximum
f ≥ 25 MHz	±330 ps, typical ±600 ps, maximum
Data position modes	Sample clock rising edge Sample clock falling edge Delay from Sample clock rising edge
Setup and hold times to STROBE[15]	
Setup time (t_{SUS})	
f < 25 MHz	1.8 ns, maximum
f ≥ 25 MHz	1.1 ns, maximum
Hold time (t_{HS})	
f < 25 MHz	2.1 ns, maximum
f ≥ 25 MHz	0.8 ns, maximum
Setup and hold times to Sample clock[16]	
Setup time (t_{SUSC})	
f < 25 MHz	1.9 ns
f ≥ 25 MHz	0.9 ns
Hold time (t_{HSC})	
f < 25 MHz	-0.6 ns
f ≥ 25 MHz	-0.4 ns
Time delay from DDC connector data to internal Sample clock (t_{DDSSC})	
f < 25 MHz	6.6 ns, typical
f ≥ 25 MHz	5.6 ns, typical

[14] Across all data channels and PFI <1..2>.

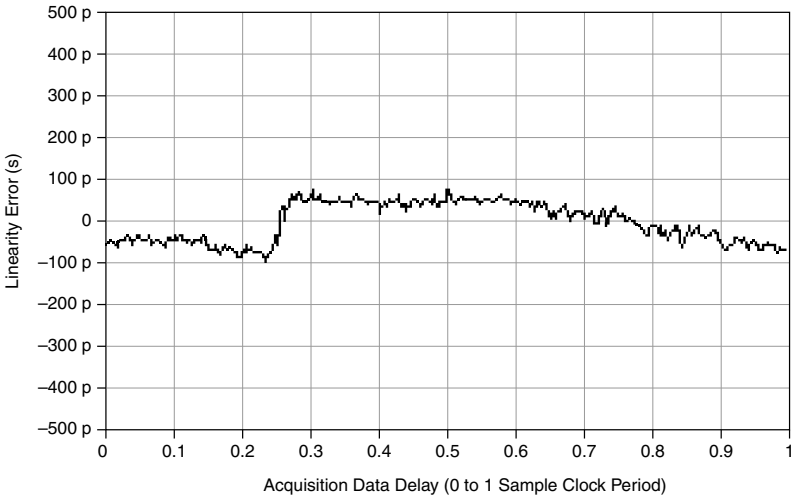
[15] At 25 MHz and higher, STROBE duty cycle is corrected to 50% while maintaining rising edge placement. Includes maximum data channel-to-channel skew.

[16] Does not include data channel-to-channel skew, t_{DDCSC}, or t_{SCDDC}.

Acquisition data delay (δ_A), for clock frequencies ≥25 MHz

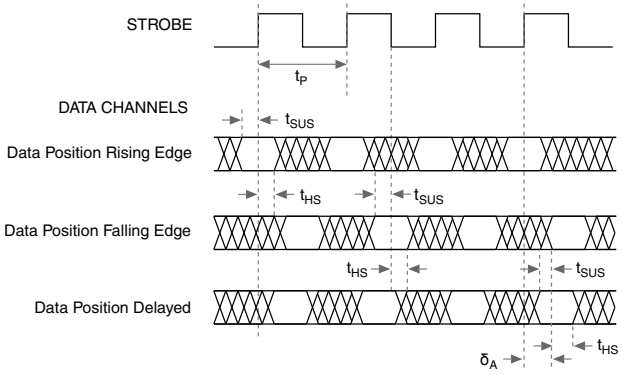
Range	0.0 to 1.0 Sample clock periods[17]
Resolution	1/256 of Sample clock period or 60 ps, whichever is greater

Figure 5. Acquisition Data Delay Normalized Linearity



[17] Refer to the *Valid Data Position Delay Ranges* figure for more information.

Figure 6. Acquisition Timing Diagram Using STROBE as the Sample Clock



t_{SUS} = Set-Up Time to STROBE

t_{HS} = Hold Time from STROBE

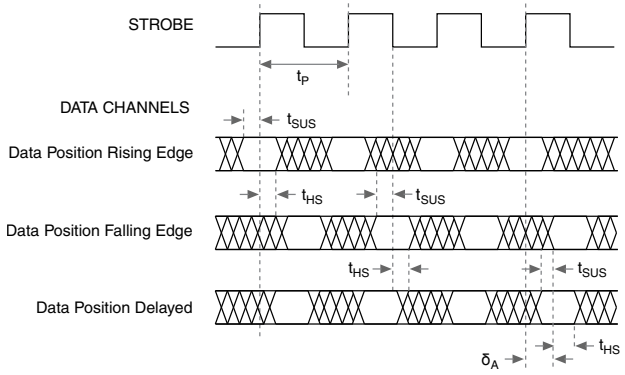
$0 \leq \delta_A \leq 1$: Pattern Acquisition Data Delay (fraction of t_P)

$t_P = \frac{1}{i}$ = Period of Sample Clock

Note: At 25 MHz and higher, STROBE duty cycle is corrected to 50% while maintaining rising edge placement.

Note SDR mode acquisition shown.

Figure 7. Acquisition Timing Diagram with Sample Clock Sources Other than STROBE



t_{SUS} = Set-Up Time to STROBE

t_{HS} = Hold Time from STROBE

$0 \leq \delta_A \leq 1$: Pattern Acquisition Data Delay (fraction of t_P)

$t_P = \frac{1}{\text{ }}$ = Period of Sample Clock

Note: At 25 MHz and higher, STROBE duty cycle is corrected to 50% while maintaining rising edge placement.

Note SDR mode acquisition shown.

CLK IN

Connector	SMB jack
Direction	Input
Destinations	1. Reference clock for the phase-locked loop (PLL) 2. Sample clock
Input coupling	AC
Input protection	±10 VDC
Input impedance	Software-selectable: 50 Ω (default) or 1 kΩ
Minimum detectable pulse width	2 ns
Clock requirements	Free-running (continuous) clock

As Sample Clock

Table 2. External Sample Clock Range

Voltage Range (V_{pk-pk})	Sine Wave	Square Wave	
	Frequency Range	Frequency Range	Duty Cycle
0.65 to 5.0	5.5 MHz to 100 MHz	20 kHz to 100 MHz	f <50 MHz: 25% to 75% f ≥50 MHz: 40% to 60%
1.0 to 5.0	3.5 MHz to 100 MHz	—	—
2.0 to 5.0	1.8 MHz to 100 MHz	—	—

As Reference Clock

Frequency range	10 MHz ±50 ppm
Voltage range	0.65 V_{pk-pk} to 5.0 V_{pk-pk}
Duty cycle	25% to 75%

STROBE

Connector	DDC
Direction	Input
Destination	Sample clock (acquisition only)
Frequency range	48 Hz to 100 MHz
Duty cycle range	f <50 MHz: 25% to 75% f ≥50 MHz: 40% to 60%
Minimum detectable pulse width	2 ns
Clock requirements	Free-running (continuous) clock
Input impedance	100 Ω differential[18]

PXI_STAR

Connector	PXI backplane
Direction	Input

[18] Data channels have a weak pull-up resistor (300 kΩ), internal to the I/O buffer, to 3.3 V . This internal pull-up resistor is a fail-safe mechanism intended to set a known state when the receiver circuit is not being driven.

Destinations	1. Sample clock 2. Start trigger 3. Reference trigger (acquisition sessions only) 4. Advance trigger (acquisition sessions only) 5. Pause trigger (generation sessions only) 6. Script trigger <0..3> (generation sessions only)
Frequency range	48 Hz to 70 MHz
Clock requirements	Free-running (continuous) clock

CLK OUT

Connector	SMB jack
Direction	Output
Sources	1. Sample clock (excluding STROBE) 2. Reference clock (PLL)
Output impedance	50 Ω, nominal
Logic type	LVCMOS
Maximum drive current	32 mA

DDC CLK OUT

Connector	DDC
Direction	Output
Source[19]	Sample clock (excluding STROBE)
Logic types	LVDS LVPECL

DDC CLK OUT LVDS

Voltage levels[20]	
Offset (V_{os})	1.125 V, minimum 1.220 V, typical 1.375 V, maximum
Differential voltage (V_{od})	247 mV, minimum 305 mV, typical 454 mV, maximum

[19] Exporting the internal Sample clock to the DDC CLK OUT in software exports the internal Sample clock to the DDC CLK OUT LVDS and DDC CLK OUT LVPECL terminals.

[20] Into a 100 Ω differential load, TIA/EIA-644 compliant.

Transition time	1 ns
Output impedance	100 Ω differential
Output protection	
Range	0 V to 5 V
Duration	Indefinite
ESD	Up to 15 kV

DDC CLK OUT LVPECL

Voltage levels[21]	
Single-Ended Output High	2.16 V, minimum 2.50 V, maximum
Single-Ended Output Low	1.38 V, minimum 1.72 V, maximum
Transition time	1 ns
Output impedance[22]	50 Ω source series, nominal
Output protection	
Range	0 V to 5 V
Duration	Indefinite
ESD	Up to 15 kV

Reference Clock (PLL)

Sources[23]	1. PXI_CLK10 (PXI backplane) 2. CLK IN (SMB jack connector) 3. None (On Board clock not locked to a reference)
Destination	CLK OUT (SMB jack connector)
Lock time	400 ms, typical
Frequencies	10 MHz ±50 ppm
Duty cycle range	25% to 75%

[21] Into open load.
[22] Series impedance on each polarity.
[23] The source provides the reference frequency for the PLL.

Waveform

Memory and Scripting

Memory architecture	The PXI-6561 uses Synchronization and Memory Core (SMC) technology in which waveforms and instructions share onboard memory. Parameters such as number of script instructions, maximum number of script instructions, maximum number of waveforms in memory, and number of samples (S) available for waveform storage are flexible and user defined.
Onboard memory size[24]	
2 Mbit/channel	
Acquisition	2 Mbit/channel (4 MBytes total)
Generation	2 Mbit/channel (4 MBytes total)
16 Mbit/channel	
Acquisition	16 Mbit/channel (32 MBytes total)
Generation	16 Mbit/channel (32 MBytes total)
128 Mbit/channel	
Acquisition	128 Mbit/channel (256 MBytes total)
Generation	128 Mbit/channel (256 MBytes total)
Generation	
Single waveform mode	Generates a single waveform once, *n* times, or continuously
Scripted mode[25]	Generates a simple or complex sequence of waveforms.
Finite repeat count	1 to 16,777,216
Waveform quantum[26]	Waveform must be an integer multiple of 4 S (samples).

[24] Maximum limit for generation sessions assumes no scripting instructions. Onboard memory size doubles with 8-bit data width (DDR mode).

[25] Use scripts to describe the waveforms to be generated, the order in which the waveforms are generated, how many times the waveforms are generated, and how the device responds to Script triggers.

[26] Regardless of waveform size, NI-HSDIO allocates waveforms into block sizes of 64 S of physical memory. Waveform quantum and block size double when using 8-bit data width (DDR mode).

Table 3. Generation Minimum Waveform Size, Samples (S)[27]

Configuration	Sample Rate
	100 MHz
Single waveform	4 S
Continuous waveform	32 S
Stepped sequence	128 S
Burst sequence	512 S

Acquisition

Minimum record size[28]	1 S
Record quantum	1 S
Total records	2,147,483,647, maximum
Total pre-Reference trigger samples	0 up to full record
Total post-Reference trigger samples	0 up to full record

Triggers

Trigger Types	Sessions	Edge Detection	Level Detection
1. Start	Acquisition and generation	Rising or falling	—
2. Pause	Acquisition and generation	—	High or low
3. Script <0..3>	Generation	Rising or falling	High or low
4. Reference	Acquisition	Rising or falling	—
5. Advance	Acquisition	Rising or falling	—

Sources

1. PFI 0 (SMB jack connector)
2. PFI <1..3> (DDC connector)
3. PXI_TRIG <0..7> (PXI backplane)
4. PXI_STAR (PXI backplane)
5. Pattern match (acquisition sessions only)
6. Software (user function call)
7. Disabled (do not wait for a trigger)

[27] Sample rate dependent. Increasing sample rate increases maximum waveform size. Waveform quantum and block size double when using 8-bit data width (DDR mode).

[28] Regardless of waveform size, NI-HSDIO allocates at least 128 bytes for a record.

Destinations[29]	
PFI 0	SMB jack connectors
PFI <1..3>	DDC connector
PXI_TRIG <0..6>	PXI backplane
Minimum required trigger pulse width	
Generation	30 ns
Acquisition[30]	Acquisition triggers must meet setup and hold time requirements.

Table 4. Trigger Rearm Time

Trigger Operation	Samples, Typical	Samples, Maximum
Start to Reference	85 S	96 S
Start to Advance	220 S	230 S
Reference to Reference	210 S	230 S

Delay from Pause trigger to Pause state[31]	
Generation sessions	32 Sample clock periods + 150 ns
Acquisition sessions	Data synchronous
Delay from trigger to digital data output	32 Sample clock periods + 85 ns

Events

Event Types	Sessions
1. Marker <0..3>	Generation
2. Data Active	Generation
3. Ready for Start	Acquisition and generation

[29] Each trigger can be routed to any destination except the Pause trigger. The Pause trigger cannot be exported for acquisition sessions.

[30] For triggers synchronous to STROBE, triggers must meet setup and hold requirements. For asynchronous triggers, pulse width must be larger than the greater of 30 ns or Clock Period + Setup + Hold.

[31] Use the Data Active event during generation to determine when the PXI-6561 enters the Pause state.

Event Types	Sessions
4. Ready for Advance	Acquisition
5. End of Record	Acquisition

Destinations[32]	1. PFI 0 (SMB jack connector) 2. PFI <1..3> (DDC connector) 3. PXI_TRIG <0..7> (PXI backplane)
Marker time resolution (placement)[33]	Markers must be placed at an integer multiple of 4 S (samples).

Miscellaneous

Warm-up time	15 minutes
On Board clock characteristics (valid only when PLL reference source is set to None)	
Frequency accuracy	±100 ppm, typical
Temperature stability	±30 ppm, typical
Aging	±5 ppm first year, typical

Software

Driver Software

Driver support for this device was first available in NI-HSDIO 1.3.

NI-HSDIO is an IVI-compliant driver that allows you to configure, control, and calibrate the PXI-6561. NI-HSDIO provides application programming interfaces for many development environments.

Application Software

NI-HSDIO provides programming interfaces, documentation, and examples for the following application development environments:

- LabVIEW
- LabWindows™/CVI™
- Measurement Studio
- Microsoft Visual C/C++
- .NET (C# and VB.NET)

[32] Except for the Data Active event, each event can be routed to any destination. The Data Active event can be routed only to the PFI channels.

[33] Marker time resolution doubles with 8-bit data width (DDR mode).

NI Measurement Automation Explorer

NI Measurement Automation Explorer (MAX) provides interactive configuration and test tools for the PXI-6561. MAX is included on the NI-HSDIO media.

Power

VDC	Current, Maximum
+3.3	1.8 A
+5	1.0 A
+12	0.4 A
-12	0.05 A

Total power	16.4 W, maximum

Physical Specifications

Dimensions	3U, one-slot, PXI/cPCI Module, 21.6 cm × 2.0 cm × 13.0 cm (8.5 in × 0.8 in × 5.1 in)
Weight	340 g (12 oz)

I/O Connectors

Label	Connector Type	Description
CLK IN	SMB jack	External Sample clock, external PLL reference input
PFI 0		Events, triggers
CLK OUT		Exported Sample clock, exported Reference clock
DIGITAL DATA & CONTROL	12X InfiniBand connector	Digital data channels, exported Sample clock, STROBE, events, triggers

Note The SHB12X-B12X LVDS cable, NI part number 192344-01, is a pass-through cable. When designing a custom fixture, notice that the cable pinout is reversed from that of the PXI-6561. For example, the PXI-6561 generates DIO 0 on pin 14. This signal connects to pin 60 at the cable end. Refer to the *NI Digital*

Waveform Generator/Analyzer Getting Started Guide or the *NI Digital Waveform Generator/Analyzer Help* at *ni.com/manuals* for more pinout information.

Environment

Note To ensure that the PXI-6561 cools effectively, follow the guidelines in the *Maintain Forced Air Cooling Note to Users* included with the PXI-6561 or available at *ni.com/manuals*. The PXI-6561 is intended for indoor use only.

Operating temperature	0 °C to 55 °C in all NI PXI chassis except the following: 0 °C to 45 °C when installed in an NI PXI-1000B or NI PXI-101x chassis
Operating relative humidity	10 to 90% relative humidity, noncondensing (meets IEC 60068-2-56)
Storage temperature	-20 °C to 70 °C
Storage relative humidity	5 to 95% relative humidity, noncondensing (meets IEC 60068-2-56)
Operating shock	30 g, half-sine, 11 ms pulse (meets IEC 60068-2-27; test profile developed in accordance with MIL-PRF-28800F)
Operating vibration	5 Hz to 500 Hz, 0.31 g_{rms} (meets IEC 60068-2-64)
Storage shock	50 g, half-sine, 11 ms pulse (meets IEC 60068-2-27; test profile developed in accordance with MIL-PRF-28800F)
Storage vibration	5 Hz to 500 Hz, 2.46 g_{rms} (meets IEC 60068-2-64; test profile exceeds requirements of MIL-PRF-28800F, Class B)
Altitude	0 to 2,000 m above sea level (at 25 °C ambient temperature)
Pollution degree	2

Compliance and Certifications

Safety

This product is designed to meet the requirements of the following electrical equipment safety standards for measurement, control, and laboratory use:

- IEC 61010-1, EN 61010-1
- UL 61010-1, CSA C22.2 No. 61010-1

Note For UL and other safety certifications, refer to the product label or the *Online Product Certification* section.

Electromagnetic Compatibility

This product meets the requirements of the following EMC standards for electrical equipment for measurement, control, and laboratory use:

- EN 61326-1 (IEC 61326-1): Class A emissions; Basic immunity
- EN 55011 (CISPR 11): Group 1, Class A emissions
- AS/NZS CISPR 11: Group 1, Class A emissions
- FCC 47 CFR Part 15B: Class A emissions
- ICES-001: Class A emissions

Note For EMC declarations, certifications, and additional information, refer to the *Online Product Certification* section.

To meet EMC compliance, the following cautions apply:

Caution The SHC68-C68-D4 shielded cables must be used when operating the PXI-6561.

Caution EMC filler panels must be installed in all empty chassis slots.

CE Compliance CE

This product meets the essential requirements of applicable European Directives, as follows:

- 2014/35/EU; Low-Voltage Directive (safety)
- 2014/30/EU; Electromagnetic Compatibility Directive (EMC)

Online Product Certification

Refer to the product Declaration of Conformity (DoC) for additional regulatory compliance information. To obtain product certifications and the DoC for this product, visit *ni.com/certification*, search by model number or product line, and click the appropriate link in the Certification column.

Environmental Management

NI is committed to designing and manufacturing products in an environmentally responsible manner. NI recognizes that eliminating certain hazardous substances from our products is beneficial to the environment and to NI customers.

For additional environmental information, refer to the *Minimize Our Environmental Impact* web page at *ni.com/environment*. This page contains the environmental regulations and directives with which NI complies, as well as other environmental information not included in this document.

Waste Electrical and Electronic Equipment (WEEE)

EU Customers At the end of the product life cycle, all NI products must be disposed of according to local laws and regulations. For more information about how to recycle NI products in your region, visit *ni.com/environment/weee*.

电子信息产品污染控制管理办法（中国 RoHS）

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