## COMPREHENSIVE SERVICES

We offer competitive repair and calibration services, as well as easily accessible documentation and free downloadable resources.

## SELL YOUR SURPLUS

We buy new, used, decommissioned, and surplus parts from every NI series. We work out the best solution to suit your individual needs.

Sell For Cash  Get Credit  Receive a Trade-In Deal

## OBSOLETE NI HARDWARE IN STOCK & READY TO SHIP

We stock **New, New Surplus, Refurbished,** and **Reconditioned** NI Hardware.

APEX WAVES

***Bridging the gap*** *between the manufacturer and your legacy test system.*


1-800-915-6216

www.apexwaves.com

sales@apexwaves.com




## *Request a Quote* CLICK HERE *PXI-6683H*

USER MANUAL

# PXIe-6672

## Timing and Synchronization Module for PXI Express

The PXIe-6672 can generate and route clock and trigger signals between devices in a single chassis or multiple chassis, providing a method to synchronize multiple devices in a PXI Express system.

This manual describes the electrical and mechanical aspects of the PXIe-6672 and contains information concerning its operation and programming.

### Conventions

**Caution** This icon denotes a caution, which advises you of precautions to take to avoid injury, data loss, or a system crash. When this symbol is marked on the product, refer to the *Safety Information* section of the *Introduction* for precautions to take.

### National Instruments Documentation

The PXIe-6672 User Manual is one piece of the documentation set for your measurement system. You could have any of several other documents describing your hardware and software. Use the documentation you have as follows:

- Measurement hardware documentation—This documentation contains detailed information about the measurement hardware that plugs into or is connected to the computer. Use this documentation for hardware installation and configuration instructions, specifications about the measurement hardware, and application hints.
- Software documentation—Refer to the NI-Sync Help, available at `ni.com/manuals`.

You can download NI documentation from `ni.com/manuals`.

### Related Documentation

The following documents contain information that you might find helpful as you read this manual.

- *NI-Sync User Manual*, available from `ni.com/manuals`.
- *PICMG 2.0 R3.0, CompactPCI Core Specification*, available from PICMG at `www.picmg.org`.
- *PXI Specification, Revision 2.1*, available from `www.pxisa.org`.
- *NI-VISA User Manual*, available from `ni.com/manuals`.
- *NI-VISA Help*, included with the NI-VISA software.

NATIONAL INSTRUMENTS

# Contents



# Introduction

The PXIe-6672 can generate and route clock and trigger signals between devices in a single chassis or multiple chassis, providing a method to synchronize multiple devices in a PXI Express system.

## What You Need to Get Started

To set up and use the PXIe-6672, you need the following items:

- PXIe-6672 Timing and Synchronization Module
- PXI Express chassis
- PXI Express embedded controller or a desktop computer connected to the PXI Express chassis using MXI-Express hardware.
- PXI EMC filler panels, National Instruments part number 778700-01
- NI-Sync driver

- One of the following software packages and documentation:
  - LabVIEW
  - LabWindows™/CVI™
  - Microsoft Visual C++ (MSVC)
- PXIe-6672 User Manual

The *NI-Sync User Manual* offers more detailed information on the software used to program the PXIe-6672. You can find this manual at `ni.com/manuals`.

# Unpacking

The PXIe-6672 is shipped in an antistatic package to prevent electrostatic damage to the module. Electrostatic discharge (ESD) can damage several components on the module.

**Caution** Never touch the exposed pins of the connectors.

To avoid such damage in handling the module, take the following precautions:

- Ground yourself using a grounding strap or by touching a grounded object.
- Touch the antistatic package to the metal part of the computer chassis before removing the module from the package.

Remove the module from the package and inspect the module for loose components or any sign of damage. Notify NI if the module appears damaged in any way. Do not install a damaged module into the computer.

Store the PXIe-6672 in the antistatic envelope when not in use.

# Software Programming Choices

When programming the PXIe-6672, you can use NI application development environment (ADE) software such as LabVIEW or LabWindows/CVI, or you can use other ADEs such as Visual C/C++.

LabVIEW features interactive graphics, a state-of-the-art interface, and a powerful graphical programming language. The LabVIEW Data Acquisition VI Library, a series of virtual instruments for using LabVIEW with National Instruments DAQ hardware, is included with LabVIEW.

LabWindows/CVI is a complete ANSI C ADE that features an interactive video interface, code generation tools, and the LabWindows/CVI Data Acquisition and Easy I/O libraries.

# Safety Information

The following section contains important safety information that you must follow when installing and using the PXIe-6672.

Do not operate the product in a manner not specified in this document. Misuse of the product can result in a hazard. You can compromise the safety protection built into the product if the product is damaged in any way. If the product is damaged, return it to National Instruments for repair.

Do not substitute parts or modify the product except as described in this document. Use the product only with the chassis, modules, accessories, and cables specified in the installation instructions. You must have all covers and filler panels installed during operation of the product.

Do not operate the product in an explosive atmosphere or where there may be flammable gases or fumes. If you must operate the product in such an environment, it must be in a suitable rated enclosure.

If you need to clean the product, use a soft, nonmetallic brush. The product must be completely dry and free from contaminants before you return it to service.

Operate the product only at or below Pollution Degree 2. Pollution is foreign matter in a solid, liquid, or gaseous state that can reduce dielectric strength or surface resistivity. The following is a description of pollution degrees:

- Pollution Degree 1 means no pollution or only dry, nonconductive pollution occurs. The pollution has no influence.
- Pollution Degree 2 means that only nonconductive pollution occurs in most cases. Occasionally, however, a temporary conductivity caused by condensation must be expected.
- Pollution Degree 3 means that conductive pollution occurs, or dry, nonconductive pollution occurs that becomes conductive due to condensation.

You must insulate signal connections for the maximum voltage for which the product is rated. Do not exceed the maximum ratings for the product. Do not install wiring while the product is live with electrical signals. Do not remove or add connector blocks when power is connected to the system. Avoid contact between your body and the connector block signal when hot swapping modules. Remove power from signal lines before connecting them or disconnecting them from the product.

Operate the product at or below the measurement category[1] marked on the hardware label. Measurement circuits are subjected to working voltages[2] and transient stresses (overvoltage) from the circuit to which they are connected during measurement or test. Measurement categories establish standard impulse to withstand voltage levels that commonly occur in electrical distribution systems. The following is a description of measurement categories:

- Measurement Category I is for measurements performed on circuits not directly connected to the electrical distribution system referred to as MAINS[3] voltage. This category is for measurements of voltages from specially protected secondary circuits. Such voltage measurements include signal levels, special hardware, limited-energy parts of hardware, circuits powered by regulated low-voltage sources, and electronics.
- Measurement Category II is for measurements performed on circuits directly connected to the electrical distribution system (MAINS[3]). This category refers to local-level electrical distribution, such as that provided by a standard wall outlet (for example, 115

[1] Measurement categories, also referred to as overvoltage or installation categories, are defined in electrical safety standard IEC 61010-1 and IEC 60664-1.

[2] Working voltage is the highest rms value of an AC or DC voltage that can occur across any particular insulation.

[3] MAINS is defined as a hazardous live electrical supply system that powers hardware. Suitably rated measuring circuits may be connected to the MAINS for measuring purposes.

AC voltage for U.S. or 230 AC voltage for Europe). Examples of Measurement Category II are measurements performed on household appliances, portable tools, and similar hardware.

- Measurement Category III is for measurement performed in the building installation at the distribution level. This category refers to measurements on hard-wired hardware such as hardware in fixed installations, distribution boards, and circuit breakers. Other examples are wiring, including cables, bus bars, junction boxes, switches, socket outlets in the fixed installation, and stationary motors with permanent connections to fixed installations.
- Measurement Category IV is for measurements performed at the primary electrical supply installation typically outside buildings. Examples include electricity meters and measurements on primary overcurrent protection devices and on ripple control units.

# Installing and Configuring

This section describes how to install the PXIe-6672 hardware and software and how to configure the device.

## Installing the Software

Refer to the `readme.htm` file that accompanies the NI-Sync software for software installation directions.

**Note** Be sure to install the driver software before installing the PXIe-6672 hardware.

## Installing the Hardware

The following are general installation instructions. Consult the chassis user manual or technical reference manual for specific instructions and warnings about installing new modules.

1. Power off and unplug the chassis.
2. Choose an available slot in the chassis. The PXIe-6672 can be installed in a System Timing Slot (marked by either a square glyph shown in *Figure 1.* on page 5 or a square glyph with a circle inside of it, as shown in *Figure 2.* on page 6), or in a non-timing PXI Express (PXIe) slot.

**Note** Star trigger functionality and the ability to replace PXI_CLK10 are not available when the PXIe-6672 is installed in a non-timing PXIe slot.

**Figure 1.** System Timing Device Slot Indicator Glyph without Circle

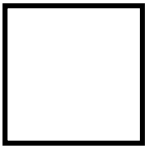
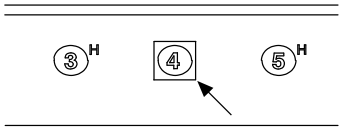


**Figure 2.** System Timing Device Slot Indicator Glyph on the PXIe-1062Q Chassis




**Note** The slot number printed on the glyph may vary from chassis to chassis.

3. Remove the filler panel for the PXI slot you located in step 2, if applicable.
4. Ground yourself using a grounding strap or by holding a grounded object. Follow the ESD protection precautions described in the *Unpacking* section of the *Introduction* section.
5. Remove any packing material from the front panel screws and backplane connectors.
6. Insert the PXIe-6672 into the PXI Express slot. Use the injector/ejector handle to fully insert the module into the chassis.
7. Screw the front panel of the device to the front panel mounting rail of the chassis.
8. If adjacent slots are not populated, use EMC filler panels to cover the opening.

**Caution**

- To ensure the specified EMC performance, you must install PXI EMC filler panels, National Instruments part number 778700-01, in all open chassis slots.
- To ensure the specified EMC performance, operate this product only with double-shielded cables and accessories (for example, RG-223 cables).

9. Visually verify the installation. Make sure the module is not touching other modules or components and is fully inserted into the slot.
10. Plug in and power on the chassis.

The PXIe-6672 is now installed.

## Configuring the Module

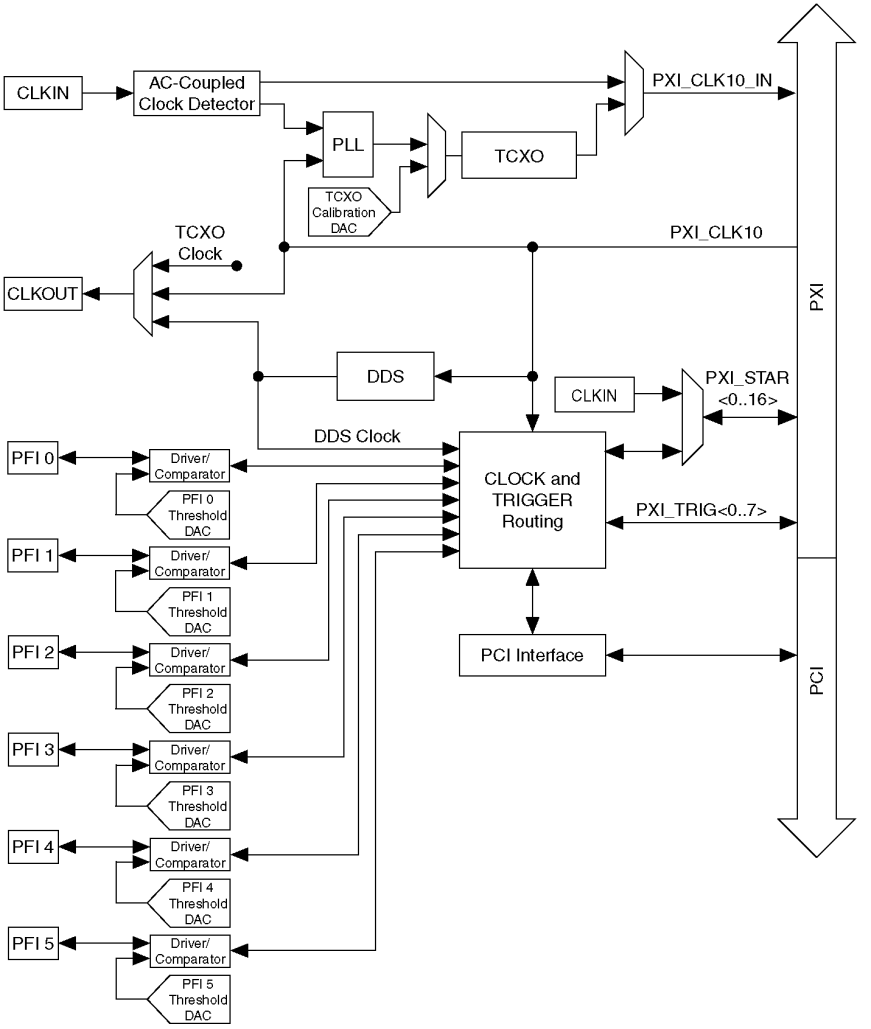
The PXIe-6672 is completely software configurable. The system software automatically allocates all module resources.

The two LEDs on the front panel provide information about module status. The *PXIe-6672 Front Panel* on page 8 section describes the LEDs in greater detail.

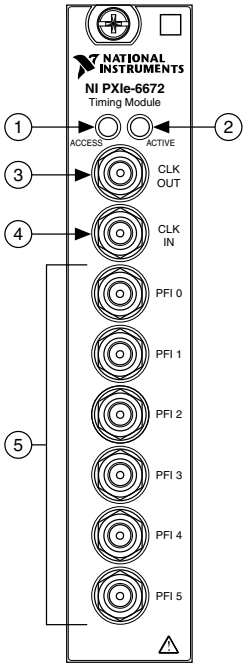
# Hardware Overview

This chapter presents an overview of the hardware functions of the PXIe-6672. *Figure 3.* on page 7 provides a functional overview of the PXIe-6672 hardware.

**Figure 3.** Functional Overview of the PXIe-6672



# PXIe-6672 Front Panel




1. Access LED
2. Active LED
3. CLKOUT Connector
4. CLKIN Connector
5. PFI<0..5> Connectors

## Access LED

The Access LED indicates the communication status of the PXIe-6672.

**Table 1.** Access LED Color Indication

| Color | Status |
|---|---|
| Off | Module is not yet functional. |
| Green | Driver has initialized the module. |
| Amber | Module is being accessed. The Access LED flashes amber for 50 ms when the module is accessed. |

## Active LED

The Active LED can indicate an error or phase-locked loop (PLL) activity. You can change the Active LED to amber, unless an error overrides the selection.

**Tip** Changing the Active LED color to amber is helpful when you want to identify devices in a multi-chassis situation or when you want an indication that your application has reached a predetermined section of the code.

**Table 2.** Active LED Color Quick Reference Table

| Color | Status |
|---|---|
| Off | Module is not yet functional |
| Green | PLL active |
| Amber | User-defined |
| Red | PXI_CLK10 has stopped, or there is a PLL error |

## Connectors

This section describes the connectors on the front panel of the PXIe-6672.

- CLKIN—AC-coupled, 50 Ω clock input. CLKIN can be programmatically routed to:
  - Directly to PXI_CLK10_IN for distribution to other modules in the chassis.
  - The reference input of the onboard oscillator's PLL circuit to route to PXI_CLK10_IN for distribution to other modules in the chassis.
  - Any PXI_STAR line.

  **Note** Refer to the PXIe-6672 Specifications for the frequency ranges for each one of these uses for CLKIN.
- CLKOUT—Clock Output. This connector is used to source a clock that can be routed programmatically from the temperature-compensated crystal oscillator (TCXO), direct digital synthesis (DDS), or the backplane clock (PXI_CLK10).
- PFI<0..5>—Programmable Function Interface<0..5>. These connectors can be used for either input or output. Additionally, PFI 0 can be used as a clock input for internally synchronizing other signals. Refer to the *Synchronous Routing* section for more information about this functionality. You can program the behavior of these PFI connections individually.

Refer to *PXIe-6672 Front Panel* on page 8 for a diagram showing the locations of these connections on the PXIe-6672 front panel.

**Caution** Connections that exceed any of the maximum ratings of input or output signals on the PXIe-6672 can damage the module and the computer. National Instruments is not liable for any damage resulting from such signal connections.

# Hardware Features

The PXIe-6672 performs two broad functions:

- Generating clock and trigger signals.
- Routing internally or externally generated signals from one location to another.

*Table 3.* on page 10 outlines the function and direction of the signals discussed in detail in the remainder of this chapter.

**Table 3.** Signal Descriptions

| Signal Name | Direction | Description |
|---|---|---|
| PXI_CLK10_IN | Out | This is a signal that can replace the native 10 MHz oscillator on the PXI backplane. PXI_CLK10_IN may originate from the onboard TCXO or from an external source. |
| PXI_CLK10 | In | This signal is the PXI 10 MHz backplane clock. By default, this signal is the output of the native 10 MHz oscillator in the chassis. A PXIe-6672 in the System Timing Slot can replace this signal with PXI_CLK10_IN. |
| TCXO Clock | Out | This is the output of the 10 MHz TCXO. The TCXO is an extremely stable and accurate frequency source. |
| CLKIN | In | CLKIN is a signal connected to the SMB input pin of the same name. CLKIN can be routed directly to PXI_CLK10_IN, used as a phase lock reference for the TCXO, or be routed to a PXI_STAR line. |
| CLKOUT | Out | CLKOUT is the signal on the SMB output pin of the same name. Either the TCXO clock, DDS clock, or PXI_CLK10 may be routed to this location. |
| DDS Clock | Out | This is the output of the DDS. The DDS frequency can be programmed with fine granularity from 1 Hz to 105 MHz. The DDS chip automatically phase-locks to PXI_CLK10. |
| PXI_STAR <0..16> | In/Out | The PXI star trigger bus connects the System Timing Slot to all other slots in a star configuration. The electrical paths of each star line are closely matched to minimize intermodule skew. A PXIe-6672 in the System Timing Slot can route signals to all other slots using the star trigger bus. |

**Table 3.** Signal Descriptions (Continued)

| Signal Name | Direction | Description |
|---|---|---|
| PFI <0..5> | In/Out | The Programmable Function Interface pins on the PXIe-6672 route timing and triggering signals between multiple PXI chassis. A wide variety of input and output signals can be routed to or from the PFI lines. |
| PXI_TRIG <0..7> | In/Out | The PXI trigger bus consists of eight digital lines shared among all slots in the PXI chassis. The PXIe-6672 can route a wide variety of signals to and from these lines. |

The remainder of this chapter describes how these signals are used, acquired, and generated by the PXIe-6672 hardware, and explains how you can route the signals between various locations to synchronize multiple measurement devices and PXI chassis.

# Clock Generation and Routing

The PXIe-6672 can generate two types of clock signals. The first type of clock is generated using the onboard DDS chip, and the second is generated with a precise 10 MHz oscillator. The following sections describe the two types of clock generation and explain the considerations for choosing either type.

The CLKOUT connector on the PXIe-6672 may be used to route the TCXO, PXI_CLK10, or DDS clock.

## Direct Digital Synthesis (DDS)

The PXIe-6672 includes built-in advanced clock generation circuitry for generating clock signals with high frequency resolution (<0.075 Hz). The clock generation circuitry is based on direct digital synthesis (DDS).

The accuracy of the frequency depends on the PXI_CLK10 reference clock, so a precise 10 MHz source improves the accuracy of the DDS output. You can replace the 10 MHz clock with the TCXO for more accurate DDS timing.

When the DDS is programmed, an update signal must be sent to it before it will begin operating as programmed. The source for this update signal is either immediate (DDS starts outputting the programmed frequency as soon as software programs it) or one of the eight PXI triggers. When one of the PXI trigger lines is used as the source for the update, frequency generation will not start until a rising edge occurs on the PXI trigger selected.

**Note** NI-Sync software defaults to an immediate update. If a PXI trigger is used instead, the user must specify the update signal source before setting any of the other DDS properties.

When more than one PXIe-6672 is used in a multiple chassis setup, the DDS frequency of both boards can be synchronized. The DDS system clock is phase locked to PXI_CLK10. When two or more chassis share a common 10 MHz clock, the DDS outputs will also be phase locked.

**Note** Refer to the *Using the PXI_CLK10 PLL* section for more information on how to ensure that two or more chassis have close PXI_CLK10 phase alignment.

To fully synchronize the DDS outputs, a common update signal source must be used and routed to the selected PXI trigger. A synchronous route to PXI_CLK10 provides the best results. Refer to the *Routing Triggers* section for details on routing trigger signals.

## Replacing PXI_CLK10

A module in System Timing Slot of a PXI Express chassis can replace the PXI_CLK10 reference clock of the chassis. The PXIe-6672 provides three options for driving a clock to the PXI_CLK10 backplane: TCXO, CLKIN, and 10 MHz PLL.

### TCXO

The PXIe-6672 features a precision 10 MHz temperature-compensated crystal oscillator (TCXO). The frequency accuracy of this clock is much greater than the frequency accuracy of the native 10 MHz PXI backplane clock (PXI_CLK10). The TCXO contains circuitry to measure the temperature of the oscillator. It uses the temperature to adjust its frequency output according to the crystal's known frequency variation across its operating temperature range. The TCXO can be routed to PXI_CLK10_IN to replace the backplane's native PXI_CLK10 to achieve more accurate synchronization.

### CLKIN

The PXIe-6672 allows the user to connect their own 10 MHz reference directly to PXI_CLK10_IN by using the CLKIN connector on the front panel. CLKIN is an AC-coupled, 50 Ω terminated input to the PXIe-6672. In order to increase the amplitude of signals the CLKIN receiver can use, the CLKIN circuitry features software-enabled attenuation, which will attenuate the input signal by a factor of five when enabled. NI-Sync software will by default configure the attenuation to be enabled. If the input signal supplied to CLKIN is less than 1.2 $V_{pp}$, the attenuation should be turned off in order to extend down the range of amplitudes CLKIN can receive.

When using CLKIN for driving PXI_CLK10_IN, refer to the user manual for your PXI Express chassis for information on the frequency range your chassis is capable of receiving on PXI_CLK10_IN.

### 10 MHz PLL

The PXIe-6672 features a phase locked loop (PLL) circuit for aligning the frequency of the TCXO with a reference clock supplied by the user from CLKIN. In this configuration, the TCXO is routed to the backplane on PXI_CLK10_IN. The PXI Express backplane will in turn phase lock the PXI_CLK10 signal to the PXI_CLK10_IN signal. The PXIe-6672 uses the PXI_CLK10 signal it receives from the backplane as feedback to the 10 MHz PLL circuitry. The PLL circuitry controls the frequency of the TCXO by varying the tuning voltage used for electronic frequency control. By increasing or decreasing the frequency of the TCXO as needed, the 10 MHz PLL of the PXIe-6672 is able to match the TCXO frequency to the reference clock supplied by the user from CLKIN.

Use of the 10 MHz PLL of the PXIe-6672 has advantages over using just CLKIN or the TCXO to drive PXI_CLK10_IN:

- Reference frequencies other than 10 MHz can be used. The 10 MHz PLL includes internal dividers to divide both the reference from CLKIN and PXI_CLK10 down as needed in order to make both a common frequency. This frequency is called the phase detector frequency, as it is the frequency at which the PLL compares edge alignment to determine if it should speed up or slow down the TCXO. The PXIe-6672 supports any reference frequency that is an integer multiple of 1 MHz to be used.
- If CLKIN stops or becomes disconnected, PXI_CLK10 is still present in the chassis.
- The 10 MHz PLL acts as a zero-delay buffer between the CLKIN connector and PXI_CLK10 at the backplane connector. Because the 10 MHz PLL uses PXI_CLK10 for feedback, it is able to create a known fixed phase relation between PXI_CLK10 and the reference supplied on CLKIN. During manufacturing, the phase relation the 10 MHz PLL maintains is adjusted so that a rising edge at the CLKIN connector will align in time with a rising edge of PXI_CLK10 at the peripheral slot connector of the backplane. This phase relation will remain in place regardless of the PXI Express chassis used, allowing for simpler multi-chassis system synchronization.

# Routing Triggers

The PXIe-6672 has versatile trigger routing capabilities. It can route signals to and from the front panel, the PXI triggers, and the PXI star triggers. In addition, CLKIN is a valid source for PXI_Star.

*Figure 4.* on page 14 and *Figure 5.* on page 14 summarize the routing features of the PXIe-6672. The remainder of this chapter details the capabilities and constraints of the routing architectures.

**Figure 4.** High-Level Schematic of PXIe-6672 Signal Routing Architecture

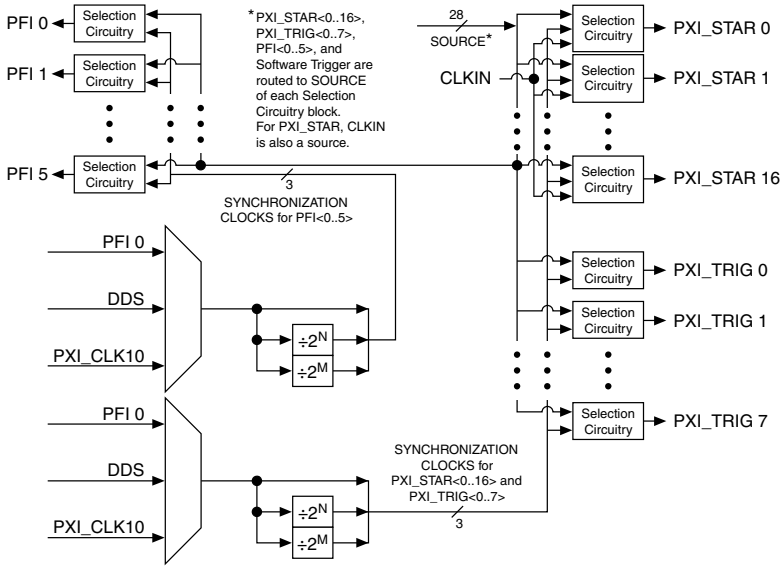
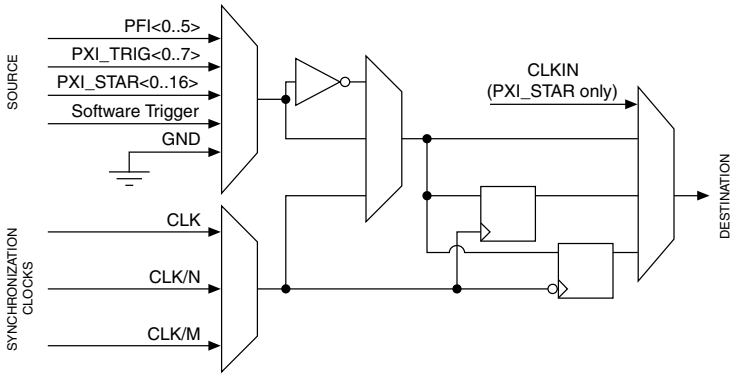



*Figure 5.* on page 14 provides a more detailed view of the Selection Circuitry referenced in *Figure 4.* on page 14.

**Figure 5.** Signal Selection Circuitry Diagram



## Determining Sources and Destinations

All signal routing operations can be characterized by a *source* (input) and a *destination*. In addition, synchronous routing operations must also define a third signal known as the *synchronization clock*. Refer to the *Choosing the Type of Routing* section for more information on synchronous versus asynchronous routing.

*Table 4.* on page 15 summarizes the sources and destinations of the PXIe-6672. The destinations are listed in the horizontal heading row, and the sources are listed in the column at the far left. An X in a cell indicates that the source and destination combination defined by that cell is a valid routing combination.

**Table 4.** Sources and Destinations for PXIe-6672 Signal Routing Operations

| | | Destinations | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | Front Panel | | | Backplane | | | Onboard |
| Sources | Front Panel | | CLKOUT | PFI<0..5> | PXI_CLK10_IN | PXI_STAR | PXI_TRIG | TCXO PLL |
| | | CLKIN | X* | X*† | X | X | X*† | X |
| | | PFI<0..5> | | X | | X | X | |
| | Backplane | PXI_CLK10 | X | X† | | X† | X† | |
| | | PXI_STAR<0..16> | | X | | X | X | |
| | | PXI TRIG <0..7> | | X | | X | X | |
| | Onboard | TCXO | X | X*† | X | X*† | X*† | |
| | | DDS | X | X† | | X† | X† | |
| | | Global Software Trigger | | X | | X | X | |

* Can be accomplished in two stages by routing source to PXI_CLK10_IN, replacing PXI_CLK10 with PXI_CLK10_IN (occurs automatically in most chassis), and then routing PXI_CLK10 to the destination. The source must be 10 MHz.

† Routing PXI_CLK10 or DDS to PFI, PXI_STAR, or PXI_TRIG is accomplished by setting PXI_CLK10 or DDS to be the synchronization clock (using the NI-Sync Property Node), and then routing the synchronization clock as the source.

## Using Front Panel PFIs as Inputs

The front-panel PFIs can receive external signals from 0 to +5 V. The input impedance can be programmatically set to 1 kΩ or 50 Ω, to match the cable impedance and minimize reflections.

**Note** Terminating the signals with a 50 Ω impedance is recommended when the source is another PXIe-6672 or any other source with a 50 Ω output.

The voltage thresholds for the front panel PFI inputs are programmable. The input signal is generated by comparing the input voltage on the PFI connectors to the voltage output of software-programmable DACs. The thresholds for the PFI lines are individually programmable, which is useful if you are importing signals from multiple sources with different voltage swings. The front panel PFI inputs can be routed to any PXI_Star triggers, PXI triggers, or other front panel PFI outputs.

## Using Front Panel PFIs as Outputs

The front panel PFI outputs are +3.3 V drivers with 50 Ω output impedance. The outputs can drive high-impedance loads or 50 Ω loads, such as a 50 Ω coaxial cable with a 50 Ω receiver.

When driving a high-impedance load, the receiver sees a +3.3 V signal. When driving a 50 Ω load, the receiver sees a single +1.6 V step—a +3.3 V step split across the 50 Ω resistors at the source and the destination. This cable configuration is the recommended setup to minimize reflections.

You can independently select the output signal source for each PFI line from one of the following sources:

- Another PFI<0..5>
- PXI triggers<0..7> (PXI_TRIG<0..7>)
- PXI_STAR<0..16>
- Global software trigger
- PFI synchronization clock

The PFI synchronization clock may be any of the following signals:

- DDS clock
- PXI_CLK10
- PFI 0 Input
- Any of the previously-listed signals divided by the first frequency divider ($2^n$, up to 512).
- Any of the previously-listed signals divided by the second frequency divider ($2^m$, up to 512).

Refer to the *Choosing the Type of Routing* section for more information on the synchronization clock.

**Note** The PFI synchronization clock is the same for all routing operations in which PFI<0..5> is defined as the output, although the divide-down ratio for this clock (full rate, first divider, second divider) may be chosen on a per route basis.

## Using the PXI Triggers

The PXI trigger bus is a set of eight electrical lines that go to every slot in a segment of a PXI chassis (multi-drop up to eight slots). Only one PXI module should drive a particular PXI_Trigger line at a given time. The signal is then received by modules in all other PXI slots. This feature makes the PXI triggers convenient in situations where you want, for instance, to trigger several devices, because all modules will receive the same trigger.

Given the architecture of the PXI trigger bus, triggering signals do not reach each slot at precisely the same time. A difference of several nanoseconds can occur between slots, especially in larger PXI chassis (which can have buffers between segments). This delay is not a problem for many applications. However, if your application requires tighter synchronization, use the PXI_STAR triggers (see next section), or use the PXI trigger bus synchronous to PXI_CLK10. National Instruments does not recommend sending asynchronous triggers over PXI_TRIG lines.

The multi-drop nature of the PXI trigger bus can introduce signal integrity issues. Therefore, National Instruments does not recommend the use of the PXI_TRIG lines for clock distribution. The preferred method for clock distribution is the use of the PXI_Star triggers.

You can independently select the output signal source for each PXI trigger line from one of the following sources:

- PFI<0..5>
- Another PXI trigger<0..7> (PXI_TRIG<0..7>)
- PXI_STAR<0..16>
- Global software trigger
- PXI_TRIG/PXI_STAR synchronization clock

The PXI_TRIG/PXI_STAR synchronization clock may be any of the following signals:

- DDS clock
- PXI_CLK10
- PFI0 Input
- Any of the previously listed signals divided by the first frequency divider ($2^n$, up to 512).
- Any of the previously listed signals divided by the second frequency divider ($2^m$, up to 512).

Refer to the *Choosing the Type of Routing* section for more information on the synchronization clock.

**Note** The PXI_TRIG/PXI_STAR synchronization clock is the same for all routing operations in which PXI_TRIG <0..7> or PXI_STAR <0..16> is defined as the output, although the divide-down ratio for this clock (full rate, first divider, second divider) may be chosen on a per route basis.

## Using the PXI Star Triggers

There are up to 17 PXI star triggers per chassis. Each trigger line is a dedicated connection between the System Timing Slot and one other slot. The PXI Specification, Revision 2.1, requires that the propagation delay along each star trigger line be matched to within 1 ns. A typical upper limit for the skew in most NI PXI chassis is 500 ps. The low skew of the PXI star trigger bus is useful for applications that require triggers to arrive at several modules nearly simultaneously.

The star trigger lines are bidirectional, so signals can be sent to System Timing Slot from a module in another slot or from System Timing Slot to the other module.

You can independently select the output signal source for each PXI star trigger line from one of the following sources:

- PFI<0..5>
- PXI triggers <0..7> (PXI_TRIG <0..7>)
- Another PXI star trigger line (PXI_STAR <0..16>)
- Global software trigger
- PXI_Trig/PXI_Star synchronization clock
- CLKIN

Refer to the *Using the PXI Triggers* section for more information on the PXI_Trig/PXI_Star synchronization clock.

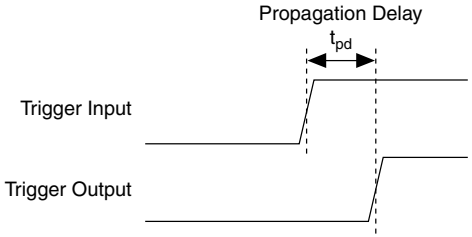
## Choosing the Type of Routing

The PXIe-6672 routes signals in one of two ways: asynchronously or synchronously. The following sections describe the two routing types and the considerations for choosing each type.

### Asynchronous Routing

Asynchronous routing is the most straightforward method of routing signals. Any asynchronous route can be defined in terms of two signals: a *source* and a *destination*. A digital pulse or train comes in on the source and is propagated to the destination. When the source signal goes from low to high, this rising edge is transferred to the destination after a propagation delay through the module. *Figure 6.* on page 18 illustrates an asynchronous routing operation.

**Figure 6.** Asynchronous Routing Operation




Some delay is always associated with an asynchronous route, and this delay varies among PXIe-6672 modules, depending on variations in temperature and chassis voltage. Typical delay times in the PXIe-6672 for asynchronous routes between various sources and destinations are given in the device's Specifications.

Asynchronous routing works well if the total system delays are not too long for the application. Propagation delay could be caused by the following reasons:

- Output delay on the source.
- Propagation delay of the signal across the backplane(s) and cable(s).
- Propagation delay of the signal through the PXIe-6672.
- Time for the receiver to recognize the signal.

Both the source and the destination of an asynchronous routing operation on the PXIe-6672 can be any of the following lines:

- Any front panel PFI pin (PFI<0..5>) as single ended.
- Any PXI star trigger line (PXI_STAR<0..16>)
- Any PXI trigger line (PXI_TRIG<0..7>)

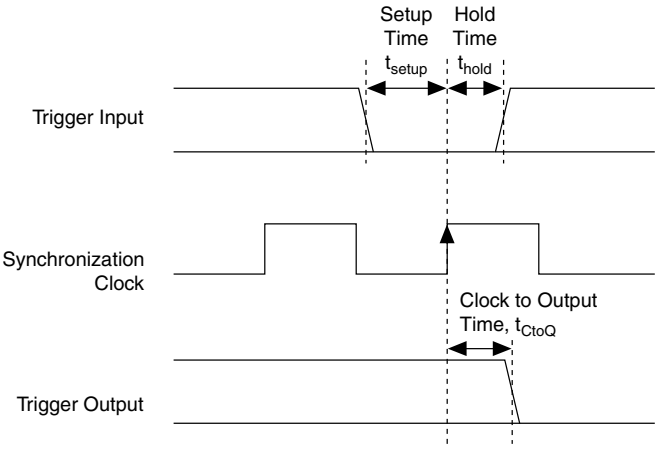
### Synchronous Routing

A synchronous routing operation is defined in terms of three signals: a *source*, a *destination*, and a *synchronization clock*. Unlike asynchronous routing, the output of a synchronous routing operation does not directly follow the input after a propagation delay. Instead, the logic state of the input is sampled on each active edge of the synchronization clock, and the output is set

to that logic state after a small delay, as shown in *Figure 7.* on page 19. Thus, the output is said to be "synchronous" with this clock.

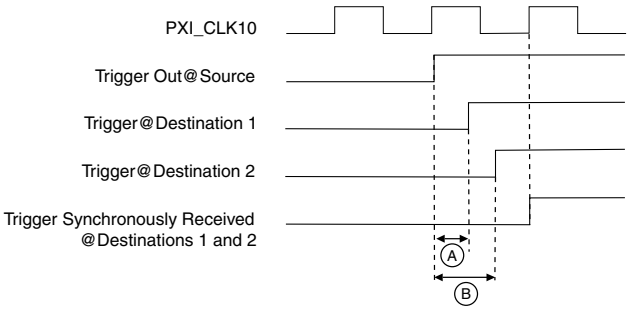
*Figure 7.* on page 19 shows a timing diagram that illustrates synchronous routing.

**Figure 7.** Synchronous Routing Operation




The PXIe-6672 board supports routing signals synchronous to either the rising or falling edge of the synchronization clock. In addition, the polarity of the destination signal can be inverted, which is useful when handling active-low digital signals. Synchronous routing can be useful for eliminating skew when sending triggers to several destinations. For example, when sending triggers using the PXI Trigger lines, the trigger arrives at each slot at a slightly different time. However, if the trigger is sent and received synchronously using a low-skew synchronization clock (for example, PXI_CLK10), all receiving devices can act on the trigger at the same time, as shown in *Figure 8.* on page 19:

**Figure 8.** Synchronous Routing to Multiple Destinations

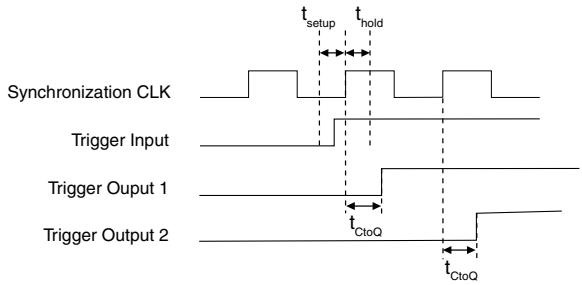



A: Propagation delay from source to destination 1.

B: Propagation delay from source to destination 2.

Synchronous routing requires the input to be stable at a logic low or logic high state within a window of time around the clock edge. This window of time around the clock edge is defined by the setup time ($t_{setup}$) and hold time ($t_{hold}$). If the input signal changes within this window of time, it is undetermined whether the output of the synchronous route will go to the old or new logic state. This is important, for example, if a source is being routed synchronously to several destinations. If the source signal changes within the setup-and-hold window around the synchronization clock dge, one of the destinations might go to the new logic level while the other destination might remain at the old logic level and change when the next synchronization clock edge occurs, as shown in *Figure 9.* on page 20:

**Figure 9.** Synchronous Routing Uncertainty with Setup-and-Hold Variations




Therefore, if your application requires that the trigger arrive at the multiple destinations simultaneously, you must ensure that the input is stable within the setup and hold window around the synchronization clock edge. For more information and possible methods to ensure this requirement is met, go to `ni.com/info` and enter the Info Code `SyncTriggerRouting`.

Possible sources for synchronous routing with the PXIe-6672 include the following sources:

- Any front panel PFI pin.
- Any PXI star trigger line (PXI_STAR<0..16>)
- Any PXI trigger line (PXI_TRIG<0..7>)
- Global software trigger
- The synchronization clock itself.

The synchronization clock for a synchronous route can be any of the following signals.

- 10 MHz PXI_CLK10
- Clock Generation (DDS)
- Front panel PFI 0 input
- Any of the previously listed signals divided by the first frequency divider ($2^n$, up to 512).
- Any of the previously listed signals divided by the second frequency divider ($2^m$, up to 512).

Refer to *Figure 4.* on page 14 and *Figure 5.* on page 14 for an illustration of how the PXIe-6672 performs synchronous routing operations.

### Generating a Single Pulse (Global Software Trigger)

The global software trigger is a single pulse with programmable delay that is fired on a software command. This signal is always routed synchronously with a clock. Therefore, asynchronous routing is not supported when the signal source is the global software trigger.

The software trigger can be delayed by up to 15 clock cycles on a per-route basis. This feature is useful if a single pulse must be sent to several destinations with significantly different propagation delays. By delaying the pulse on the routes with shorter paths, you can compensate for the propagation delay. An example of such a situation would be when a trigger pulse must arrive nearly simultaneously at the local backplane and the backplane of another chassis separated by 50 m of coaxial cable.

# Calibration

This chapter discusses the calibration of the PXIe-6672.

Calibration consists of verifying the measurement accuracy of a device and correcting for any measurement error. The PXIe-6672 is factory calibrated before shipment at 23 ±5 °C to the levels indicated in the device's specifications. The associated calibration constants—the corrections that were needed to meet specifications—are stored in the onboard nonvolatile memory (EEPROM). The driver software uses these stored values.

## Factory Calibration

The factory calibration of the PXIe-6672 involves calculating and storing four calibration constants. These values control the accuracy of four features of the device, which are discussed in the following sections.

### TCXO Frequency

The TCXO frequency can be varied over a small range. The output frequency of the TCXO is adjusted using this constant to meet the specification listed in the device's specifications. This calibration applies only to the PXIe-6672.

### PXI_CLK10 Phase

When using the PLL to lock PXI_CLK10 to an external reference clock, the phase between the clocks can be adjusted. The time between rising edges of PXI_CLK10 and the input clock is minimized using this constant.

### DDS Start Trigger Phase

To start the DDS reliably, the DDS start trigger must arrive within a certain window of time. The phase of the DDS start trigger is controlled by this constant to meet the setup and hold-time requirements of the DDS.

### DDS Initial Phase

The phase of the DDS output is adjusted using this constant so that the DDS outputs from multiple PXIe-6672 modules are aligned.

## Additional Information

Refer to ni.com/calibration for additional information on NI calibration services.

# Compliance

### Electromagnetic Compatibility Information

This hardware has been tested and found to comply with the applicable regulatory requirements and limits for electromagnetic compatibility (EMC) as indicated in the hardware's Declaration of Conformity (DoC)[4]. These requirements and limits are designed to provide reasonable protection against harmful interference when the hardware is operated in the intended electromagnetic environment. In special cases, for example when either highly sensitive or noisy hardware is being used in close proximity, additional mitigation measures may have to be employed to minimize the potential for electromagnetic interference.

**Caution** To ensure the specified EMC performance, operate this product only with double-shielded cables and accessories (for example, RG-223 cables).

While this hardware is compliant with the applicable regulatory EMC requirements, there is no guarantee that interference will not occur in a particular installation. To minimize the potential for the hardware to cause interference to radio and television reception or to experience unacceptable performance degradation, install and use this hardware in strict accordance with the instructions in the hardware documentation and the DoC[4].

If this hardware does cause interference with licensed radio communications services or other nearby electronics, which can be determined by turning the hardware off and on, you are encouraged to try to correct the interference by one or more of the following measures:

- Reorient the antenna of the receiver (the device suffering interference).
- Relocate the transmitter (the device generating interference) with respect to the receiver.
- Plug the transmitter into a different outlet so that the transmitter and the receiver are on different branch circuits.

Some hardware may require the use of a metal, shielded enclosure (windowless version) to meet the EMC requirements for special EMC environments, such as for marine use or in heavy industrial areas. Refer to the hardware's user documentation and the DoC[4] for product installation requirements.

When the hardware is connected to a test object or to test leads, the system may become more sensitive to disturbances or may cause interference in the local electromagnetic environment.

---

[4] The Declaration of Conformity (DoC) contains important EMC compliance information an dinstructions for the user or installer. To obtain the DoC for this product, visit ni.com/certification, search by model number or product line, and click the appropriate link in the Certification column.

Operation of this hardware in a residential area is likely to cause harmful interference. Users are required to correct the interference at their own expense or cease operation of the hardware.

Changes or modifications not expressly approved by National Instruments could void the user's right to operate the hardware under the local regulatory rules.

## Electromagnetic Compatibility Information

This hardware has been tested and found to comply with the regulatory requirements and limits for electromagnetic compatibility (EMC) as indicated in the hardware's Declaration of Conformity (DoC).

If this hardware does cause interference with licensed radio communications services or other nearby electronics, which can be determined by turning the hardware off and on, you are encouraged to try to correct the interference by one or more of the following measures:

- Reorient the antenna of the receiver (the device suffering interference).
- Relocate the transmitter (the device generating interference) with respect to the receiver.
- Plug the transmitter into a different outlet so that the transmitter and the receiver are on different branch circuits.

Some hardware may require the use of a metal, shielded enclosure (windowless version) to meet the EMC requirements for special EMC environments such as for marine use or in heavy industrial areas. Refer to the hardware's user documentation and the DoC[5] for product installation requirements.

When the hardware is connected to a test object or to test leads, the system may become more sensitive to disturbances or may cause interference in the local electromagnetic environment.

Operation of this hardware in a residential area is likely to cause harmful interference. Users are required to correct the interference at their own expense or cease operation of the hardware.

Changes or modifications not expressly approved by National Instruments could void the user's right to operate the hardware under the local regulatory rules.

**Caution** To ensure the specified EMC performance, operate this product only with double-shielded cables (such as RG-223 double-shielded cables) and accessories.

**Caution** To ensure the specified EMC performance, you must install PXI EMC filler panels, National Instruments part number 778700-01, in all open chassis slots.

# Legal Information

*Limited Warranty*

*Copyright*

[5] The Declaration of Conformity (DoC) contains important EMC compliance information and instructions for the user and installer. To obtain the DoC for this product, visit ni.com/certification, search by model number or product line, and click the appropriate link in the Certification column.

*Trademarks*

*Patents*

*Export Compliance Information*

*Warning Regarding Use of NI Products*

# Limited Warranty

This document is provided "as is" and is subject to being changed, without notice, in future editions. For the latest version, refer to `ni.com/manuals`. NI reviews this document carefully for technical accuracy; however, NI MAKES NO EXPRESS OR IMPLIED WARRANTIES AS TO THE ACCURACY OF THE INFORMATION CONTAINED HEREIN AND SHALL NOT BE LIABLE FOR ANY ERRORS.

NI warrants that its hardware products will be free of defects in materials and workmanship that cause the product to fail to substantially conform to the applicable NI published specifications for one (1) year from the date of invoice.

For a period of ninety (90) days from the date of invoice, NI warrants that (i) its software products will perform substantially in accordance with the applicable documentation provided with the software and (ii) the software media will be free from defects in materials and workmanship.

If NI receives notice of a defect or non-conformance during the applicable warranty period, NI will, in its discretion: (i) repair or replace the affected product, or (ii) refund the fees paid for the affected product. Repaired or replaced hardware will be warranted for the remainder of the original warranty period or ninety (90) days, whichever is longer. If NI elects to repair or replace the product, NI may use new or refurbished parts or products that are equivalent to new in performance and reliability and are at least functionally equivalent to the original part or product.

You must obtain an RMA number from NI before returning any product to NI. NI reserves the right to charge a fee for examining and testing hardware not covered by the Limited Warranty.

This Limited Warranty does not apply if the defect of the product resulted from improper or inadequate maintenance, installation, repair, or calibration (performed by a party other than NI); unauthorized modification; improper environment; use of an improper hardware or software key; improper use or operation outside of the specification for the product; improper voltages; accident, abuse, or neglect; or a hazard such as lightning, flood, or other act of nature.

THE REMEDIES SET FORTH ABOVE ARE EXCLUSIVE AND THE CUSTOMER'S SOLE REMEDIES, AND SHALL APPLY EVEN IF SUCH REMEDIES FAIL OF THEIR ESSENTIAL PURPOSE.

EXCEPT AS EXPRESSLY SET FORTH HEREIN, PRODUCTS ARE PROVIDED "AS IS" WITHOUT WARRANTY OF ANY KIND AND NI DISCLAIMS ALL WARRANTIES,

EXPRESSED OR IMPLIED, WITH RESPECT TO THE PRODUCTS, INCLUDING ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, TITLE OR NON-INFRINGEMENT, AND ANY WARRANTIES THAT MAY ARISE FROM USAGE OF TRADE OR COURSE OF DEALING. NI DOES NOT WARRANT, GUARANTEE, OR MAKE ANY REPRESENTATIONS REGARDING THE USE OF OR THE RESULTS OF THE USE OF THE PRODUCTS IN TERMS OF CORRECTNESS, ACCURACY, RELIABILITY, OR OTHERWISE. NI DOES NOT WARRANT THAT THE OPERATION OF THE PRODUCTS WILL BE UNINTERRUPTED OR ERROR FREE.

In the event that you and NI have a separate signed written agreement with warranty terms covering the products, then the warranty terms in the separate agreement shall control.

# Copyright



## End-User License Agreements and Third-Party Legal Notices

You can find end-user license agreements (EULAs) and third-party legal notices in the following locations:

- Notices are located in the `<National Instruments>\_Legal Information` and `<National Instruments>` directories.
- EULAs are located in the `<National Instruments>\Shared\MDF\Legal \license` directory.
- Review `<National Instruments>\_Legal Information.txt` for information on including legal information in installers built with NI products.

## U.S. Government Restricted Rights

If you are an agency, department, or other entity of the United States Government ("Government"), the use, duplication, reproduction, release, modification, disclosure or transfer of the technical data included in this manual is governed by the Restricted Rights provisions under Federal Acquisition Regulation 52.227-14 for civilian agencies and Defense Federal Acquisition Regulation Supplement Section 252.227-7014 and 252.227-7015 for military agencies.

### IVI Foundation Copyright Notice

Content from the IVI specifications reproduced with permission from the IVI Foundation.

The IVI Foundation and its member companies make no warranty of any kind with regard to this material, including, but not limited to, the implied warranties of merchantability and fitness for a particular purpose. The IVI Foundation and its member companies shall not be liable for errors contained herein or for incidental or consequential damages in connection with the furnishing, performance, or use of this material.

## Trademarks

Refer to the *NI Trademarks and Logo Guidelines* at *ni.com/trademarks* for more information on NI trademarks.

ARM, Keil, and µVision are trademarks or registered of ARM Ltd or its subsidiaries.

LEGO, the LEGO logo, WEDO, and MINDSTORMS are trademarks of the LEGO Group.

TETRIX by Pitsco is a trademark of Pitsco, Inc.

FIELDBUS FOUNDATION™ and FOUNDATION™ are trademarks of the Fieldbus Foundation.

EtherCAT® is a registered trademark of and licensed by Beckhoff Automation GmbH.

CANopen® is a registered Community Trademark of CAN in Automation e.V.

DeviceNet™ and EtherNet/IP™ are trademarks of ODVA.

Go!, SensorDAQ, and Vernier are registered trademarks of Vernier Software & Technology. Vernier Software & Technology and vernier.com are trademarks or trade dress.

Xilinx is the registered trademark of Xilinx, Inc.

Taptite and Trilobular are registered trademarks of Research Engineering & Manufacturing Inc.

FireWire® is the registered trademark of Apple Inc.

Linux® is the registered trademark of Linus Torvalds in the U.S. and other countries.

Handle Graphics®, MATLAB®, Simulink®, Stateflow®, and xPC TargetBox® are registered trademarks, and Simulink Coder™, TargetBox™, and Target Language Compiler™ are trademarks of The MathWorks, Inc.

Tektronix®, Tek, and Tektronix, Enabling Technology are registered trademarks of Tektronix, Inc.

The Bluetooth® word mark is a registered trademark owned by the Bluetooth SIG, Inc.

The ExpressCard™ word mark and logos are owned by PCMCIA and any use of such marks by National Instruments is under license.

The mark LabWindows is used under a license from Microsoft Corporation. Windows is a registered trademark of Microsoft Corporation in the United States and other countries.

Other product and company names mentioned herein are trademarks or trade names of their respective companies.

Members of the National Instruments Alliance Partner Program are business entities independent from NI and have no agency, partnership, or joint-venture relationship with NI.

## Patents

For patents covering the NI products/technology, refer to the appropriate location: **Help»Patents** in your software, the `patents.txt` file on your media, or the *National Instruments Patent Notice* at *ni.com/patents*.

## Export Compliance Information

Refer to the *Export Compliance Information* at `ni.com/legal/export-compliance` for the National Instruments global trade compliance policy and how to obtain relevant HTS codes, ECCNs, and other import/export data.

## WARNING REGARDING USE OF NATIONAL INSTRUMENTS PRODUCTS

YOU ARE ULTIMATELY RESPONSIBLE FOR VERIFYING AND VALIDATING THE SUITABILITY AND RELIABILITY OF THE PRODUCTS WHENEVER THE PRODUCTS ARE INCORPORATED IN YOUR SYSTEM OR APPLICATION, INCLUDING THE APPROPRIATE DESIGN, PROCESS, AND SAFETY LEVEL OF SUCH SYSTEM OR APPLICATION.

PRODUCTS ARE NOT DESIGNED, MANUFACTURED, OR TESTED FOR USE IN LIFE OR SAFETY CRITICAL SYSTEMS, HAZARDOUS ENVIRONMENTS OR ANY OTHER ENVIRONMENTS REQUIRING FAIL-SAFE PERFORMANCE, INCLUDING IN THE OPERATION OF NUCLEAR FACILITIES; AIRCRAFT NAVIGATION; AIR TRAFFIC CONTROL SYSTEMS; LIFE SAVING OR LIFE SUSTAINING SYSTEMS OR SUCH OTHER MEDICAL DEVICES; OR ANY OTHER APPLICATION IN WHICH THE FAILURE OF THE PRODUCT OR SERVICE COULD LEAD TO DEATH, PERSONAL INJURY, SEVERE PROPERTY DAMAGE OR ENVIRONMENTAL HARM (COLLECTIVELY, "HIGH-RISK USES"). FURTHER, PRUDENT STEPS MUST BE TAKEN TO PROTECT AGAINST FAILURES, INCLUDING PROVIDING BACK-UP AND SHUT-DOWN MECHANISMS. NI EXPRESSLY DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY OF FITNESS OF THE PRODUCTS OR SERVICES FOR HIGH-RISK USES.

372185H-01 October 2, 2019