Where to Start with the NI PXI-7831R

Thank you for purchasing a National Instruments PXI-7831R. This document explains how to set up the hardware system and use the NI PXI-7831R. This reconfigurable I/O (RIO) device has 96 digital I/O (DIO) lines, eight independent, 16-bit analog output (AO) channels, and eight independent, 16-bit analog input (AI) channels.

A user-reconfigurable field-programmable gate array (FPGA) controls the digital and analog I/O on the NI PXI-7831R. The FPGA on the RIO device allows you to define the functionality and timing of the device, whereas traditional multifunction I/O (MIO) devices have a fixed functionality provided by an application-specific integrated circuit (ASIC). You can change the functionality of the FPGA on the RIO device by using LabVIEW, a graphical programming environment, and the LabVIEW FPGA module to create and download a custom virtual instrument (VI) to the FPGA. You can reconfigure the RIO device with a new VI at any time. Using LabVIEW, you can graphically design the timing and functionality of the RIO device without having to learn the low-level programming language or hardware description language (HDL) that is traditionally used for FPGA design.

Note If you have LabVIEW and not the LabVIEW FPGA module, you cannot create new FPGA VIs. You can only create VIs that run in LabVIEW to control existing FPGA VIs.

Some applications require tasks such as real-time, floating-point processing or data logging while performing I/O and logic on the RIO device. You can use the LabVIEW Real-Time Module to perform these additional applications while also communicating with and controlling the RIO device.

The RIO device contains flash memory to store VIs for instant loading of the FPGA when the system is powered on.

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NATIONAL INSTRUMENTS

What You Need to Get Started

This section contains two lists that detail what you need to get started using the NI PXI-7831R with the LabVIEW Real-Time Module or with Windows 2000/XP.

Getting Started with Windows 2000/XP

To set up and use the NI PXI-7831R with Windows 2000/XP, you need the following items:

- ❑ NI PXI-7831R
- ❑ The following software packages:
  - LabVIEW version 7.0 or later
  - NI Device Drivers CD
  - LabVIEW FPGA Module version 7.0 or later (required to develop custom FPGA VIs for the RIO device)
- ❑ PXI/CompactPCI chassis and a PXI/CompactPCI embedded controller, running Windows 2000/XP (or any computer running Windows 2000/XP and a MXI-3 link to a PXI/CompactPCI chassis)
- ❑ At least one cable and terminal block for connecting signals to the NI PXI-7831R
- ❑ The following documents are included on the NI Device Drivers CD and are also available at `ni.com/manuals` (optional):
  - *LabVIEW FPGA Module Release Notes*
  - *LabVIEW FPGA Module User Manual*
  - *NI PXI-7831R User Manual*
- ❑ The *LabVIEW Help*, which is available by selecting **Help»VI, Function, & How-To Help** from LabVIEW

Getting Started with the LabVIEW Real-Time Module

To set up and use the NI PXI-7831R with the LabVIEW FPGA Module and the LabVIEW Real-Time Module, you need the following items:

- ❑ NI PXI-7831R
- ❑ The following software packages:
  - LabVIEW version 7.0 or later
  - NI Device Drivers CD

  - LabVIEW FPGA Module version 7.0 or later (required only if you are developing custom FPGA VIs for the RIO device)
  - LabVIEW Real-Time Module version 7.0 or later

- ❑ PXI/CompactPCI chassis and real-time PXI controller
- ❑ One of the following host computers, depending upon your application, running Windows 2000/XP:
  - PC
  - Laptop computer
  - PXI/CompactPCI embedded controller
- ❑ At least one cable and terminal block for connecting signals to the NI PXI-7831R
- ❑ Category 5 (Cat-5) crossover cable (if the real-time PXI system is not configured on a network); you need a regular network cable if you are configured on a network
- ❑ The following documents are included on the NI Device Drivers CD and are also available at `ni.com/manuals` (optional):
  - *LabVIEW FPGA Module Release Notes*
  - *LabVIEW FPGA Module User Manual*
  - *LabVIEW Real-Time Module User Manual*
  - *NI PXI-7831R User Manual*
- ❑ The *LabVIEW Help*, which is available by selecting **Help»VI, Function, & How-To Help** from LabVIEW

Installing the Software

The following software installation instructions describe how to install the NI Device Drivers software for use without the LabVIEW FPGA Module. If you are using the FPGA Module, refer to the *LabVIEW FPGA Module Release Notes* document for software installation instructions.

Note NI recommends that you install LabVIEW 7.0 or later before installing the NI Device Drivers software. For LabVIEW installation instructions, refer to the *LabVIEW Release Notes* document.

Complete the following steps to install the necessary components from the NI Device Drivers CD.

1. Log onto the computer as an administrator or as a user with administrative privileges.
2. Insert the NI Device Drivers CD (for LabVIEW 7.0 or later) into the CD drive.
3. Run `setup.exe` from the NI Device Drivers CD.
4. Follow the instructions that appear on the screen until you reach the Feature Tree window.
5. In the Feature Tree window, you can select the components to install. You must install all the components for NI-VISA, NI-RIO, and NI Measurement & Automation Explorer. You also can install other components.
6. Complete the driver installation and remove the NI Device Drivers CD.
7. You must shut down your computer before installing any hardware.

Unpacking

The RIO device is shipped in an antistatic package to prevent electrostatic damage to the device. Electrostatic discharge (ESD) can damage several components on the device.

Caution *Never* touch the exposed pins of connectors.

To avoid such damage when handling the devices, take the following precautions:

- Ground yourself using a grounding strap or by holding a grounded object.
- Touch the antistatic package to a metal part of the computer chassis before removing the devices from the package.

Remove the devices from the package and inspect the devices for loose components or any other sign of damage. Notify NI if the devices appear damaged in any way. Do *not* install damaged devices into the computer.

Store the NI PXI-7831R in the antistatic envelope when not in use.

Installing the Hardware

You can install the NI PXI-7831R in any available PXI slot in the PXI/CompactPCI chassis.

The following are general installation instructions, so consult the computer user manual or technical reference manual for specific instructions and warnings.

Note You must install the software before installing the hardware. For software installation instructions, refer to the *Installing the Software* section.

1. Power off and unplug the PXI/CompactPCI chassis.
2. Choose an unused PXI/CompactPCI peripheral slot.
3. Make sure there are no lighted LEDs on the chassis. If any are lit, wait until they go out before continuing the installation.
4. Remove the filler panel for the peripheral slot that you chose.
5. Ground yourself using a grounding strap or by holding a grounded object. Follow the electrostatic discharge protection precautions described in the *Unpacking* section.
6. Insert the NI PXI-7831R into the slot. Use the injector/ejector handle to fully inject the NI PXI-7831R into place.
7. Screw the front panel of the NI PXI-7831R to the front panel mounting rails of the PXI/CompactPCI chassis.
8. Visually verify the installation by making sure the NI PXI-7831R is not touching other devices or components and is fully inserted into the slot.
9. Plug in and power on the PXI/CompactPCI chassis.

The NI PXI-7831R is now installed.

Connecting Signals

The NI PXI-7831R has two DIO connectors with 40 DIO lines per DIO connector, and one MIO connector with eight AI lines, eight AO lines, and 16 DIO lines.

Figure 1 shows the I/O connector locations for the NI PXI-7831R. The I/O connectors are numbered starting at zero. The text in parentheses indicates whether each I/O connector is an MIO connector or a DIO connector.

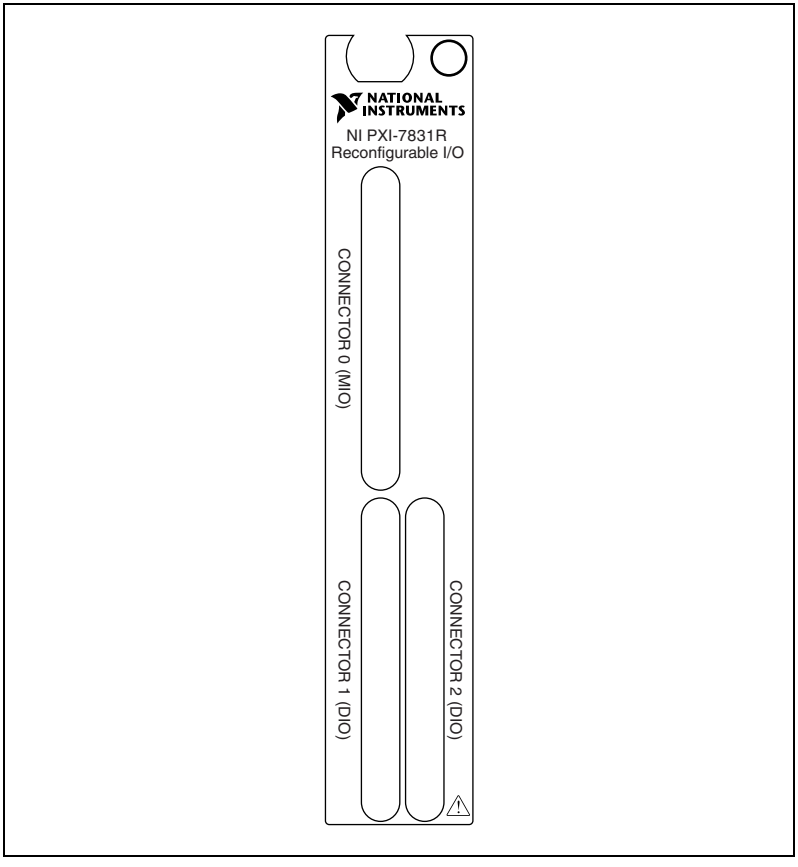

Figure 1. NI PXI-7831R Connector Locations

Figure 2 shows the I/O connector pin assignments for the I/O connectors on the NI PXI-7831R. The DIO connector pin assignment applies to connectors <1..2> on the NI PXI-7831R. The MIO connector pin assignment applies to connector 0 on the NI PXI-7831R.

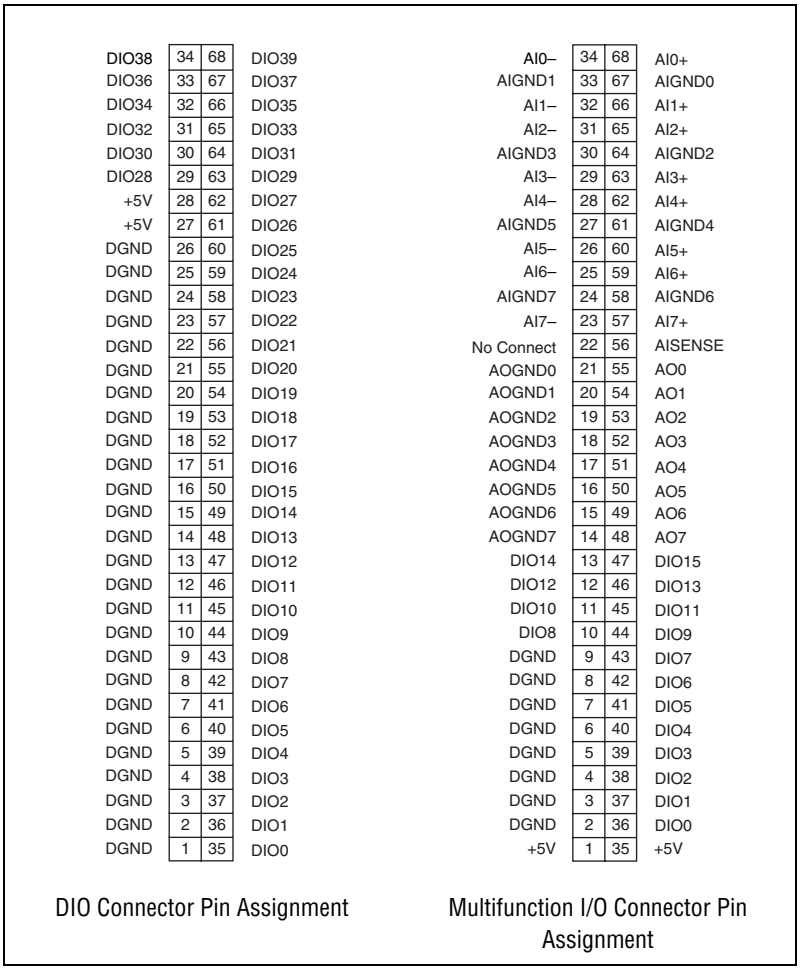

Figure 2. NI PXI-7831R I/O Connector Pin Assignments

Connecting I/O Signals

To access the signals on the I/O connectors, you must use at least one cable and one signal accessory. If you are connecting to a terminal block such as an SCB-68, you should use the SH68-C68-S cable. Plug the small VHDCI connector end of the SH68-C68-S shielded cable into the appropriate I/O connector on the NI PXI-7831R, and connect the other end of the SH68-C68-S cable into the terminal block.

NI also provides cables for connecting the NI PXI-7831R directly to 5B and SSR analog and digital signal conditioning backplanes. The NSC68-262650 plugs directly into the MIO connector on the PXI-7831R and routes the signals to connectors that can be attached directly to 5B backplanes for the analog signals and SSR backplanes for the digital signals. The NSC68-5050 plugs directly into the DIO connectors on the PXI-7831R and routes the signals to connectors that can be attached directly to SSR backplanes.

Refer to the *NI PXI-7831R User Manual* for more information on connecting I/O signals.

Caution Connections that exceed any of the maximum ratings of input or output signals on the NI PXI-7831R can damage the NI PXI-7831R and the computer. Refer to the *NI PXI-7831R User Manual* for the maximum input ratings for each signal. NI is *not* liable for any damage resulting from such signal connections.

Getting Started Example

The following instructions guide you through running a simple example on the PXI-7831R. Running this example confirms that you have installed your software and hardware correctly, and it provides a brief introduction to using LabVIEW to program the PXI-7831R. This example uses the default FPGA VI, which is installed along with the NI-RIO software, and which is also programmed into the flash memory on the PXI-7831R before the device is shipped from the factory.

Note The following example can be run by all users, even if you are not using the FPGA Module. However, if you are using the FPGA Module, you might wish to consult the *LabVIEW FPGA Module Release Notes* for more information on getting started with the FPGA Module.

Complete the following steps to open and run the example program.

1. Launch LabVIEW.
2. (Real-Time Module users only) Select the networked Real-Time PXI system from the **Execution Target** list in the **LabVIEW** dialog box to target LabVIEW to the Real-Time system containing the PXI-7831R.
3. Click the **Open** arrow and select **Examples** from the pull-down menu in the **LabVIEW** dialog box. The **Example Finder** window appears.
4. Select **Directory Structure** on the **Browse** tab to browse the examples by directory structure.

5. Navigate to `LabVIEW 7.0\examples\FPGA\Applets \Default 7831\` in the listbox. Notice that a brief description of the example appears in the **Example** description field of the **Example Finder** dialog box.
6. Double-click `1 RIO Board (Host).vi` in the listbox to launch the 1 RIO Board (Host) VI example.
7. Click the **Run** button.
8. If you are running a Real-Time system, a **Downloading** dialog box appears to display the progress of the example VI as it downloads to the Real-Time controller.

   Some users might see a **Downloading** dialog box briefly appear to display the progress of the FPGA VI as it downloads to the FPGA on the NI PXI-7831R. This dialog box only appears if the FPGA VI is not already downloaded to the FPGA.
9. The example should now be running and returning data from the PXI-7831R. The example is acquiring data from AI channel 1 and displaying that data on the indicator labeled **AI 1**. The data is displayed as a signed 16-bit number that varies from –32768 to 32767 as the voltage on AI channel 1 varies from –10.0 V to +10.0 V. If you have a signal source available, connect it to AI channel 1 (connect AI1+ to the signal, and AI1– to ground) and confirm that the data returned corresponds to the voltage input. If you do not have a signal source available, connect AI1+ and AI1– both to ground and confirm that the number returned by the **AI 1** indicator is close to 0.
10. The **Loop Period** control determines the analog input sampling rate. This period is specified in cycles of the PXI-7831R onboard 40 MHz oscillator. So, specifying a **Loop Period** of 40,000,000 results in the analog input being sampled once every second. Vary the **Loop Period** and watch how it affects the update rate of the AI 1 indicator. If you set the **Loop Period** too low, the computer cannot read data from the AI channel as fast as it is sampled. In this case, the **Overrun** indicator lights up indicating that you are trying to run the example too fast.
11. Click the **STOP** button to stop the VI. If you encountered any problems running the VI, refer back to the software and hardware installation instructions in this document and verify that everything is installed correctly.
12. Select **Window»Show Block Diagram** from the 1 RIO Board (Host) VI toolbar to view the block diagram. This example actually consists of two separate VIs—the 1 RIO Board (Host) VI, which runs on the Windows or LabVIEW Real-Time machine, and a second VI, Default 7831R (FPGA) VI, which runs on the PXI-7831R FPGA. As you look at the 1 RIO Board (Host) VI block diagram, the left-most terminal on the block diagram is an Open FPGA VI Reference function that downloads the Default 7831R (FPGA) VI to the FPGA on the

PXI-7831R. A reference to this VI running on the FPGA is passed to the subsequent nodes on the block diagram. These nodes can interact with the VI running on the FPGA by reading and writing its indicators and controls to control the execution of the FPGA VI. After the While Loop on the 1 RIO Board (Host) VI block diagram finishes execution, the Close FPGA VI Reference function stops the execution of the VI on the FPGA. Refer to the context help for the 1 RIO Board (Host) VI for more information about the operation of this VI.

13. The Default 7831R (FPGA) VI that runs on the PXI-7831R FPGA provides much more functionality than the 1 RIO Board (Host) VI actually uses. The Default 7831R (FPGA) VI provides a timed loop synchronizing all of the I/O available on the PXI-7831R (8 AI, 8 AO, and 96 DIO). The Default 7831R (FPGA) VI offers a variety of different timing modes that allow it to run off of its own internal loop timer, or to synchronize its operation with other devices in the system. To view the Default 7831R (FPGA) VI, double-click the Open FPGA VI Reference function on the 1 RIO Board (Host) VI block diagram using the selection tool. This opens the front panel for the Default 7831R (FPGA) VI. Refer to the context help for the Default 7831R (FPGA) VI for more information about this VI. You can also look at the block diagram code to see how this VI operates.
14. Close the 1 RIO Board (Host) VI and the Default 7831R (FPGA) VI, and exit LabVIEW when you are done. For more information using FPGA VIs like the Default 7831R (FPGA) VI, refer to the *LabVIEW FPGA Module User Manual*.

Where To Go From Here

Refer to the following documentation for information about the LabVIEW FPGA Module, RIO hardware, and VIs needed for your application.

- *LabVIEW FPGA Module Release Notes*—This document describes the software installation and other known software issues.
- *LabVIEW FPGA Module User Manual*—This manual describes the LabVIEW FPGA Module software and techniques for building applications in LabVIEW with the FPGA Module. Even if you do not have the FPGA module installed, NI recommends that you read *Chapter 4, Communicating with FPGA VIs*.
- *NI PXI-7831R User Manual*—This manual describes the electrical and mechanical aspects of the NI PXI-7831R device and contains information concerning its operation and programming.
- *LabVIEW Help*—This help describes the VIs and function reference information.