Getting Results with the NI PXI-6585R

This document explains how to install and configure the National Instruments PXI-6585R, comprised of an NI FlexRIO FPGA module (NI PXI-79*xx*R) and an NI 6585 FlexRIO adapter module. This document also contains tutorial sections that demonstrate how to generate and acquire samples using a LabVIEW FPGA example VI and how to create and run your own LabVIEW project with the NI PXI-6585R.

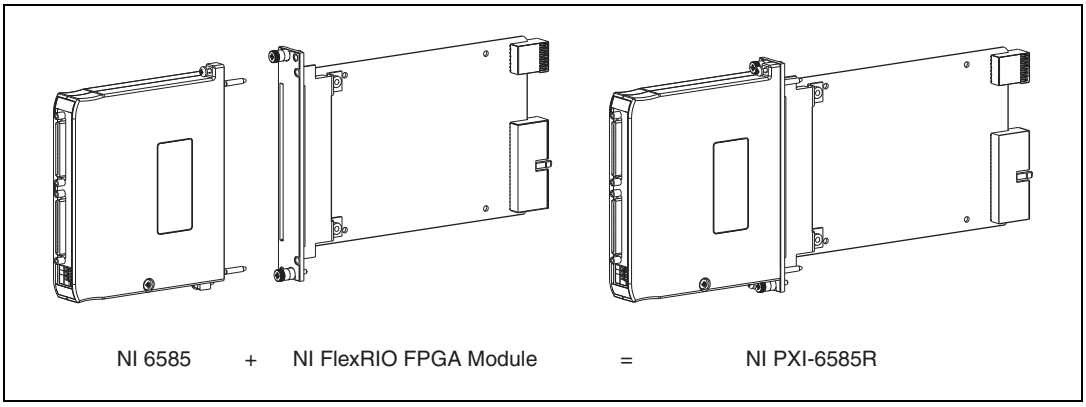


Figure 1. NI PXI-6585R

Required Components

The following items are necessary to set up and use the NI PXI-6585R:

- ❑ The NI PXI-6585R kit containing the following:
  - NI PXI-79*xx*R FlexRIO FPGA module
  - NI 6585 FlexRIO adapter module
- ❑ The following software packages:
  - LabVIEW
  - LabVIEW FPGA Module
  - (Optional) LabVIEW Real-Time Module
  - NI-RIO device drivers
  - NI FlexRIO Adapter Module Support

  Refer to *Step 1. Install Application Software and Driver*, for information about NI FlexRIO software support.
- ❑ PXI/CompactPCI chassis with PXI/CompactPCI embedded controller, or MXI kit and a PC, running Windows Vista/2000 or Windows XP Pro x32 Service Pack 1 or 2.
- ❑ SHC68-C68-D3 cable (NI part number 188143-01) for connecting signals to the NI PXI-6585R.

Step 1. Install Application Software and Driver

Before installing the NI PXI-6585R, you must install the application software and device driver. Visit `ni.com/info` and enter `rdsoftwareversion` to determine which minimum versions of software you need for the device you are using.

Refer to the *LabVIEW Release Notes* for installation instructions for LabVIEW and system requirements for the LabVIEW software. Refer to the *LabVIEW Upgrade Notes* for additional information about upgrading to the most recent version of LabVIEW for Windows.

Refer to the *LabVIEW FPGA Module Release and Upgrade Notes* for installation instructions and information about getting started with the LabVIEW FPGA Module.

Refer to the *LabVIEW Real-Time Module Release and Upgrade Notes* for system requirements, installation instructions, and additional information about using the LabVIEW Real-Time Module.

Refer to the *NI-RIO Readme* on NI-RIO installation media for system requirements and installation instructions for the NI-RIO driver.

Refer to the *NI FlexRIO Adapter Module Support Readme* on NI FlexRIO Adapter Module Support installation media for system requirements and installation instructions.

The LabVIEW documents are available from `ni.com/manuals`. In LabVIEW, you can also view the LabVIEW Manuals directory that contains these documents by selecting **Start»All Programs» National Instruments»LabVIEW»LabVIEW Manuals**.

Step 2. Install the NI PXI-6585R

This section describes how to unpack and install the NI FlexRIO FPGA module and the NI 6585.

Note You *must* install LabVIEW, LabVIEW FPGA Module, NI-RIO, and NI FlexRIO Adapter Module Support before installing the NI PXI-6585R.

Unpacking

The NI FlexRIO FPGA module and the NI 6585 are shipped in antistatic packages to prevent electrostatic discharge from damaging device components. To prevent such damage when handling the device, take the following precautions:

- Ground yourself using a grounding strap or by holding a grounded object, such as your computer chassis.
- Touch the antistatic package to a metal part of the computer chassis before removing the device from the package.

Caution *Never* touch the exposed pins of connectors.

Remove the device from the package and inspect the devices for loose components or any other sign of damage. Notify NI if the device appears damaged in any way. Do *not* install a damaged device into the chassis.

Store the NI FlexRIO FPGA module and NI 6585 in the antistatic envelopes when not in use.

Installing the NI FlexRIO FPGA Module

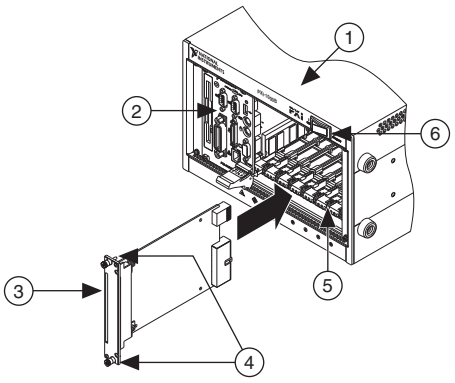
You can install the NI FlexRIO FPGA module in any available PXI, PXI-1, or PXI hybrid slot in the PXI or CompactPCI chassis.

Note You must install the software before installing the hardware. For software installation information, refer to *Step 1. Install Application Software and Driver*.

1. Power off and unplug the PXI chassis.

Caution Refer to the *Read Me First: Safety and Electromagnetic Compatibility* document packaged with your PXI chassis or device before removing equipment covers or connecting or disconnecting any signal wires.

2. Remove the filler panel of an unused PXI, PXI-1, or PXI hybrid slot on the PXI chassis.
3. Touch any metal part of the chassis to discharge any static electricity.
4. Insert the NI FlexRIO FPGA module into the PXI slot, as shown in Figure 2.



1	PXI Chassis	4	Front-Panel Mounting Screws
2	PXI System Controller	5	Module Guides
3	NI FlexRIO FPGA Module	6	Power Switch

Figure 2. Installing an NI FlexRIO FPGA Module in a PXI Chassis

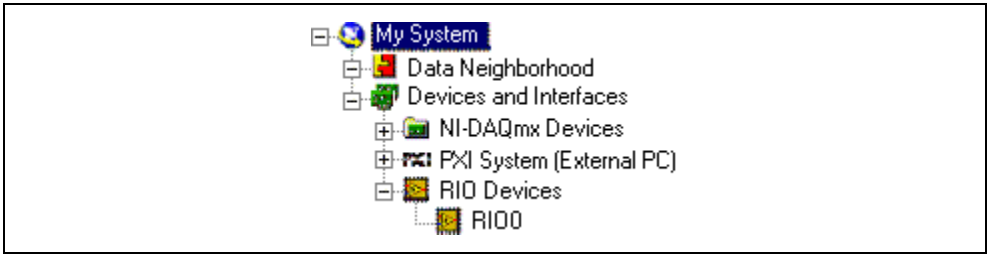
5. Secure the device front panel to the chassis front panel mounting rail using the front-panel mounting screws.
6. Plug in and power on the PXI chassis.

Windows recognizes any newly installed device the first time the computer reboots after hardware is installed. On some Windows systems, the Found New Hardware wizard opens with a dialog box for every NI device installed. **Install the software automatically (Recommended)** is selected by default. Click **Next** or **Yes** to install the software for the device.

Confirming That the Device Is Recognized

To confirm that the NI FlexRIO FPGA module is recognized, complete the following steps.

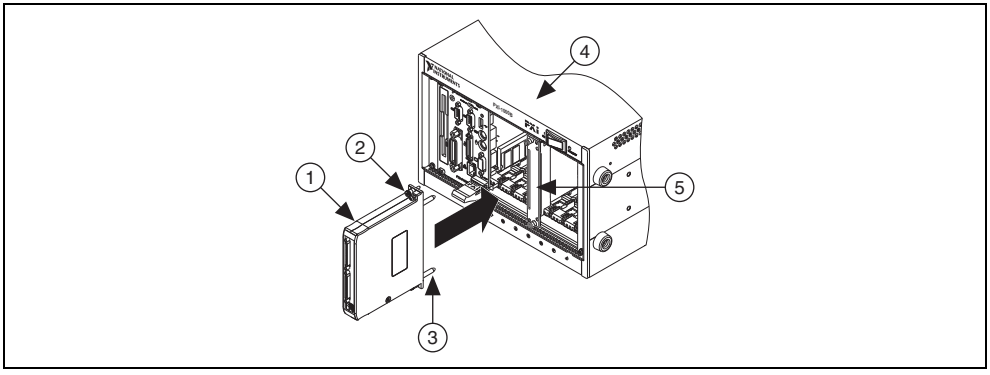
1. Select **Start»All Programs»National Instruments»Measurement & Automation** to open Measurement & Automation Explorer (MAX).
2. Expand **Devices and Interfaces**.
3. Verify that the device appears under **Devices and Interfaces»RIO Devices**.



Installing the NI 6585 Adapter Module

Complete the following steps to connect the NI 6585 FlexRIO adapter module to the NI FlexRIO FPGA module.

1. Gently insert the guide pins and the high-density card edge of the NI 6585 into the corresponding connectors of the NI FlexRIO FPGA module. The connection may be tight, but do *not* force the adapter module into place.



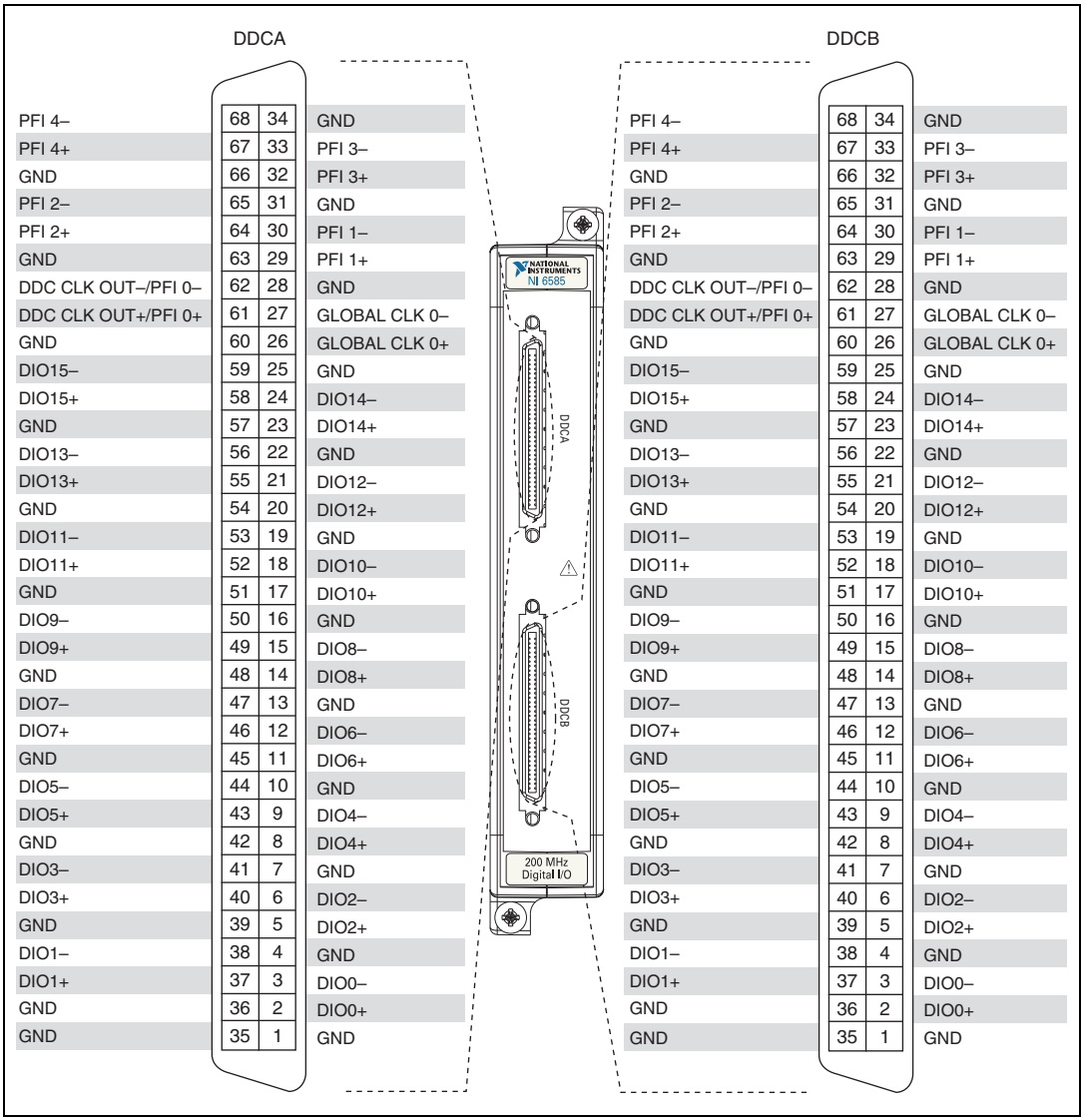
1	NI 6585 FlexRIO Adapter Module	4	PXI Chassis
2	Captive Screw	5	NI FlexRIO FPGA Module
3	Guide Pin		

Figure 3. Installing the NI 6585

2. Tighten the captive screws on the NI 6585 to secure it to the NI FlexRIO FPGA module.

Step 3. Connect Signals

Figure 4 shows the digital data connector (DDC) pin assignments for the NI 6585. Refer to the *NI 6585 Specifications* for signal information.



DDCA				DDCB			
PFI 4–	68	34	GND	PFI 4–	68	34	GND
PFI 4+	67	33	PFI 3–	PFI 4+	67	33	PFI 3–
GND	66	32	PFI 3+	GND	66	32	PFI 3+
PFI 2–	65	31	GND	PFI 2–	65	31	GND
PFI 2+	64	30	PFI 1–	PFI 2+	64	30	PFI 1–
GND	63	29	PFI 1+	GND	63	29	PFI 1+
DDC CLK OUT–/PFI 0–	62	28	GND	DDC CLK OUT–/PFI 0–	62	28	GND
DDC CLK OUT+/PFI 0+	61	27	GLOBAL CLK 0–	DDC CLK OUT+/PFI 0+	61	27	GLOBAL CLK 0–
GND	60	26	GLOBAL CLK 0+	GND	60	26	GLOBAL CLK 0+
DIO15–	59	25	GND	DIO15–	59	25	GND
DIO15+	58	24	DIO14–	DIO15+	58	24	DIO14–
GND	57	23	DIO14+	GND	57	23	DIO14+
DIO13–	56	22	GND	DIO13–	56	22	GND
DIO13+	55	21	DIO12–	DIO13+	55	21	DIO12–
GND	54	20	DIO12+	GND	54	20	DIO12+
DIO11–	53	19	GND	DIO11–	53	19	GND
DIO11+	52	18	DIO10–	DIO11+	52	18	DIO10–
GND	51	17	DIO10+	GND	51	17	DIO10+
DIO9–	50	16	GND	DIO9–	50	16	GND
DIO9+	49	15	DIO8–	DIO9+	49	15	DIO8–
GND	48	14	DIO8+	GND	48	14	DIO8+
DIO7–	47	13	GND	DIO7–	47	13	GND
DIO7+	46	12	DIO6–	DIO7+	46	12	DIO6–
GND	45	11	DIO6+	GND	45	11	DIO6+
DIO5–	44	10	GND	DIO5–	44	10	GND
DIO5+	43	9	DIO4–	DIO5+	43	9	DIO4–
GND	42	8	DIO4+	GND	42	8	DIO4+
DIO3–	41	7	GND	DIO3–	41	7	GND
DIO3+	40	6	DIO2–	DIO3+	40	6	DIO2–
GND	39	5	DIO2+	GND	39	5	DIO2+
DIO1–	38	4	GND	DIO1–	38	4	GND
DIO1+	37	3	DIO0–	DIO1+	37	3	DIO0–
GND	36	2	DIO0+	GND	36	2	DIO0+
GND	35	1	GND	GND	35	1	GND

Figure 4. NI 6585 Connector Pin Assignments

Caution Connections that exceed any of the maximum ratings of input or output signals on the NI PXI-6585R can damage the device and the chassis. NI is *not* liable for any damage resulting from such signal connections. For the maximum input and output ratings for each signal, refer to the *NI 6585 Specifications*, available from `ni.com/manuals`.

For information about connecting I/O signals, refer to the *NI 6585 Specifications*, available from `ni.com/manuals`.

Step 4. Use Your NI PXI-6585R with a LabVIEW FPGA Example VI

The NI FlexRIO Adapter Module Support installation includes a variety of example projects to help get you started. This section demonstrates how to use an existing LabVIEW FPGA example project to generate and acquire samples with the NI PXI-6585R. This example requires an SHC68-C68-D3 cable.

Note Examples available for your device are dependent on the device-specific minimum software requirements. For more information about software requirements for your device, refer to *Step 1. Install Application Software and Driver*.

Each NI PXI-6585R example project includes:

- A LabVIEW FPGA VI that can be compiled and run embedded in FPGA hardware
- A Host VI that runs in LabVIEW for Windows and interacts with the LabVIEW FPGA VI

Note In software, NI FlexRIO adapter modules are referred to as *IO Modules*.

Complete the following steps to run an example that generates a waveform from DDCB and acquires the waveform on DDCA.

1. Connect one end of a SHC68-C68-D3 cable to DDCA on the NI PXI-6585R, and the other end to DDCB.
2. Launch LabVIEW.
3. In the **Getting Started** window, click **Find Examples** to display the NI Example Finder.
4. In the **NI Example Finder** window, select **Hardware Input and Output»FlexRIO**. This directory holds several example projects designed to help you get started using the NI PXI-6585R.
5. Select **IO Modules,** then **NI 6585 Finite Acquisition and Generation - Simple.lvproj**.
6. In the **Project Explorer** window, open **NI 6585 Finite Acquisition and Generation Simple (Host).vi** under **My Computer**. The host VI opens. The VI uses the NI PXI-7952R as the FPGA target. If you are not using an NI PXI-7952R, complete the following steps to change the FPGA target.

Note All example projects are configured for RIO0. If your device is not RIO0, you must update the target device name by right-clicking your device in the **Project Explorer** window, selecting **Properties**, and entering the correct target device name in the **Resource** box. You can find your target device name in MAX by following the steps listed in the *Confirming That the Device Is Recognized* section.

   a. Select **Window»Show Block Diagram** to open the VI block diagram.
   b. On the block diagram, right-click the Open FPGA icon (PXI-7952R) and select **Configure Open FPGA VI Reference**.
   c. In the **Configure Open FPGA VI Reference** window, click the **Browse Project** button in the Open VI section.
   d. In the **Select VI** window that opens, expand the tree view for your device, select the VI under your device and click **OK**.
   e. Click **OK** in the **Configure Open FPGA VI Reference** window.
   f. Save the VI.

7. On the front panel, enter appropriate values in the **Num Samples**, **Generation Constant**, and **Timeout (ms)** boxes and select a generation mode in the **Generation Mode** box.

8. Click the **Run** button to run the VI. The NI PXI-6585R generates samples from the data channels on DDCB and acquires those samples on the DDCA channels. If the samples in the DDCA Port 0 - Acquired pane are identical to those in the DDCB Port 0 - Generated pane, the Verified? LED lights.

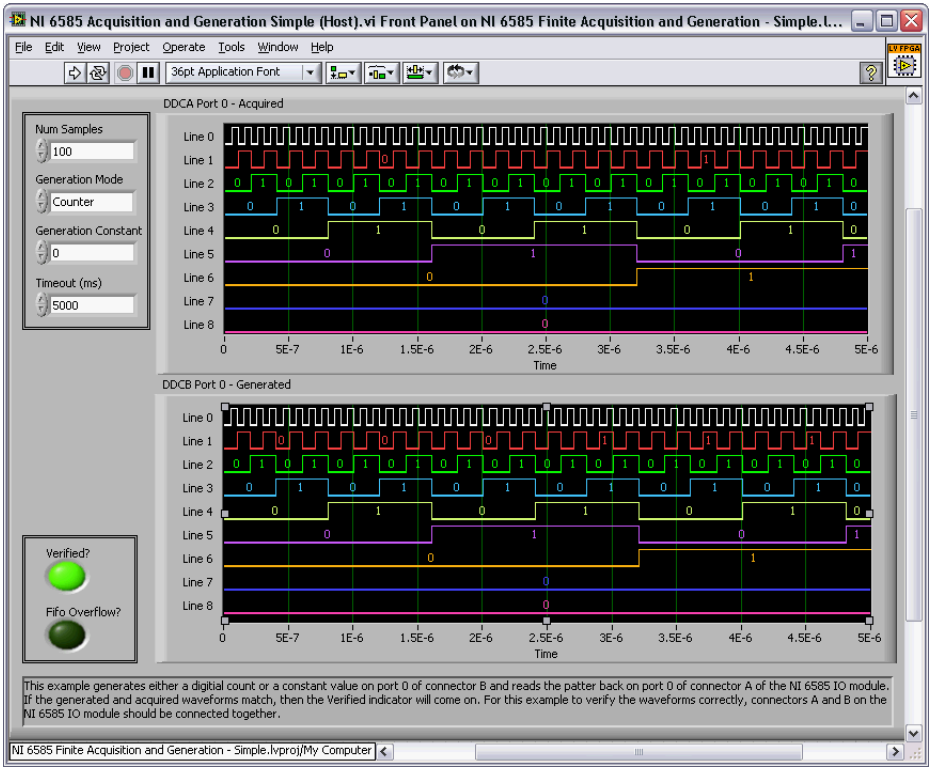


Figure 5. NI 6585 Finite Acquisition and Generation Simple (Host) VI Front Panel

If the samples do not match, check your cable connections and verify that the NI 6585 is securely connected to the NI FlexRIO FPGA module.

9. Close the VI.

Step 5. Create a LabVIEW Project and Run a VI on an FPGA Target

This section demonstrates how to create a LabVIEW project, FPGA VI, and host VI that writes a value to the NI PXI-6585R and reads that value back. This exercise also demonstrates how to compile the FPGA VI on to your target and run a VI on the host machine.

Note Disconnect all signals from the NI PXI-6585R connectors before running this VI.

Creating a Project

1. Launch LabVIEW.
2. In the **Getting Started** window, click **Empty Project**. The new project opens in the **Project Explorer** window.
3. Save the project as `Data RW.lvproj`.

Creating an FPGA Target VI

1. In the **Project Explorer** window, right-click **My Computer** and select **New»Targets and Devices**.
2. In the **Add Targets and Devices on My Computer** window, select the **Existing Target or Device** radio button and expand the FPGA Target. The target is discovered.
3. Select your device and click **OK**. The target and target properties are loaded into the project tree.
4. In the **Project Explorer** window, right-click the FPGA target and select **New»VI**. A blank VI opens. Select the block diagram window.
5. In the **Project Explorer** window, expand **FPGA Target (RIO*x*, PXI-79*xx*R)**.
6. Right-click **IO Module** and select **Properties**. In the General category, you can see the available CLIP for the NI 6585 in the Component Level IP pane. If the category information is greyed-out, put a check mark in the Enable IO Module checkbox.

Note For more information about CLIP (component-level IP) for the NI 6585, refer to the *NI 6585 Component-Level Intellectual Property* section.

7. Select **NI 6585 Basic Connector** to use the connector-based CLIP. Click **OK**.
8. In the **Project Explorer** window, expand the **IO Module (NI 6585 : NI 6585 Basic Connector)** tree view.
9. Select **DDCA_Data_Rd**, **DDCA_Data_Wr**, and **DDCA_Data_WE** and drag them onto the block diagram.
10. Add a While Loop around the three Data nodes, as shown in Figure 6.
11. Wire a numeric constant to the input of the IO Module\DDCA_Data_WE node.
12. Wire an indicator from the output of the IO Module\DDCA_Data_Rd node.
13. Wire a control to the write input of the IO Module\DDCA_Data_Wr node.
14. Wire a false constant to the stop condition of the While Loop.

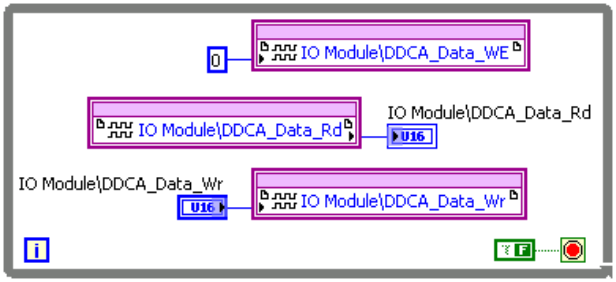


Figure 6. Data RW (FPGA).vi Block Diagram

Tip Click the **Clean Up Diagram** button on the toolbar to tidy VI block diagrams.

15. Save the VI as `Data RW (FPGA).vi`.
16. Close the VI.
17. In the Project Explorer window under **My Computer**, expand the tree view for your device, right-click **Data RW (FPGA).vi** and select **Compile** to compile the files for your target.

    The **Generating Intermediate Files** window opens and displays the compilation progress. The **LabVIEW PFPGA Compile Server** window opens and runs. The compilation takes several minutes.

18. When the compilation finishes, click the **Stop Server** button.
19. Click **OK** in the **Successful Compile Report** window. Close the VI without saving changes.

Creating a Host VI

1. In the **Project Explorer** window, right-click **My Computer** and select **New»VI**. A blank VI opens. Select the block diagram window.
2. Add the Open FPGA VI Reference (from the FPGA Interface function menu) to the block diagram.
3. Right-click the Open FPGA VI Reference (labeled No Target) and select **Configure Open FPGA VI Reference**.
4. In the **Configure Open FPGA VI Reference** window, click the **VI** button in the Open section.
5. In the **Select VI** window that opens, select **Data RW (FPGA).vi** under your device, and click **OK**.
6. Click **OK** in the **Configure Open FPGA VI Reference** window. The new target name appears under Open FPGA VI Reference in the block diagram.
7. Add a While Loop to the block diagram with a control on the loop condition, as shown in Figure 7.
8. Add the Read/Write Control (from the FPGA Interface function menu) inside the While Loop.
9. Wire the Open FPGA VI Reference FPGA VI Reference Out to the Read/Write Control FPGA VI Reference In.
10. Wire the Open FPGA VI Reference FPGA VI error out to the Read/Write Control error in.
11. Click the **Unselected** node of Read/Write Control and select **IO Module\DDCA_Data_Wr**.
12. Wire a control to the IO Module\DDCA_Data_Wr input.
13. Expand the bottom of the Read/Write Control to expose another node. Click the new node and select **IO Module\DDCA_Data_Rd**.
14. Wire an indicator from the IO Module\DDCA_Data_Rd output.
15. Add the Close FPGA VI Reference (from the FPGA Interface function menu) outside the While Loop.
16. Wire the Read/Write Control FPGA VI Reference Out to the Close FPGA VI Reference FPGA VI Reference In.
17. Wire the Read/Write Control error out to the Close FPGA VI Reference error in.

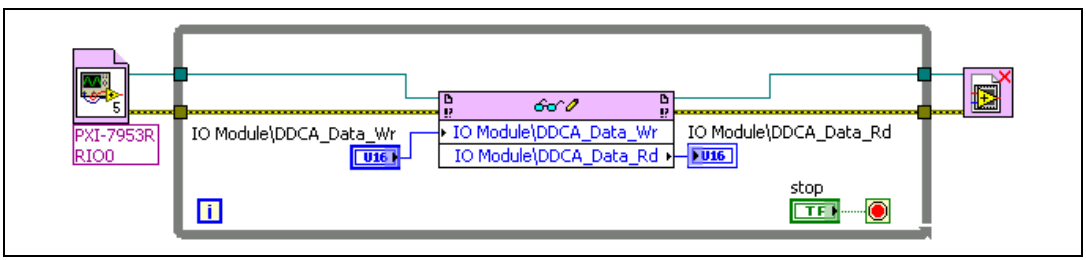


Figure 7. Data RW (Host).vi Block Diagram

18. Save the VI as `Data RW (Host).vi`.

Running the Host VI

1. Open the front panel of `Data RW (Host).vi`.
2. Click the **Run** button to run the VI.

3. Enter a number into the IO Module\DDCA_Data_Wr control to push different values to channel 0. Notice that the IO Module\DDCA_Data_Rd indicator shows the same number. This data value is actively driven onto channel 0 of DDCA on the NI 6585, then is read back using internal connections. Refer to the *NI 6585 Specifications*, available at `ni.com/manuals`, for a block diagram of the channel layout.
4. Click the **STOP** button on the front panel and close the VI.

NI 6585 Component-Level Intellectual Property

The LabVIEW FPGA Module includes a feature for HDL IP integration called component-level intellectual property (CLIP).

NI FlexRIO devices support two types of CLIP: user-defined and socketed. User-defined CLIP allows users to insert HDL IP into an FPGA target, enabling VHDL code to communicate directly with an FPGA VI.

FlexRIO devices also support socketed CLIP, which provides the same IP integration functionality of the user-defined CLIP, while also allowing the CLIP to communicate directly with circuitry external to the FPGA. Adapter module socketed CLIP allows your IP to communicate directly with both the FPGA VI and the external adapter module connector interface.

Figure 8 shows the relationship between an FPGA VI and CLIP.

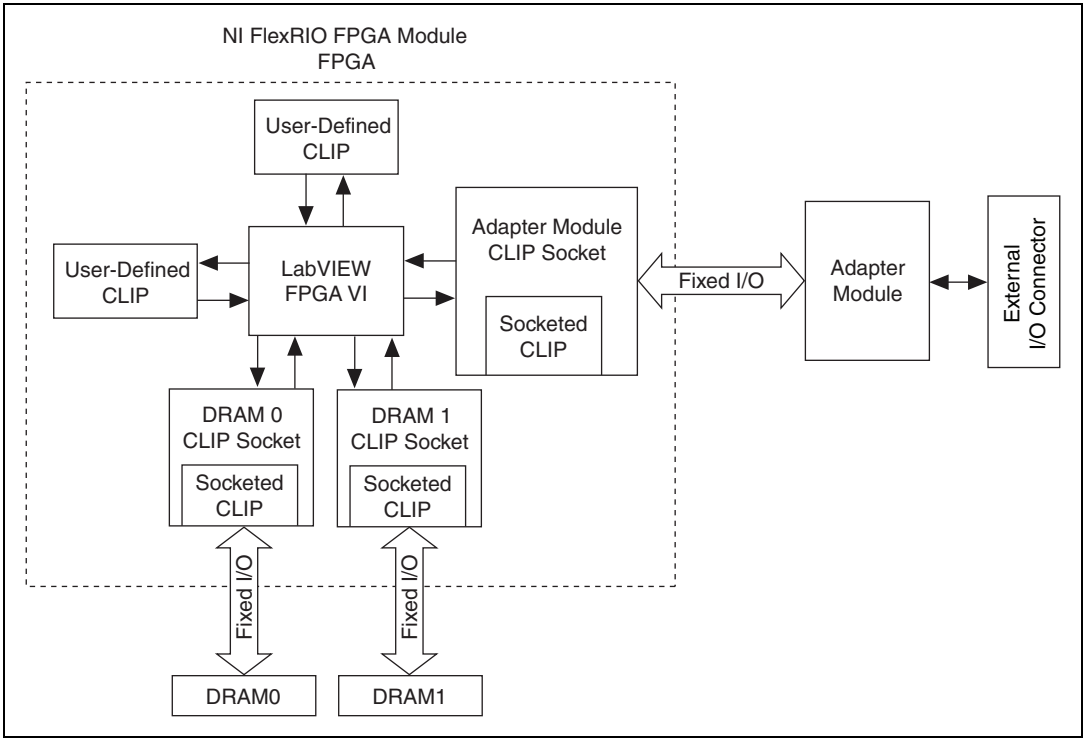


Figure 8. CLIP Relationship

The NI 6585 ships with socketed CLIP that is used to add module I/O to the LabVIEW project. The NI-developed NI 6585 CLIP are as follows:

- **NI 6585 Basic Channel**—Provides read/write access to all low-voltage differential signal (LVDS) channels using a simple channel-based interface. Each I/O line has a write enable signal. This CLIP provides a clock signal for export on each connector. The clock inputs from the NI 6585 are passed to LabVIEW FPGA for use in the FPGA VI. This CLIP also allows for individual clock output inversion.
- **NI 6585 Basic Connector CLIP**—Provides read/write access to all low-voltage differential signal (LVDS) lines on each connector, where the lines are grouped per connector. The individual data lines for each connector are accessed using a U16 data type in LabVIEW FPGA. Each I/O line has a write enable signal. This CLIP also allows for individual clock output inversion.
- **NI 6585 DDR Connector CLIP**—Provides read/write access to all low-voltage differential signal (LVDS) lines on each connector, where the lines are grouped per connector. The individual data lines for each connector are accessed using a U16 data type in LabVIEW FPGA. Data from each edge of the clock is presented as "rising" and "falling." Each I/O line has a write enable signal. This CLIP also allows for individual clock output inversion.

Refer to the *NI FlexRIO Adapter Module Support* topic of the *FlexRIO Help* for information regarding FlexRIO CLIP, configuring the NI 6585 with a socketed CLIP, and a list of available socketed CLIP and provided signals.

Where to Go From Here

The following resources contain information for writing applications and taking measurements with the NI PXI-6585R:

Software Documentation

- LabVIEW FPGA documentation:
  - *Getting Started with LabVIEW FPGA 8.x*—This KnowledgeBase, available at `ni.com/kb`, provides links to the top resources that can be used to assist in getting started with programming in LabVIEW FPGA.
  - *FPGA Module* book in the *LabVIEW Help*—Select **Help»Search the LabVIEW Help** in LabVIEW to view the *LabVIEW Help*. Browse the **FPGA Module** book in the **Contents** tab for information about how to use the FPGA Module to create VIs that run on the NI PXI-6585R.
  - *LabVIEW FPGA Module Release and Upgrade Notes*—Contains information about installing the LabVIEW FPGA Module, describes new features, and provides upgrade information. To access this document, refer to `ni.com/manuals`. In LabVIEW 8.0 or later, you can also view the LabVIEW Manuals directory that contains this document by selecting **Start» All Programs»National Instruments»LabVIEW»LabVIEW Manuals**.
- *National Instruments Example Finder*—LabVIEW contains an extensive library of VIs and example programs for use with FlexRIO devices. To access the NI Example Finder, open LabVIEW and select **Help»Find Examples**, then select **Hardware Input and Output»FlexRIO**.

  You can also access device-specific examples by selecting **Add device** from the **Hardware** pull-down menu in the NI Example Finder window.
- *FlexRIO Help*—This book provides instructions for using LabVIEW and the LabVIEW FPGA Module with NI FlexRIO devices. This document is located in the *FPGA Module* in the *LabVIEW Help*.

Device-Specific Documentation

- NI FlexRIO FPGA module specifications—Lists the specifications of your NI FlexRIO FPGA module. To access, refer to `ni.com/manuals`.
- *NI 6585 Specifications*—Lists the specifications and signal information for the NI 6585. To access this document, refer to `ni.com/manuals`.

Additional Resources

- *LabVIEW FPGA IPNet*—Offers resources for browsing, understanding, and downloading LabVIEW FPGA functions or IP (Intellectual Property). Use this resource to acquire IP that you need for your application, download examples to help learn programming techniques, and explore the depth of IP offered by the LabVIEW FPGA platform. To access the LabVIEW FPGA IPNet, visit `ni.com/ipnet`.
- `ni.com/flexrio`—Contains product information, and helpful links to the FlexRIO forum and the NI community for FlexRIO devices.

Where to Go for Support

The National Instruments Web site is your complete resource for technical support. At `ni.com/support` you have access to everything from troubleshooting and application development self-help resources to email and phone assistance from NI Application Engineers.

National Instruments corporate headquarters is located at 11500 North Mopac Expressway, Austin, Texas, 78759-3504. National Instruments also has offices located around the world to help address your support needs. For telephone support in the United States, create your service request at `ni.com/support` and follow the calling instructions or dial 512 795 8248. For telephone support outside the United States, contact your local branch office:

Australia 1800 300 800, Austria 43 662 457990-0, Belgium 32 (0) 2 757 0020,
Brazil 55 11 3262 3599, Canada 800 433 3488, China 86 21 5050 9800,
Czech Republic 420 224 235 774, Denmark 45 45 76 26 00, Finland 358 (0) 9 725 72511,
France 01 57 66 24 24, Germany 49 89 7413130, India 91 80 41190000, Israel 972 3 6393737,
Italy 39 02 41309277, Japan 0120-527196, Korea 82 02 3451 3400, Lebanon 961 (0) 1 33 28 28,
Malaysia 1800 887710, Mexico 01 800 010 0793, Netherlands 31 (0) 348 433 466,
New Zealand 0800 553 322, Norway 47 (0) 66 90 76 60, Poland 48 22 328 90 10,
Portugal 351 210 311 210, Russia 7 495 783 6851, Singapore 1800 226 5886,
Slovenia 386 3 425 42 00, South Africa 27 0 11 805 8197, Spain 34 91 640 0085,
Sweden 46 (0) 8 587 895 00, Switzerland 41 56 2005151, Taiwan 886 02 2377 2222,
Thailand 662 278 6777, Turkey 90 212 279 3031, United Kingdom 44 (0) 1635 523545

375190A-01 May09