INSTALLATION GUIDE

8-Slot NI PXIe-1062Q Backplane

This guide describes installation requirements for the 8-slot NI PXIe-1062Q backplane.

Contents

NATIONAL INSTRUMENTS

NI PXIe-1062Q Chassis Backplane Overview

This section provides an overview of the backplane features for the NI PXIe-1062Q chassis. Figure 1 shows the backplane.

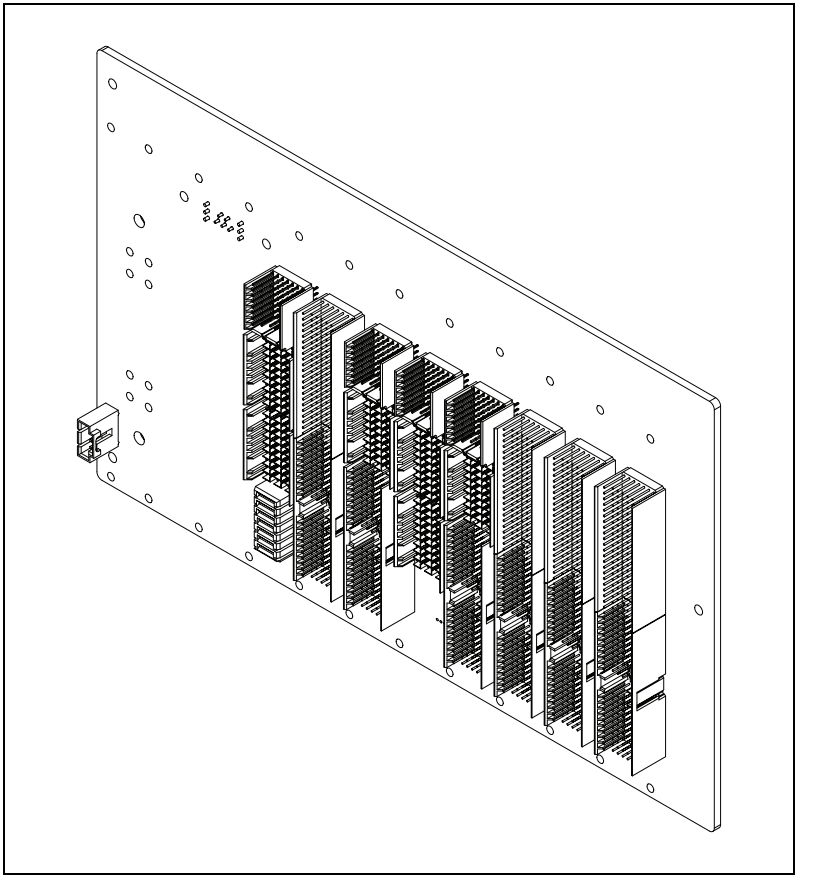


Figure 1. 8-Slot NI PXIe-1062Q Backplane

Interoperability with CompactPCI

With the NI PXIe-1062Q, you can use the following devices in a single PXI Express chassis:

- PXI Express-compatible products
- CompactPCI Express-compatible 4-Link system controller products
- CompactPCI Express-compatible Type-2 peripheral products
- PXI peripheral products
- Standard CompactPCI peripheral products

System Controller Slot

The system controller slot is slot 1 of the chassis and is a 4-Link configuration system slot as defined by the CompactPCI Express and PXI Express specifications. It has three system controller expansion slots for system controller modules that are wider than one slot. These slots allow the system controller to expand to the left to prevent the system controller from using peripheral slots.

The backplane routes a x4 PCI Express link from the system controller slot to slots 3, 4, and 5, and a x1 PCI Express link to a PCI Express to PCI Translation Bridge on the backplane. The PCI Express to PCI Translation Bridge on the backplane provides a 32-bit/33 MHz PCI bus to slots 2, 3, 5, 6, 7, and 8.

The system controller slot also has connectivity to some PXI features, such as PXI_CLK10, PXI Star, PXI Trigger Bus, and PXI Local Bus 6.

The system controller can control the power supply with the PS_ON# signals. A logic low on this line turns on the power supply.

Hybrid Peripheral Slots

The chassis includes two hybrid peripheral slots as defined by the *PXI-5 PXI Express Hardware Specification*: slot 3 and slot 5. A hybrid peripheral slot can accept the following peripheral modules:

- A PXI Express peripheral with a x4 or x1 PCI Express link to the system slot.
- A CompactPCI Express Type-2 peripheral with a x4 or x1 PCI Express link to the system slot.
- A hybrid-compatible PXI peripheral module modified by replacing the J2 connector with an XJ4 connector installed in the upper eight rows of J2. Refer to the *PXI Express Specification* for details. The PXI peripheral communicates through the backplane 32-bit PCI bus.
- A CompactPCI 32-bit peripheral on the backplane 32-bit PCI bus.

The hybrid peripheral slots provide full PXI Express functionality and 32-bit PXI functionality except for PXI Local Bus. The hybrid peripheral slot connects only to PXI Local Bus 6 left and right.

PXI Peripheral Slots

Four PXI peripheral slots accept PXI or CompactPCI peripherals: slot 2, slot 6, slot 7, and slot 8. These slots are on the backplane 32-bit PCI bus. These slots offer full PXI functionality, but have no PXI Express features. The 64-bit PCI signals on the P2 connectors are not connected.

System Timing Slot

The system timing slot is slot 4. The system timing slot accepts the following peripheral modules:

- A PXI Express system timing module with a x4 or x1 PCI Express link to the system slot.
- A PXI Express peripheral with a x4 or x1 PCI Express link to the system slot.
- A CompactPCI Express Type-2 peripheral with a x4 or x1 PCI Express link to the system slot.

The system timing slot has three dedicated differential pairs (PXIe_DSTAR) connected from the TP2 connector to the XP3 connector for each hybrid peripheral slot, as well as routed back to the XP3 connector of the system timing slot, as shown in Figure 2. You can use the PXIe_DSTAR pairs for high-speed triggering, synchronization, and clocking. Refer to the *PXI Express Specification* for details.

The system timing slot also has a single-ended (PXI Star) trigger connected to every slot. Refer to Figure 2 for details.

The system timing slot has a pin (PXI_CLK10_IN) through which a system timing module can source a 10 MHz clock to which the backplane phase-locks. Refer to the *System Reference Clock* section for details.

The system timing slot has a pin (PXIe_SYNC_CTRL) through which a system timing module can control the PXIe_SYNC100 timing. Refer to the *PXI Express Specification* and the *PXIe_SYNC_CTRL* section for details.

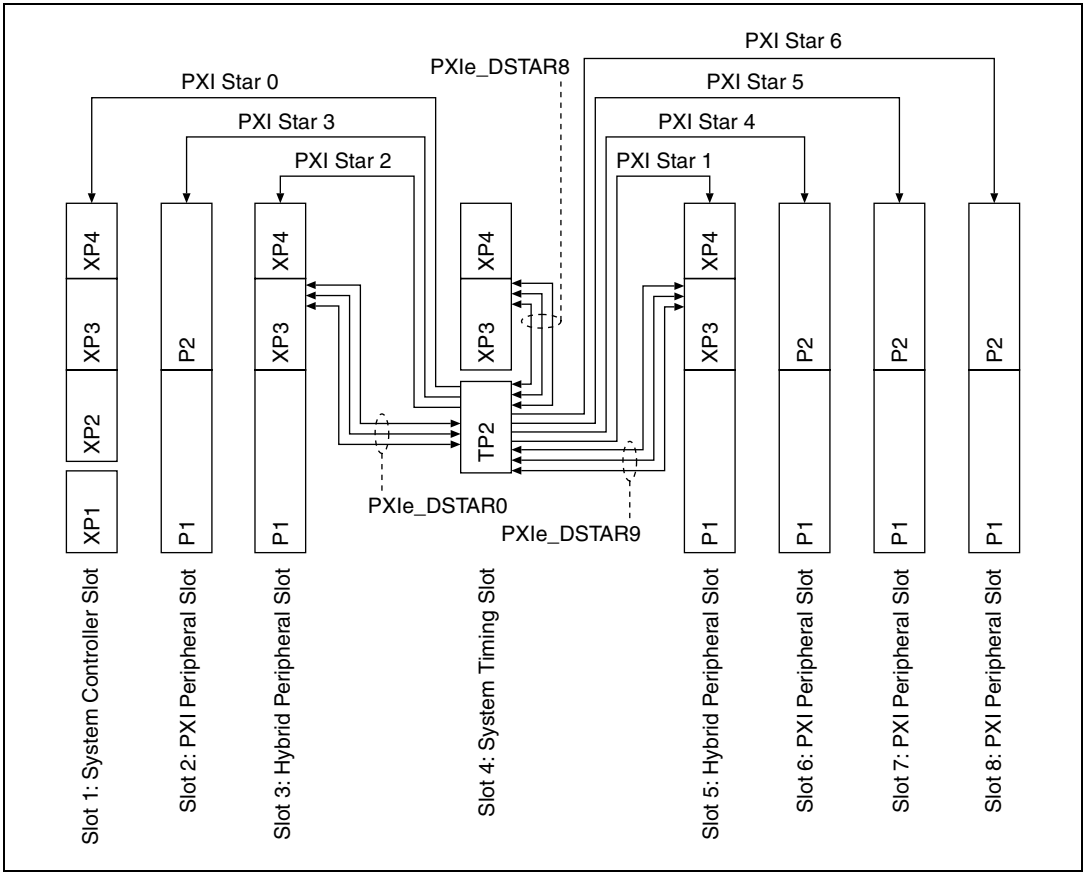


Figure 2. PXIe_DSTAR and PXI Star Connectivity Diagram

PXI Local Bus

The PXI backplane local bus is a daisy-chained bus that connects each peripheral slot with adjacent peripheral slots to the left and right, as shown in Figure 3.

The backplane routes the full 13-line PXI Local Bus between adjacent PXI slots (slots 6, 7, and 8) and PXI Local Bus 6 between all other slots. Refer to Figure 3 for details. The left local bus 6 from slot 1 is not routed anywhere, and the right local bus signals from slot 8 are not routed anywhere.

Local bus signals may range from high-speed TTL signals to analog signals as high as 42 V.

Initialization software uses the configuration information specific to each adjacent peripheral module to evaluate local bus compatibility.

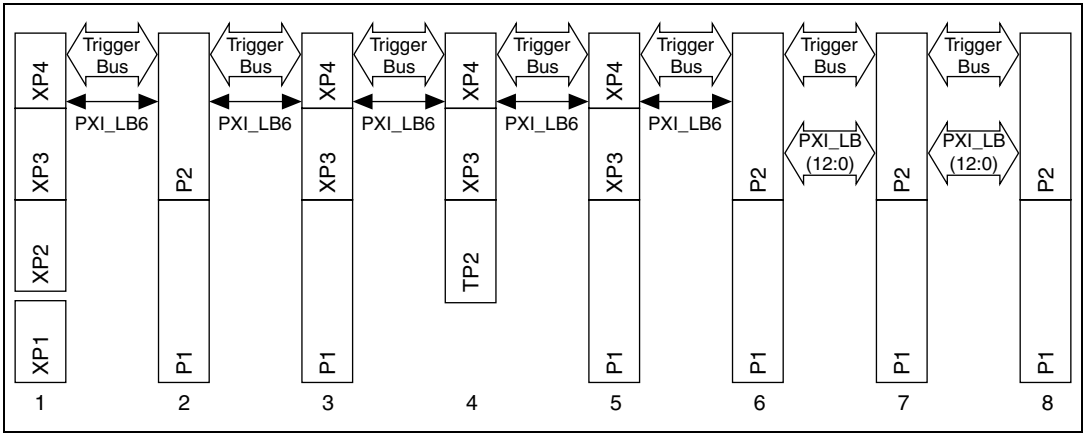


Figure 3. PXI Trigger Bus and Local Bus Connectivity Diagram

PXI Trigger Bus

All slots share eight trigger lines.You can use these trigger lines in a variety of ways. For example, you can use triggers to synchronize the operation of several different PXI peripheral modules. In other applications, one module can control carefully timed sequences of operations performed on other modules in the system. Modules can pass triggers to one another, allowing precisely timed responses to asynchronous external events the system is monitoring or controlling.

System Reference Clock

The NI PXIe-1062Q chassis supplies the PXI 10 MHz system clock signal (PXI_CLK10) independently driven to each peripheral slot, and PXIe_CLK100 and PXIe_SYNC100 to the hybrid slots and system timing slot.

An independent buffer (having a source impedance matched to the backplane and a skew of less than 250 ps between slots) drives PXI_CLK10 to each peripheral slot. Refer to Figure 4 for the PXI_CLK10 routing configuration. You can use this common reference clock signal to synchronize multiple modules in a measurement or control system.

An independent buffer drives PXIe_CLK100 to the hybrid peripheral slots and system timing slot. Refer to Figure 4 for the routing configuration of PXIe_CLK100. These clocks are matched in skew to less than 100 ps. The differential pair must be terminated on the peripheral with LVPECL termination for the buffer to drive PXIe_CLK100, so that when there is no peripheral or a peripheral that does not connect to PXIe_CLK100, no clock is driven on the pair to that slot.

An independent buffer drives PXIe_SYNC100 to the hybrid peripheral slot and system timing slot. Refer to Figure 4 for the routing configuration of PXIe_SYNC100. These clocks are matched in skew to less than 100 ps. The differential pair must be terminated on the peripheral with LVPECL termination for the buffer to drive PXIe_SYNC100, so that when there is no peripheral or a peripheral that does not connect to PXIe_SYNC100, no SYNC100 signal is driven on the pair to that slot.

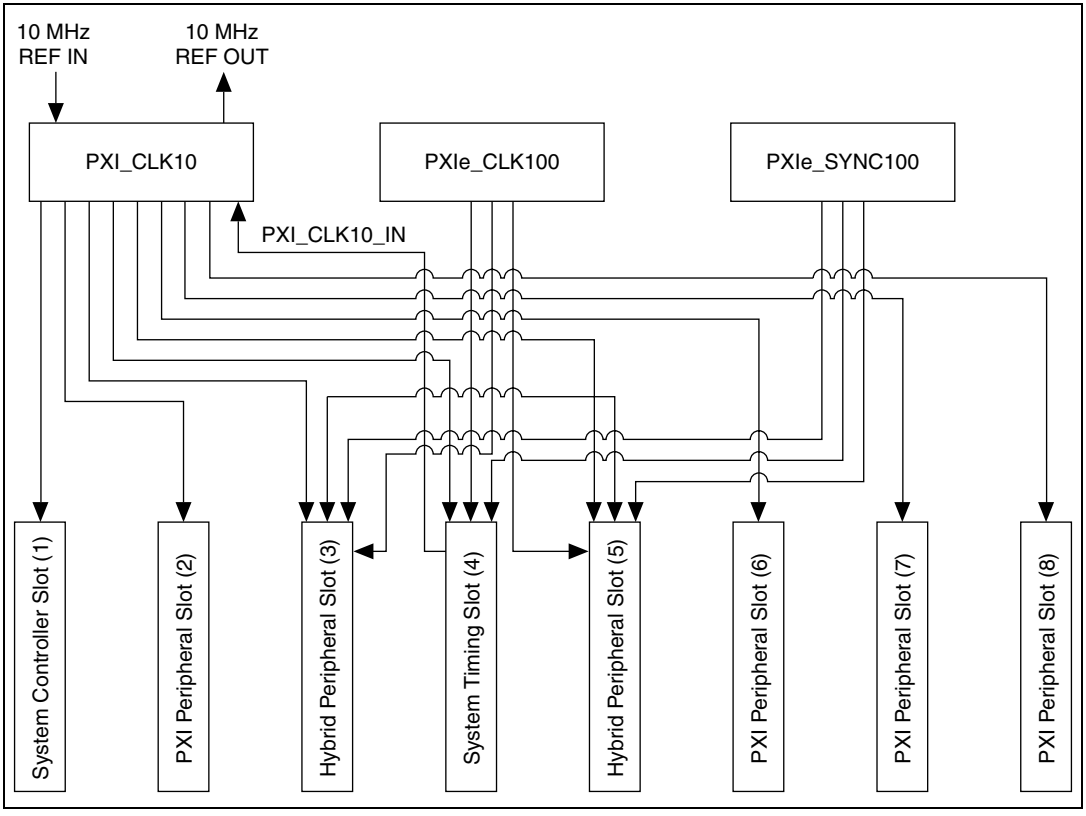


Figure 4. Distribution of PXI_CLK10, PXIe_CLK100, and PXIe_SYNC100

PXI_CLK10, PXIe_CLK100, and PXIe_SYNC100 have the default timing relationship described in Figure 5.

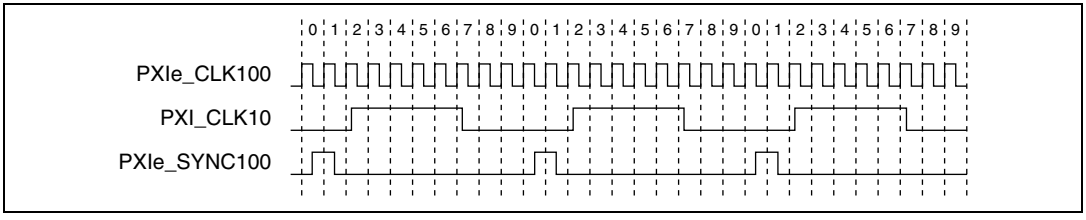


Figure 5. System Reference Clock Default Behavior

To synchronize the system to an external clock, you can drive PXI_CLK10 from an external source through the PXI_CLK10_IN pin on the system timing slot. Refer to Table 10, *XP4 Connector Pinout for the System Timing Slot*, for the pinout. When a 10 MHz clock is detected on this pin, the backplane automatically phase-locks the PXI_CLK10, PXIe_CLK100, and PXIe_SYNC100 signals to this external clock and distributes these signals to the slots. (Refer to Figure 4 for the distribution of PXI_CLK10, PXIe_CLK100, and PXIe_SYNC100.) Refer to *Backplane Specifications* for the specification information for an external clock provided on the PXI_CLK10_IN pin of the system timing slot.

You also can drive a 10 MHz clock on the 10 MHz REF IN pin of connector J27. When a 10 MHz clock is detected on this connector, the backplane automatically phase-locks the PXI_CLK10, PXIe_CLK100, and PXIe_SYNC100 signals to this external clock and distributes these signals to the slots. (Refer to Figure 4 for the distribution of PXI_CLK10, PXIe_CLK100, and PXIe_SYNC100.) Refer to *Backplane Specifications* for the specification information for an external clock provided on the 10 MHz REF IN pin of connector J27.

If the 10 MHz clock is present on both the PXI_CLK10_IN pin of the system timing slot and the 10 MHz REF IN pin of connector J27, the signal on the system timing slot is selected. Refer to Table 1, which explains how the backplane selects the 10 MHz clocks.

Table 1. Backplane External Clock Input Truth Table

System Timing Slot PXI_CLK10_IN	Connector J27 10 MHz REF IN	Backplane PXI_CLK10, PXIe_CLK100, and PXIe_SYNC100
No clock present	No clock present	Backplane generates its own clocks
No clock present	10 MHz clock present	PXI_CLK10, PXIe_CLK100, and PXIe_SYNC100 all phase-locked to connector J27—10 MHz REF IN
10 MHz clock present	No clock present	PXI_CLK10, PXIe_CLK100, and PXIe_SYNC100 all phase-locked to system timing slot—PXI_CLK10_IN
10 MHz clock present	10 MHz clock present	PXI_CLK10, PXIe_CLK100, and PXIe_SYNC100 all phase-locked to system timing slot—PXI_CLK10_IN

A copy of the backplane PXI_CLK10 is exported to the 10 MHz REF OUT pin of connector J27. An independent buffer drives this clock. Refer to *Backplane Specifications* for the specification information for the 10 MHz REF OUT signal on connector J27.

PXIe_SYNC_CTRL

PXIe_SYNC100 is by default a 10 ns pulse synchronous to PXI_CLK10. The frequency of PXIe_SYNC100 is 10/*n* MHz, where *n* is a positive integer. The default for *n* is 1, giving PXIe_SYNC100 a 100 ns period. However, the backplane allows *n* to be programmed to other integers. For example, setting *n* = 3 creates a PXIe_SYNC100 with a 300 ns period while still maintaining its phase relationship to PXI_CLK10. The *n* value can be any positive integer from 1 to 255.

The system timing slot has a control pin for PXIe_SYNC100 called PXIe_SYNC_CTRL, for use when *n* > 1. Refer to Table 9, *XP3 Connector Pinout for the System Timing Slot*, for the system timing slot pinout. Refer to *Backplane Specifications* for the PXIe_SYNC_CTRL input specifications.

By default, a high level detected by the backplane on the PXIe_SYNC_CTRL pin causes a synchronous restart for the PXIe_SYNC100 signal. On the next PXI_CLK10 edge, the PXIe_SYNC100 signal restarts. This allows several chassis to have their PXIe_SYNC100 in phase with each other. Refer to Figure 6 for timing details with this method.

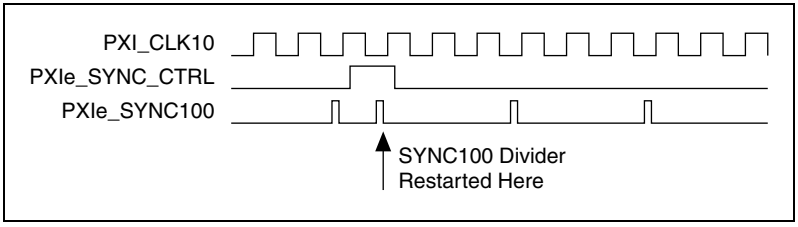


Figure 6. PXIe_SYNC100 at 3.33 MHz Using PXIe_SYNC_CTRL as Restart

Mechanical Requirements

Mounting

Figure 7 shows the backplane dimensions. There are 24 holes available for mounting with M2.5 hardware.

Use all mounting holes for proper backplane support.

Two mounting holes on top of the backplane have plated annular pads on the front and back of the backplane. Use these mounting holes to connect the backplane ground to the chassis in which the backplane is mounted. If you do not want to connect the backplane ground to the chassis, use insulated washers at these mounting holes. Refer to Figure 9 for the mounting hole positions.

Cooling

Note National Instruments is not responsible for damage to the backplane if inadequate cooling is used.

You should mount a fan below the backplane. Airflow should be from the bottom to the top of the PXI modules. You must determine the airflow requirements for your system based on the *PXI Hardware Specification*.

Handling

Cautions Be careful to avoid bending or otherwise damaging the pins on the backplane connectors. Bent pins may cause functional failures or damage when the backplane is powered.

To protect both yourself and the backplane from electrical hazards, leave the chassis powered off until you finish installing the PXI controller and modules.

Caution Electrostatic discharge can damage your equipment. To avoid such damage, discharge the static built up on your body by touching a grounded metal object before handling the PXI equipment. Then touch the antistatic plastic package containing the backplane to a metal part of your PXI chassis before removing the backplane from the packaging.

Dimensions

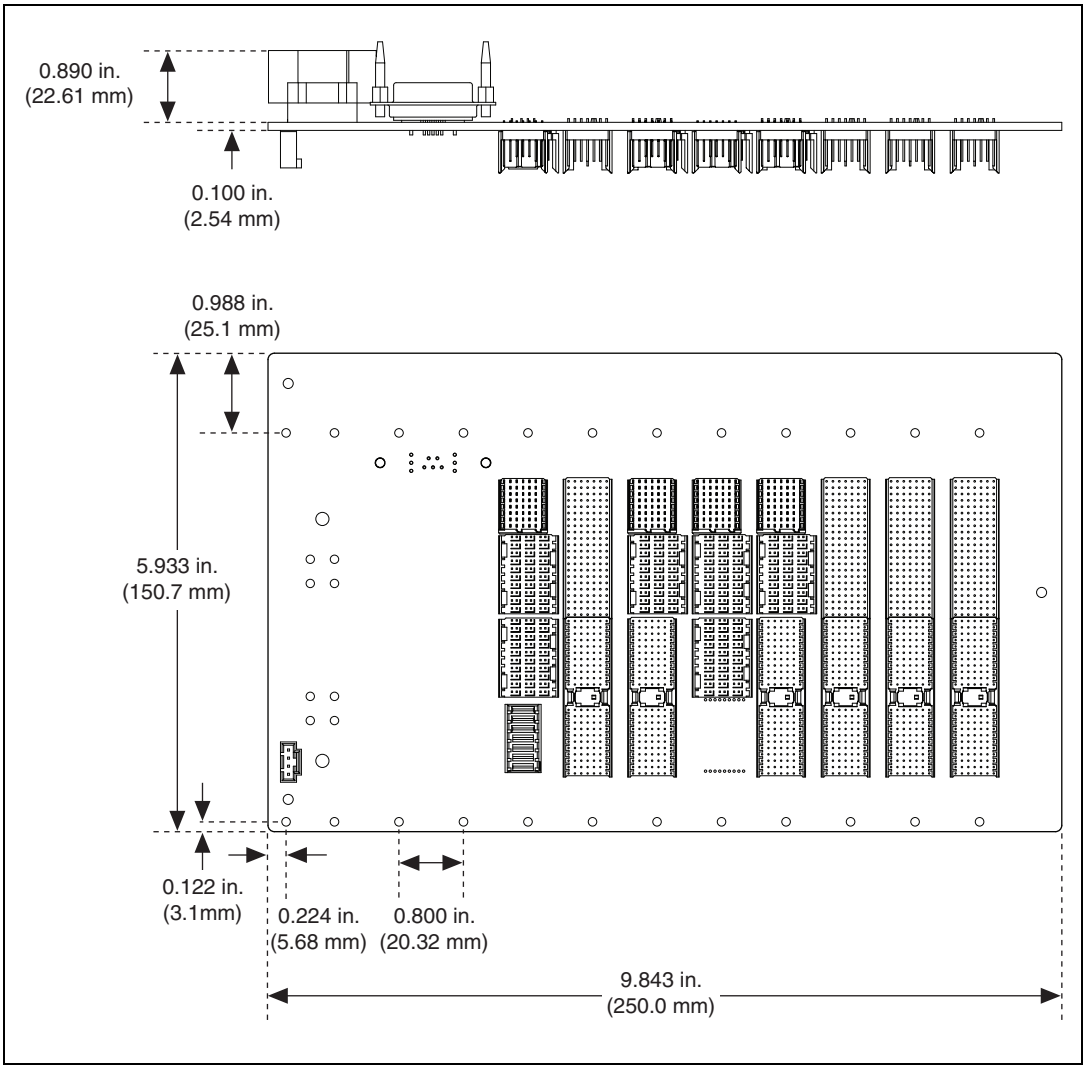
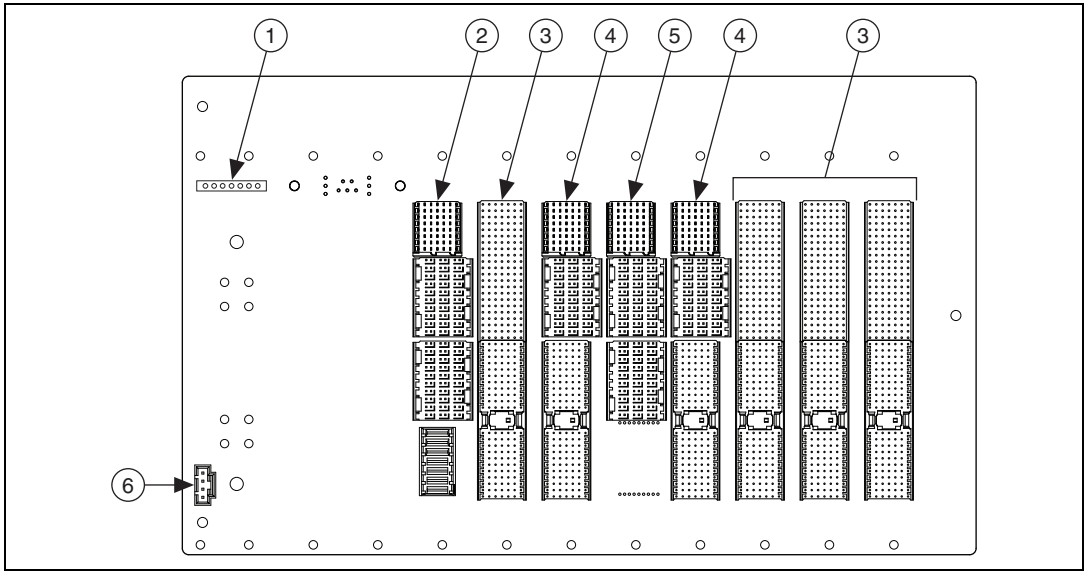


Figure 7. Dimensions

Electrical Requirements

PXI Connectors

The PXI and PXI Express connectors have pin descriptions defined in the *PXI Hardware Specification* and *PXI Express Hardware Specification*. Figure 8 shows the connectors.



1	Header W1 (Not Installed)	3	PXI Peripheral Slots (2, 6–8)	5	System Timing Slot
2	Slot 1 (Controller Slot)	4	Hybrid Peripheral Slots (3, 5)	6	Connector J26

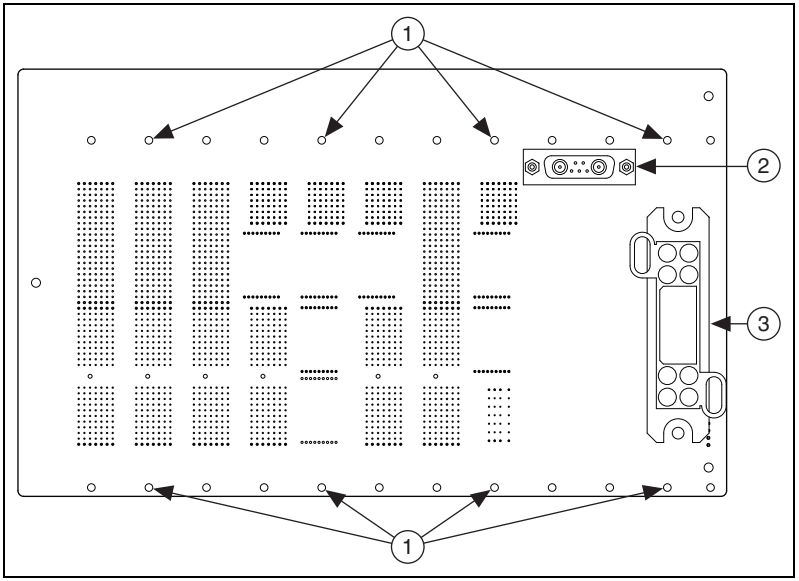
Figure 8. PXI, W1, and J26 Connectors

Power

Refer to the *PXI Express Hardware Specification* for power requirements and to the specifications of the chosen power supply to determine the minimum load required.

Connector J29

Connector J29 is the NI PXIe-1062Q backplane power supply connector. Figure 9 shows the J29 location. Refer to Table 2 for the pin descriptions. Connector J29 consists of eight larger #12 pins (1–4 and 26–29) for power and 21 #20 pins (5–25) used mainly for signaling. Table 2 also indicates which pins must be connected for basic backplane operation.



1	Plated Mounting Holes (8x)	3	Connector J29
2	Connector J27		

Figure 9. Backplane Power and CLK10 Connectors

Refer to the CompactPCI Express specification for details regarding PS_ON# and PS_OK.

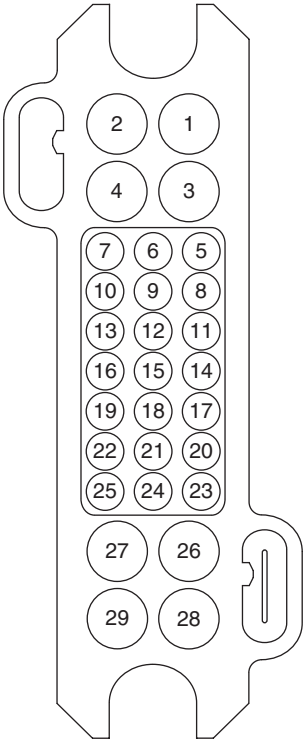
Caution Do not use the voltage sense pins (22, 23, and 25) to power the board. These pins are connected by thin trace to the backplane center and are for voltage sensing only. Providing current through these pins may damage the backplane. If your power supply has voltage sensing, use these pins; otherwise, leave them unconnected. Pins with "power plane" in the description are connected to the backplane's internal power planes and are suitable for carrying current.

Note Tyco Electronics manufactures the J29 mating connector, which you can order with part number 298-08-01100.

Note The connector SMBus pins are connected to the backplane SMBus, which the CompactPCI Express specification defines. (The specification also defines uses and addressing. Improper use of the SMBus could result in system controller malfunctions.

There are two SMBus slave devices on the NI PXIe-1062Q backplane. The Backplane Descriptor EEPROM is at slave address $A4_H$ as defined by the CompactPCI Express specification, and the backplane clocking CPLD is at slave address $5A_H$. If you must connect an SMBus slave device to the J29 SMBus pins, use slave address 58_H.

Table 2. Connector J29 Pin Descriptions

Connector	Pin	Signal	Description	Required for Basic Power Up
	1	+3.3V	+3.3 V power plane	Yes
	2	GND	Ground plane	Yes
	3	+3.3V	+3.3 V power plane	Yes
	4	GND	Ground plane	Yes
	5	5VAUX	5 V_{AUX} power plane	Yes
	6	GND	Ground plane	Yes
	7	–12V	–12 V power plane	Yes
	8	GND	Ground plane	Yes
	9	SMBCLK	Backplane SMBus clock	No
	10	SMBDAT	Backplane SMBus data	No
	11	SMBALERT#	Backplane SMBus alert#	No
	12	PS_ON#	Output from system slot J12—pin D2	No
	13	PS_OK	Input to system slot from power supply	Yes
	14	LED1	J26—pin 3	No
	15	LED2	J26—pin 4	No
	16	GND	Ground plane	Yes
	17	–12V	–12 V power plane	Yes
	18	GND	Ground plane	Yes
	19	GND	Ground plane	Yes
	20	12V_FAN	W1—pin 7 (not installed)	No
	21	GND	Ground plane	Yes
	22	+12V_SENSE	+12 V sense only, no power	No
	23	+3.3V_SENSE	+3.3 V sense only, no power	No
	24	GND	Ground plane	Yes
	25	+5V_SENSE	+5 V sense only, no power	No
	26	+12V	+12 V power plane	Yes
	27	GND	Ground plane	Yes
	28	+5V	+5 V power plane	Yes
	29	GND	Ground plane	Yes

Connector J27

Connector J27 is for interfacing with the backplane PXI_CLK10 circuitry. Figure 9 shows the J27 location, and Figure 10 shows the pin descriptions. Positronic manufactures the J27 mating connector, which you can order with part number CBD7W2M2000Z-759.1.

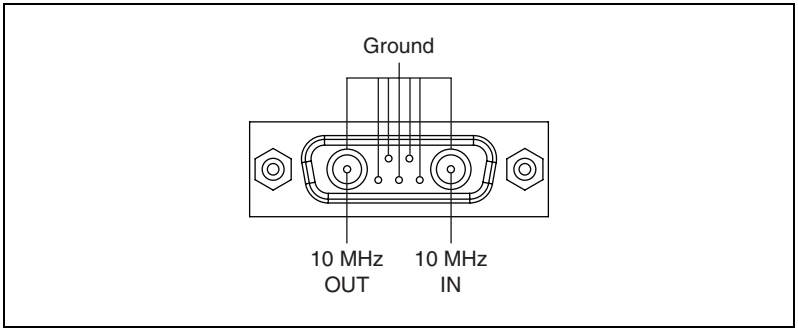


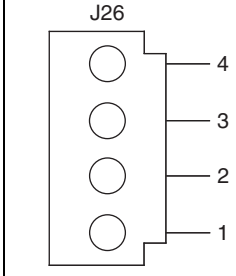
Figure 10. J27 Connector

Connector J26

Use connector J26 in conjunction with J29 for interfacing with an inhibit switch and LED. You do not need to connect anything to J26 for basic backplane power up. The power button (PWRBTN#) signal is a momentary pushbutton signal that tells the system controller to enable or inhibit the power supply. You can use signals LED1 and LED2 to drive a bicolor LED in the power switch, but you also can use these signals to carry another digital signal.

Figure 8 shows the J26 connector location. Refer to Table 3 for the pin descriptions.

Table 3. Connector J26 Pin Descriptions

Connector	Pin	Signal	Description
	1	PWRBTN#	Input to system slot J12—pin F2
	2	GND	Ground plane
	3	LED1	J29—pin 14
	4	LED2	J29—pin 15

Connector W1

Connector W1 is for a header used for monitoring the power supply voltage outputs. These signals cannot carry significant current for powering an external device. Figure 8 shows the W1 connector location.

Caution Using the connector W1 signals to carry current to power external devices may damage the backplane.

Backplane Specifications

Size .....3U-sized; one system slot (with three system expansion slots) and seven peripheral slots. Compliant with IEEE 1101.10 mechanical packaging. PXI Specification Revision 2.0 compliant. Accepts both PXI and CompactPCI (PICMG 2.0 R 3.0) 3U modules.

Backplane bare-board material .....UL 94 V-0 Recognized

Backplane connectors .....Conform to IEC 917 and IEC 1076-4-101, and are UL 94 V-0 rated

RoHS .....8-slot NI PXIe-1062Q backplane is RoHS-compliant

10 MHz System Reference Clock (PXI_CLK10)

Maximum clock skew between slots.....250 ps

Built-in 10 MHz clock

- Accuracy.....±25 ppm (guaranteed over the operating temperature range)
- Maximum jitter.....5 ps RMS in 10 Hz to 1 MHz range

External clock sources

- Connectors.....Connector J27 on rear of backplane or slot 2 J2 (pin D17)
- Input frequency.....10 MHz ±100 ppm or better

Input amplitude

Connector J27 ..... 200 mV_{pp} to 5 V_{pp}, 10 MHz squarewave or sinewave

Slot 2 ..... 5 V or 3.3 V, 10 MHz TTL signal

Input impedance ..... 50 Ω ± 5 Ω (rear connector)

Maximum jitter introduced by backplane circuitry ..... 1 ps RMS in 10 Hz to 1 MHz range

External clock output, connector J27

Connector ..... Connector J27 on rear of backplane (ground-referenced)

Output amplitude ..... 1 V_{pp} ±20% squarewave into 50 Ω
2 V_{pp} into open circuit

Output impedance ..... 50 Ω ± 5 Ω

Pinouts

This section describes the connector pinouts for the NI PXIe-1062Q chassis backplane.

Table 4 shows the XP1 connector pinout for the system controller slot.

Table 5 shows the XP2 connector pinout for the system controller slot.

Table 6 shows the XP3 connector pinout for the system controller slot.

Table 7 shows the XP4 connector pinout for the system controller slot.

Table 8 shows the TP2 connector pinout for the system timing slot.

Table 9 shows the XP3 connector pinout for the system timing slot.

Table 10 shows the XP4 connector pinout for the system timing slot.

Table 11 shows the P1 connector pinout for the peripheral slots.

Table 12 shows the P2 connector pinout for the peripheral slots.

Table 13 shows the P1 connector pinout for the hybrid peripheral slots.

Table 14 shows the XP3 connector pinout for the hybrid peripheral slots.

Table 15 shows the XP4 connector pinout for the hybrid peripheral slots.

For more detailed information, refer to the *PXI-5 PXI Express Hardware Specification*, Revision 2.0. Contact the PXI Systems Alliance for a copy of the specification.

System Controller Slot Pinouts

Table 4. XP1 Connector Pinout for the System Controller Slot

Pins	Signals
A	GND
B	12V
C	12V
D	GND
E	5V
F	3.3V
G	GND

Table 5. XP2 Connector Pinout for the System Controller Slot

Pin	A	B	ab	C	D	cd	E	F	ef
1	3PETp1	3PETn1	GND	3PERp1	3PERn1	GND	3PETp2	3PETn2	GND
2	3PETp3	3PETn3	GND	3PERp3	3PERn3	GND	3PERp2	3PERn2	GND
3	4PETp0	4PETn0	GND	4PERp0	4PERn0	GND	4PETp1	4PETn1	GND
4	4PETp2	4PETn2	GND	4PERp2	4PERn2	GND	4PERp1	4PERn1	GND
5	4PETp3	4PETn3	GND	4PERp3	4PERn3	GND	RSV	RSV	GND
6	RSV	RSV	GND	RSV	RSV	GND	RSV	RSV	GND
7	RSV	RSV	GND	RSV	RSV	GND	RSV	RSV	GND
8	RSV	RSV	GND	RSV	RSV	GND	RSV	RSV	GND
9	RSV	RSV	GND	RSV	RSV	GND	RSV	RSV	GND
10	RSV	RSV	GND	RSV	RSV	GND	RSV	RSV	GND

Table 6. XP3 Connector Pinout for the System Controller Slot

Pin	A	B	ab	C	D	cd	E	F	ef
1	RSV	RSV	GND	RSV	RSV	GND	RSV	RSV	GND
2	RSV	RSV	GND	PWR_OK	PS_ON#	GND	LINKCAP	PWRBTN#	GND
3	SMBDAT	SMBCLK	GND	4RefClk+	4RefClk–	GND	2RefClk+	2RefClk–	GND
4	RSV	PERST#	GND	3RefClk+	3RefClk–	GND	1RefClk+	1RefClk–	GND
5	1PETp0	1PETn0	GND	1PERp0	1PERn0	GND	1PETp1	1PETn1	GND
6	1PETp2	1PETn2	GND	1PERp2	1PERn2	GND	1PERp1	1PERn1	GND
7	1PETp3	1PETn3	GND	1PERp3	1PERn3	GND	2PETp0	2PETn0	GND
8	2PETp1	2PETn1	GND	2PERp1	2PERn1	GND	2PERp0	2PERn0	GND
9	2PETp2	2PETn2	GND	2PERp2	2PERn2	GND	2PETp3	2PETn3	GND
10	3PETp0	3PETn0	GND	3PERp0	3PERn0	GND	2PERp3	2PERn3	GND

Table 7. XP4 Connector Pinout for the System Controller Slot

Pin	Z	A	B	C	D	E	F
1	GND	GA4	GA3	GA2	GA1	GA0	GND
2	GND	5Vaux	GND	SYSEN#	WAKE#	ALERT#	GND
3	GND	RSV	RSV	RSV	RSV	RSV	GND
4	GND	RSV	RSV	RSV	RSV	RSV	GND
5	GND	PXI_TRIG3	PXI_TRIG4	PXI_TRIG5	GND	PXI_TRIG6	GND
6	GND	PXI_TRIG2	GND	RSV	PXI_STAR	PXI_CLK10	GND
7	GND	PXI_TRIG1	PXI_TRIG0	RSV	GND	PXI_TRIG7	GND
8	GND	RSV	GND	RSV	RSV	PXI_LBR6	GND

System Timing Slot Pinouts

Table 8. TP2 Connector Pinout for the System Timing Slot

Pin	A	B	ab	C	D	cd	E	F	ef
1	PXIe_DSTARC0+	PXIe_DSTARC0–	GND	PXIe_DSTARC8+	PXIe_DSTARC8–	GND	PXIe_DSTARB8+	PXIe_DSTARB8–	GND
2	PXIe_DSTARA0+	PXIe_DSTARA0–	GND	PXIe_DSTARC9+	PXIe_DSTARC9–	GND	PXIe_DSTARA8+	PXIe_DSTARA8–	GND
3	PXIe_DSTARB0+	PXIe_DSTARB0–	GND	NC	NC	GND	PXIe_DSTARA9+	PXIe_DSTARA9–	GND
4	NC	NC	GND	PXI_STAR0	PXI_STAR1	GND	PXIe_DSTARB9+	PXIe_DSTARB9–	GND
5	NC	NC	GND	PXI_STAR2	PXI_STAR3	GND	NC	NC	GND
6	NC	NC	GND	PXI_STAR4	PXI_STAR5	GND	NC	NC	GND

Table 8. TP2 Connector Pinout for the System Timing Slot (Continued)

Pin	A	B	ab	C	D	cd	E	F	ef
7	NC	NC	GND	PXI_STAR6	NC	GND	NC	NC	GND
8	NC	NC	GND	NC	NC	GND	NC	NC	GND
9	NC	NC	GND	NC	NC	GND	NC	NC	GND
10	NC	NC	GND	NC	NC	GND	NC	NC	GND

Table 9. XP3 Connector Pinout for the System Timing Slot

Pin	A	B	ab	C	D	cd	E	F	ef
1	PXIe_CLK100+	PXIe_CLK100–	GND	PXIe_SYNC100+	PXIe_SYNC100–	GND	PXIe_DSTARC+	PXIe_DSTARC–	GND
2	PRSNT#	PWREN#	GND	PXIe_DSTARB+	PXIe_DSTARB–	GND	PXIe_DSTARA+	PXIe_DSTARA–	GND
3	SMBDAT	SMBCLK	GND	RSV	RSV	GND	RSV	RSV	GND
4	MPWRGD*	PERST#	GND	RSV	RSV	GND	1RefClk+	1RefClk–	GND
5	1PETp0	1PETn0	GND	1PERp0	1PERn0	GND	1PETp1	1PETn1	GND
6	1PETp2	1PETn2	GND	1PERp2	1PERn2	GND	1PERp1	1PERn1	GND
7	1PETp3	1PETn3	GND	1PERp3	1PERn3	GND	1PETp4	1PETn4	GND
8	1PETp5	1PETn5	GND	1PERp5	1PERn5	GND	1PERp4	1PERn4	GND
9	1PETp6	1PETn6	GND	1PERp6	1PERn6	GND	1PETp7	1PETn7	GND
10	RSV	RSV	GND	RSV	RSV	GND	1PERp7	1PERn7	GND

Table 10. XP4 Connector Pinout for the System Timing Slot

Pin	Z	A	B	C	D	E	F
1	GND	GA4	GA3	GA2	GA1	GA0	GND
2	GND	5Vaux	GND	SYSEN#	WAKE#	ALERT#	GND
3	GND	12V	12V	GND	GND	GND	GND
4	GND	GND	GND	3.3V	3.3V	3.3V	GND
5	GND	PXI_TRIG3	PXI_TRIG4	PXI_TRIG5	GND	PXI_TRIG6	GND
6	GND	PXI_TRIG2	GND	ATNLED	PXI_CLK10_IN	PXI_CLK10	GND
7	GND	PXI_TRIG1	PXI_TRIG0	ATNSW#	GND	PXI_TRIG7	GND
8	GND	PXIe_SYNC_CTRL	GND	RSV	PXI_LBL6	PXI_LBR6	GND

Peripheral Slot Pinouts

Table 11. P1 Connector Pinout for the Peripheral Slot

Pin	Z	A	B	C	D	E	F
25	GND	5V	REQ64#	ENUM#	3.3V	5V	GND
24	GND	AD[1]	5V	V(I/O)	AD[0]	ACK64#	GND
23	GND	3.3V	AD[4]	AD[3]	5V	AD[2]	GND
22	GND	AD[7]	GND	3.3V	AD[6]	AD[5]	GND
21	GND	3.3V	AD[9]	AD[8]	M66EN	C/BE[0]#	GND
20	GND	AD[12]	GND	V(I/O)	AD[11]	AD[10]	GND
19	GND	3.3V	AD[15]	AD[14]	GND	AD[13]	GND
18	GND	SERR#	GND	3.3V	PAR	C/BE[1]#	GND
17	GND	3.3V	IPMB_SCL	IPMB_SDA	GND	PERR#	GND
16	GND	DEVSEL#	GND	V(I/O)	STOP#	LOCK#	GND
15	GND	3.3V	FRAME#	IRDY#	BD_SEL#	TRDY#	GND
12–14	Key Area						
11	GND	AD[18]	AD[17]	AD[16]	GND	C/BE[2]#	GND
10	GND	AD[21]	GND	3.3V	AD[20]	AD[19]	GND
9	GND	C/BE[3]#	IDSEL	AD[23]	GND	AD[22]	GND
8	GND	AD[26]	GND	V(I/O)	AD[25]	AD[24]	GND
7	GND	AD[30]	AD[29]	AD[28]	GND	AD[27]	GND
6	GND	REQ#	GND	3.3V	CLK	AD[31]	GND
5	GND	BRSVP1A5	BRSVP1B5	RST#	GND	GNT#	GND
4	GND	IPMB_PWR	HEALTHY	V(I/O)	INTP	INTS	GND
3	GND	INTA#	INTB#	INTC#	5V	INTD#	GND
2	GND	TCK	5V	TMS	TDO	TDI	GND
1	GND	5V	–12V	TRST#	+12V	5V	GND

Table 12. P2 Connector Pinout for the Peripheral Slot

Pin	Z	A	B	C	D	E	F
22	GND	GA4	GA3	GA2	GA1	GA0	GND
21	GND	PXI_LBR0	GND	PXI_LBR1	PXI_LBR2	PXI_LBR3	GND
20	GND	PXI_LBR4	PXI_LBR5	PXI_LBL0	GND	PXI_LBL1	GND
19	GND	PXI_LBL2	GND	PXI_LBL3	PXI_LBL4	PXI_LBL5	GND
18	GND	PXI_TRIG3	PXI_TRIG4	PXI_TRIG5	GND	PXI_TRIG6	GND
17	GND	PXI_TRIG2	GND	RSV	PXI_STAR	PXI_CLK10	GND
16	GND	PXI_TRIG1	PXI_TRIG0	RSV	GND	PXI_TRIG7	GND
15	GND	PXI_BRSVA15	GND	RSV	PXI_LBL6	PXI_LBR6	GND
14	GND	RSV	RSV	RSV	GND	RSV	GND
13	GND	RSV	GND	V(I/O)	RSV	RSV	GND
12	GND	RSV	RSV	RSV	GND	RSV	GND
11	GND	RSV	GND	V(I/O)	RSV	RSV	GND
10	GND	RSV	RSV	RSV	GND	RSV	GND
9	GND	RSV	GND	V(I/O)	RSV	RSV	GND
8	GND	RSV	RSV	RSV	GND	RSV	GND
7	GND	RSV	GND	V(I/O)	RSV	RSV	GND
6	GND	RSV	RSV	RSV	GND	RSV	GND
5	GND	RSV	GND	V(I/O)	RSV	RSV	GND
4	GND	V(I/O)	64EN#	RSV	GND	RSV	GND
3	GND	PXI_LBR7	GND	PXI_LBR8	PXI_LBR9	PXI_LBR10	GND
2	GND	PXI_LBR11	PXI_LBR12	UNC	PXI_LBL7	PXI_LBL8	GND
1	GND	PXI_LBL9	GND	PXI_LBL10	PXI_LBL11	PXI_LBL12	GND

Hybrid Slot Pinouts

Table 13. P1 Connector Pinout for the Hybrid Slot

Pin	Z	A	B	C	D	E	F
25	GND	5V	REQ64#	ENUM#	3.3V	5V	GND
24	GND	AD[1]	5V	V(I/O)	AD[0]	ACK64#	GND
23	GND	3.3V	AD[4]	AD[3]	5V	AD[2]	GND
22	GND	AD[7]	GND	3.3V	AD[6]	AD[5]	GND
21	GND	3.3V	AD[9]	AD[8]	M66EN	C/BE[0]#	GND
20	GND	AD[12]	GND	V(I/O)	AD[11]	AD[10]	GND
19	GND	3.3V	AD[15]	AD[14]	GND	AD[13]	GND
18	GND	SERR#	GND	3.3V	PAR	C/BE[1]#	GND
17	GND	3.3V	IPMB_SCL	IPMB_SDA	GND	PERR#	GND
16	GND	DEVSEL#	GND	V(I/O)	STOP#	LOCK#	GND
15	GND	3.3V	FRAME#	IRDY#	BD_SEL#	TRDY#	GND
12–14	Key Area						
11	GND	AD[18]	AD[17]	AD[16]	GND	C/BE[2]#	GND
10	GND	AD[21]	GND	3.3V	AD[20]	AD[19]	GND
9	GND	C/BE[3]#	IDSEL	AD[23]	GND	AD[22]	GND
8	GND	AD[26]	GND	V(I/O)	AD[25]	AD[24]	GND
7	GND	AD[30]	AD[29]	AD[28]	GND	AD[27]	GND
6	GND	REQ#	GND	3.3V	CLK	AD[31]	GND
5	GND	BRSVP1A5	BRSVP1B5	RST#	GND	GNT#	GND
4	GND	IPMB_PWR	HEALTHY#	V(I/O)	INTP	INTS	GND
3	GND	INTA#	INTB#	INTC#	5V	INTD#	GND
2	GND	TCK	5V	TMS	TDO	TDI	GND
1	GND	5V	–12V	TRST#	+12V	5V	GND

Table 14. XP3 Connector Pinout for the Hybrid Slot

Pin	A	B	ab	C	D	cd	E	F	ef
1	PXIe_CLK100+	PXIe_CLK100–	GND	PXIe_SYNC100+	PXIe_SYNC100–	GND	PXIe_DSTARC+	PXIe_DSTARC–	GND
2	PRSNT#	PWREN#	GND	PXIe_DSTARB+	PXIe_DSTARB–	GND	PXIe_DSTARA+	PXIe_DSTARA–	GND
3	SMBDAT	SMBCLK	GND	RSV	RSV	GND	RSV	RSV	GND
4	MPWRGD*	PERST#	GND	RSV	RSV	GND	1RefClk+	1RefClk–	GND
5	1PETp0	1PETn0	GND	1PERp0	1PERn0	GND	1PETp1	1PETn1	GND
6	1PETp2	1PETn2	GND	1PERp2	1PERn2	GND	1PERp1	1PERn1	GND
7	1PETp3	1PETn3	GND	1PERp3	1PERn3	GND	1PETp4	1PETn4	GND
8	1PETp5	1PETn5	GND	1PERp5	1PERn5	GND	1PERp4	1PERn4	GND
9	1PETp6	1PETn6	GND	1PERp6	1PERn6	GND	1PETp7	1PETn7	GND
10	RSV	RSV	GND	RSV	RSV	GND	1PERp7	1PERn7	GND

Table 15. XP4 Connector Pinout for the Hybrid Slot

Pin	Z	A	B	C	D	E	F
1	GND	GA4	GA3	GA2	GA1	GA0	GND
2	GND	5Vaux	GND	SYSEN#	WAKE#	ALERT#	GND
3	GND	12V	12V	GND	GND	GND	GND
4	GND	GND	GND	3.3V	3.3V	3.3V	GND
5	GND	PXI_TRIG3	PXI_TRIG4	PXI_TRIG5	GND	PXI_TRIG6	GND
6	GND	PXI_TRIG2	GND	ATNLED	PXI_STAR	PXI_CLK10	GND
7	GND	PXI_TRIG1	PXI_TRIG0	ATNSW#	GND	PXI_TRIG7	GND
8	GND	RSV	GND	RSV	PXI_LBL6	PXI_LBR6	GND