SC Express

PXIe-4310 User Manual

8-channel, 16-bit, 400 kS/s/ch, Ch-Ch Isolated Analog Input Module

May 2017
377025A-01

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Contents

Chapter 1
Getting Started

Installation 1-1
Module Specifications 1-1

Chapter 2
Using the PXIe-4310

Isolation 2-1
Signal Connections 2-2
Working Voltage Range 2-4
Input Ranges 2-5
Analog Input Filter 2-6
Self Calibration 2-7
Device Pinout 2-7
    I/O Connector Signal Description 2-9
PXIe-4310 Block Diagram 2-10

Chapter 3
Acquiring Analog Input

Analog Input Data Acquisition Methods 3-1
    Software-Timed Acquisitions 3-1
    Hardware-Timed Acquisitions 3-1
    Aggregate versus Single Channel Sampling Rates 3-2
Getting Started with AI Applications in Software 3-2
Analog Input Timing Signals 3-3
    AI Sample Clock Signal 3-3
        Using an Internal Source 3-3
        Using an External Source 3-4
        Routing AI Sample Clock Signal to an Output Terminal 3-4
    AI Sample Clock Timebase Signal 3-4
    AI Start Trigger Signal 3-5
        Routing AI Start Trigger to an Output Terminal 3-6
        Retriggerable Analog Input 3-6
    AI Reference Trigger Signal 3-7
        Using a Digital Source 3-8
        Using an Analog Source 3-9
        Routing AI Reference Trigger to an Output Terminal 3-9
    AI Pause Trigger Signal 3-9
        Using a Digital Source 3-10
        Routing AI Pause Trigger Signal to an Output Terminal 3-10

Clock Generation and Routing 3-10
Reference Clock 3-11
10 MHz RefClk 3-11
PXI Express Clock and Trigger Signals 3-11
PXIe_CLK100 3-11
PXIe_SYNC100 3-12
PXI_CLK10 3-12
PXI Triggers 3-12
PXI_STAR Trigger 3-12
PXIe_DSTAR<A..C> 3-13
Synchronizing Multiple Devices 3-13
Triggering 3-15
Analog Edge Triggering 3-15
Analog Edge Triggering With Hysteresis 3-15
Window Triggering 3-16
Digital Input Triggering 3-17

Chapter 4
Accessories
TB-4310 (10V)/TB-4310 (600V) Accessory 4-1
Accessory Auto-Detection 4-1
Accessory Power 4-2

Appendix A
NI Services

1 Getting Started

The NI PXIe-4310 provides eight, simultaneously sampled, analog input channels, each with channel-to-channel and channel-to-earth isolation. The PXIe-4310 has a 10 V maximum measurement range when using a TB-4310 (10V) that can be expanded to 600 V when using a TB-4310 (600V). Each channel of the PXIe-4310 has a 16-bit ADC with three programmable filter settings and four gain settings. Two input PFI lines are available on the module for triggering/clocking.

Installation

Refer to the *PXIe-4310 and TB-4310 (10V)/TB-4310 (600V) Getting Started Guide and Terminal Block Specifications* for step-by-step installation instructions, accessory details, and a complete listing of supported accessories.

Note For a complete list of terminal blocks supported by a specific release of NI-DAQmx, refer to the *NI-DAQmx Readme*, available on the version-specific download page or installation media.

Module Specifications

Refer to the *PXIe-4310 Specifications* document for module specifications.

2

Using the PXIe-4310

This chapter describes how to connect AI input signals to the PXIe-4310. It also provides the I/O connector signal pin assignments of the module.

Driver support for the PXIe-4310 was first available in NI-DAQmx 17.1. For the list of devices supported by a specific release, refer to the *NI-DAQmx Readme*, available on the version-specific download page or installation media.

Caution To ensure the specified EMC performance, operate this product only with shielded cables and shielded accessories. Use only twisted, shielded pair cables (Belden 83319 or equivalent) for channel connections.

Caution When this symbol is marked on a product. This icon denotes a caution, which advises you of precautions to take to avoid injury, data loss, or a system crash.

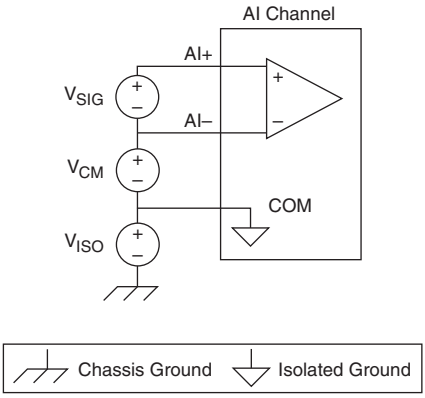
Isolation

The PXIe-4310 provides channel-to-channel and channel-to-earth isolation. Refer to the *PXIe-4310 Specifications* for information about Safety Voltage operating levels.

Signal Connections

Figure 2-1 shows the voltages V_{SIG}, V_{CM}, and V_{ISO}, which are used to describe signal connections in this section.

Figure 2-1. V_{SIG}, V_{CM}, and V_{ISO} Signal Connections



V_{SIG} is the voltage difference between AI<0..7>+ and AI<0..7>-. This is the desired signal to be measured. V_{CM} is the common-mode voltage with respect to the AI isolated ground, COM<0..7>, calculated by subtracting COM<0..7> from AI<0..7>-. V_{ISO} is the isolation voltage with respect to the chassis ground of the measurement device.

The analog input channels are floating with respect to chassis ground and each other. If you make a ground-referenced connection between the signal source and the PXIe-4310 input, make sure the voltage on the AI+, AI-, and COM connections are within the safety voltage limits to ensure safe operation. Refer to the *PXIe-4310 Specifications* for more information about Safety Voltages.

The COM terminal for each channel must be connected to the reference ground of the AI source. Failure to connect COM results in inaccurate measurements. You can connect the COM terminal directly to the negative terminal of the source as shown in Figure 2-2 or to an isolated ground of the source as long as the working voltage specification of the PXIe-4310 is not violated.

To ensure the specified EMC performance, wire the AI+ and AI- signals as twisted pairs and use the COM as a shield. The COM connection should be made as close to the source as possible to take advantage of the differential nature of this device.

Figure 2-2 and 2-3 show the ground referenced and floating sources with low source impedance (<100 Ω).

Figure 2-2. Ground Referenced Source Signal Connection

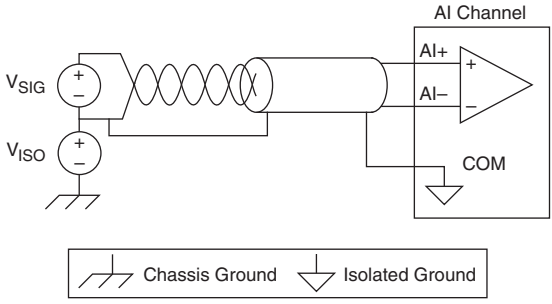
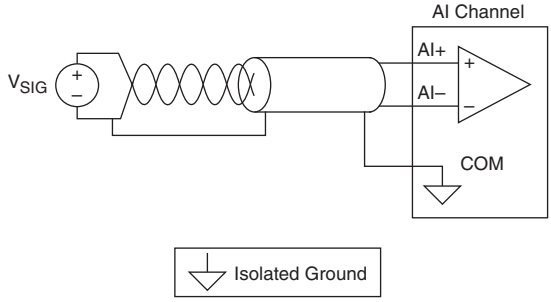


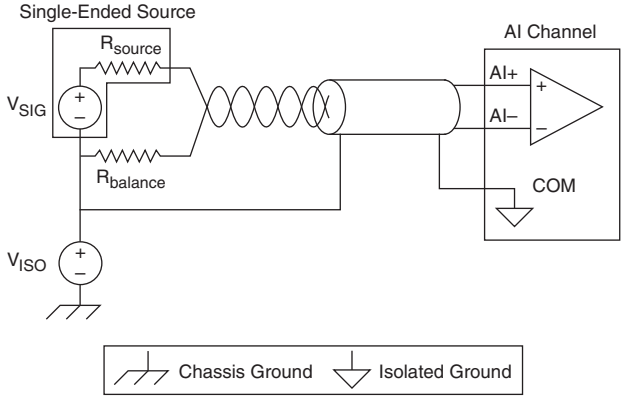
Figure 2-3. Floating Source Signal Connection



For signals with source impedance >100 Ω, it is important to maintain a balanced source impedance, which means that both terminals of the source have equal impedance to the signal source ground. Providing a balanced source impedance is critical to achieving optimal noise rejection, since any noise pickup will induce a noise voltage common to both conductors, which can then be rejected by the analog input Programmable Gain Instrumentation Amplifier (PGIA). Noise pickup in a system with an unbalanced source impedance will induce noise voltages of different amplitudes on each conductor, which appears as a differential voltage that will be measured as a signal voltage. Additionally, if the isolation voltage (V_{ISO}) is a time varying voltage or noisy DC source, a balanced source impedance is critical in ensuring that V_{ISO} is common to both inputs, which maximizes the ability of the PGIA to reject V_{ISO}. A mismatch in the source impedance can cause a portion of V_{ISO} to appear as a differential voltage between AI+ and AI-.

Figure 2-4 shows how to connect a high impedance, unbalanced source. A resistor, $R_{balance} = R_{source}$, has been added between the signal ground and AI- to balance the output of the source output impedance with respect to the signal ground.

Figure 2-4. Signal Connection for a High Impedance Source



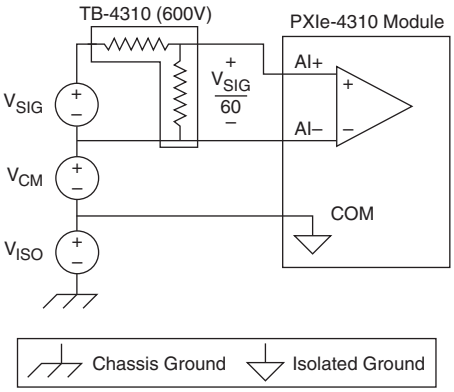
Working Voltage Range

The PGIA normally operates by amplifying signals of interest (V_{SIG}) while rejecting common-mode signals under the following three conditions:

- The common-mode voltage (V_{CM}), which is equivalent to subtracting COM <0..7> from AI <0..7>-, must be less than ±11 V.
- The signal voltage (V_{SIG}), which is equivalent to subtracting AI <0..7>- from AI <0..7>+, must be less than or equal to the range selection of the given channel. If V_{SIG} is greater than the range selected, the signal clips and information is lost.
- The total working voltage of the positive input, which is equivalent to ($V_{CM} + V_{SIG}$), or subtracting COM <0..7> from AI <0..7>+, must be less than the maximum working voltage specification. Refer to the *PXIe-4310 Specifications* working voltage limits. When using the TB-4310 (600V), divide the input signal voltage (V_{SIG}) by 60 when calculating the working voltage, as shown in Figure 2-5.

If any of these conditions are exceeded, the input voltage is clamped until the fault condition is removed. Measurements performed while the input is clamped will return a constant, noiseless voltage reading that corresponds to the exact positive or negative full scale voltage.

Figure 2-5. Signal Connections when using TB-4310 (600V)



Refer to the *PXIe-4310 and TB-4310 (10V)/TB-4310 (600V) Getting Started Guide and Terminal Block Specifications* for details about signal terminal locations.

Input Ranges

The input range is the maximum differential voltage, the difference between AI+ and AI-, that can be measured. Selecting an input range sets the gain of the PGIA. You can individually program the input range of each AI channel on your PXIe-4310 module.

The input range affects the resolution of the PXIe-4310 module for an AI channel. Resolution refers to the voltage of one ADC code. For example, a 16-bit ADC converts analog inputs into one of 65,536 (= 2^{16}) codes—that is, one of 65,536 possible digital values. These values are spread fairly evenly across the input range. So, for an input range of -10 V to 10 V, the voltage of each code of a 16-bit ADC is:

$$\frac{10\ \text{V} - (-10\ \text{V})}{2^{16}} = 305\ \mu\text{V}$$

Choose an input range that matches the expected input range of your signal. A large input range can accommodate a large signal variation, but reduces the voltage resolution. Choosing a smaller input range improves the voltage resolution, but may result in the input signal going out of range.

Note The PXIe-4310 module uses a calibration method that requires codes (typically about 5% of the codes) outside of the specified range. This calibration method improves absolute accuracy, but it decreases the nominal resolution of input ranges by about 5% over what the formula shown above would indicate.

Table 2-1 shows the input ranges and resolutions supported by the PXIe-4310 module.

Table 2-1. PXIe-4310 Input Range and Nominal Resolution

Input Range	Nominal Resolution Assuming 5% Over Range
-10 V to 10 V	320 µV
-5 V to 5 V	160 µV
-2 V to 2 V	64 µV
-1 V to 1 V	32 µV

Analog Input Filter

The PXIe-4310 has selectable filter settings per channel. Each channel can independently be set to one of the three available lowpass filter settings: 10 kHz, 100 kHz, and Disable. The 10 kHz and 100 kHz filters are 2-pole Butterworth filters, and their designation refers to the -3 dB cut-off frequency. The Disable setting bypasses the filters and allows measurements in the full bandwidth of the PXIe-4310.

Self Calibration

Self-calibration measures the onboard reference voltage of the module and adjusts the self-calibration constants to account for any errors caused by short-term fluctuations in the environment.

NI recommends that you self-calibrate the PXIe-4310 module after installation and whenever the ambient temperature changes. Self-calibration should be performed after the module has warmed up for the recommended time period. Refer to the *PXIe-4310 Specifications* for the module warm-up time and self-calibration conditions.

You can initiate self-calibration using Measurement & Automation Explorer (MAX), by completing the following steps.

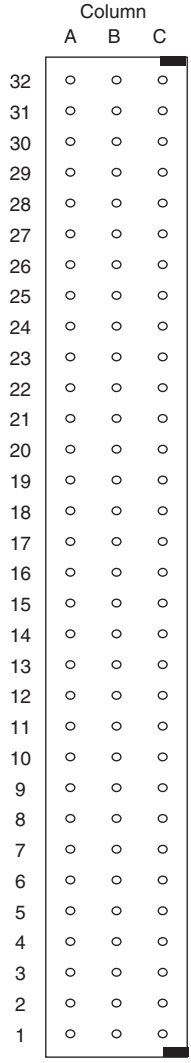
1. Launch MAX.
2. Select **My System»Devices and Interfaces»**your module.
3. Initiate self-calibration using one of the following methods:
   - Click **Self-Calibrate** in the upper right corner of MAX.
   - Right-click the name of the module in the MAX configuration tree and select Self-Calibrate from the drop-down menu.

Note You can also programmatically self-calibrate the module with NI-DAQmx, as described in *Device Calibration* in the *NI-DAQmx Help* or the *LabVIEW Help*.

Device Pinout

Table 2-2 shows the pinout of the front connector of the PXIe-4310. Refer to the *I/O Connector Signal Description* section for definitions of each signal. Refer to the *PXIe-4310 and TB-4310 (10V)/TB-4310 (600V) Getting Started Guide and Terminal Block Specifications* for signal locations on the terminal block.

Table 2-2. Front Signal Pin Assignments

Front Connector Diagram	Pin Number	Column A	Column B	Column C	Channel
 — is no connection, isolation barrier, RSVD is reserved	32	AI0-	AI0+	—	0
	31	COM0	—	—	
	30	—	—	—	—
	29	—	COM1	—	1
	28	AI1-	AI1+	—	
	27	—	—	—	—
	26	—	—	—	
	25	AI2-	AI2+	—	2
	24	COM2	—	—	
	23	—	—	—	—
	22	—	COM3	—	3
	21	AI3-	AI3+	—	
	20	—	—	—	—
	19	—	—	—	
	18	AI4-	AI4+	—	4
	17	COM4	—	—	
	16	—	—	—	—
	15	—	COM5	—	5
	14	AI5-	AI5+	—	
	13	—	—	—	—
	12	—	—	—	
	11	AI6-	AI6+	—	6
	10	COM6	—	—	
	9	—	—	—	—
	8	—	—	—	
	7	—	—	—	
	6	—	COM7	—	7
	5	AI7-	AI7+	—	
	4	PFI0	PFI1	—	
	3	RSVD	RSVD	—	
	2	RSVD	COM 7	—	
	1	RSVD	RSVD	—	

I/O Connector Signal Description

Table 2-3 describes the signals found on the I/O connectors.

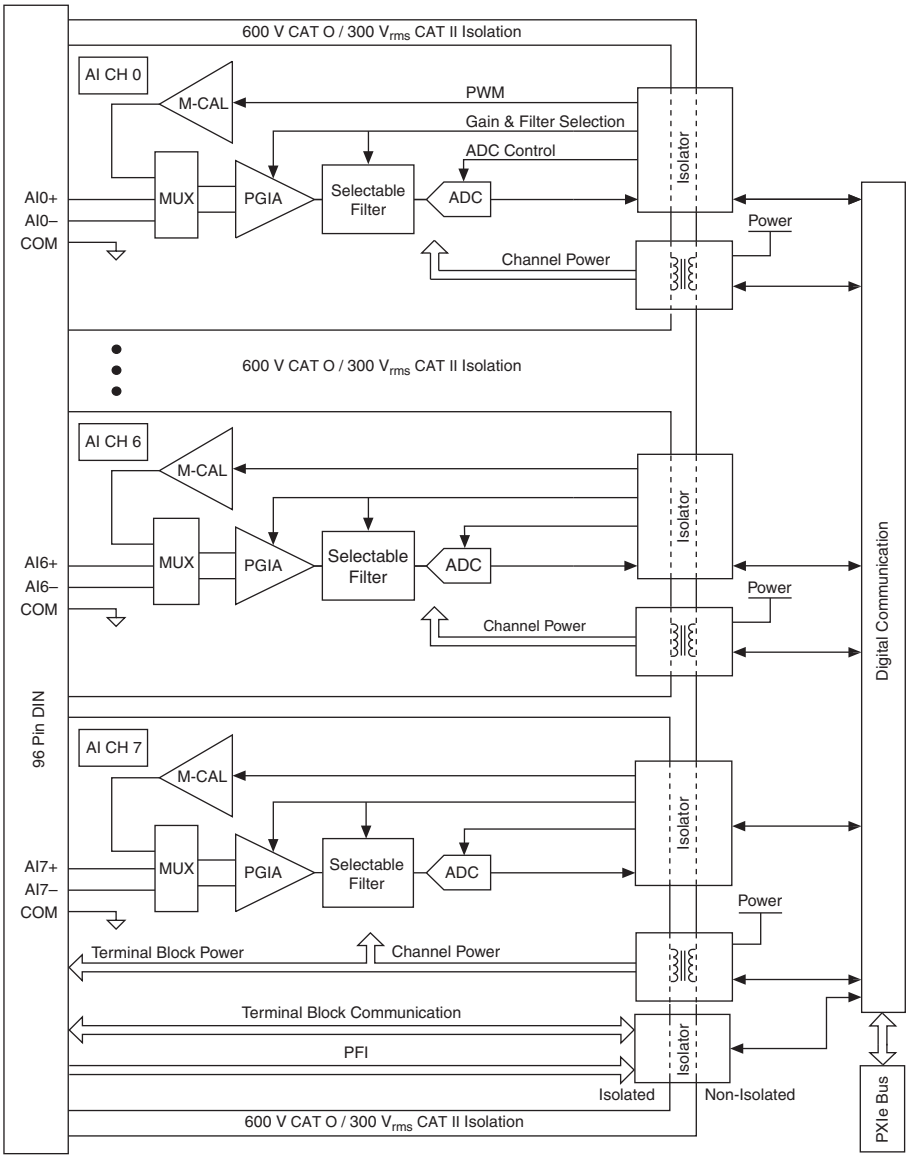
Table 2-3. I/O Connector Signal Descriptions

Signal Names	Reference	Direction	Description
COM <0..7>	—	—	Analog Input Isolated Ground—These terminals are the reference point for differential analog input measurements.
AI <0..7>+, AI <0..7>-	COM <0..7>	Input	Analog Input Channels 0 to 7—AI+ and AI- are the positive and negative inputs of differential analog input.
PFI <0, 1>	COM 7	Input	Programmable Function Interface Channels 0 to 1—Each of these terminals can be individually configured as PFI terminals. They can be used to supply a start, reference, or pause trigger, or be used as an external timing source for AI. **Note**: These channels may only be referenced to channel 7 in order to maintain safety isolation.
RSVD	COM 7	Bi-Directional	These pins are reserved for communication with the accessory.

PXIe-4310 Block Diagram

Figure 2-6 shows the block diagram of the PXIe-4310 module.

Figure 2-6. PXIe-4310 Block Diagram



3

Acquiring Analog Input

This section describes the methods available for acquiring analog input data.

Analog Input Data Acquisition Methods

When performing analog input measurements, you can either perform software-timed or hardware-timed acquisitions.

Software-Timed Acquisitions

With a software-timed acquisition, software controls the rate of the acquisition. Software sends a separate command to the hardware to initiate each ADC conversion. In NI-DAQmx, software-timed acquisitions are referred to as having on-demand timing. Software-timed acquisitions are also referred to as immediate or static acquisitions and are typically used for reading a single sample of data.

Hardware-Timed Acquisitions

With hardware-timed acquisitions, a digital hardware signal (AI Sample Clock) controls the rate of the acquisition. This signal can be generated internally on your device or provided externally.

Hardware-timed acquisitions have several advantages over software-timed acquisitions:

- The time between samples can be much shorter.
- The timing between samples is deterministic.
- Hardware-timed acquisitions can use hardware triggering.

Hardware-timed operations can be buffered or hardware-timed single point (HWTSP). A buffer is a temporary storage in computer memory for to-be-transferred samples.

- Buffered—In a buffered acquisition, data is moved from the onboard FIFO memory of the DAQ device to a PC buffer using DMA before it is transferred to application memory. Buffered acquisitions typically allow for much faster transfer rates than HWTSP acquisitions because data is moved in large blocks, rather than one point at a time.

  One property of buffered I/O operations is the sample mode. The sample mode can be either finite or continuous:

  – Finite sample mode acquisition refers to the acquisition of a specific, predetermined number of data samples. Once the specified number of samples has been read in, the acquisition stops. If you use a reference trigger, you must use finite sample mode.

  – Continuous acquisition refers to the acquisition of an unspecified number of samples. Instead of acquiring a set number of data samples and stopping, a continuous

acquisition continues until you stop the operation. Continuous acquisition is also referred to as double-buffered or circular-buffered acquisition.

If data cannot be transferred across the bus fast enough, the FIFO becomes full. New acquisitions overwrite data in the FIFO before it can be transferred to host memory. The device generates an error in this case. With continuous operations, if the application program does not read data out of the PC buffer fast enough to keep up with the data transfer, the buffer could reach an overflow condition, causing an error to be generated.

- Hardware-timed single point (HWTSP)—Typically, HWTSP operations are used to read single samples at known time intervals. While buffered operations are optimized for high throughput, HWTSP operations are optimized for low latency and low jitter. In addition, HWTSP can notify software if it falls behind hardware. These features make HWTSP ideal for real-time control applications. HWTSP operations, in conjunction with the `wait for next sample clock` function, provide tight synchronization between the software layer and the hardware layer. Refer to the white paper *NI-DAQmx Hardware-Timed Single Point Lateness Checking* for more information. To access this document, go to `ni.com/info` and enter the Info Code `daqhwtsp`.

Aggregate versus Single Channel Sampling Rates

The PXIe-4310 module has one ADC per channel, so the single channel maximum sample rate can be achieved on all channels simultaneously.

The total aggregate sample rate determines the maximum bus bandwidth used by the device. The aggregate sample rate is the product of the maximum sample rate for a single channel multiplied by the number of AI channels that the device supports.

Table 3-1 shows the single channel and total aggregate rates for PXIe-4310 module.

Table 3-1. Analog Input Rates for PXIe-4310 Module

Single Channel	Total Aggregate
400 kS/s	3.2 MS/s

Getting Started with AI Applications in Software

You can use a PXIe-4310 module in the following simultaneous analog input applications:

- Single-point analog input
- Finite analog input
- Continuous analog input

The PXIe-4310 module uses the NI-DAQmx driver. NI-DAQmx includes a collection of programming examples to help you get started developing an application. You can modify examples to develop a new application or add example code to an existing application.

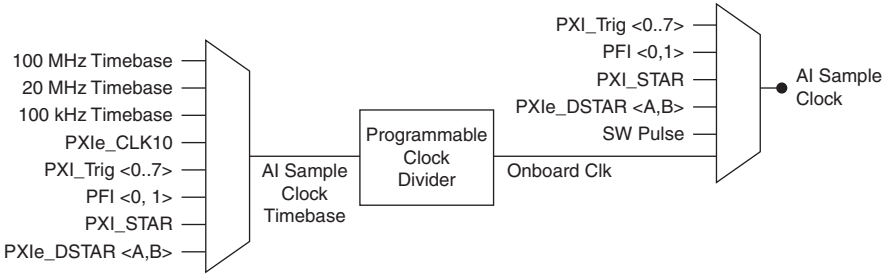
Note For more information about programming analog input applications and triggers in software, refer to the *NI-DAQmx Help* or the *LabVIEW Help*.

To locate LabVIEW, LabWindows™/CVI™, Measurement Studio, Visual Basic, and ANSI C examples go to ni.com/info and enter the Info Code daqmxexp.

Analog Input Timing Signals

Figure 3-1 summarizes all of the timing options provided by the analog input timing engine.

Figure 3-1. Analog Input Timing Options



The PXIe-4310 features the following analog input timing signals:

- AI Sample Clock Signal
- AI Sample Clock Timebase Signal
- AI Start Trigger Signal
- AI Reference Trigger Signal
- AI Pause Trigger Signal

AI Sample Clock Signal

The PXIe-4310 module uses the AI Sample Clock (ai/SampleClock) signal to initiate an acquisition on each active analog input channel. Since there is one ADC per channel, the AI Sample Clock signal controls the sample period for all of the channels in a task. Since there is one timing engine per module, all analog channels on a module must use the same sample clock.

You can specify an internal or external source for the AI Sample Clock. You can also specify whether the measurement sample begins on the rising or falling edge of the AI Sample Clock pulse.

Using an Internal Source

One of the following internal signals can drive the AI Sample Clock:

- AI Sample Clock Timebase (divided down).
- A pulse initiated by host software that does a software, *on demand,* acquisition.

A programmable internal counter divides down the AI Sample Clock Timebase to generate the AI Sample Clock. The output of the counter is called the Onboard Clock signal. Onboard Clock is the default sample clock source for hardware-timed acquisitions unless you specify an external source.

Several other internal signals can be routed to the AI Sample Clock Signal through internal routes. Refer to *Device Routing in MAX* in the *NI-DAQmx Help* or the *LabVIEW Help* for more information.

Using an External Source

One of the following external signals can be used as the source of AI Sample Clock:

- PFI <0,1>
- PXI_Trig <0..7>
- PXI_STAR
- PXIe_DSTAR <A,B>

Routing AI Sample Clock Signal to an Output Terminal

You can route AI Sample Clock out to any PXI_Trig <0..7>, or PXIe_DSTARC terminal. The output terminal signal pulses for each AI Sample Clock, with the rising edge of each pulse coincident with the start of the ADC conversion. The active edge of this output pulse cannot be changed.

All PFI terminals are inputs only, and cannot be used to export the AI Sample Clock.

AI Sample Clock Timebase Signal

The AI Sample Clock Timebase (ai/SampleClockTimebase) signal is divided down to provide a source for the AI Sample Clock.

You can route any of the following signals to be the AI Sample Clock Timebase signal:

- 100 MHz Timebase (default)
- 20 MHz Timebase
- 100 kHz Timebase
- PXI_CLK10
- PXI_Trig <0..7>
- PFI <0,1>
- PXI_STAR
- PXIe_DSTAR <A, B>

AI Sample Clock Timebase is not available as an output on the I/O connector.

You might use the AI Sample Clock Timebase if you want to use an external clock signal, but need to divide the signal down. If you want to use an external sample clock signal, but do not need to divide the signal, you should use AI Sample Clock rather than AI Sample Clock Timebase.

You might also use the AI Sample Clock Timebase if you want to synchronize multiple measurement devices by locking to a shared clock. For more information, refer to the *Synchronizing Multiple Devices* section.

You can configure the polarity selection for AI Sample Clock Timebase as either rising or falling edge, except on 100 MHz Timebase or 20 MHz Timebase.

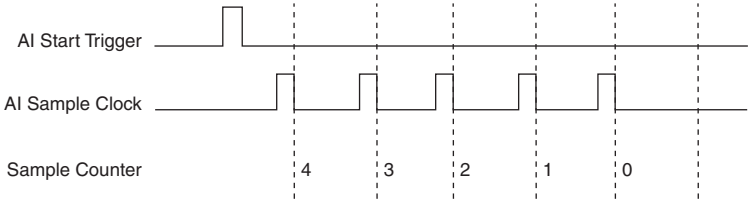
AI Start Trigger Signal

You can use the AI Start Trigger (ai/StartTrigger) signal to begin a measurement acquisition. If you do not use triggers, begin a measurement with a software command by starting a task, which creates a software generated pulse to start the acquisition. Once the acquisition begins, configure the acquisition to stop:

- When a certain number of points are sampled (in finite mode)
- After a hardware reference trigger (in finite mode)
- With a software command (in continuous mode)

An acquisition that uses a start trigger (but not a reference trigger) is sometimes referred to as a posttriggered acquisition. An acquisition with posttrigger data allows you to view data that is acquired after a trigger event is received. A typical posttrigger DAQ sequence is shown in Figure 3-2. The sample counter is loaded with the specified number of posttrigger samples, in this example, five. The value decrements with each pulse on AI Sample Clock, until the value reaches zero and all desired samples have been acquired.

Figure 3-2. Typical Posttriggered DAQ Sequence



Your DAQ device only acquires data after a start trigger pulse. The device ignores AI Sample Clock if a start trigger pulse has not occurred.

In place of a software generated pulse, you can use any of the following digital signals as the AI Start Trigger Source:

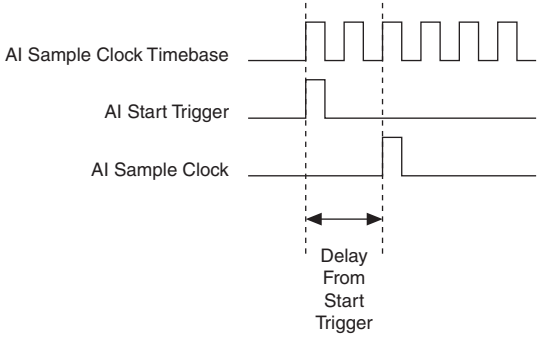
- PFI <0,1>
- PXI_Trig <0..7>
- PXI_STAR
- PXIe_STAR <A,B>

The source can also be one of several other internal signals on your device. Refer to *Device Routing in MAX* in the *NI-DAQmx Help* or the *LabVIEW Help* for more information.

You can also specify whether the measurement acquisition begins on the rising edge or falling edge of AI Start Trigger.

When using an internally generated AI Sample Clock, you can specify a configurable delay from the AI Start Trigger pulse to the first AI Sample Clock pulse. By default, this delay is set to two ticks of the AI Sample Clock Timebase signal. Figure 3-3 shows the relationship of AI Sample Clock to AI Start Trigger.

Figure 3-3. AI Sample Clock and AI Start Trigger



Routing AI Start Trigger to an Output Terminal

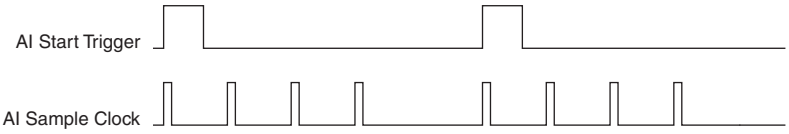
You can route AI Start Trigger out to and PXI_TRIG <0..7> or PXIe_DSTARC terminal. The output is an active high pulse. All PFI terminals are inputs only, and cannot be used to export AI Start Trigger.

Retriggerable Analog Input

To use a digital source as the AI Reference Trigger, the AI Start Trigger can also be configured to be retriggerable. The timing engine will generate the AI Sample Clock for the configured acquisition in response to each pulse on an AI Start Trigger signal.

The timing engine ignores the AI Start Trigger signal while the clock generation is in progress. After the clock generation is finished, the counter waits for another Start Trigger to begin another clock generation. Figure 3-4 shows a retriggerable analog input with four samples per trigger.

Figure 3-4. Retriggerable Analog Input



Note Waveform information from LabVIEW will not reflect the delay between triggers. They will be treated as a continuous acquisition with constant t0 and dt information.

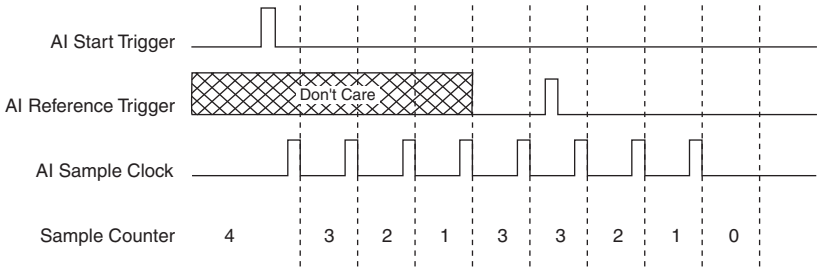
Reference triggers are retriggerable.

AI Reference Trigger Signal

A reference trigger can be used to acquire samples before and after a trigger event. This type of acquisition is sometimes referred to as a pretriggered acquisition. An acquisition with pretrigger data allows you to view data that is acquired before the trigger of interest, in addition to data acquired after the trigger. The trigger of interest that transitions the device from taking pretrigger data to taking posttrigger data is the AI Reference Trigger (ai/ReferenceTrigger) signal.

Figure 3-5 shows a typical pretriggered DAQ sequence. In the sequence, when the AI Start Trigger pulse occurs, the sample counter is loaded with the number of pretrigger samples, which is four in this example. The value decrements with each pulse on AI Sample Clock, until the value reaches zero. The sample counter is then immediately loaded with the number of posttrigger samples, which is three in this example. The sample counter for posttrigger samples does not start decrementing until the AI Reference Trigger pulse has occurred.

Figure 3-5. Typical Pretriggered DAQ Sequence



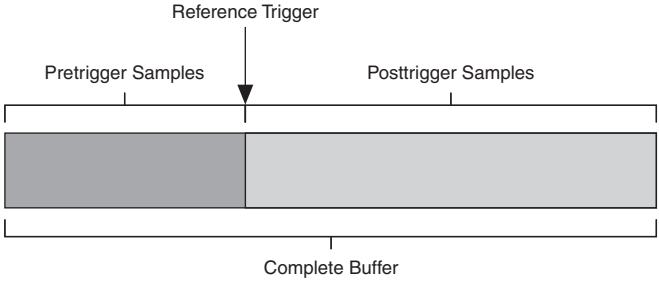
To take a pretriggered acquisition, specify a buffer of finite size and a number of pretrigger samples (samples that occur before the reference trigger). The number of posttrigger samples (samples that occur after the reference trigger) desired is the buffer size minus the number of pretrigger samples.

If an AI Reference Trigger pulse occurs before the specified number of pretrigger samples are acquired, the trigger pulse is ignored. Otherwise, after the AI Reference Trigger pulse occurs, the sample value decrements with each pulse on AI Sample Clock until the specified number of posttrigger samples have been acquired.

Once the acquisition begins, the DAQ device writes samples to the buffer. After the DAQ device captures the specified number of pretrigger samples, the DAQ device begins to look for the reference trigger condition. If the reference trigger condition occurs before the DAQ device captures the specified number of pretrigger samples, the DAQ device ignores the condition.

If the buffer becomes full, the DAQ device continuously discards the oldest samples in the buffer to make space for the next sample. This data can be accessed (with some limitations) before the DAQ device discards it. For more information, go to `ni.com/info` and enter the Info Code `rdcanq`. When the reference trigger occurs, the DAQ device continues to write samples to the buffer until the buffer contains the number of posttrigger samples desired. Figure 3-6 shows the final buffer.

Figure 3-6. Referenced Trigger Final Buffer



Using a Digital Source

To use a digital source as the AI Reference Trigger, specify a source and an edge. The source can be any of the following signals:

- PFI <0, 1>
- PXI_Trig <0..7>
- PXI_STAR
- PXIe_DSTAR <A, B>

The source can also be one of several internal signals on your DAQ device. Refer to *Device Routing in MAX* in the *NI-DAQmx Help* or the *LabVIEW Help* for more information.

You can specify whether the measurement acquisition begins taking posttrigger samples on the rising edge or falling edge of AI Reference Trigger.

Using an Analog Source

When you use an analog trigger source, the acquisition begins taking posttrigger samples on the rising edge of the Analog Comparison Event signal. For more information, refer to the *Triggering* section.

Routing AI Reference Trigger to an Output Terminal

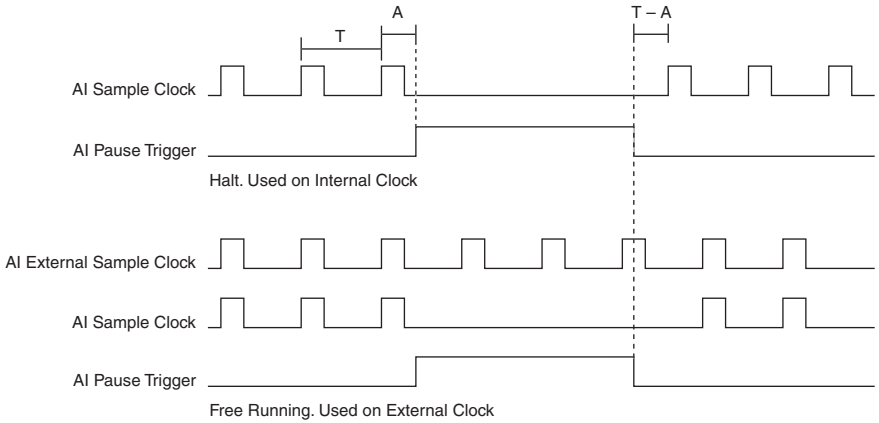
You can route the AI Reference Trigger signal to an PXI_TRIG <0..7> or PXIe_DSTARC terminal.

All PFI terminals are inputs only and cannot be used to export the AI Reference Trigger.

AI Pause Trigger Signal

Use the AI Pause Trigger (ai/PauseTrigger) signal to pause and resume a measurement acquisition. When using the internal sample clock, the sample clock is halted while the pause trigger signal is active and resumes when the signal is inactive. When using an external free running sample clock, the AI Sample Clock edges are masked by the pause trigger. You can program the active level of the pause trigger to be high or low. Figure 3-7 shows an example of using the AI Pause Trigger with an internal or external sample clock. In Figure 3-7, T represents the period, and A represents the unknown time between the sample clock active edge and the pause trigger.

Figure 3-7. Halt (Internal Clock) and Free Running (External Clock)



Using a Digital Source

To use a digital source as the AI Reference Trigger, specify a source and an edge. The source can be any of the following signals:

- PFI <0, 1>
- PXI_Trig <0..7>
- PXI_STAR
- PXIe_DSTAR <A, B>

The source can also be one of several other internal signals on your DAQ device. Refer to *Device Routing in MAX* in the *NI-DAQmx Help* or the *LabVIEW Help* for more information.

Routing AI Pause Trigger Signal to an Output Terminal

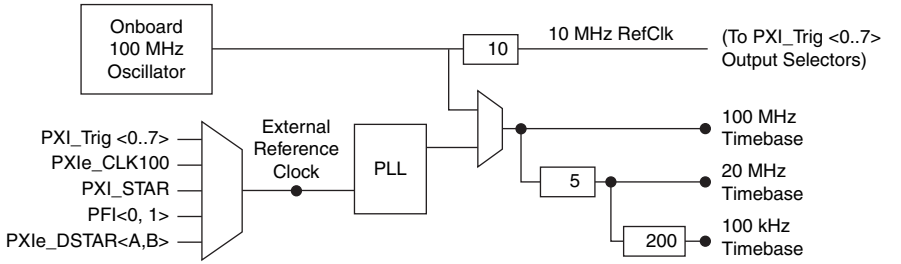
You can route the AI Pause Trigger out to any PXI_Trig <0..7>, PXI_STAR, or PXIe_DSTARC terminal.

Note Pause triggers are only sensitive to the level of the source, not the edge.

Clock Generation and Routing

The clock generation and routing circuity creates the main timing signals for your PXIe-4310 module. All internally generated analog input timing signals are derived from these main timing signals. The clock generation and routing subsystem also allows you to synchronize the clocking of multiple measurement devices in a PXI Express chassis. Figure 3-8 summarizes the functions of the clock generation and routing subsystem.

Figure 3-8. External Clock Reference



Reference Clock

The clock generation subsystem uses either an internal or external source as the reference clock to generate timing signals. The only internal source for the reference clock is the onboard 100 MHz oscillator. An external reference clock can be sourced using the signals shown in Table 3-2.

Table 3-2. Clock Signal Sourcing

Signal	Description
PXI_Trig<0..7>	Bidirectional bus connecting each board in a chassis.
PFI<0,1>	External user input.
PXIe_Clk100	100 MHz clock routed to all slots in the chassis.
PXI_STAR	Point-to-point route from the System Timing Slot to all other slots.
PXIe_DSTAR<A, B>	Point-to-point differential routes from the System Timing Slot to all other slots.

Since the external reference clock is the input of a PLL, it must be 5 MHz, 10 MHz, 20 MHz, or 100 MHz. The PLL locks to the external reference clock and produces a 100 MHz output.

Caution Do not disconnect an external clock once the modules have been synchronized or are used by a task. Doing so may cause NI-DAQmx to return an error. Make sure that all tasks using a reference clock are stopped before disconnecting it.

The 100 MHz reference clock is used to generate the 100 MHz timebase, 20 MHz timebase, and 100 kHz timebase, which can be used as the AI Sample Clock timebase.

10 MHz RefClk

The 10 MHz reference clock is generated by dividing down the onboard 100 MHz oscillator. The 10 MHz RefClk can be used to synchronize other devices to the PXIe-4310 module. The 10 MHz RefClk can be routed to the PXI_Trig <0..7> terminals. Other devices connected to the PXI_Trig bus can use this signal as a clock input.

PXI Express Clock and Trigger Signals

PXIe_CLK100

PXIe_CLK100 is a common, low-skew 100 MHz reference clock used for synchronization of multiple modules in a PXI Express measurement or control system. The PXI Express backplane is responsible for generating PXIe_CLK100 independently to each peripheral slot in a PXI Express chassis. For more information, refer to the *PXI Express Specification* at `www.pxisa.org`.

PXIe_SYNC100

PXIe_SYNC100 is a common, low-skew 10 MHz reference clock with a 10% duty cycle for synchronization of multiple modules in a PXI Express measurement or control system. The PXI Express backplane is responsible for generating PXIe_SYNC100 independently to each peripheral slot in a PXI Express chassis. PXIe_SYNC100 allows modules using PXIe_CLK100 as their reference to recreate the timing of the PXI_CLK10 signal while taking advantage of the lower skew of PXIe_CLK100. For more information, refer to the *PXI Express Specification* at `www.pxisa.org`.

PXI_CLK10

PXI_CLK10 is a common, low-skew 10 MHz reference clock for synchronization of multiple modules in a PXI measurement or control system. The PXI backplane is responsible for generating PXI_CLK10 independently to each peripheral slot in a PXI chassis. In PXI Express chassis, the PXI_CLK10 signal is in phase with PXIe_CLK100.

Note PXI_CLK10 cannot be used as a reference clock for SC Express modules.

PXI Triggers

A PXI/PXI Express chassis provides eight bused trigger lines to each module in a system. Triggers may be passed from one module to another, allowing precisely timed responses to asynchronous external events that are being monitored or controlled. Triggers can be used to synchronize the operation of several different PXI peripheral modules.

In a PXI chassis with more than eight slots, the PXI trigger lines may be divided into multiple independent buses. Refer to the documentation for your chassis for details.

PXI_STAR Trigger

In a PXI Express system, the Star Trigger bus implements a dedicated trigger line between the system timing slot and the other peripheral slots. The Star Trigger can be used to synchronize multiple modules or to share a common trigger signal among modules.

A system timing controller can be installed in the system timing slot to provide trigger signals to other peripheral modules. Systems that do not require this functionality can install any standard peripheral module in this system timing slot.

An SC Express module receives the Star Trigger signal (PXI_STAR) from a System timing controller. PXI_STAR can be used as a trigger signal for input operations.

An SC Express module is not a system timing controller. An SC Express module can be used in the system timing slot of a PXI system, but the system will not be able to use the Star Trigger feature.

PXIe_DSTAR<A..C>

PXI Express devices can provide high-quality and high-frequency point-to-point connections between each slot and a system timing slot. These connections come in the form of three low-voltage differential star triggers that route between a PXI Express system timing controller and a peripheral device. Using multiple connections simplifies the creation of applications because of the increased routing capabilities.

Table 3-3 describes the three differential star (DSTAR) lines and how they are used.

Table 3-3. PXIe_DSTAR Line Descriptions

Trigger Line	Purpose
PXIe_DSTARA	Distributes high-speed, high-quality clock signals from the system timing slot to the peripherals (input).
PXIe_DSTARB	Distributes high-speed, high-quality trigger signals from the system timing slot to the peripherals (input).
PXIe_DSTARC	Sends high-speed, high-quality trigger or clock signals from the peripherals to the system timing slot (output).

The DSTAR lines are only available for PXI Express devices when used with a PXI Express system timing module. For more information, refer to the *PXI Express Specification* at `www.pxisa.org`.

Synchronizing Multiple Devices

On PXI Express systems, you can synchronize devices to PXIe_CLK100. In this application the PXI Express chassis acts as the master timing source. Each PXI Express module uses PXIe_CLK100 as its reference clock. Adding channels from multiple modules to the same NI-DAQmx task will perform synchronization automatically.

Another option in PXI Express systems is to use PXI_STAR. The Star Trigger controller device acts as the master timing source and drives PXI_STAR with a clock signal. Each target module uses PXI_STAR as its external reference clock.

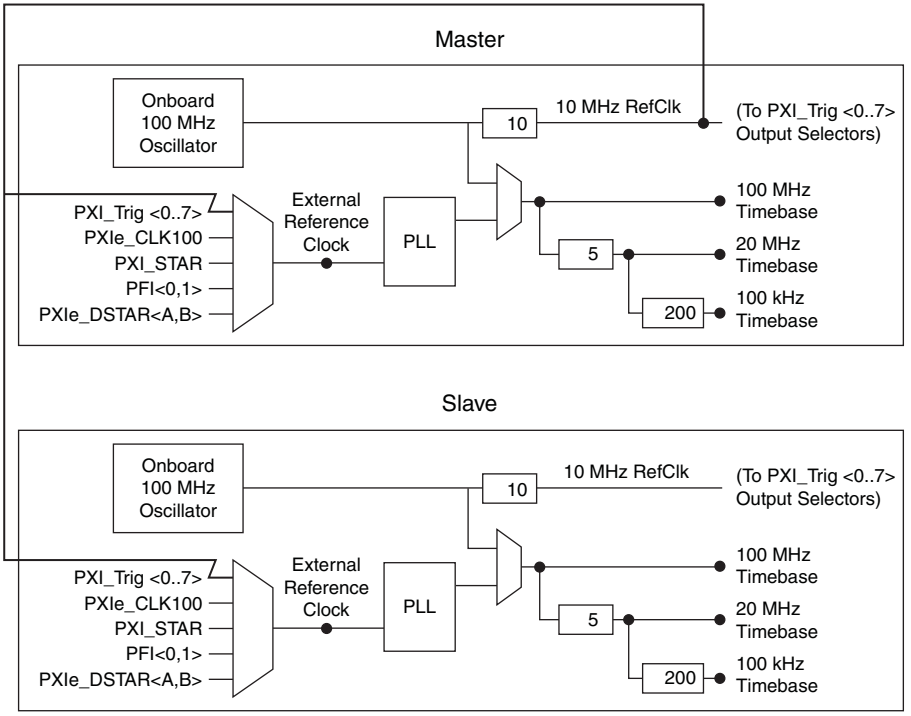
Another option in PXI Express Systems is to use PXI_Trig <0..7>. Choose one module to be the master timebase. The master module routes its 10 MHz RefClk to one of the PXI_Trig <0..7> signals. All modules (including the master module) then use the 10 MHz RefClk as an external reference clock source.

Sharing a trigger between multiple devices using PXI trigger lines introduces skew in the trigger signal, due to the propagation delay of the signal. The PXIe-4310 can compensate for that skew by locking the trigger to a clock (PXIe_SYNC100) that is derived from the reference clock (PXIe_CLK100). When you lock triggers to a clock, the device responds to those triggers on a subsequent edge of that clock, rather than immediately. Therefore, skew correction results in increased latency.

When you add multiple PXIe-4310 modules to the same NI-DAQmx task, NI-DAQmx automatically enables trigger skew correction. To enable trigger skew correction for applications that use multiple NI-DAQmx tasks, specify which device is the master and which devices are the slaves using the **SyncType** DAQmx Trigger property.

Once all of the devices are using or referencing a common timebase, you can synchronize operations across them by sending a common start trigger out across the PXI_Trig bus and setting their sample clock rates to the same value as shown in Figure 3-9.

Figure 3-9. Synchronization Operation



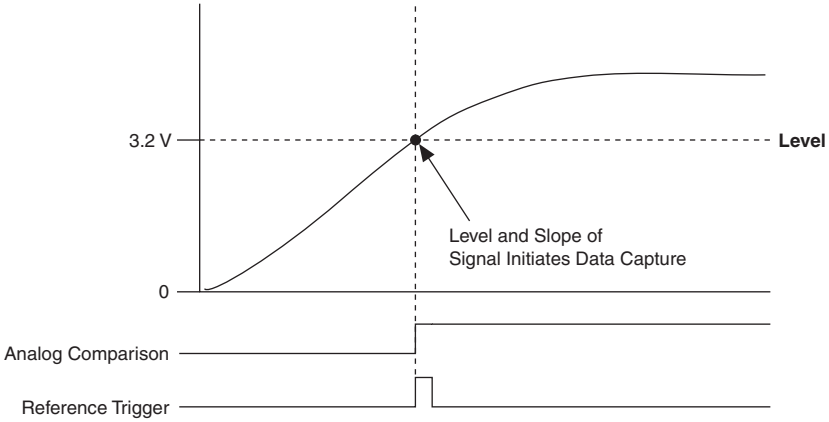
Triggering

The following sections provide details about analog and digital triggering of the PXIe-4310 module.

Analog Edge Triggering

For analog edge triggering, configure the device to detect a certain signal level and slope, either rising or falling. Figure 3-10 shows an example of rising edge analog triggering. The trigger asserts when the signal starts below level and then crosses above level.

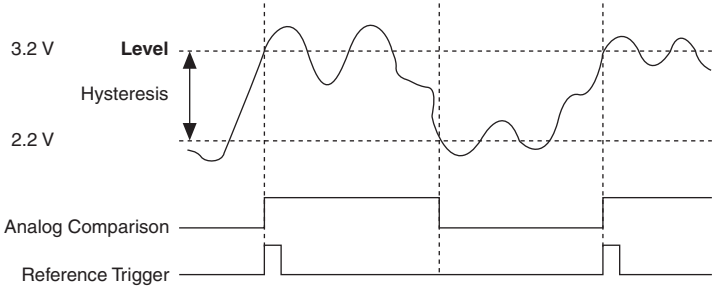
Figure 3-10. Analog Trigger Level



Analog Edge Triggering With Hysteresis

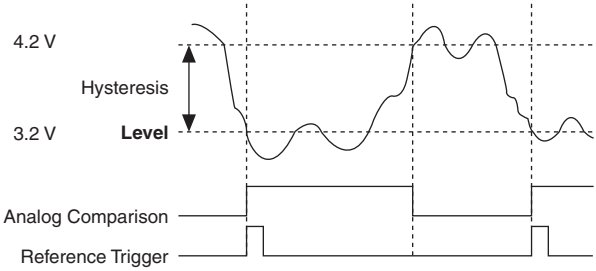
When you add hysteresis to analog edge triggering, you add a window above or below the trigger level. This trigger often is used to reduce false triggering due to noise or jitter in the signal. For example, if you add a hysteresis of 1 V to the example in Figure 3-11, which uses a level of 3.2 V, the signal must start at or drop below 2.2 V to arm the trigger. The trigger asserts when the signal rises above 3.2 V and deasserts when it falls below 2.2 V, as shown in Figure 3-11.

Figure 3-11. Analog Edge Triggering with Hysteresis on Rising Slope



When using hysteresis with a falling slope, the trigger is armed when the signal starts above Level, plus the hysteresis value, and asserts when the signal crosses below Level. For example, if you add a hysteresis of 1 V to a level of 3.2 V, the signal must start at or rise above 4.2 V to arm the trigger. The trigger asserts as the signal falls below 3.2 V and deasserts when it rises above 4.2 V, as shown in Figure 3-12.

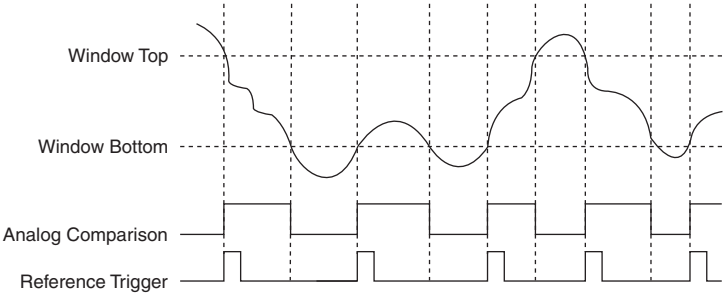
Figure 3-12. Analog Edge Triggering with Hysteresis on Falling Slope



Window Triggering

A window trigger occurs when an analog signal either passes into (enters) or passes out of (leaves) a window defined by two levels. Specify the levels by setting a value for the top and bottom window boundaries. Figure 3-13 demonstrates a trigger that acquires data when the signal enters the window. You can also program the trigger circuit to acquire data when the signal leaves the window.

Figure 3-13. Window Triggering



Digital Input Triggering

You can configure the PXIe-4310 device to start or pause an acquisition in response to a digital trigger signal from either PFI <0, 1>, PXIe_DSTAR <A, B>, PXI_Trig <0..7>, or PXI_STAR. The trigger circuit can respond to a rising, falling, or level sensitive signal, in one of the following three modes:

- Start—Begins an acquisition when trigger is met.
- Reference—A certain number of pre-trigger and post-trigger samples are specified around the trigger.
- Pause—Acquisition is put on hold when trigger is met (level sensitive only).

In addition, the trigger circuit provides a programmable filter to help with noisy trigger signals. The filter checks that the trigger condition is met for different time intervals before triggering. The filter can select from 90 ns, 5.12 µs, 2.56 ms, or a custom defined time interval. For information about configuring digital filters, refer to the *NI-DAQmx Help*.

4

Accessories

This section describes the accessories available for the PXIe-4310 module.

TB-4310 (10V)/TB-4310 (600V) Accessory

The TB-4310 (10V)/TB-4300 (600V) terminal blocks provide screw terminal connectivity for the PXIe-4310. The TB-4310 (600V) provides 60x attenuation to the input signal voltage to expand the input range of the PXIe-4310 to 600V.

- The TB-4310 (10V) is strictly a voltage feedthrough terminal block.
- The TB-4310 (600V) provides 60x attenuation to the voltage with additional high-voltage protection circuitry and expands the range of the PXIe-4310 to 600 V.

Refer to the *PXIe-4310 and TB-4310 (10V)/TB-4310 (600V) Getting Started Guide and Terminal Block Specifications* for more information about the TB-4310 (10V)/TB-4310 (600V) terminal block accessories.

Scaling constants for the TB-4310 (600V) are stored in the EEPROM and are used by the software to automatically apply scaling to the signal for the selected range.

Accessory Auto-Detection

SC Express modules automatically detect compatible accessories or terminal blocks. The RSVD pins on the I/O connector provide power to the accessories as well as digital communication lines. This allows software to detect when accessories are inserted or removed. In addition, software can automatically identify the specific terminal block as well as access any calibration or scaling information associated with the terminal block.

MAX allows you to see which accessories are currently connected to your module. In MAX, expand **Devices and Interfaces** and locate your module. If a terminal block is connected to your module, it will be displayed beneath the module. Unsupported terminal blocks appear in MAX with an X next to them.

NI-DAQmx property nodes can be used to programmatically access information about connected accessories in your application. Refer to the *NI-DAQmx Help* for documentation about programmatically accessing accessory status.

Accessory Power

The PXIe-4310 provides auxiliary power for accessories connected to the module and has protection in the event of a fault condition. If a fault occurs in the form of an over-power condition, the power supply latches off until it is reset. To reset after a fault condition perform a Device Reset in MAX or programmatically in your Application Development Environment (ADE).

A

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  - **Calibration**—Through regular calibration, you can quantify and improve the measurement performance of an instrument. NI provides state-of-the-art calibration services. If your product supports calibration, you can obtain the calibration certificate for your product at ni.com/calibration.
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  - The Skills Guide assists you in identifying the proficiency requirements of your current application and gives you options for obtaining those skills consistent with your time and budget constraints and personal learning preferences. Visit ni.com/skills-guide to see these custom paths.
  - NI offers courses in several languages and formats including instructor-led classes at facilities worldwide, courses on-site at your facility, and online courses to serve your individual needs.
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  - **Software Support Service Membership**—The Standard Service Program (SSP) is a renewable one-year subscription included with almost every NI software product, including NI Developer Suite. This program entitles members to direct access to NI Applications Engineers through phone and email for one-to-one technical support, as well as exclusive access to online training modules at ni.com/self-paced-training. NI also offers flexible extended contract options that guarantee your SSP benefits are available without interruption for as long as you need them. Visit ni.com/ssp for more information.
- **Declaration of Conformity (DoC)**—A DoC is our claim of compliance with the Council of the European Communities using the manufacturer's declaration of conformity. This system affords the user protection for electromagnetic compatibility (EMC) and product safety. You can obtain the DoC for your product by visiting ni.com/certification.

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