COMPREHENSIVE SERVICES

We offer competitive repair and calibration services, as well as easily accessible documentation and free downloadable resources.

SELL YOUR SURPLUS

We buy new, used, decommissioned, and surplus parts from every NI series. We work out the best solution to suit your individual needs.

Sell For Cash Get Credit Receive a Trade-In Deal

OBSOLETE NI HARDWARE IN STOCK & READY TO SHIP

We stock **New, New Surplus, Refurbished,** and **Reconditioned** NI Hardware.

APEX WAVES

Bridging the gap *between the manufacturer and your legacy test system.*

1-800-915-6216

www.apexwaves.com

sales@apexwaves.com

Request a Quote CLICK HERE *PXIe-4340*

SC Express

NI PXIe-4340 User Manual

4 Ch, 24-bit, 25.6 kS/s Simultaneous AC LVDT Input Module

May 2016
377014A-01

NATIONAL INSTRUMENTS™

Worldwide Technical Support and Product Information

ni.com

Worldwide Offices

Visit ni.com/niglobal to access the branch office websites, which provide up-to-date contact information, support phone numbers, email addresses, and current events.

National Instruments Corporate Headquarters

11500 North Mopac Expressway Austin, Texas 78759-3504 USA

Tel: 866 ASK MYNI (275 6964)

For further support information, refer to the *NI Services* appendix. To comment on National Instruments documentation, refer to the National Instruments website at ni.com/info and enter the Info Code feedback.

Legal Information

Limited Warranty

This document is provided ‘as is’ and is subject to being changed, without notice, in future editions. For the latest version, refer to `ni.com/manuals`. NI reviews this document carefully for technical accuracy; however, NI MAKES NO EXPRESS OR IMPLIED WARRANTIES AS TO THE ACCURACY OF THE INFORMATION CONTAINED HEREIN AND SHALL NOT BE LIABLE FOR ANY ERRORS.

NI warrants that its hardware products will be free of defects in materials and workmanship that cause the product to fail to substantially conform to the applicable NI published specifications for one (1) year from the date of invoice.

For a period of ninety (90) days from the date of invoice, NI warrants that (i) its software products will perform substantially in accordance with the applicable documentation provided with the software and (ii) the software media will be free from defects in materials and workmanship.

If NI receives notice of a defect or non-conformance during the applicable warranty period, NI will, in its discretion: (i) repair or replace the affected product, or (ii) refund the fees paid for the affected product. Repaired or replaced Hardware will be warranted for the remainder of the original warranty period or ninety (90) days, whichever is longer. If NI elects to repair or replace the product, NI may use new or refurbished parts or products that are equivalent to new in performance and reliability and are at least functionally equivalent to the original part or product.

You must obtain an RMA number from NI before returning any product to NI. NI reserves the right to charge a fee for examining and testing Hardware not covered by the Limited Warranty.

This Limited Warranty does not apply if the defect of the product resulted from improper or inadequate maintenance, installation, repair, or calibration (performed by a party other than NI); unauthorized modification; improper environment; use of an improper hardware or software key; improper use or operation outside of the specification for the product; improper voltages; accident, abuse, or neglect; or a hazard such as lightning, flood, or other act of nature.

THE REMEDIES SET FORTH ABOVE ARE EXCLUSIVE AND THE CUSTOMER’S SOLE REMEDIES, AND SHALL APPLY EVEN IF SUCH REMEDIES FAIL OF THEIR ESSENTIAL PURPOSE.

EXCEPT AS EXPRESSLY SET FORTH HEREIN, PRODUCTS ARE PROVIDED "AS IS" WITHOUT WARRANTY OF ANY KIND AND NI DISCLAIMS ALL WARRANTIES, EXPRESSED OR IMPLIED, WITH RESPECT TO THE PRODUCTS, INCLUDING ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, TITLE OR NON-INFRINGEMENT, AND ANY WARRANTIES THAT MAY ARISE FROM USAGE OF TRADE OR COURSE OF DEALING. NI DOES NOT WARRANT, GUARANTEE, OR MAKE ANY REPRESENTATIONS REGARDING THE USE OF OR THE RESULTS OF THE USE OF THE PRODUCTS IN TERMS OF CORRECTNESS, ACCURACY, RELIABILITY, OR OTHERWISE. NI DOES NOT WARRANT THAT THE OPERATION OF THE PRODUCTS WILL BE UNINTERRUPTED OR ERROR FREE.

In the event that you and NI have a separate signed written agreement with warranty terms covering the products, then the warranty terms in the separate agreement shall control.

Copyright

End-User License Agreements and Third-Party Legal Notices

You can find end-user license agreements (EULAs) and third-party legal notices in the following locations:

- Notices are located in the `<National Instruments>\_Legal Information` and `<National Instruments>` directories.
- EULAs are located in the `<National Instruments>\Shared\MDF\Legal\license` directory.
- Review `<National Instruments>\_Legal Information.txt` for information on including legal information in installers built with NI products.

U.S. Government Restricted Rights

If you are an agency, department, or other entity of the United States Government (“Government”), the use, duplication, reproduction, release, modification, disclosure or transfer of the technical data included in this manual is governed by the Restricted Rights provisions under Federal Acquisition Regulation 52.227-14 for civilian agencies and Defense Federal Acquisition Regulation Supplement Section 252.227-7014 and 252.227-7015 for military agencies.

Trademarks

Refer to the *NI Trademarks and Logo Guidelines* at `ni.com/trademarks` for more information on National Instruments trademarks.

ARM, Keil, and µVision are trademarks or registered of ARM Ltd or its subsidiaries.

LEGO, the LEGO logo, WEDO, and MINDSTORMS are trademarks of the LEGO Group.

TETRIX by Pitsco is a trademark of Pitsco, Inc.

FIELDBUS FOUNDATION™ and FOUNDATION™ are trademarks of the Fieldbus Foundation.

Patents

For patents covering National Instruments products/technology, refer to the appropriate location: **Help»Patents** in your software, the patents.txt file on your media, or the *National Instruments Patent Notice* at ni.com/patents.

Export Compliance Information

Refer to the *Export Compliance Information* at ni.com/legal/export-compliance for the National Instruments global trade compliance policy and how to obtain relevant HTS codes, ECCNs, and other import/export data.

WARNING REGARDING USE OF NATIONAL INSTRUMENTS PRODUCTS

YOU ARE ULTIMATELY RESPONSIBLE FOR VERIFYING AND VALIDATING THE SUITABILITY AND RELIABILITY OF THE PRODUCTS WHENEVER THE PRODUCTS ARE INCORPORATED IN YOUR SYSTEM OR APPLICATION, INCLUDING THE APPROPRIATE DESIGN, PROCESS, AND SAFETY LEVEL OF SUCH SYSTEM OR APPLICATION.

PRODUCTS ARE NOT DESIGNED, MANUFACTURED, OR TESTED FOR USE IN LIFE OR SAFETY CRITICAL SYSTEMS, HAZARDOUS ENVIRONMENTS OR ANY OTHER ENVIRONMENTS REQUIRING FAIL-SAFE PERFORMANCE, INCLUDING IN THE OPERATION OF NUCLEAR FACILITIES; AIRCRAFT NAVIGATION; AIR TRAFFIC CONTROL SYSTEMS; LIFE SAVING OR LIFE SUSTAINING SYSTEMS OR SUCH OTHER MEDICAL DEVICES; OR ANY OTHER APPLICATION IN WHICH THE FAILURE OF THE PRODUCT OR SERVICE COULD LEAD TO DEATH, PERSONAL INJURY, SEVERE PROPERTY DAMAGE OR ENVIRONMENTAL HARM (COLLECTIVELY, “HIGH-RISK USES”). FURTHER, PRUDENT STEPS MUST BE TAKEN TO PROTECT AGAINST FAILURES, INCLUDING PROVIDING BACK-UP AND SHUT-DOWN MECHANISMS. NI EXPRESSLY DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY OF FITNESS OF THE PRODUCTS OR SERVICES FOR HIGH-RISK USES.

Contents

Chapter 1
Getting Started

Chapter 2
Using the Module

Chapter 3
SC Express Considerations

Appendix A
NI Services

Figures

Tables

1 Getting Started

The NI PXIe-4340 provides four simultaneously sampled AC LVDT input channels. The PXIe-4340 can operate at sample rates up to 25.6 kS/s/ch. Each channel has a 24-bit ADC and independently selectable excitation frequency and voltage.

Installation

Refer to the *NI PXIe-4340 and TB-4340 User Guide and Terminal Block Specifications* document for step-by-step software and hardware installation instructions.

Note For a complete list of terminal blocks supported by a specific release of NI-DAQmx, refer to the *NI-DAQmx Readme*, available on the version-specific download page or installation media.

Module Specifications

Refer to the *NI PXIe-4340 Device Specifications* document for module specifications.

Module Accessories

Refer to ni.com/scexpress for information about and a complete listing of supported accessories.

2

Using the Module

This chapter describes how to connect LVDT, RVDT, resolver, and synchro signals to the PXIe-4340. It also provides the I/O connector signal pin assignments of the module.

Driver support for the PXIe-4340 was first available in NI-DAQmx 15.5. For the list of devices supported by a specific release, refer to the *NI-DAQmx Readme*, available on the version-specific download page or installation media.

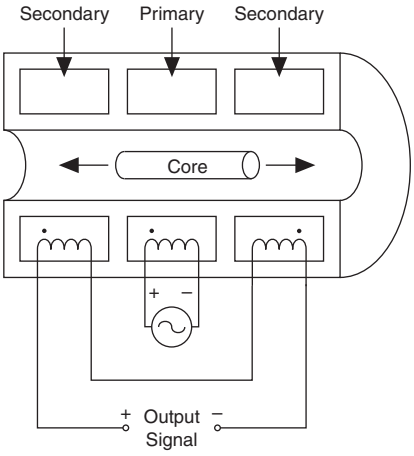
Caution To ensure the specified EMC performance, operate this product only with shielded cables and shielded accessories. Use only twisted, shielded pair cables for channel connections.

Caution To ensure the specified EMC performance, the length of all I/O cables must be no longer than 30 m (100 ft.).

LVDTs, RVDTs, Resolvers, and Synchros

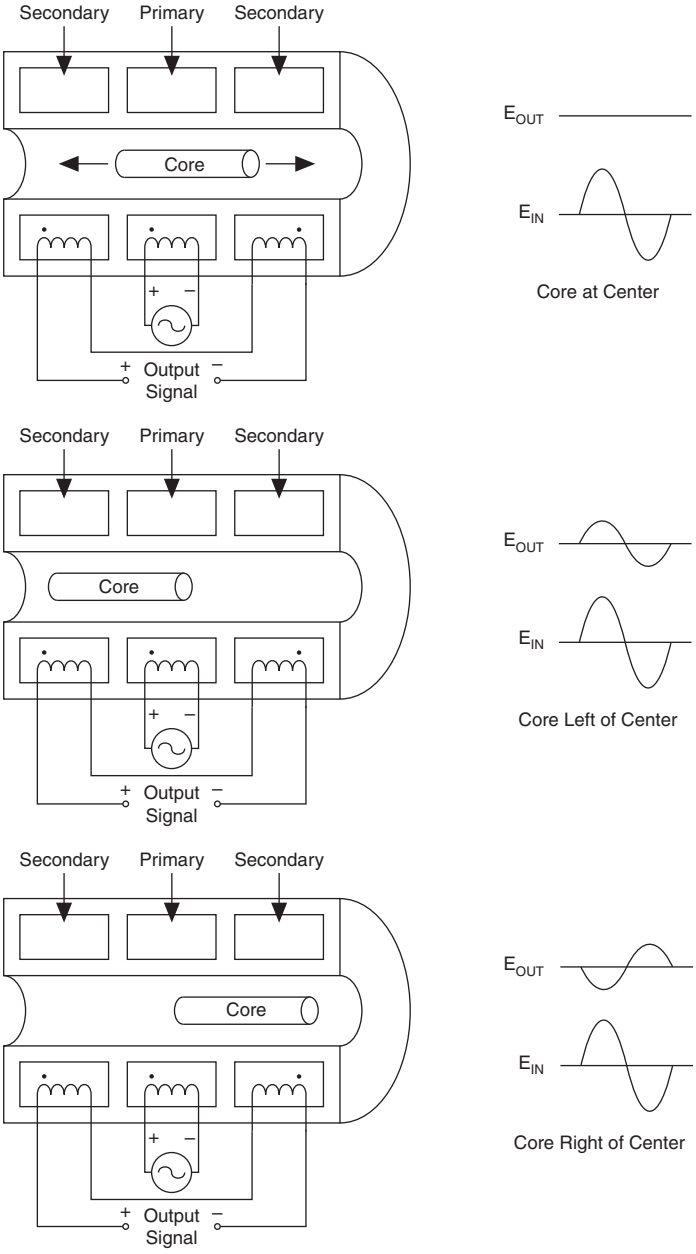
An LVDT is a device for measuring linear position. Figure 2-1 shows a cut-away view of an LVDT.

Figure 2-1. Cutaway View of an LVDT



The primary winding, located at center, is excited with a sine-wave voltage. The resulting magnetic field is coupled through the movable core into the secondary windings located on either side of the primary. With the core at center, both secondaries have the same induced voltage. With the series connection and polarity shown, the resulting output signal is zero. If the core moves to the left, the left secondary is more strongly coupled to the primary than the right secondary, resulting in a stronger induced voltage in the left secondary and an output signal that is in phase with the primary excitation voltage. The more the core moves off center, the stronger the imbalance and the greater the output signal. Moving the core to the right of center results in the same behavior, but with the output signal out of phase with the excitation signal. Figure 2-2 shows these core locations and the resulting induced voltage and phase.

Figure 2-2. LVDT Core Locations with Resulting Induced Voltage and Phase



LVDTs are frequently used in applications where ruggedness, operation over large temperature ranges, insensitivity to contamination, or long life are important considerations. They are extremely reliable in harsh conditions.

An RVDT is the rotational version of an LVDT. The angular measurement range of typical RVDTs is between ±30° and ±70°.

Resolvers are similar to RVDTs, but employ secondaries at right angles that produce two simultaneous signal voltages proportional to the sine and cosine of the shaft angle. Thus, resolvers can measure over 360° of rotation and do not need to pass through 0° before making absolute position measurements, as is required by quadrature encoders.

LVDTs, RVDTs, and resolvers are advantageous in hostile operating environments. Resolvers are often easier to use than RVDTs. All that is needed to convert measured voltages to degrees is an arctangent function; there are no scaling considerations.

Synchros function similarly to resolvers, but have three secondaries (stators) that produce three simultaneous signals proportional to the sine of the shaft position, each offset by 120°. Therefore, synchros can measure over 360° of rotation with a unique combination of stator voltages across the entire range.

Remote Sense

Remote sense continuously and automatically corrects for errors in excitation leads. Its use is most critical in applications that employ long wires and/or small gauge wires, as these have higher resistance. The resistance in the wires that connect the excitation voltage to the primary winding causes a voltage drop, which is a source of gain error. The PXIe-4340 includes remote sense to compensate for this gain error. Connect remote sense inputs of the PXIe-4340 to the excitation voltage wires of the sensor as close to the sensor as possible. Refer to Figures 2-3 through 2-7.

Due to the unique digital demodulation employed on the PXIe-4340, remote sense can also be used to sense the excitation of synchronized channels to measure accurate ratios across channels for sensors with multiple secondaries, such as resolvers and synchros. Refer to the *Connecting Resolver Signals* and *Connecting Synchro Signals* sections for more information.

Connecting LVDT and RVDT Signals

This section provides information regarding connecting LVDT and RVDT signals. Figures 2-3 through 2-5 show the connections made to a 4-, 5-, and 6-wire LVDT or RVDT using the PXIe-4340 with the TB-4340 terminal block.

Figure 2-3. 4-Wire Connection to an LVDT or RVDT

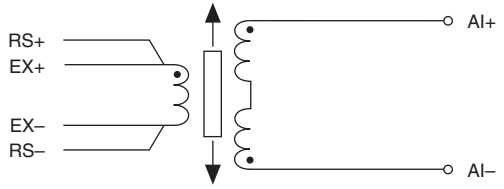


Figure 2-4. 5-Wire Connection to an LVDT or RVDT

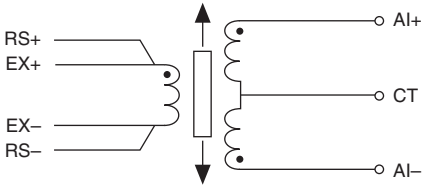
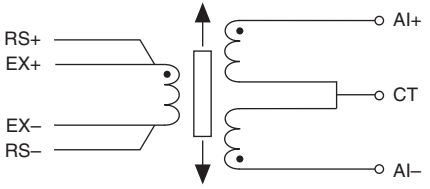


Figure 2-5. 6-Wire Connection to an LVDT or RVDT

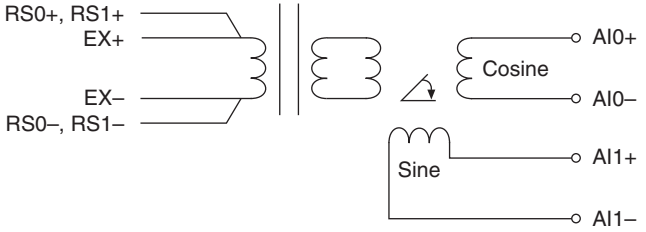


Note The PXIe-4340 does not require connection to the center tap of 5- and 6-wire LVDTs. For 5-wire sensors, NI recommends leaving your CT lead disconnected. For 6-wire sensors, NI recommends connecting the two CT leads only to each other. For wire management, you may choose to connect your CT leads to the floating CT terminal on the TB-4340.

Connecting Resolver Signals

This section provides information regarding connecting resolver signals. Figure 2-6 shows the connections made between a resolver and the PXIe-4340 using the TB-4340 terminal block. A single resolver requires the use of two synchronized channels. The excitation of either channel, but not both, can be used. Both channels must be configured for remote sense to guarantee accuracy.

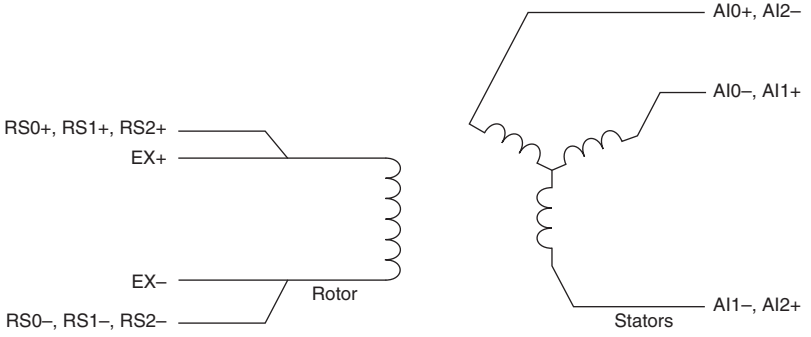
Figure 2-6. Resolver Connections



Connecting Synchro Signals

This section provides information regarding connecting synchro signals. Figure 2-7 shows the connections made between a synchro and the PXIe-4340 using the TB-4340 terminal block. A single synchro requires the use of three synchronized channels. The excitation of any one of the synchronized channels can be used, but all channels must be configured for remote sense to guarantee accuracy.

Figure 2-7. Synchro Connections



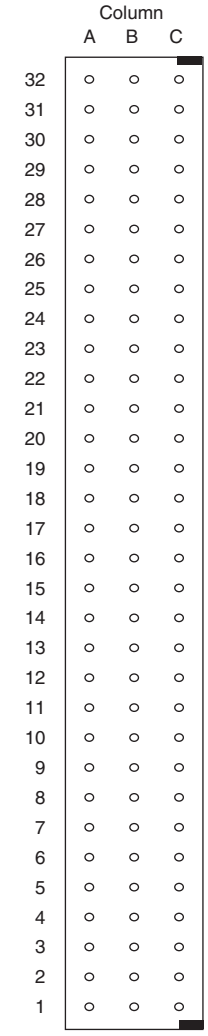
Self-Calibration

The PXIe-4340 can adjust its ratiometric gain and offset to cancel out the drift of the analog circuitry. In addition, self-calibration nulls the DC component of the excitation source and adjusts its amplitude against an internal reference. The PXIe-4340 does not support external adjustment.

Module Pinout

Table 2-1 shows the pinout of the front connector of the PXIe-4340. Refer to the *I/O Connector Signal Descriptions* section for definitions of each signal. Refer to the *NI PXIe-4340 and TB-4340 User Guide and Terminal Block Specifications* for signal locations on the terminal block.

Table 2-1. Front Connector Signal Pin Assignments

Front Connector Diagram	Row Number	Column A	Column B	Column C
	32	AIGND	EX0+	AI0+
	31	NC	EX0-	AI0-
	30	NC	RS0-	RS0+
	29	NC	NC	NC
	28	NC	NC	NC
	27	NC	NC	NC
	26	AIGND	EX1+	AI1+
	25	NC	EX1-	AI1-
	24	NC	RS1-	RS1+
	23	NC	NC	NC
	22	NC	NC	NC
	21	NC	NC	NC
	20	NC	NC	NC
	19	NC	NC	NC
	18	NC	NC	NC
	17	NC	NC	NC
	16	NC	NC	NC
	15	NC	NC	NC
	14	AIGND	EX2+	AI2+
	13	NC	EX2-	AI2-
	12	NC	RS2-	RS2+
	11	NC	NC	NC
	10	NC	NC	NC
	9	NC	NC	NC
	8	AIGND	EX3+	AI3+
	7	NC	EX3-	AI3-
	6	NC	RS3-	RS3+
	5	PFI0	NC	NC
	4	NC	NC	NC
	3	NC	NC	NC
RSVD is reserved NC is no connection	2	RSVD	DGND	RSVD
	1	RSVD	RSVD	RSVD

I/O Connector Signal Descriptions

Table 2-2 describes the signals found on the I/O connector.

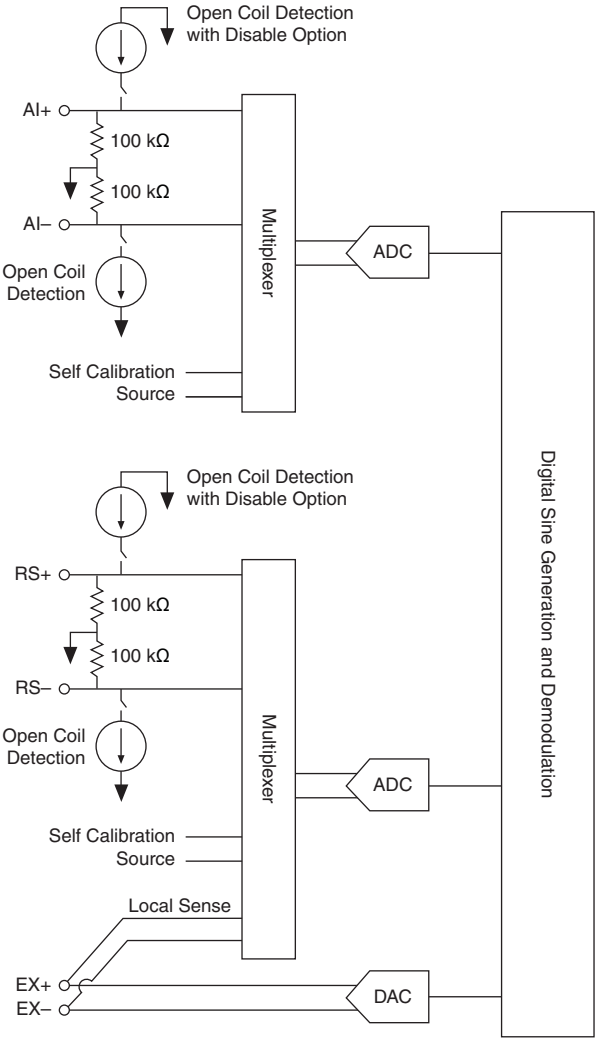
Table 2-2. I/O Connector Signal Descriptions

Signal Names	Direction	Description
AIGND	—	Analog Input Ground
AI<0..3>+	Input	Positive inputs of the differential analog input channels 0 to 3.
AI<0..3>-	Input	Negative inputs of the differential analog input channels 0 to 3.
EX<0..3>+	Output	Positive outputs of the differential excitation channels 0 to 3.
EX<0..3>-	Output	Negative outputs of the differential excitation channels 0 to 3.
RS<0..3>+	Input	Positive inputs of the remote sense input channels 0 to 3.
RS<0..3>-	Input	Negative inputs of the remote sense input channels 0 to 3.
RSVD	—	These pins are reserved for communication with the accessory.
DGND	—	Digital ground—this pin supplies the reference for module digital signals and is connected to the module digital ground.
PFI0	Input or Output	3.3 V digital signal for sending or receiving trigger and synchronization signals.

PXIe-4340 Block Diagram

Figure 2-8 shows the block diagram of the PXIe-4340. The analog signal conditioning for each channel consists of a lowpass filter for each input and remote sense channel. Each conditioned signal is then digitized by a dedicated 24-bit delta-sigma ADC to achieve simultaneous data acquisition. After the signal is digitized, it is demodulated before being sent to software.

Figure 2-8. PXIe-4340 Single-Channel Block Diagram



Open Coil Detection

When open coil detection is enabled, the PXIe-4340 turns on current sources in parallel to the AI and RS lines to sense open coils. If the lines become disconnected, the module detects the increase in voltage and reports this condition to software. The PXIe-4340 also senses the impedance connected to the excitation lines and reports a high-impedance connection to

software. This means that open coil detection will report open coils on the unused excitation lines with sensors that use multiple channels and one excitation, such as synchros and resolvers.

Overcurrent Detection

The PXIe-4340 is protected against overcurrents and overvoltages on the excitation terminals. If excessive current is detected at either of the excitation pins, a relay at the output disables the excitation for approximately one second. This prevents damage to the module, but may cause erroneous readings. Overcurrent conditions are reported to software.

Signal Acquisition Considerations

This section contains information about signal acquisition concepts, including operation modes, delta-sigma converters, filtering, timing, triggering, and synchronization.

Excitation Verification

The TB-4340 provides excitation verification pins that are pulled to the excitation lines by 4.7 kΩ resistors. These terminals allow external gross checks for monitoring the excitation of the PXIe-4340. The resistors prevent faults on the excitation verification pins from affecting excitation, but reduce the accuracy of the voltage measured because the higher impedance is more sensitive to loading from the verification instrument.

Demodulation

The PXIe-4340 digitizes oversampled data, which is digitally demodulated. The digital demodulation process uses constant delay filters to extract the relative amplitudes and phases of the voltages on the primary and secondary LVDT windings. The amplitudes are divided to determine the ratiometric voltage and the phase is used to determine the sign. Small amplitude signals can cause the phase detector to become noisy.

ADC

The PXIe-4340 ADCs use a conversion method known as delta-sigma modulation. This approach involves oversampling the input signal and then decimating and filtering the resulting data to achieve the desired sample rate. The PXIe-4340 supports rates of 1 S/s to 25.6 kS/s.

Operation Modes

The PXIe-4340 supports two modes of operation: Buffered Mode and Hardware-Timed Single Point Mode. In a Buffered Mode acquisition, oversampled data is decimated to your requested sample rate and digital filters are applied to filter out frequency content above the Nyquist frequency. These digital filters introduce group delay and for some applications this may be undesirable. For this reason, the PXIe-4340 also supports Hardware-Timed Single Point Mode in which the oversampled data is only filtered in the demodulator to reduce the group delay.

Buffered Mode Acquisitions

In Buffered Mode, the PXIe-4340 uses digital filters to provide an accurate representation of core displacement while rejecting the excitation. These filters discriminate between signals based on the frequency range or bandwidth of the signal. Signals within the digital filter bandwidth, centered around the excitation frequency, are returned.

Buffered Mode Filters

A digitizer or ADC might sample signals containing frequency components above the Nyquist limit. The undesirable effect of the digitizer modulating out-of-band components into the Nyquist bandwidth is aliasing. The greatest danger of aliasing is that you cannot determine if aliasing occurred by looking at the ADC output. If an input signal contains several frequency components or harmonics, some of these components might be represented correctly while others contain aliased artifacts.

Lowpass filtering to reduce components above the Nyquist frequency either before or during the digitization process can reduce the magnitude of aliased components. In Buffered Mode, the PXIe-4340 employs both digital and analog lowpass filters to achieve this protection.

In Buffered Mode, the PXIe-4340 uses an oversampled architecture and sharp digital filters[1] with cut-off frequencies that track the sampling rate. Therefore, the filter automatically adjusts to follow the Nyquist frequency. This filtering is performed in addition to the filtering provided by the demodulator. This means that the digital filter bandwidth increases until reaching the full bandwidth of the demodulation filter, where it stops increasing with sample rate. Refer to the *NI PXIe-4340 Device Specifications* for the aggregate digital filter bandwidth in Buffered Mode.

Filter Group Delay

The digital filtering performed by the PXIe-4340 produces a delay of many samples worth of time between when an event occurs on the input signal going into the PXIe-4340 and when the data associated with that event is available at the output of the acquisition and filtering process. This delay is called the group delay.

In order to simplify synchronization with other modules, the PXIe-4340 compensates for this group delay in the following ways:

- The Sample Clock output from the PXIe-4340 is generated at the point in time when the input signal is valid at the ADC input pins. When acquiring data, the PXIe-4340 generates a Sample Clock, then waits for the data associated with that Sample Clock to be acquired, then returns that data. As a result, any other acquisitions timed with this Sample Clock line up with the data returned by the PXIe-4340.
- Any triggers generated or received by the PXIe-4340 are interpreted based on their relationship to the Sample Clock. For example, a Start Trigger that starts an acquisition results in data from the next Sample Clock being returned as the first point in the

[1] Looser filters with degraded alias-free bandwidth are used for sample rates <25 Hz. This is done in order to reduce the large group delays associated with filtering at lower sample rates.

acquisition. Refer to the *Triggering and Filter Delay* section for more details about how this affects analog trigger events.

- On demand software sampling returns a single sample from an acquisition running at the maximum supported sample rate of the module. For any on-demand, software timed acquisition the PXIe-4340 waits for the group delay to elapse before returning the sample. As a result, the data returned aligns closely in time with the software request and is delayed by the sum of the analog input delay and digital filter delay.[1]

Synchronizing Channels

Channels on the same board configured with the same excitation frequency and amplitude are automatically synchronized. You can synchronize more than two channels used for resolvers or combinations of resolvers, LVDTs, RVDTs, and synchros. You can also synchronize more than two channels used for resolvers or combinations of resolvers, LVDTs, RVDTs, and synchros by assigning the same voltage and frequency across the channels.

Hardware-Timed Single Point Acquisitions

Hardware-Timed Single Point (HWTSP) is a Hardware-Timed Acquisition Mode in which a digital hardware signal (Sample Clock) controls the rate of the acquisition. The Sample Clock signal can be imported or internally generated on the PXIe-4340 using the sample rate configured with a NI-DAQmx task.

During Buffered acquisitions, the device may wait to transfer data to the host machine to build larger bus transactions. This optimizes throughput. During HWTSP acquisitions, the device sends data to the host in response to every sample clock. This optimizes latency.

These features make HWTSP ideal for real-time control applications. HWTSP acquisitions, in conjunction with the wait for next sample clock function, provide more deterministic synchronization between software and the hardware. Refer to the *NI-DAQmx Hardware-Timed Single Point Lateness Checking* document for more information. To access this document, go to `ni.com/info` and enter the Info Code `daqhwtsp`.

Hardware-Timed Single Point Acquisition Model

The HWTSP data path is optimized for low-latency applications and is different than the data path used in Buffered Mode acquisitions.

When in HWTSP, the demodulation and sampling systems can be modeled as being decoupled, which allows you to configure the demodulator and sampling systems independently. This

---

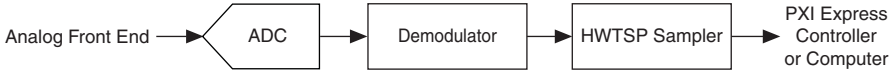
[1] The maximum sample rate of the PXIe-4340 is 25.6 kS/s. In addition to the fixed analog input delay, you must also account for the digital-filter group delay. For 25.6 kS/s with 5 kHz excitation, the digital filter group delay is $.88544\ \text{ms} + \frac{29\ \text{S}}{25.6\ \text{kS/s}} = 3.01825\ \text{ms}$.

The total delay is 3.01825 ms + 0.7 µs = 3.01895 ms. Refer to the *NI PXIe-4340 Device Specifications* for more information.

decoupling means that the full bandwidth of the demodulator is always available to the sampling system. Therefore, caution must be taken so the core displacement frequency does not exceed the Nyquist frequency. Otherwise, high frequency components of the displacement may become aliased.

Figure 2-9 shows the HWTSP data path model.

Figure 2-9. HWTSP Data Path Model



The ADC samples the input stream, which is then processed by the demodulator. The demodulated signal is then routed to the sampling system, which returns the sample to the PXI Express controller or computer based on the Sample Clock signal.

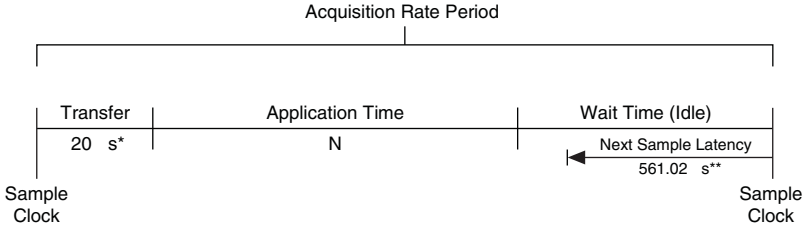
Maximum HWTSP Rate Analysis

During HWTSP acquisitions the maximum achievable acquisition rate without missing a sample is affected by both the transfer and application time. Refer to Figure 2-10.

$$Rate_{MAX} = \frac{1}{TransferTime + ApplicationTime}$$

Note HWTSP acquisitions can detect if they cannot keep up with the acquisition rate. Refer to the *Hardware-Timed Single Point Sample Mode* topic in the *NI-DAQmx Help* for more information.

Figure 2-10. Transfer Time and Application Time Relationship



*Transfer time may vary depending on system.
**561.02 s is the approximate latency for excitation frequencies between 5 kHz and 10 kHz.

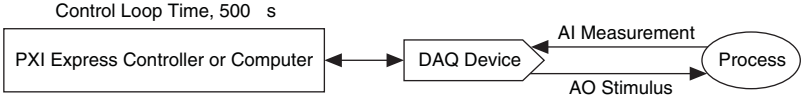
Note For control applications, it is important to consider the group delay of the data being acquired and analyzed when calculating the control system bandwidth. Regardless of the sample rate, the bandwidth of the system is as follows:

$$bandwidth = \frac{1}{TransferTime + ApplicationTime + AnalogGroupDelay + HWTSP\ Latency}$$

2 kHz Control Loop Rate Calculation Example

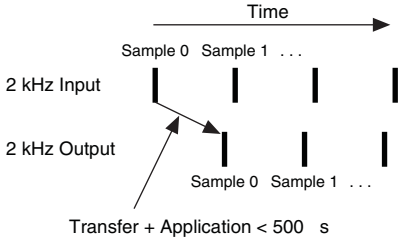
Figure 2-11 represents a typical control system in which you have a process to control, a DAQ device for signal measurement and stimulus generation, and a PXI Express controller or computer to process data and return an appropriate AO value to the process.

Figure 2-11. Typical Control System



To successfully close a 2 kHz control loop, make sure that the time difference between the time the AI sample is acquired and the time the AO stimulus is generated is <500 µs. Refer to Figure 2-12.

Figure 2-12. Input and Output of a Control System with Bandwidth ≥2 kHz



To make sure that your application can run and control a process at 2 kHz, and that the first output is generated within the first sample period, make sure that the following conditions are satisfied:

$$Transfer\ Time + Application\ Time \leq 500\ \mu s \quad (2\text{-}1)$$

where:

Transfer Time—the time it takes to transfer samples between the DAQ device and the PXI Express controller or computer.

Application Time—the time it takes for the PXI Express controller or computer to analyze the acquired data and generate the AO stimulus.

Using Equation 2-1 and the Transfer Time from the sample system described in this section, you can determine that an application time of 480 µs is required to close a 2 kHz control loop.

$$Application\ Time \leq 500\ \mu s - Transfer\ Time$$

$$Application\ Time \leq 500\ \mu s - 20\ \mu s$$

$$Application\ Time \leq 480\ \mu s$$

Any application taking more than 480 µs will fail to close the 2 kHz control loop.

When analyzing the bandwidth of the system, you must consider the delay of all the components of the system. When using an excitation frequency between 5 kHz and 10 kHz, the bandwidth of the control loop is as follows:

$$ControlBandwidth = \frac{1}{TransferTime + ApplicationTime + AnalogGroupDelay + HWTSP\ Latency}$$

$$ControlBandwidth = \frac{1}{20\,\mu s + 480\,\mu s + 0.7\ \mu s + 560.32\ \mu s}$$

$$Control\ Bandwidth = 942.5\ Hz$$

Note You can increase the bandwidth of the system by either reducing the application time or by using an excitation frequency in a faster demodulation latency range.

Timing and Triggering

This section contains information about timing and triggering.

Sample Clock Timebase

The ADCs require an oversample clock to drive the conversion. The oversample clock frequency is greater than the sample rate. On the PXIe-4340 modules the oversample clock is produced from a 100 MHz reference clock. This 100 MHz reference clock can be phase locked with the PXI Express backplane 100 MHz clock or be generated by an internal timebase that runs freely. Multiple modules can be synchronized by selecting the PXI Express backplane 100 MHz clock as the reference clock source for all the modules. Refer to the *Reference Clock Synchronization* section for more information.

External Clock

The PXIe-4340 ADCs cannot be clocked from external sources such as encoders or tachometers. However, signal processing features in the Sound and Vibration Measurement Suite often provide an excellent alternative to external clocking in encoder and tachometer applications. Visit ni.com/soundandvibration for more information about the Sound and Vibration Measurement Suite.

Digital Triggering

You can configure the PXIe-4340 modules to start an acquisition in response to a digital trigger signal from one of the PXI Express backplane trigger lines or the PFI from the front connector. The trigger circuit can respond either to a rising or a falling edge.

Analog Triggering

Analog triggering allows you to trigger your application based on an input signal and trigger level you define. You can configure the analog trigger circuitry to monitor any input channel acquiring data. Choosing an input channel as the trigger channel does not change the input channel acquisition specifications.

The analog trigger signal can be used as a reference trigger only. In a reference-triggered acquisition, you configure the module to acquire a certain number of pre-trigger samples and a certain number of post-trigger samples. Reference-triggered acquisitions can therefore only be configured as finite tasks. The analog trigger on the PXIe-4340 cannot be used as a start trigger. This restriction is a result of the way the module compensates for the filter group delay.

When using an analog reference trigger, the module first waits for the specified number of pre-trigger samples to be acquired. Once enough pre-trigger samples are acquired, the reference trigger will occur the next time the analog trigger condition is met. You can also route the resulting reference trigger event to supported digital terminals. Refer to the Device Routes in NI Measurement & Automation Explorer (MAX) for additional information.

During repetitive triggering on a waveform, you might observe jitter because of the uncertainty of where a trigger level falls compared to the actual digitized data. Although this trigger jitter is never greater than one sample period, it might be significant when the sample rate is only twice the bandwidth of interest. This jitter usually has no effect on data processing, and you can decrease this jitter by sampling at a higher rate.

You can use several analog triggering modes with the PXIe-4340 modules including analog edge, analog edge with hysteresis, and window triggering.

Triggering and Filter Delay

The PXIe-4340 interprets triggers based on where they occur in time. The hardware automatically compensates for its group delay such that data from this module will line up closely in time with the occurrence of the trigger event. However, the group delay affects how long it takes to receive data when starting an acquisition. Since linear phase FIR filters are used in the digital filtering, it is necessary to wait for the filter group delay to elapse after sending a

sync pulse before the start trigger can be correctly handled in time. Step 6 in the *Reference Clock Synchronization* section allows NI-DAQmx to handle this delay automatically. After the digital start trigger, you cannot read data for the first sample in software until the digital filter group delay has elapsed. Therefore, it takes a total of twice the digital filter group delay to start an acquisition. You can insert additional time between when the sync pulse occurs and when the start trigger occurs. This will not affect the time it takes before samples are available after the start trigger, which is always the group delay time. Group delay time increases as sample rates decrease. Refer to the *NI PXIe-4340 Device Specifications* document for details regarding the group delay at different sample rates.

Synchronization

Some applications require tight synchronization between input and output operations on multiple modules. Synchronization is important to minimize skew between channels and to eliminate clock drift between modules in long-duration operations. You can synchronize the analog input operations on two or more PXIe-4340 modules to extend the channel count for your measurements. In addition, the PXIe-4340 can synchronize with other product families using Reference Clock Synchronization.

Reference Clock Synchronization

With Reference Clock Synchronization, master and slave modules generate their ADC oversample clock from the shared 100 MHz reference clock from the PXI Express backplane (PXIe_CLK100). The backplane supplies an identical copy of this clock to each peripheral slot. In addition, multiple chassis can be synchronized by using a timing and synchronization board to lock the 100 MHz clock across chassis.

When you acquire data from multiple modules within the same NI-DAQmx task, NI-DAQmx will automatically handle all of the Reference Clock Synchronization details required to synchronize the modules within the task. This is known as a Multi-Device Task.

To perform Reference Clock Synchronization when using multiple NI-DAQmx tasks that are acquiring at the same rate, complete the following steps to synchronize the hardware.

1. Specify PXIe_CLK100 as the reference clock source for all modules to force all the modules to lock to the reference clock on the PXI Express chassis.
2. Choose an arbitrary PXIe-4340 master module to issue a sync pulse on one of the PXIe Trigger lines. The sync pulse resets the ADCs and oversample clocks, phase aligning all the clocks in the system to within nanoseconds.
3. Configure the rest of the modules in your system to receive their sync pulse from the sync pulse master module. This will ensure all ADCs are running in lockstep.
4. Choose one module to be the start trigger master. This does not have to be the same module you chose in step 2.
5. Configure the rest of the modules in your system to receive their start trigger from the start trigger master module. This ensures that all modules will begin returning data on the same sample.

6. Set the synchronization type of the Start Trigger slaves at **DAQmx Trigger»Advanced»Synchronization»Synchronization Type** to Slave and that of the Master to Master.
7. Query **DAQmx Timing»More»Synchronization Pulse»Synchronization Time** on all modules being synchronized, choose the maximum value and set that as the **DAQmx Timing»More»Synchronization Pulse»Minimum Delay To Start** on the module from which the synchronization pulse originates.
8. Commit all of the sync pulse slave module tasks using the DAQmxTaskControl VI/Function. This sets them up to expect the sync pulse from the master.
9. Commit the sync pulse master module task using the DAQmxTaskControl VI/Function. This will issue the sync pulse.
10. Start all of the start trigger slave module tasks. This sets them up to expect the start trigger from the master.
11. Start the start trigger master module task. You can now acquire data.

Tip Consider using a Multi-Device task when synchronizing multiple devices at the same rate.

Tip You can find example VIs in the NI Example Finder. Select **Help»Find Examples** to launch the NI Example Finder.

Consider the following caveat to using Reference Clock Synchronization:

- The PXIe-4340 automatically compensates for its filter group delay. However, some other device families do not compensate for their filter delay. In this case, manually compensate for group delay in the waveforms when you synchronize between device families if this level of synchronization is required for your application.

Timing Engines and DSP Streams

This section gives an overview of the internal implementation of the PXIe-4340 and how the module can be configured. The use of NI-DAQmx software allows you to easily configure the PXIe-4340 without you understanding the internal workings of the device.

Timing Engines

When you create a task in software, that software task interacts with one or more timing engines in the PXIe-4340. There are a total of four timing engines in hardware that can be operated simultaneously. Each of these timing engines can have individualized configuration settings for timing, triggering, and the sample mode. Depending on the sample mode selected, the timing engine will use either a Buffered Mode or Hardware-Timed Single Point DSP stream.

DSP Streams

The DSP streams in the PXIe-4340 perform the digital signal processing on the acquired data before sending the data to software. There are two types of DSP streams: Buffered Mode streams and Hardware-Timed Single Point streams. The PXIe-4340 has four streams for each of these types and each stream handles one channel. Therefore, it is possible to use all 4 channels in either Buffered Mode or Hardware-Timed Single Point Mode.

Accessory Auto-Detection

SC Express modules automatically detect compatible accessories or terminal blocks. The RSVD pins on the I/O connector provide power to the accessories as well as digital communication lines. This allows software to detect when accessories are inserted or removed. In addition, software can automatically identify the specific terminal block as well as access any calibration or scaling information associated with the terminal block.

MAX allows you to see which accessories are currently connected to your module. In MAX, expand **Devices and Interfaces** and locate your module. If a terminal block is connected to your module, it will be displayed beneath the module. Unsupported terminal blocks appear in MAX with an X next to them.

NI-DAQmx property nodes can be used to programmatically access information about connected accessories in your application. Refer to the *NI-DAQmx Help* for documentation about programmatically accessing accessory status.

3

SC Express Considerations

This chapter details the clock and trigger functionality available through the PXI Express chassis.

SC Express Clock and Trigger Signals

PXIe_CLK100

PXIe_CLK100 is a common, low-skew 100 MHz reference clock used for synchronization of multiple modules in a PXI Express measurement or control system. The PXI Express backplane is responsible for generating PXIe_CLK100 independently to each peripheral slot in a PXI Express chassis. For more information, refer to the *PXI Express Specification* at `www.pxisa.org`.

PXIe_SYNC100

PXIe_SYNC100 is a common, low-skew 10 MHz reference clock with a 10% duty cycle for synchronization of multiple modules in a PXI Express measurement or control system. The PXI Express backplane is responsible for generating PXIe_SYNC100 independently to each peripheral slot in a PXI Express chassis. PXIe_SYNC100 allows modules using PXIe_CLK100 as their reference to recreate the timing of the PXI_CLK10 signal while taking advantage of the lower skew of PXIe_CLK100. For more information, refer to the *PXI Express Specification* at `www.pxisa.org`.

PXI_CLK10

PXI_CLK10 is a common, low-skew 10 MHz reference clock for synchronization of multiple modules in a PXI measurement or control system. The PXI backplane is responsible for generating PXI_CLK10 independently to each peripheral slot in a PXI chassis. In PXI Express chassis, the PXI_CLK10 signal is in phase with PXIe_CLK100.

Note PXI_CLK10 cannot be used as a reference clock for SC Express modules.

PXI Triggers

A PXI/PXI Express chassis provides eight bused trigger lines to each module in a system. Triggers may be passed from one module to another, allowing precisely timed responses to asynchronous external events that are being monitored or controlled. Triggers can be used to synchronize the operation of several different PXI peripheral modules.

In a PXI chassis with more than eight slots, the PXI trigger lines may be divided into multiple independent buses. Refer to the documentation for your chassis for details.

PXI_STAR Trigger

In a PXI Express system, the Star Trigger bus implements a dedicated trigger line between the system timing slot and the other peripheral slots. The Star Trigger can be used to synchronize multiple modules or to share a common trigger signal among modules.

A system timing controller can be installed in the system timing slot to provide trigger signals to other peripheral modules. Systems that do not require this functionality can install any standard peripheral module in this system timing slot.

An SC Express module receives the Star Trigger signal (PXI_STAR) from a System timing controller. PXI_STAR can be used as a trigger signal for input operations.

An SC Express module is not a System timing controller. An SC Express module can be used in the system timing slot of a PXI system, but the system will not be able to use the Star Trigger feature.

PXIe_DSTAR<A..C>

PXI Express devices can provide high-quality and high-frequency point-to-point connections between each slot and a system timing slot. These connections come in the form of three low-voltage differential star triggers that route between a PXI Express system timing controller and a peripheral device. Using multiple connections simplifies the creation of applications because of the increased routing capabilities.

Table 3-1 describes the three differential star (DSTAR) lines and how they are used.

Table 3-1. PXIe_DSTAR Line Descriptions

Trigger Line	Purpose
PXIe_DSTARA	Distributes high-speed, high-quality clock signals from the system timing slot to the peripherals (input).
PXIe_DSTARB	Distributes high-speed, high-quality trigger signals from the system timing slot to the peripherals (input).
PXIe_DSTARC	Sends high-speed, high-quality trigger or clock signals from the peripherals to the system timing slot (output).

The DSTAR lines are only available for PXI Express devices when used with a PXI Express system timing module. For more information, refer to the *PXI Express Specification* at `www.pxisa.org`.

A

NI Services

NI provides global services and support as part of our commitment to your success. Take advantage of product services in addition to training and certification programs that meet your needs during each phase of the application life cycle; from planning and development through deployment and ongoing maintenance.

To get started, register your product at ni.com/myproducts.

As a registered NI product user, you are entitled to the following benefits:

- Access to applicable product services.
- Easier product management with an online account.
- Receive critical part notifications, software updates, and service expirations.

Log in to your MyNI user profile to get personalized access to your services.

Services and Resources

- **Maintenance and Hardware Services**—NI helps you identify your systems' accuracy and reliability requirements and provides warranty, sparing, and calibration services to help you maintain accuracy and minimize downtime over the life of your system. Visit ni.com/services for more information.
  - **Warranty and Repair**—All NI hardware features a one-year standard warranty that is extendable up to five years. NI offers repair services performed in a timely manner by highly trained factory technicians using only original parts at a NI service center.
  - **Calibration**—Through regular calibration, you can quantify and improve the measurement performance of an instrument. NI provides state-of-the-art calibration services. If your product supports calibration, you can obtain the calibration certificate for your product at ni.com/calibration.
- **System Integration**—If you have time constraints, limited in-house technical resources, or other project challenges, National Instruments Alliance Partner members can help. To learn more, call your local NI office or visit ni.com/alliance.

- **Training and Certification**—The NI training and certification program is the most effective way to increase application development proficiency and productivity. Visit ni.com/training for more information.
  - The Skills Guide assists you in identifying the proficiency requirements of your current application and gives you options for obtaining those skills consistent with your time and budget constraints and personal learning preferences. Visit ni.com/skills-guide to see these custom paths.
  - NI offers courses in several languages and formats including instructor-led classes at facilities worldwide, courses on-site at your facility, and online courses to serve your individual needs.
- **Technical Support**—Support at ni.com/support includes the following resources:
  - **Self-Help Technical Resources**—Visit ni.com/support for software drivers and updates, a searchable KnowledgeBase, product manuals, step-by-step troubleshooting wizards, thousands of example programs, tutorials, application notes, instrument drivers, and so on. Registered users also receive access to the NI Discussion Forums at ni.com/forums. NI Applications Engineers make sure every question submitted online receives an answer.
  - **Software Support Service Membership**—The Standard Service Program (SSP) is a renewable one-year subscription included with almost every NI software product, including NI Developer Suite. This program entitles members to direct access to NI Applications Engineers through phone and email for one-to-one technical support, as well as exclusive access to online training modules at ni.com/self-paced-training. NI also offers flexible extended contract options that guarantee your SSP benefits are available without interruption for as long as you need them. Visit ni.com/ssp for more information.
- **Declaration of Conformity (DoC)**—A DoC is our claim of compliance with the Council of the European Communities using the manufacturer's declaration of conformity. This system affords the user protection for electromagnetic compatibility (EMC) and product safety. You can obtain the DoC for your product by visiting ni.com/certification.

For information about other technical support options in your area, visit ni.com/services, or contact your local office at ni.com/contact.

You also can visit the Worldwide Offices section of ni.com/niglobal to access the branch office websites, which provide up-to-date contact information, support phone numbers, email addresses, and current events.