
PXle-5840 User Manual

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PXIe-5840

6 GHz, 1 GHz Bandwidth, RF PXI Vector Signal Transceiver

- 9 kHz to 6 GHz frequency range
- Up to 1 GHz of instantaneous bandwidth

PXle-5840 Front Panel and LEDs

Front Panel and LEDs

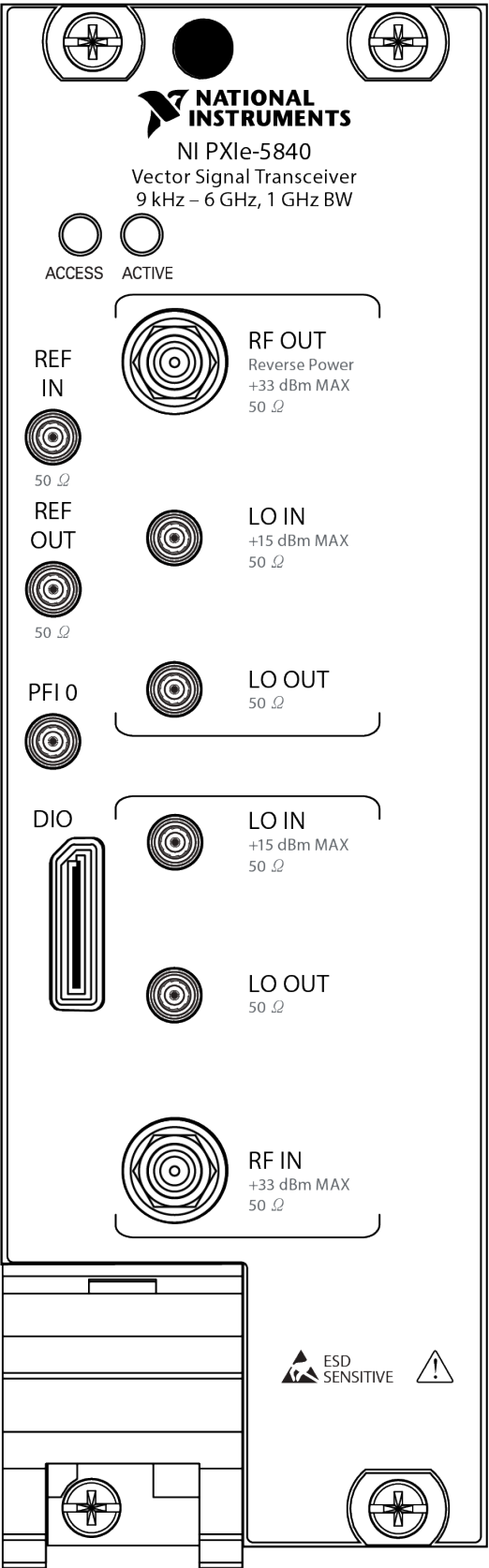


Table 1. General Connector Descriptions

Connector	Use	Connector Type
REF IN	Input terminal that allows for the use of an external 10 MHz Reference Clock.	MMPX (f)
REF OUT	Output terminal that can export a 10 MHz Reference Clock or the 156.25 MHz Data Clock.	MMPX (f)
PFI 0	Programmable-function digital I/O (DIO) connector for use with triggers or events.	MMPX (f)
DIO	Multi-signal DIO connector that provides access to FPGA multi-gigabit transceivers (MGTS) and general purpose LVCMOS signals.	Nano-Pitch



Notice The DIO connector is not an OcuLink interface. Do not connect the DIO connector on the PXIe-5840 to the OcuLink interface of another device. NI is not liable for any damage resulting from such signal connections.

Table 2. RF Connector Descriptions

Connector		Use	Connector Type
RF OUT	RF OUT	Output terminal for RF signals.	SMA (f)
	LO IN	Input terminal that allows for the use of an external local oscillator (LO) for RF OUT.	MMPX (f)
	LO OUT	Output terminal for exporting the RF OUT LO source.	MMPX (f)
RF IN	LO IN	Input terminal that allows the use of an external LO for RF IN.	MMPX (f)

Connector		Use	Connector Type
	LO OUT	Output terminal for exporting the RF IN LO source.	MMPX (f)
	RF OUT	Input terminal for RF signals.	SMA (f)

Table 3. LED Indicators

LED	Indications
ACCESS	Indicates the basic hardware status of the device. Off—The device is not yet functional or has detected a problem with a PXI Express power rail. Amber—The device is being accessed. Accessed means that you are writing to the device setup registers to control the device, reading from the device to monitor the device status, or transferring data to/from the device. Green—The device is controllable through the software.
ACTIVE	Off—The device is idle. Solid green—The device is generating a waveform. Dim amber—The device is waiting for an acquisition Reference Trigger. Solid amber—The device is acquiring a waveform. Solid red—The device has detected an error. The LED remains red until the error condition is

LED	Indications
	removed. Note The indicators are listed in increasing order of priority. For example, if you are generating a waveform using NI-RFSG and waiting on an acquisition Reference Trigger in NI-RFSA, the LED is dim amber.

DIO Connector Pinout

Reserved	A1	B1	5.0 V
GND	A2	B2	GND
MGT Rx+ 0	A3	B3	MGT Tx+ 0
MGT Rx− 0	A4	B4	MGT Tx− 0
GND	A5	B5	GND
MGT Rx+ 1	A6	B6	MGT Tx+ 1
MGT Rx− 1	A7	B7	MGT Tx− 1
GND	A8	B8	GND
DIO 4	A9	B9	DIO 6
DIO 5	A10	B10	DIO 7
GND	A11	B11	GND
MGT REF+ / DIO 0	A12	B12	DIO 2
MGT REF− / DIO 1	A13	B13	DIO 3
GND	A14	B14	GND
MGT Rx+ 2	A15	B15	MGT Tx+ 2
MGT Rx− 2	A16	B16	MGT Tx− 2
GND	A17	B17	GND
MGT Rx+ 3	A18	B18	MGT Tx+ 3
MGT Rx− 3	A19	B19	MGT Tx− 3
GND	A20	B20	GND
5.0 V	A21	B21	Reserved

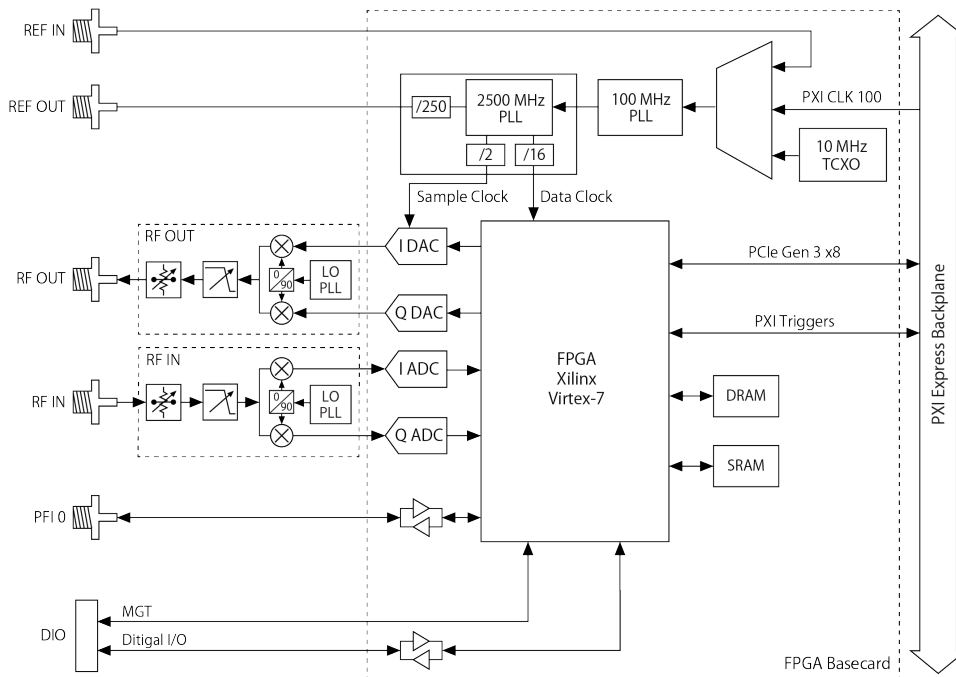
PFI 0 Connector Using NI-RFSA and NI-RFSG

PFI 0 is a bidirectional connector. When programming the PXle-5840 using NI-RFSA or NI-RFSG, the PFI 0 terminal can accept a trigger from an external source or export an event or trigger.

Refer to the ***PXle-5840 Specifications*** document for information about acceptable input signal characteristics for the PFI 0 line and output signal characteristics.

PXIe-5840 Block Diagram

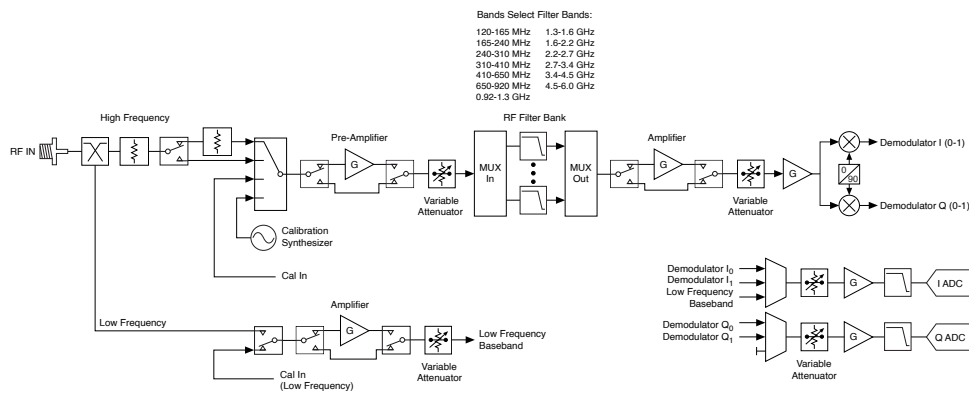
The PXIe-5840 has the RF Input, RF Output, FPGA Basecard, and LO Path subsystems.



Note Some calibration-related routing paths and front panel connectors have been omitted from the illustration of the high-level block diagram for simplicity.

RF Input Subsystem

The PXIe-5840 has two configurable RF paths comprised of an independent vector signal analyzer (RF input) path and vector signal generator (RF output) path. The following high-level block diagram represents the PXIe-5840 RF input path.



The PXIe-5840 RF input path is AC coupled and covers a frequency range of 9 kHz to 6,000 MHz center frequency. For frequencies below 120 MHz (low frequency), RF input signals are directly sampled via analog-to-digital conversion. Frequencies greater than 120 MHz (high frequency) are translated to baseband via a single stage direct conversion (I/Q) downconverter, allowing for wide instantaneous bandwidth.

High Frequency RF Input Path

The high frequency subsystem of the RF input path consists of a programmable and filtered front end that feeds into a direct conversion downconverter. Once at baseband frequencies, the signal is sampled with an analog-to-digital converter (ADC) capable of up to 1,000 MHz of complex equalized bandwidth.

RF attenuation greater than 70 dB can be nominally configured through the combination of switchable attenuation and programmable step attenuators. RF attenuation is automatically chosen in conjunction with amplification stages to provide optimal reference levels over the support range of the device.

A switchable pre-amplifier is also configurable in the front end of the device to further optimize the signal path for noise figure. This pre-amplifier can be configured for bypass, forced inline, or automatically configured based on application needs. The configurable range of reference levels may vary based on which option is selected for the pre-amplifier.

Low Frequency RF Input Path

The low frequency subsystem of the RF input path is used to directly sample RF input signals below 120 MHz. The RF input signal is provided via a frequency selective diplexer to programmable gain components before being filtered and sampled with an

analog-to-digital converter.

The programmable gain elements at low frequency consist of a switchable amplifier and a programmable attenuator. When disabled, the switched amplifier is bypassed by a 10 dB attenuator. The programmable attenuator is capable of 31 dB attenuation in 1 dB steps.

Refer to the ***RF Path Transitions*** topic for more information on using the low frequency RF input path.

Cal In Path

The RF input subsystem has internal calibration capability in both the high frequency and low frequency paths. Cal In is used in conjunction with Cal Out from the RF Output subsystem to facilitate steps within the following VIs or functions:

- NI-RFSA Self-Calibrate VI or niRFSA_SelfCalibrate
- NI-RFSG Self-Calibrate VI or niRFSG_SelfCal
- NI-RFSA Self-Calibrate Range VI or niRFSA_SelfCalibrateRange
- NI-RFSG Self-Calibrate Range VI or niRFSG_SelfCalibrateRange

Related concepts:

- [RF Path Transitions](#)
- [Quadrature Mixing \(Direct Conversion\)](#)

RF Input Signal Path

The RF source signal takes the following path from the PXIe-5840 front panel to the PXI Express controller.

1. The RF signal is connected to the RF IN front panel connector.
2. The RF signal is passed through the frequency-selective path of the front end diplexer to either the high frequency or low frequency path.
3. The signal is amplified or attenuated based on the reference level to the required mixer level, based on available gain in the selected RF path. The amplification and attenuation maintain optimized dynamic range and avoid signal saturation or ADC overflow.

4. The RF signal is frequency-translated based on the signal path used:
 - When in the high frequency path, the attenuated or amplified signal is mixed with a 0° phase and 90° phase LO signal at the tuned center frequency, translating the resulting signal into a pair of I and Q signals 90° out-of-phase from each other. These I and Q signals are then conditioned and sampled by an ADC converter.
 - When in the low frequency path, the attenuated or amplified signal is directly passed to signal conditioning and the ADC without frequency translation.
5. The translated signal is sampled by the ADC at 1,250 MS/s. The resulting signals are accessible through LabVIEW FPGA I/O nodes for further processing or transfer to the host computer.

RF IN Signal Gain and Attenuation

The RF IN signal path chooses gain and attenuation settings based on the requested reference level.

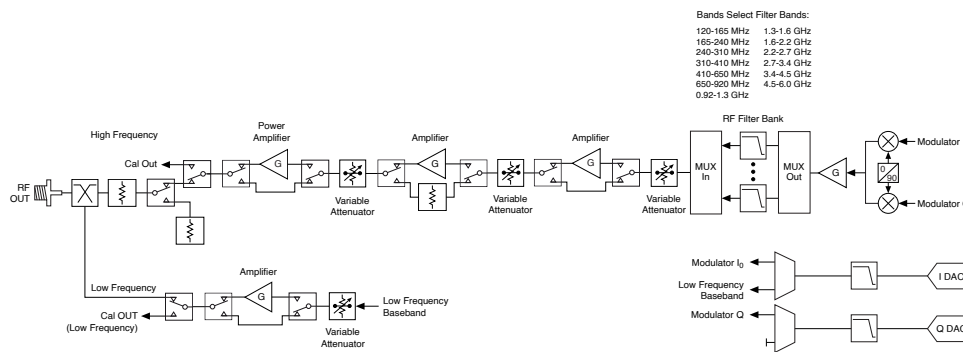
The gain definition measured in calibration is adjusted and applied according to the following equation:

$$\text{RF Input Gain (dB)} = \text{Complex Power}_{\text{ADC}}(\text{dB}) - \text{Real Power}_{\text{RF IN Terminal}}(\text{dB})$$

The resulting gain scales the acquired data to reference back to the RF IN front panel connector. The reported gain scales both I and Q evenly. If you compute power by reading I/Q data and running a power spectrum or Fast Fourier Transform (FFT), scale the gain by a gain compensation value of 0.5 or reduce the power result by 3 dB. If you use Spectrum Mode, NI-RFSA scales the power for you.

RF Output Subsystem

The PXIe-5840 has two configurable RF paths comprised of an independent vector signal analyzer (RF input) path and vector signal generator (RF output) path. The following high-level block diagram represents the PXIe-5840 RF output path.



The PXle-5840 RF output path is AC coupled and covers a frequency range of 9 kHz to 6,000 MHz center frequency. For frequencies below 120 MHz (low frequency), RF output signals are directly generated via digital-to-analog (DAC) conversion. Frequencies greater than 120 MHz (high frequency) are translated from baseband I and Q signals to the specified RF frequency via a single stage direct conversion (I/Q) upconverter, allowing for a wide instantaneous bandwidth.

High Frequency RF Output Path

The high frequency subsystem of the RF output path consists of a wideband direct conversion upconverter and a front end signal path with programmable RF filtering and gain stages. I and Q baseband signals generated by the DAC are mixed and combined to create an RF signal with up to 1,000 MHz of complex equalized bandwidth centered at the specified RF center frequency. This signal can then be conditioned for both bandwidth and level.

Greater than 80 dB of RF attenuation can be configured nominally through the combination of switchable fixed attenuation and programmable step attenuators. RF attenuation is automatically chosen in conjunction with amplification to provide optimal reference levels over the support range of the device. There are two switchable amplifiers and one switchable high power amplifier.

The switchable high power amplifier is used for generating signals significantly larger than 0 dBm. This amplification stage is automatically selected based on output power level setting and extends the available peak power range to +20 dBm, calibrated. Additional power may be achieved above +20 dBm, however it is not guaranteed to meet absolute or relative accuracy specifications.

Low Frequency RF Output Path

The low frequency subsystem of the RF output path is used to directly generate the requested RF output signals below 120 MHz from the DAC. The RF signal is generated from the DAC through programmable gain stages and transmitted from the RF OUT front panel connector through a frequency selective diplexer. This allows for a seamless transition from low frequency to high frequency paths. Refer to the ***RF Path Transitions*** topic for more information about using the low frequency path.

The low frequency path programmable gain stages consist of a 31 dB step attenuator with 1 dB resolution and a switchable amplification stage. The off state of the switchable amplifier has additional fixed attenuation integrated into it. This provides a nominal gain range of +5 dB to -40 dB. Additional attenuation is possible with the DAC full scale configuration settings as well as digital waveform scaling.



Note NI recommends external attenuation for applications requiring a significant amount of analog attenuation when using the low frequency RF output path.

Related concepts:

- [Quadrature Mixing \(Direct Conversion\)](#)
- [RF Path Transitions](#)

RF Output Signal Path

The RF output signal takes the following path from the PXIe-5840 FPGA to the RF OUT front panel connector.

1. The I and Q digital signals are sent to the baseband digital-to-analog (DAC) converter through a LabVIEW FPGA I/O node after being written from the host.
2. The DAC converts the digital I and Q waveforms into analog I and Q signals at 1,250 MS/s. Internal to the DAC, the output is two times interpolated to 2,500 MS/s.
3. Based on the specified center frequency, the analog I and Q signals are conditioned and passed either to the direct conversion modulator high frequency path, or sent directly to the low frequency path for additional level control.
4. Depending on the selection of high frequency path or low frequency path, the

converted RF frequency is further attenuated or amplified based on the specified output power settings.

5. The conditioned RF output signal is transmitted from the PXle-5840RF OUT front panel connector through a frequency selective diplexer stage.

Using the PXle-5840 in CW Mode

You can use the PXle-5840 as a continuous waveform (CW) generator when programming the PXle-5840 using NI-RFSG. To generate a CW signal, use NI-RFSGConfigure Generation Mode.

Average Power and Crest Factor Considerations

Crest factor is the difference between peak signal power and average power.

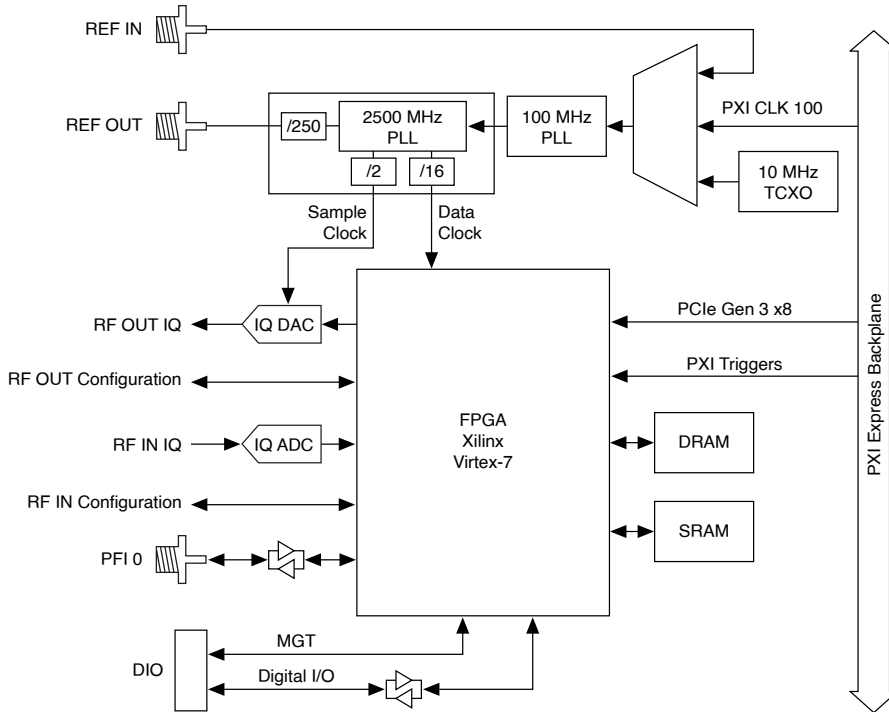
The crest factor for a sinusoidal signal, as is used in CW mode, is 3 dB. In other words, the average RMS power of the sinusoid is 3 dB less than its peak instantaneous power. For modulated signals, specifically orthogonal frequency-division multiplexing (OFDM), the crest factor can be much larger, in the order of 10 dB to 12 dB.

Consider both the average power and the crest factor of a signal when you configure the device for generation. The PXle-5840 supports a maximum specified peak output power. Generating signals beyond specification are not guaranteed to be calibrated or linear. If the peak power is set higher than specified as a result of signal crest factor added with requested average power, severe saturation might occur or the reverse power protection circuitry of the PXle-5840 may be enabled. Refer to the **PXle-5840 Specifications** for more information about output power range specifications.

FPGA Basecard Subsystem

The PXle-5840 has an FPGA basecard, represented by the following high-level block diagram.

Figure 1. PXle-5840 Basecard Block Diagram



The FPGA basecard of the PXIe-5840 consists of the following components: FPGA, Clocking, ADC and DAC, PFI 0, Digital I/O, DRAM, SRAM, PCIe Interface, and PXI triggers

Xilinx Virtex-7 FPGA

The PXle-5840 contains a Xilinx Virtex-7 VX690T FPGA, which is used for system configuration, digital data movement, and digital signal processing.

The FPGA has direct connections to the ADC, DAC, PCI Express bus, DRAM, SRAM, PFI 0, digital I/O, and PXI trigger lines, allowing for custom programming using LabVIEW FPGA to meet the needs of many types of applications.

The Xilinx Virtex-7 FPGA has the following resources.

Table 4. Reconfigurable FPGA Resources

Resource Type	Number
Slice registers	866,400
Slice look-up tables (LUT)	433,200
DSP48E1s	3600

Resource Type	Number
18 Kb block RAMs	2940

Clocking

The PXIe-5840 has multiple clocks available on the device and inside the FPGA. The main device clock is the Sample Clock, which is used to clock the ADC, clock the DAC, and create the Data Clock for the related FPGA logic.

Sample Clock

The Sample Clock runs at 1.25 GHz and is exported by the phase-locked loop (PLL).

You can select one of the following resources as the reference signal for the PLL:

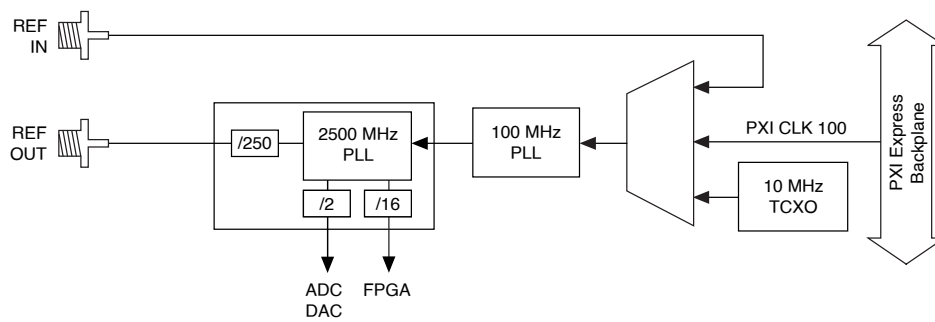
- The internal temperature compensated crystal oscillator (TCXO)
- The REF IN front panel connector
- PXI_CLOCK

While the Sample Clock frequency is fixed at 1.25 GHz, you can achieve high-resolution I/Q data rates using the Fractional Interpolator and Fractional Decimator DSP FPGA VIs.

Data Clock

The Sample Clock is divided by eight to create the Data Clock, which is sent to the FPGA.

The Data Clock runs at 156.25 MHz, and it is the main clock used for the acquisition and generation data paths inside the FPGA. Because the Data Clock is one-eighth the rate of the Sample Clock, eight samples are processed on each cycle of the Data Clock.



FPGA Clocks

The following table lists the clocks available in the FPGA. In addition to these clocks, LabVIEW FPGA allows for derived clocks at user-defined frequencies.

Name	Frequency (MHz)	Description
Data Clock	156.25	Main clock used for the acquisition and generation data paths in the FPGA.
Data Clock x2	312.5	In-phase with the Data Clock and used for DSP VIs.
Data Clock x4	625	In-phase with the Data Clock.
40 MHz Onboard Clock	40	Free-running 40 MHz oscillator.
200 MHz Onboard Clock	200	Free-running 200 MHz oscillator.
PXIe_CLK100	100	100 MHz clock from the backplane.

Front Panel Clocking Connectors

You can use the PXIe-5840 REF IN front panel connector to apply an external 10 MHz reference to the device.

ADC and DAC

The PXIe-5840 uses a dual-channel, 14-bit ADC and 16-bit DAC.

The ADC and DAC are clocked at 1.25 GS/s to provide up to 1 GHz of complex bandwidth, and high-resolution I/Q data rates are achieved by using the Fractional

Interpolator and Fractional Decimator DSP FPGA VIs. The ADC and DAC are automatically synchronized to the Data Clock domain inside the FPGA, which allows for interfacing to both the ADC and DAC in the same clock domain with full synchronization.

PFI 0 Connector

PFI 0 is a 3.3 V LVTTTL, bidirectional, general-purpose digital I/O signal.

The most common use of PFI 0 is as a trigger input or a marker/event output. However, because the PFI 0 I/O buffer is connected directly to the FPGA, you can program the PFI 0 functionality for custom applications using LabVIEW FPGA.

Refer to the **PXle-5840 Specifications** document for information about acceptable characteristics for input and output signals for PFI 0.

DRAM

The PXle-5840 has two banks of dynamic random-access memory (DRAM), which are independently accessible from the FPGA.

Refer to the **PXle-5840 Specifications** document for information about the DRAM size and throughput. These DRAM banks are general purpose, but they are often used for storing waveforms to be generated or waveforms that have been acquired.



Note National Instruments recommends using LabVIEW FPGA memory items for most applications requiring the use of DRAM.

Configuring DRAM with FPGA Memory Items

Use the FPGA memory item interface to use DRAM in the same way that you use block memory and look-up tables (LUT). DRAM memory items appear in the **Project Explorer** window under the FPGA target. The FPGA memory item interface allows you to partition the physical DRAM banks into multiple memory items.

Complete the following steps to configure DRAM with FPGA memory items.

1. To create a target-scoped memory item, right-click the FPGA target in the Project Explorer window and select **New » Memory** from the shortcut menu.

The Memory Properties dialog box appears.

2. Select **DRAM** from the **Implementation** pull-down menu.
3. Select the DRAM bank you want to use from the **DRAM bank** pull-down menu.
4. Type in the number of elements based upon your desired memory size in the **Requested number of elements** textbox.
5. Click **OK** in the Memory Properties dialog box.

The memory item is now populated in the Project Explorer window under the target.

6. Use the memory item in an FPGA VI.

SRAM

The PXle-5840 has one bank of static random-access memory (SRAM), which is accessible from the FPGA.

Refer to the **PXle-5840 Specifications** document for information about the SRAM size and throughput.

SRAM Interface

The PXle-5840 supports SRAM access through socketed component-level IP (CLIP).

Refer to the **PXle-5840 Specifications** document to determine the available amount of onboard SRAM for your device.

Configuring SRAM with Socketed CLIP

Use the socketed CLIP interface to communicate directly with the onboard SRAM. Socketed CLIP lists all memory interfaces that are compatible with the SRAM. The SRAM CLIP is present in the LabVIEW project by default but is disabled.

Complete the following steps to configure SRAM with socketed CLIP:

1. Right-click the SRAM CLIP and select **Properties** from the shortcut menu to display the SRAM Properties dialog box.
2. Select **Enable Memory** if it is not already selected to display the SRAM configuration options.
3. Select the appropriate clock for your project in the Clock Selections dialog box.

You can use the SRAM CLIP in any single clock domain. You can select only clocks already added to the project.

SRAM Properties Dialog Box

Right-click the **SRAM Bank** item in the Project Explorer window and select **Properties** from the shortcut menu to display this dialog box. Check the **Enable SRAM** checkbox if it is not already selected to display the following pages in the Category list:

- General
- Clock Selections

General Page

Use the **General** page to configure the type of memory interface that should be used when communicating with external SRAM.

To display this page, in the SRAM Properties dialog box, select **General** from the **Category** list.

This page contains the following components:

- **Enable SRAM**—Enables the SRAM. Unchecking this box disables access to the SRAM.
- **Memory Interface**—Lists all memory interfaces that are compatible with the SRAM. If multiple versions of a memory interface are available, the version information displays next to the memory interface name.
- **Details**—Displays general information about the SRAM memory interface.
- **Path**—Displays the file system path to the XML file for the currently selected memory interface file.
- **Reload**—Reloads the currently selected memory interface in the table. Use the Reload button if you modify a memory interface XML file on disk after you

configure it for use with your FPGA target. Reload updates the I/O in the LabVIEW project and details information, but changes may not be visible in the Memory Interface or Path dialog boxes.

The PXle-5840 ships with one memory interface support option, which provides access to the external SRAM memory.

Clock Selections Page

Use the **Clock Selections** page to link each clock port defined by the component-level IP (CLIP) to a clock on the FPGA target. You must add the FPGA clock to the LabVIEW project before you can link to the FPGA clock.

To display this page, in the SRAM Properties dialog box, select **Clock Selections** from the **Category** list.

This page includes the following components:

- **Component-Level IP Clock**—Lists clock(s) defined in the CLIP declaration XML file.
- **Connection**—Lists clocks available on the FPGA target.

Power and Thermal Monitoring and Shutdown Conditions

The PXle-5840 is protected against excessive temperatures and power consumption and shuts down in the presence of excessive heat or power consumption. When the module shuts down, it automatically loads a low-power, nearly empty FPGA image. Any user instrument driver session or FPGA I/O stops, and any program that tries to read or write to the module returns an error.

To recover from thermal shutdown, resolve the excessive temperature and restart the system, or reset the device from MAX. Check that the ambient temperature around the chassis is within specifications and that the device is receiving proper airflow. Make sure that chassis fans are clean and that filler panels or slot blockers cover any empty slots to maximize cooling airflow. Position the chassis so that inlet and outlet vents are not obstructed.

To recover from an over-power shutdown, restart the system or reset the device from MAX. Avoid running the application or FPGA VI that triggered the excess power

consumption. Reducing the ambient temperature and improving cooling and airflow may also reduce power consumption.

Monitor temperature and power consumption in your application to detect shutdown conditions. To monitor how far the module is from the temperature limit, use the FPGA Temperature property or the NIRFSA_ATTR_FPGA_TEMPERATURE attribute. The thermal shutdown limit is 98 degrees Celsius. To monitor how far the module is from the power limit, use the Module Power Consumption property or the NIRFSA_ATTR_MODULE_POWER_CONSUMPTION attribute. The power consumption shutdown limit is 100 W.



Note Ensure your application has a wide enough margin to allow for temperature and power variations between your development environment and deployment environment. The deployed application may run hotter or cooler than in it does in development due to hardware differences or variations in ambient temperature, air flow, chassis positioning, adjacent modules, power consumption, and other factors.

PCI Express Interface

The PXle-5840 has a PCI Express (up to Gen3 x8) backplane connection, which is used for programmed I/O, DMA transfers, and peer-to-peer streaming.

Related concepts:

- [Peer-to-Peer Data Streaming](#)

DIGITAL I/O (DIO)

The PXle-5840 DIGITAL I/O (DIO) connector supports eight parallel LVCMOS lines in addition to four lanes of high speed serial multi-gigabit transceivers (MGT), using a 42-pin Molex Nano-Pitch I/O connector. The eight LVCMOS lines support 1.2 V, 1.5 V, 1.8 V, 2.5 V, and 3.3 V voltage levels and can be used in a variety of applications including serial peripheral interface bus (SPI), inter-integrated circuit (I2C) bus, and digital triggering and events. You can control the lines directly from the instrument's onboard FPGA.

The PXle-5840 DIGITAL I/O (DIO) can use DIO signals in a variety of applications including serial peripheral interface bus (SPI), inter-integrated circuit (I²C) bus, and digital triggering and events.

Signal	Type	Direction	Description
MGT Tx± <3..0>	Xilinx Virtex-7 GTH	Output	Dedicated MGT transmit differential pairs (AC-coupled).
MGT Rx± <3..0>			Dedicated MGT receive differential pairs (AC-coupled).
MGT REF±	Differential	Input	User reference clock source for Virtex-7 GTH banks. This clock is multiplexed with DIO <1..0> at the connector. The reference clock function and the DIO function of these pins cannot be used at the same time.
DIO <1..0>	Single-ended	Bidirectional	Single data rate (SDR) is default. Double data rate (DDR) can be achieved using user-supplied component-level IP (CLIP) or IP integration node. DIO <1..0> are multiplexed with a user-supplied MGT reference clock. The DIO and reference clock functions cannot be used at the same time.
DIO <7..2>			
5.0 V	DC	Output	Single-ended LVCMOS digital lines. 5.0 V power source, off by default.


Note Refer to the *PXle-5840*

Signal	Type	Direction	Description
			Specifications document available at ni.com/ manuals for the voltage and current capabilities.
GND	Ground	—	Connector ground.

Cables and Accessories

NI offers several cables and accessories that are compatible with the DIO connector.

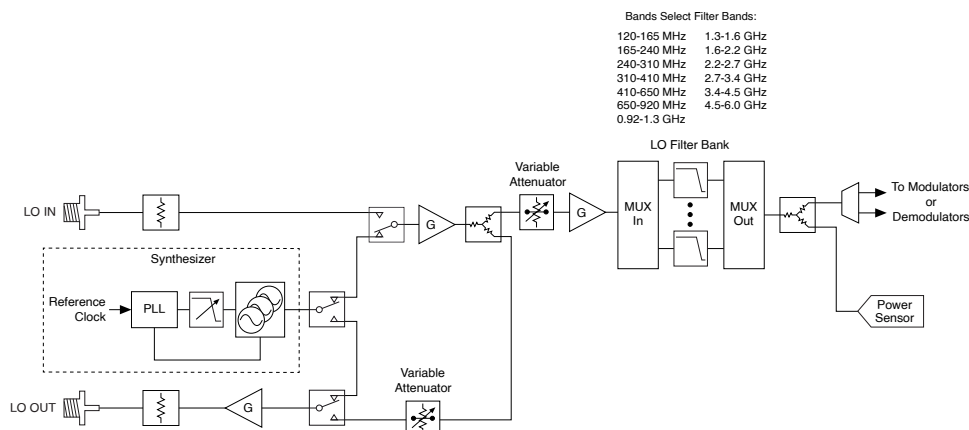


Note These cables and accessories use a custom pinout that matches the PXIe-5840 DIO connector and maintains the 50 Ω transmission line environment. The use of other Molex Nano-Pitch I/O cables is not recommended.

Category	Part Number	Description
Cable	785486-01	OCuLink x4, 1 m cable
	786215-01	OCuLink x4 to mini-SAS HD, 1 m cable
Connector (cable required)	786335-01	SCB-8 Noise Rejecting, Shielded Molex Nano-Pitch I/O connector block

LO Path

The PXIe-5840 has two tunable local oscillators (LO) for the RF input and RF output signal paths. The following high-level block diagram represents the common design of these two LO paths.



The LO path consists of the following individual blocks:

- Synthesizer
- Signal distribution and LO source selection
- LO out signal path

Synthesizer

The onboard synthesizer of the PXIe-5840 consists of integrated tunable voltage control oscillators (VCO), phase-locked loops (PLL), and RF dividers. The combined circuitry is capable of tuning from 9 kHz to 6,000 MHz.

Signal Distribution and LO Source Selection

The LO source is distributed to the downconverter or upconverter and the LO output signal path through the Signal Distribution. You can select the LO source as either the onboard synthesizer or the LO IN front panel connector. Refer to the External Local Oscillator section of the **Local Oscillators** topic for more information about using an external LO with the LO IN front panel connector.

LO Out Signal Path

The PXIe-5840 supports the export of the LO signal to the LO OUT front panel connector. The LO output signal path can either export the LO directly from the synthesizer or through a programmable gain stage. Refer to the **Interconnecting Multiple PXIe-5840 RF Channels (Homogeneous Channel Types)** topic for more information on using the features of the LO output signal path.

Related concepts:

- [Local Oscillators](#)
- [RF Output Subsystem](#)
- [Interconnecting Multiple PXle-5840 RF Channels \(Homogeneous Channel Types\)](#)

Improving NI-TClk Synchronization of RF Instruments

The PXIe-5840 supports NI-TClk, which allows for multi-instrument synchronization with fine alignment. You can use NI-RFSA and NI-RFSG to further optimize NI-TClk synchronization.

Refer to the ***NI-TClk Synchronization Help*** for more information about instrument synchronization.

Related information:

- [NI-TClk Synchronization Help](#)

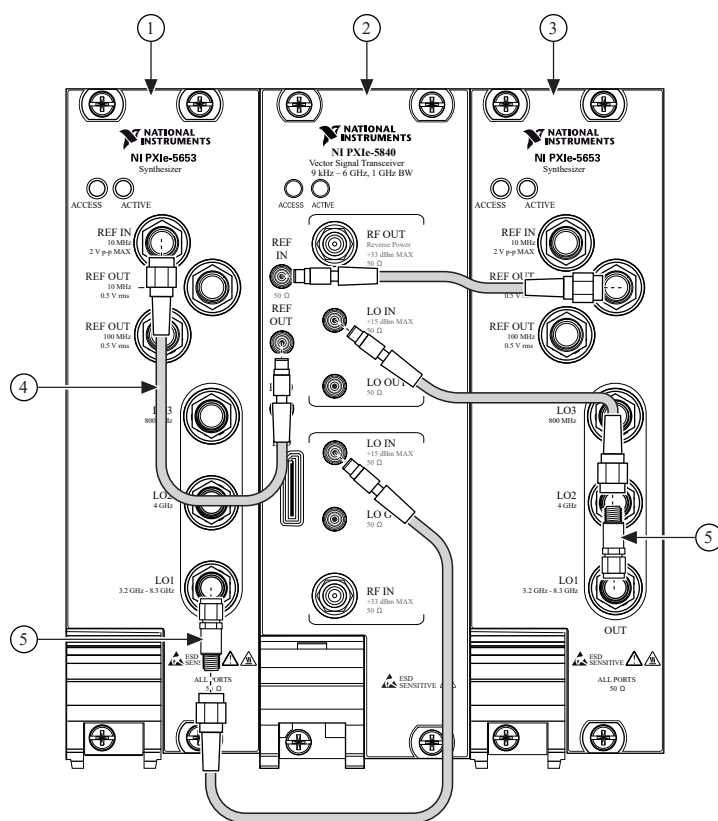
Associating the PXIe-5840 and PXIe-5653 Modules

You must associate the PXIe-5653 LO source with the PXIe-5840 to use the modules together.

Complete the following steps to interconnect the PXIe-5840 and two PXIe-5653 modules. For detailed instructions about how to install a PXI Express module, refer to the ***PXIe-5840 Getting Started Guide***.

1. Install a PXIe-5653 for use with RF IN in an available PXI Express slot.
2. Install a PXIe-5840.
3. Install a PXIe-5653 for use with RF OUT.
4. Using a flexible SMA (m)-to-MMPX (m) cable, connect the REF IN connector on the PXIe-5653 for use with RF IN to the REF OUT connector on the PXIe-5840.
5. Using a flexible SMA (m)-to-MMPX (m) cable, connect the REF OUT connector on the PXIe-5653 for use with RF OUT to the REF IN connector on the PXIe-5840.
6. Using a flexible SMA (m)-to-MMPX (m) cable, add 9 dB of attenuation, and connect the LO1 connector on the PXIe-5653 for use with RF IN to the RF IN LO IN connector on the PXIe-5840.
7. Using a flexible SMA (m)-to-MMPX (m) cable, add 9 dB of attenuation, and connect the LO1 connector on the PXIe-5653 for use with RF OUT to the RF OUT LO IN connector on the PXIe-5840.

The following figure shows the default configuration of the PXIe-5840 and two PXIe-5653 modules.



1. PXIe-5653 For Use With RF IN
2. PXIe-5840
3. PXIe-5653 For Use With RF OUT
4. SMA (m)-to-MMPX (m) Cable (x4)
5. 9 dB of Attenuation (x2)

Associating Devices in MAX

After interconnecting the PXIe-5840 and PXIe-5653 modules, complete the following steps to allow the modules to share an LO:

1. Launch MAX by navigating to **Start » All Programs » National Instruments » Measurement & Automation** or by clicking the MAX desktop icon.
2. In the Configuration pane, expand the **Devices and Interfaces** tree item to see the list of installed devices.
3. Expand the chassis tree item, for example, **NI PXIe-1085 "Chassis 1"**. MAX lists all available devices under the chassis.
4. In the PXIe-5840 Associated Devices section, use the **RF In LO In** list to specify the PXIe-5653 for use with RF IN.

5. For any PXIe-5840 daisy-chained devices, in the PXIe-5840 Associated Devices section, use the **RF In LO In** list or the **RF Out LO In** list and select **External**.
6. Click **Save** in the MAX toolbar.



Note For detailed information about MAX, refer to the Measurement & Automation Explorer Help by selecting **Help » MAX Help**.

Calibrating the Devices

Perform the following steps to calibrate the devices:

1. Run the niRFSA Self Cal VI or niRFSA_SelfCalibrate function or run the niRFSG Self Cal VI or niRFSG_SelfCalibrate function.
Enter the result of your step here (optional).
2. Unassociate the PXIe-5840 and PXIe-5653 modules.
3. Run the niRFSG 5840 Align LO Daisy Chain VI or the niRFSG_5840_AlignLODaisyChain function.

Other Considerations

There are two conditions in which the module will use the PXIe-5840 Onboard LO:

- When NI-RFSA is operating in Spectrum Mode.
- When the center frequency is < 3.2 GHz.

The Perform Thermal Correction VI will not apply correction to the PXIe-5653.



Note (Optional) You can drive the PXI backplane clock with the PXIe-5653 Reference Clock source by connecting the REF OUT connector of the PXIe-5653 for use with RF OUT to the Chassis CLK IN connector and set the Reference Clock Source property or the NIRFSG_ATTR_REF_CLOCK_SOURCE attribute to PXI_ClkMaster. Other modules in the system should set their Reference Clock Source to PXI_CLK.

Peer-to-Peer Data Streaming

The PXIe-5840 supports peer-to-peer (P2P) data streaming using the NI-P2P API. **Peer-to-peer streaming** exchanges data directly between supported devices, bypassing the host computer memory and making applications that require real-time data transfer between devices possible.

For more information about the following terminology, refer to the NI-P2P peer-to-peer streaming driver documentation.

- **Stream**—The data path connection between two peer-to-peer endpoints. A peer-to-peer stream is independent of the data generation and consumption of the two peers.
- **Endpoint**—The collection of hardware resources needed to support one end of a peer-to-peer stream. Multiple peer-to-peer endpoints may exist in a single device.
- **Writer Peer**—The peer sending the data over the bus to the reader peer.
- **Reader Peer**—The peer receiving the data over the bus from the writer peer.

Vector signal transceivers support simultaneous streaming between both peer-to-peer endpoints.

Related information:

- [NI Peer-to-Peer Streaming Help](#)
- [Understanding the Peer-to-Peer Data Streaming Architecture](#)

Configuring a Peer-to-Peer Endpoint

Any driver property that is associated with an instance of an endpoint is an endpoint-based property.

Related tasks:

- [Stopping Peer-to-Peer Generation](#)
- [Stopping Peer-to-Peer Acquisition](#)

Configuring a Peer-to-Peer Endpoint with NI-RFSG

1. Set the Active Channel property using an appropriate string when configuring endpoint-based properties.
The syntax "FIFOendpointN" is used to tell NI-RFSG which RF vector signal transceiver endpoint is being specified, where **N** is an integer starting with 0. If the RF vector signal transceiver supports multiple endpoints, the first is "FIFOendpoint0", the second is "FIFOEndpoint1, " and so on.
2. Set the P2P Enabled property to True.
3. To determine how many endpoints your RF vector signal transceiver supports, query the Endpoint Count property.
4. Perform either a continuous generation or a finite generation.
 - Continuous generation: Set the Number of Records is Finite property to False
 - Finite generation: Set the Is Finite P2P Generation property to True, and set the Number of P2P Samples to Generate property to the number of samples that should be generated

Configuring a Peer-to-Peer Endpoint with NI-RFSA

1. Set the Active Channel property using an appropriate string when configuring endpoint-based properties.
The syntax "FIFOendpointN" is used to tell NI-RFSA which RF vector signal transceiver endpoint is being specified, where **N** is an integer starting with 0. If the RF vector signal transceiver supports multiple endpoints, the first is "FIFOendpoint0", the second is "FIFOEndpoint1, " and so on.
2. Set the P2P Enabled property to True.
3. To determine how many endpoints your RF vector signal transceiver supports, query the P2P FIFO Endpoint Count property.
4. Perform either a continuous acquisition or a finite acquisition.
 - Continuous acquisition: Set the Number of Records is Finite property to False
 - Finite acquisition: Set the Number of Samples is Finite property to True and set the Number of Samples property to the number of samples that should be acquired

Configuring a Peer-to-Peer Stream

To configure a peer-to-peer stream using the NI-P2P API, a writer and reader handle for each endpoint are required.

Use Get Stream Endpoint Handle to generate a reader endpoint handle.

Configuring Flow Control

To configure flow control in NI-RFSA and NI-RFSG, complete the following steps:

1. Call Get Stream Endpoint Handle for your driver to get the RF vector signal transceiver reader handle and the appropriate handle from the writer peer API.
2. Call NI-P2PCreate Peer to Peer Stream to configure NI-P2P with information regarding each endpoint to link the endpoints into a stream.
You must specify both a reader and writer endpoint handle.

Starting Peer-to-Peer Generation

If the RF vector signal transceiver begins generating data from a peer-to-peer stream immediately after the first sample is received, the device may not have enough data to continue the generation and can underflow at startup. This problem is due to latency across the bus, and it is especially likely when heavy, possibly unrelated, traffic is on the bus. To avoid underflow at startup, prime the endpoint with data before starting generation so the device has a backlog of data to insulate the generation from the bursty nature of data flowing across the bus.

The following two methods are available for preparing the RF vector signal transceiver endpoint for startup:

- **NI-RFSG StartTrig.P2PEndpointFullness.Level** —Starts generation after the endpoint receives the specified number of samples. If no number of samples is specified, the driver automatically selects an appropriate value. This method should work for most applications and requires the least amount of configuration. This property is used when StartTrig.Type is set to P2P Endpoint Fullness.
- **Manual preparation**—Configure the application so that the writer peer sends data to the RF vector signal transceiver endpoint prior to the RF vector signal

transceiver initiating generation.

To prepare for generation manually, complete the following steps:

1. Configure both peers for peer-to-peer streaming.
2. Link both peers with NI-P2PCreate Peer to Peer Stream.
3. Enable the stream in either of the following ways:
 - Set `enable_stream` to True with NI-P2PCreate Peer to Peer Stream
 - Call NI-P2PEnable Peer to Peer Stream
4. Start the writer peer first so that it begins sending data to the RF vector signal transceiver prior to initiation.
5. Depending on the language you are using, query the following after starting the writer peer to ensure that sufficient data has been transferred to the RF vector signal transceiver.
 - LabVIEW: NI-RFSGSpace Available in Endpoint
 - C: NIRFSG_ATTR_P2P_ENDPOINT_FULLNESS_START_TRIGGER_LEVEL or NIRFSG_ATTR_P2P_SPACE_AVAILABLE_IN_ENDPOINT
6. Call NI-RFSGInitiate.

Stopping Peer-to-Peer Generation

Avoid receiving an underflow error by using a supported technique to stop peer-to-peer generation.

Use either of the following techniques to stop peer-to-peer generation without generating an underflow error:

Option	Description
Is Finite P2P Generation	If the RF vector signal transceiver receives the specified number of samples from the writer peer, the NI-RFSG session completes without an underflow error. Use Number of P2P Samples to Generate to specify the sample number
Continuous Generation Using User-Requested Abort	Using the NI-RFSGAbort or NI-RFSGCheck Generation Status returns True for <code>Done</code> . However, if the writer peer is not configured carefully for this event, it may overflow because the RF vector signal transceiver is no longer

Option	Description
	allowing it to send data through the stream.

In either preceding technique, use NI-RFSGCheck Generation Status function to determine whether generation is complete. After generation is done, you can abort the generation using NI-RFSGAbort. When generation aborts, all data in the endpoint is cleared to prepare the device for subsequent generations.



Note When using the NI-P2P API to configure the stream, call NI-P2PFlush and Disable Peer to Peer Stream or NI-P2PDisable Peer to Peer Stream and wait for the `done?` parameter from NI-RFSGCheck Generation Status to assert before aborting the RF vector signal transceiver. If data is still in the endpoint when NI-RFSGAbort is called, it is cleared to prepare the device for subsequent generations.

Stopping Peer-to-Peer Acquisition

When stopping peer-to-peer acquisition, you must clear the data from the stream before starting a new acquisition.

Use either of the following techniques to clear the stream:

- Call NI-P2PFlush and Disable Peer to Peer Stream before starting a new acquisition. This function automatically clears the remaining data from the stream.
- Configure the reader peer to read the remaining samples in the stream, then call NI-P2PDisable Peer to Peer Stream before starting a new acquisition.

Device Warm-Up

NI recommends warming up the PXIe-5840 hardware for 30 minutes before operation.

The unit is fully functional prior to this time, but frequency, amplitude accuracy, and other specifications are not at warranted levels until the device has fully completed warming up.



Note Warm up begins when the PXI Express chassis has been powered on and the operating system has completely loaded.

Power On, Reset, and Download Conditions

The PXIe-5840 sets some hardware circuitry to certain states at power on and at device reset. The PXIe-5840 applies certain conditions to the device state upon FPGA reset.

Power On Conditions

Power on conditions are present after powering on or restarting the system and until an FPGA VI has been uploaded to the device.

- DIO lines are configured as input terminals.
- PFI 0 line is configured as an input terminal.
- PXI trigger lines are not configured and appear to the bus as high impedance.
- ADCs are configured by the board driver for 1.25 GS/s operation.
- DACs are configured by the board driver 1.25 GS/s operation.

Reset Conditions

The following conditions apply to the FPGA reset device state, which is supported using the Reset Device button in MAX or by using the NI System Configuration API.

- DIO lines are configured as input terminals.
- PFI 0 line is configured as an input terminal.
- PXI trigger lines are not configured and appear to the bus as high impedance; however, reservations are maintained.
- ADC states are maintained.
- DAC states are maintained.



Note Reset conditions apply only when using the instrument design libraries.

Download Conditions

The following conditions apply to the device state upon downloading a new FPGA VI to the PXIe-5840.

- DIO lines are configured as input terminals.
- PFI 0 line is configured as an input terminal.
- PXI trigger lines are not configured and appear to the bus as high impedance; however, reservations are released.
- ADC states are maintained.
- DAC states are maintained.



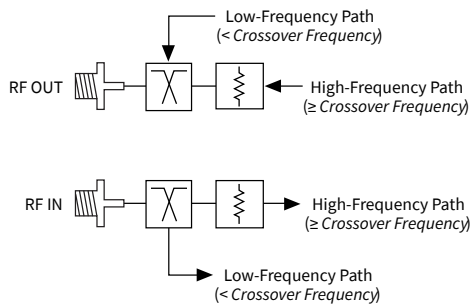
Note The Data Clock is disabled immediately after downloading a new FPGA VI to the PXIe-5840. The driver re-enables the Data Clock automatically.

Spurious Performance

Direct conversion topologies do not allow for multiple stages of filtering common in multistage IF systems. Any signals present within the instantaneous bandwidth of the device are converted down to baseband.

RF Path Transitions

The PXle-5840 supports acquisition and generation of RF signals from to . For both the RF Input and RF Output channels, the transition from low frequency to high frequency is implemented with a passive diplexer scheme. This passes RF energy below 120 MHz to the low frequency path and RF energy above 120 MHz to the high frequency path. Because the diplexer has a frequency response of its own, it is possible to extend RF frequency coverage above or below 120 MHz in both paths.



While the automatic selection of the signal path using the NI-RFSA or NI-RFSG driver is optimal for most use cases, some applications may require you to select a particular mode of operation. Example situations where this may be useful include measurements or applications sensitive to speed, phase noise, relative gain, or dynamic range.

For example, the high frequency path is implemented with a wide range of amplification and attenuation as a result of more stages within the signal chain. This is useful for applications that may require a significant amount of analog attenuation or amplification. The high frequency path also mixes the RF signal to and from baseband, so phase noise may be degraded compared to a directly sampled signal. Some performance parameters may have more or less impact depending on the nature of the application. Refer to **RF Input Subsystem** and **RF Output Subsystem** for more information about the PXle-5840 components and frequency paths.

RF Input Signal Path Selection

The primary method of controlling which path is used on the PXIe-5840 is based on center frequency. For RF Input, this frequency is tied to the NI-RFSA IQ Carrier Frequency property in I/Q mode. Refer to the ***NI RF Vector Signal Analyzers Help*** for more information about using the PXIe-5840 in I/Q mode.

The NI-RFSA Downconverter Center Frequency property, NI-RFSA LO Frequency property, or NI-RFSA Downconverter Frequency Offset property can be used to further specify which path the device uses in addition to the NI-RFSA IQ Carrier Frequency property. You can use the NI-RFSA Downconverter Center Frequency property, or, for an external LO, the NI-RFSA LO Frequency property to lock the device into the low-frequency or high-frequency path despite the value specified for I/Q carrier frequency. When you set the NI-RFSA Signal Bandwidth property, NI-RFSA may choose a downconverter center frequency for you. Refer to the ***Automatic Frequency Offset*** section for information on how to automatically offset the downconverter frequency.



Note The downconverter center frequency is coerced to 0 Hz when it is set to any value less than 120 MHz. Refer to the ***Programming Reference*** section in the ***NI RF Vector Signal Analyzers Help*** for more information about the NI-RFSA Downconverter Center Frequency property.

Figure 1. I/Q Carrier Frequency or Center Frequency Set to 100 MHz

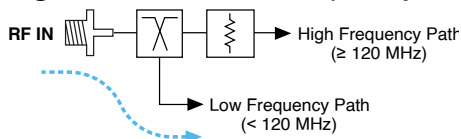


Figure 1. I/Q Carrier Frequency or Center Frequency Set to 125 MHz

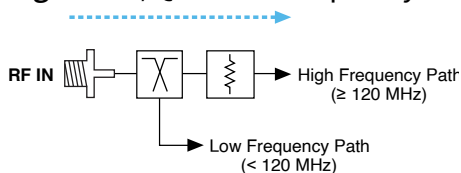


Figure 1. I/Q Carrier Frequency or Center Frequency Set to 100 MHz and Downconverter Center Frequency Set to 125 MHz

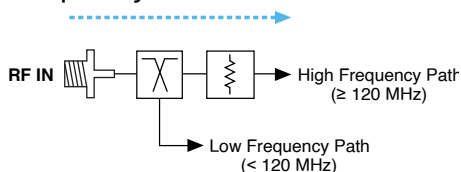
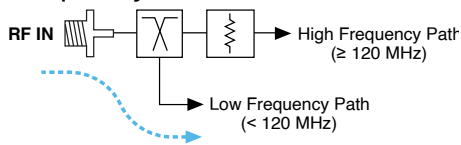


Figure 1. I/Q Carrier Frequency or Center Frequency Set to 150 MHz and Downconverter Center Frequency Set to Less Than 120 MHz



Note Calibrated performance is bound by the equalization bandwidth at a given frequency. As such, the ability to digitally tune to a frequency with the NI-RFSA IQ Carrier Frequency property or NI-RFSA Center Frequency property is restricted to within $\pm 0.5 \times$ Equalized Bandwidth of the downconverter center frequency. You can exceed this limitation by using the NI-RFSA Allow Out of Specification User Settings property.

RF Output Signal Path Selection

Similar to RF Input, the RF Output channel is divided into a low frequency signal path and high frequency signal path. RF energy is diverted to either path through a diplexer with a crossover frequency of 120 MHz. The signal path is automatically configured when the NI-RFSG Frequency property is modified. If you set the NI-RFSG Frequency property value below 120 MHz, the low frequency signal path is used, while frequency values greater than or equal to 120 MHz are generated with the high frequency signal path.

Similar to RF input signal path selection, in I/Q mode you can override the signal path used for RF output with the NI-RFSG Upconverter Center Frequency property. Using the NI-RFSG Upconverter Center Frequency property locks the device into the low-frequency or high-frequency signal path despite the specified frequency value. If you set the NI-RFSG Signal Bandwidth property, NI-RFSG may select an upconverter center frequency for you. Refer to the **Automatic Frequency Offset** section for information on how to automatically offset the upconverter frequency.



Note The NI-RFSG Upconverter Center Frequency property is coerced to 0 Hz when set to any value less than 120 MHz. Refer to the **Programming Reference** section in the *NI RF Signal Generators Help* for more information about the NI-RFSG Upconverter Center Frequency property.

The following figures illustrate examples of configuring the signal path selection based on the NI-RFSG Frequency and NI-RFSG Upconverter Center Frequency properties.

Figure 1. Frequency (Hz) Set to 100 MHz

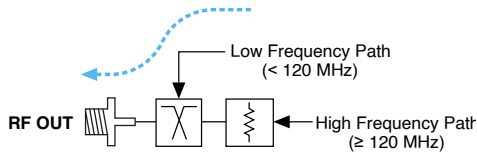


Figure 1. Frequency (Hz) Set to 125 MHz

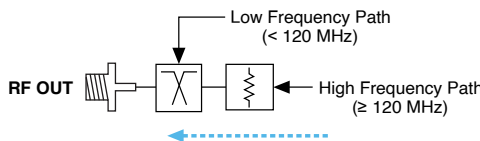


Figure 1. Frequency (Hz) Set to 100 MHz and Upconverter Center Frequency Set to 125 MHz

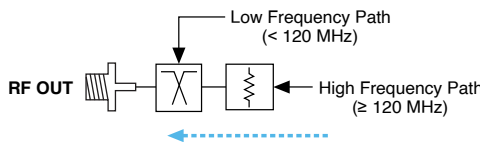
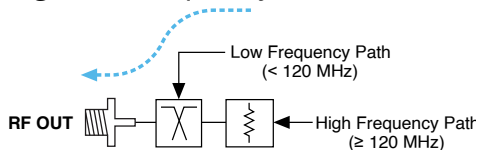


Figure 1. Frequency (Hz) Set to 150 MHz and Upconverter Center Frequency Set to Less Than 120 MHz



Note Calibrated performance is bound by the equalization bandwidth at a given frequency. As such, the ability to digitally tune to a frequency with the Frequency property is restricted to within $\pm 0.5 \times \text{Equalized Bandwidth}$ of the upconverter center frequency. It is possible to exceed this limitation by using the NI-RFSG Allow Out of Specification User Settings property.

Related concepts:

- [RF Input Subsystem](#)
- [RF Output Subsystem](#)

Related tasks:

- [RF Input Signal Path](#)
- [RF Output Signal Path](#)
- [Using In-Band Retuning](#)

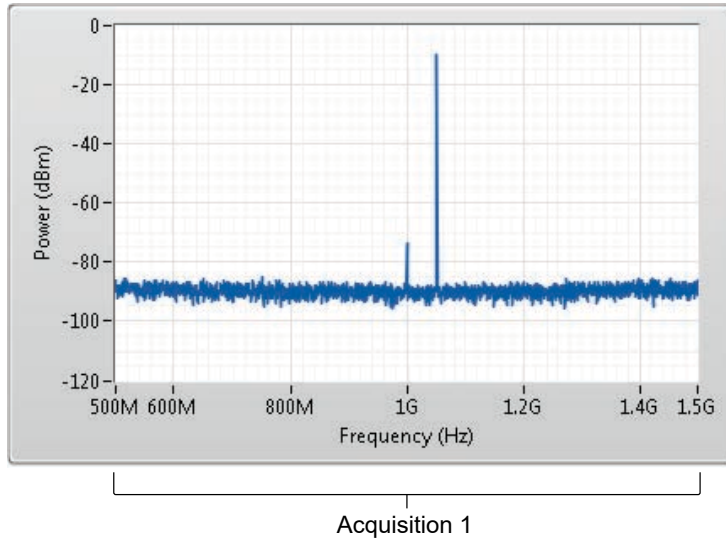
Frequency Offset

You can combine the capabilities of LO tuning and digital frequency shift function through additional digital processing on the FPGA to configure the PXIe-5840 to operate with a downconverter or upconverter frequency offset. Frequency offset tunes the LO away from the signal. Use the NI-RFSA Downconverter Frequency Offset Mode property or the NI-RFSG Upconverter Frequency Offset Mode property to ask the driver to select an offset, or set the **NI-RFSA Downconverter Frequency Offset** property or the **NI-RFSG Upconverter Frequency Offset** property to configure a user-defined offset.

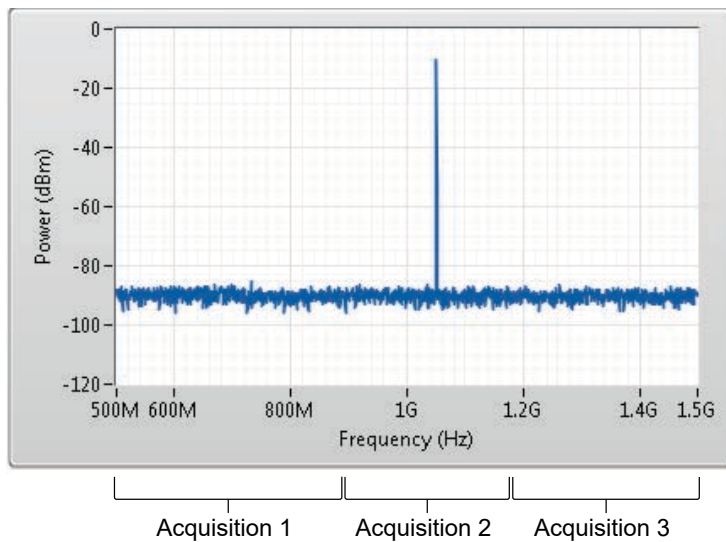
The use of frequency offset through digital frequency shift is at the expense of restricted instantaneous bandwidth. For example, for an automatic offset, the driver places the LO outside the signal bandwidth which restricts the signal bandwidth to 50% of the device instantaneous bandwidth after subtracting an LO guard band.

The following figures illustrate a 1,000 MHz direct conversion acquisition versus a 1,000 MHz frequency offset acquisition. Notice the different constraints and distortions in each figure.

The direct conversion acquisition illustrated in the following figure involves a single acquisition to cover 1,000 MHz using the PXIe-5840. There are distortions present that effectively constrain the dynamic range of the spectrum, however. A primary example of this is the residual LO power, also known as carrier or LO leakage. Residual LO power is an artifact of the quadrature architecture used in direct conversion devices. Use the equation $|x| > (BW/2)$ to calculate the minimum frequency shift needed to avoid LO leakage, where x is the minimum digital frequency shift and **BW** is the required bandwidth.

Figure 1. Spectrum Acquisition with Direct Conversion (Single Span)

The following figure illustrates that you can acquire the same 1,000 MHz using frequency offset with minimal distortion present from direct conversion architectures. However, when you use frequency offset, the effective bandwidth of the device is restricted. The 1,000 MHz acquisition that took a single acquisition using direct conversion takes three acquisitions using frequency offset configuration.

Figure 1. Spectrum Acquisition with Frequency Offset (Multi-Span)

Images can occur when using the PXIe-5840 with frequency offset because of imperfections of the gain imbalance and skew between the I and Q channels. Residual sideband images are suppressed by calibration, but images can still be a complication when using frequency offset.



Note If you use the LO in integer mode, the usable bandwidth may be further reduced by frequency error correction.

Using In-Band Retuning

In-band retuning allows an NI VST to quickly tune between signals of interest or generation within a given instantaneous bandwidth by keeping the LO constant and using digital frequency shifts in the digital data path. The advantages of in-band retuning include reduced settling time for both frequency and amplitude.

In-band retuning can occur only within the supported instantaneous bandwidth of the instrument. You can use digital tuning in combination with LO tuning to more efficiently sweep over a spectrum for supported applications.

You can use in-band retuning by setting the instrument instantaneous bandwidth and leaving the downconverter center frequency fixed, which significantly reduces reconfiguration and settling times.

To perform in-band returning, set the relevant property, based on your RF driver as follows, to a value within the instantaneous bandwidth of the VST.

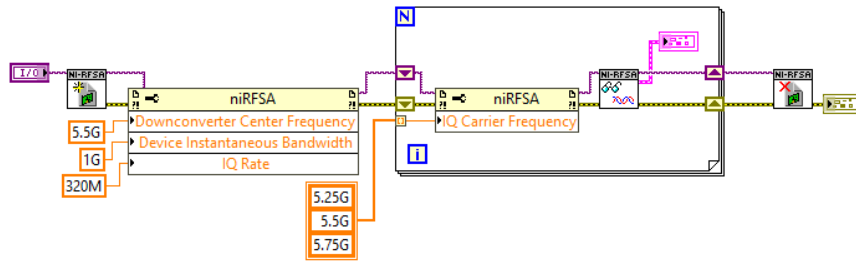
- NI-RFSA: Downconverter Center Frequency
- NI-RFSG: Upconverter Center Frequency

Programming for In-Band Returning

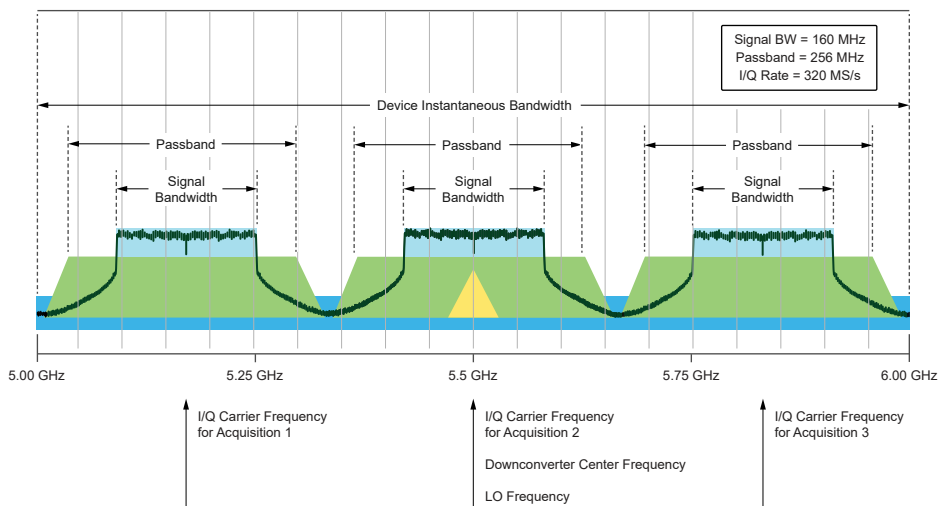
This example shows how to programmatically set an NI VST for in-band retuning during acquisition using NI-RFSA.



Note This example illustrates frequency and bandwidth concepts by portraying a generic example instrument of 1 GHz bandwidth; values and figures may not necessarily reflect the frequencies, bandwidth, or LO step size of your instrument.



The following figure shows three acquisitions with only digital frequency shift reconfigurations.



Local Oscillators

There are separate local oscillators (LOs) on the PXIe-5840 for each RF signal path. The separate LOs allow for different LO frequencies between RF input and RF output channels.

The individual LOs of RF input and RF output channels are referenced to a common clock source in their phase-locked loop circuitry. This configuration ensures that the relative frequency error between the individual LOs is a net of zero and allows for precision tuning of channels in the frequency domain. If you specify an external Reference Clock source, both RF input and RF output LOs reference this source.

You can configure each oscillator in both integer and fractional tuning modes.

The following table describes each mode and its capabilities. The configured tuning mode is unique for each LO.

Tuning Mode	Supported Frequency Step Resolution
Integer	1 MHz
	5 MHz
	10 MHz
	25 MHz
	50 MHz
	100 MHz
Fractional	≥50 kHz, configurable 400 kHz default

Running the device in fractional tuning mode can create close-in spurs related to the intermodulation of the VCO and the phase detect frequency harmonics. Refer to the **PXIe-5840 Specifications** document for more information about spurious performance.

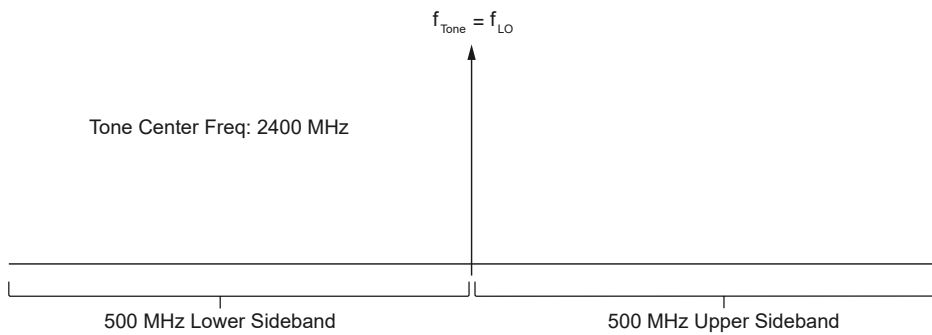
Frequency Correction (LO Coercion)

In both integer and fractional tuning modes, you can use digital frequency correction in the FPGA to compensate for any difference between the requested frequency and the coerced LO frequency. Refer to the **PXIe-5840 Specifications** for more information about integer and fractional tuning modes.

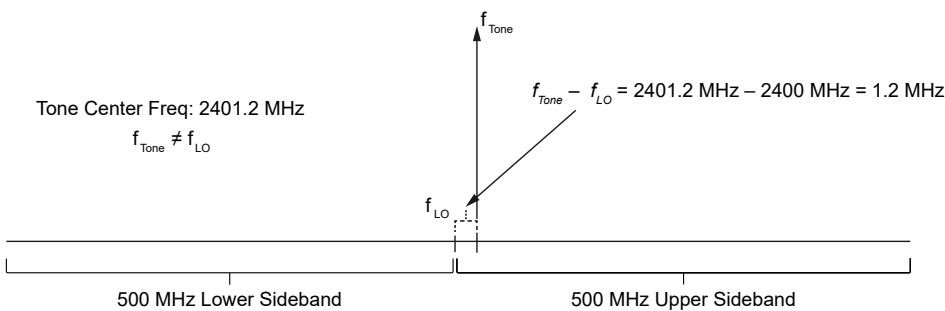


Note Digital frequency correction is implemented automatically in the NI-RFSA and NI-RFSG APIs.

The following figure shows a tone generated at a tuned frequency of 2,400 MHz. The tuned frequency is an even multiple of the 5 MHz integer step size and as such is also the LO frequency. This example does not require digital shift, so 1 GHz of equalized bandwidth is available.



The following figure shows a tone generated at a tuned frequency of 2,401.2 MHz. The closest multiple of the 5 MHz integer step size is 2,400 MHz, which creates a frequency error of 1.2 MHz between the requested frequency and the LO frequency. Digital frequency shifting on the FPGA corrects for the 1.2 MHz offset.



External Local Oscillator

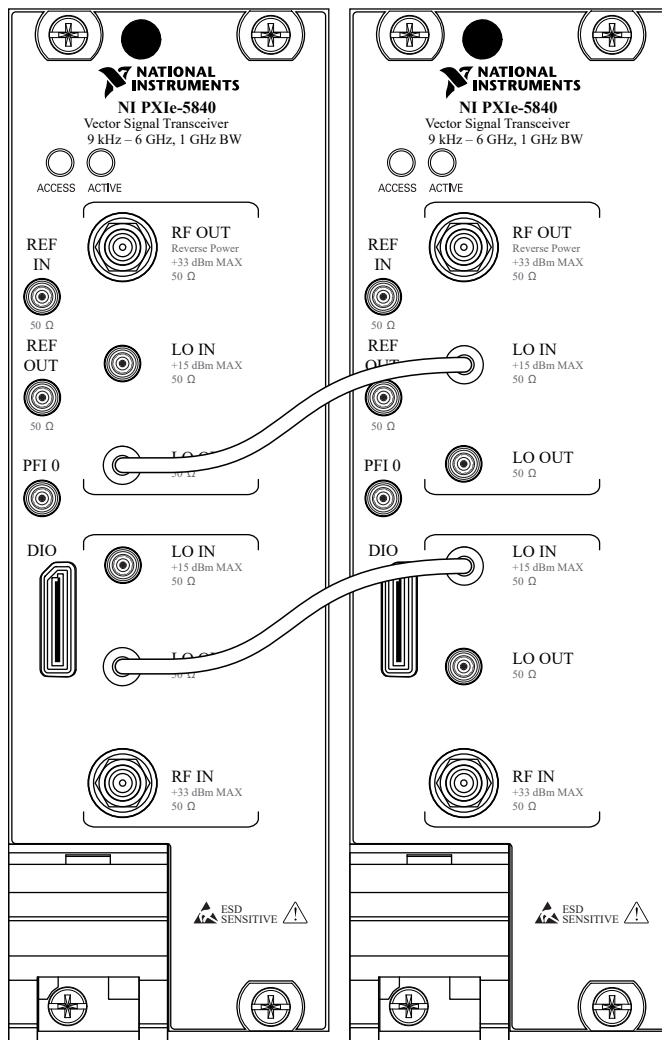
The PXIe-5840 uses an internal measurement circuit that allows flexibility in external LO power. This flexibility ensures that the external LO arrives at the mixing stage with the same power level as the internal LO, which subsequently minimizes effects on sensitive specifications such as amplitude accuracy, residual LO power, and quadrature impairments.

By default, the PXIe-5840 is calibrated to assume a nominal external LO present at the LO IN (RF IN 0 and RF OUT 0) front panel connectors at 0 dBm. NI recommends external LO calibration if the external LO source varies from this nominal value by more than ± 0.25 dB. Calibrating the external LO aligns the external LO path gain of the PXIe-5840 over the full frequency range for the specific external LO source.

Interconnecting Multiple PXIe-5840 RF Channels (Homogeneous Channel Types)

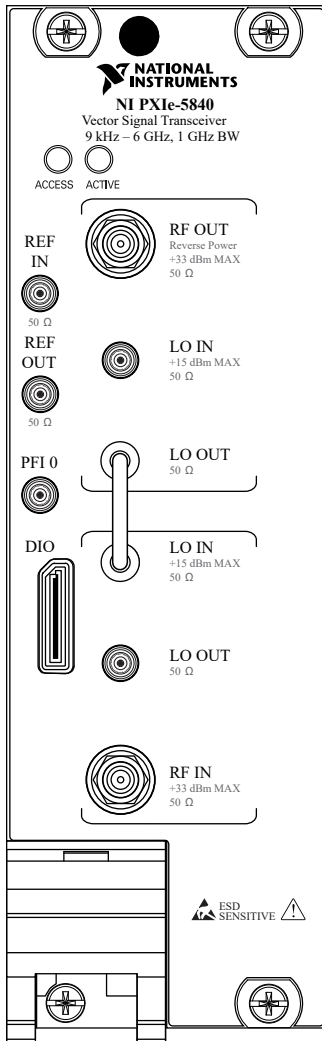
There are certain RF applications that benefit from phase coherency or phase synchronization between multiple RF input and/or RF output channels.

One key aspect of this synchronization is sharing local oscillators (LO) to provide a common phase reference to the RF input or RF output channel of each interconnected module. The PXIe-5840 allows for import and export of the individual LOs on each RF input and RF output channel. The following figure illustrates recommended cabling for interconnecting LOs between multiple modules. The connections shown are between channels of similar type (for example, RF input to RF input or RF output to RF output).

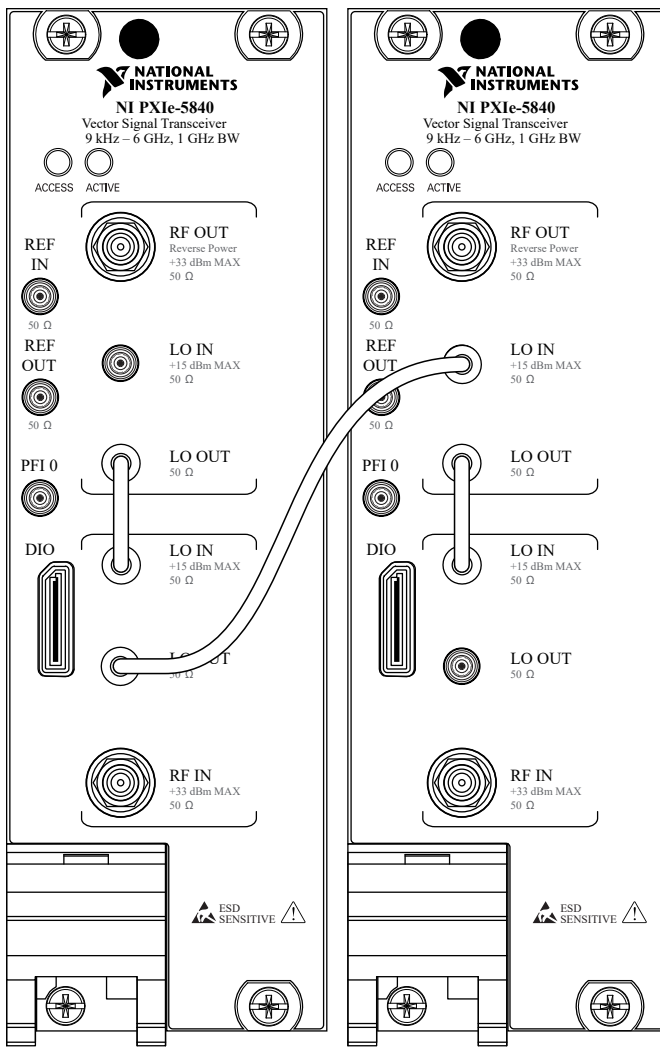


Interconnecting Receive and Transmit Channels

A more specific application may require the RF input and RF output channels to share an LO. The following figure illustrates how to share an LO between the RF input and RF output channels on a single module.



The following figure illustrates how to share an LO between the RF input and RF output channels on multiple modules.



Note For upconverter or downconverter center frequencies less than 120 MHz, the PXIe-5840RF input and output path directly sample the RF signal without an LO driven mixing stage. As such, LO sharing below 120 MHz is not supported.



Note The RF output channel expects a 3 dBm LO power level above 3.6 GHz, and the RF input channel expects a 0 dBm LO power level. This expectation can affect performance for frequencies above 3.6 GHz and should be considered when implementing applications.

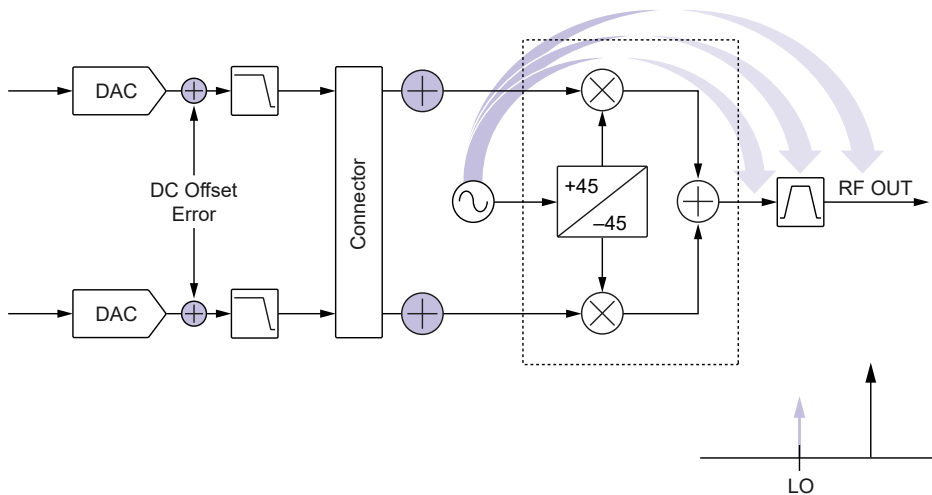
Quadrature Mixing (Direct Conversion)

Quadrature mixing (direct conversion) allows for the complex modulation or

demodulation of signals as represented by two orthogonal signals, I and Q. Quadrature mixing has the added benefit of an increased complex bandwidth that allows for bandwidths up to the sample rate of the DAC.

Analog quadrature mixing exposes the signal to impairments because of the imperfections of the circuitry involved. These imperfections can create distortion products or unwanted signals, which may degrade modulation and demodulation quality. The following section illustrates key impairments involved in quadrature mixing and how they affect the respective signal.

The following figure shows a typical quadrature transmission device. The shaded sections represent the presence of several impairments, including DC offsets within the various baseband sections and LO signal power leaking into the RF path because of insufficient isolation.

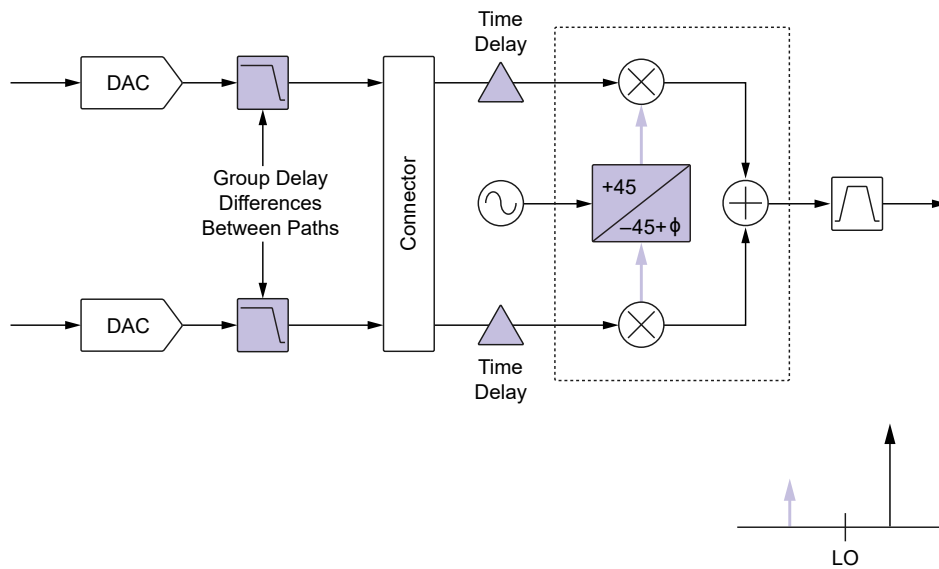


Offsets and the lack of LO isolation can cause unwanted distortion, defined as residual LO power, which is always centered on the tuned LO frequency. Digital equalization schemes can help suppress residual LO power. This suppression improves the performance of the system for many modulation schemes.

For an I/Q waveform to be represented perfectly, I and Q should have a gain ratio of 1 and be 90 degrees out of phase (orthogonal). Several components in an analog quadrature mixing system can corrupt the gain or the phase offset. These impairments are known as gain imbalance and skew.

The shaded sections in the following figure represent several components that affect

the phase offset and create skew.



The presence of gain imbalance or skew-related impairments creates a distortion at the negative complex frequency of the tone of interest. This distortion is referred to as the residual sideband image or the image. Wideband applications drive the necessity to suppress this distortion to avoid unwanted signals that can corrupt transmitted or received data. On the PXIe-5840 calibrated digital equalization suppresses most of the image to improve the performance of the system.

Configuring Attenuator Hold

Attenuator hold—holding the power level fixed while adjusting the digital gain—ensures the analog path is not altered while the instrument is in the Generation state.

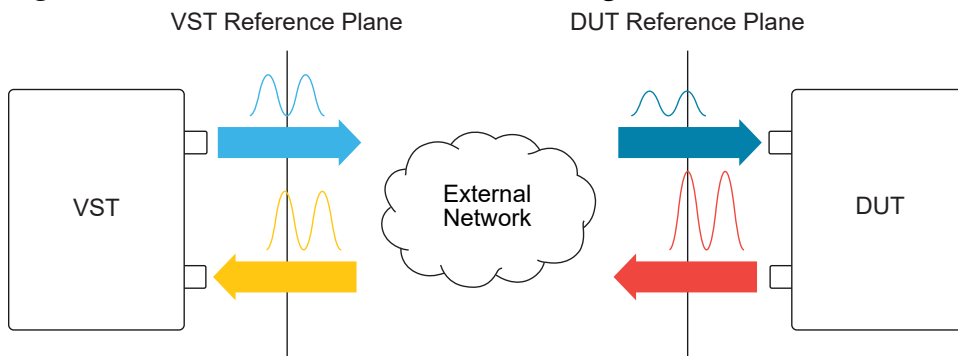
To configure attenuator hold, adjust the digital gain by completing the following steps:

1. Configure the NI-RFSGPower Level (dB) property to the max desired output power level.
2. Adjust the digital gain using the NI-RFSGDigital Gain (dB) property to reach the final desired output power level.
3. Initiate generation.
4. Adjust the digital gain to adjust the output power as desired.

De-embedding Overview

NI RF instrument performance specifications are for signals at the instrument's ports. However, you must also account for external cabling and components between the instrument and DUT, which also affects input and output signals.

Figure 1. Effect of the External Network on Signals



De-embedding is the process of removing the effects of these components on an input or output signal, so the accuracy of the instrument is extended to the DUT.

The NI-RFSA and NI-RFSG instrument drivers can de-embed measurements and generations using your characterization data. To use this feature, first characterize the external components with an S-parameter table. Once the tables are passed to the driver, they can be applied to move the reference plane from the instrument port to the DUT port.

The NI driver compensates for the effects of the networks by modifying the analog path and adjusting the data with digital signal processing (DSP).

When using NI-RFSG, the signal seen at the DUT port matches the requested signal. When using NI-RFSA, the data returned from the driver reflects the signal at the DUT port rather than the signal seen at the instrument's input port.

S-parameters

S-parameters characterize the effects of a linear network on a signal when it passes from one port of the network to another port. For purposes of de-embedding for VST operation, the instrument driver compensates for the effects of the networks by modifying the analog path and adjusting the data with DSP.

S-parameters of the de-embedding network can be obtained by either extracting them using a vector network analyzer (VNA) or by simulating the network in an RF computer assisted design (CAD) tool.

NI-RFSA and NI-RFSG support de-embedding of two port networks. Two port networks are characterized by four s-parameters. S-parameters are written in the format ***S_{nm}***, where ***n***, designates the receiving port, and ***m***, designates the driving port. Each S-parameter is referred to as a gain or reflection term.

The following table illustrates which terms characterize gain or reflection of the network.

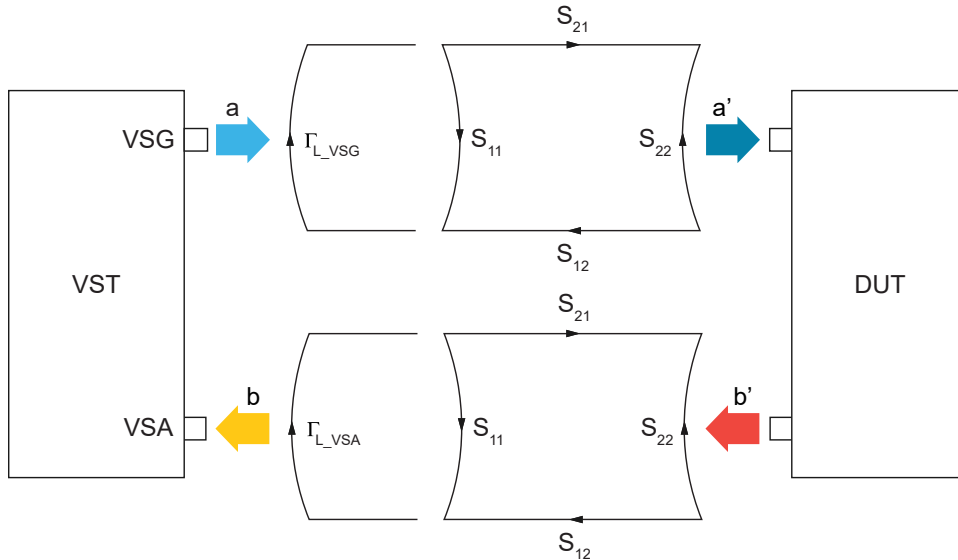
Table 5. S-parameters

S-parameter	Description
S_{11}	reflection (input reflection)
S_{12}	gain (forward transmission)
S_{21}	gain (reverse isolation)
S_{22}	reflection (output reflection)

Gain terms, S_{12} and S_{21} , model the gain an input signal experiences as it passes through the network to the receiving port. The reflection terms, S_{11} and S_{22} , are used when computing the effects of signal reflection due to impedance mismatch between the network's ports and driving ports.

The following figure provides a visualization of the external network as an S-parameter model. Signal ***b'***, output from the DUT, passes through the external network and arrives at the VST as signal ***b***. Signal ***a***, generated by the VST, passes through the network and arrives at the DUT as signal ***a'***. The following are reflection terms for the instrument ports:

- Γ_{L_VSA}
- Γ_{L_VSG}

Figure 1. S-parameter modeling of an external network for NI-RFSA and NI-RFSG

Scalar De-embedding

Scalar de-embedding compensates only for the gain term of the S-parameters.

In the previous figure, the DUT output is connected to port2 of the external network and port1 is connected to the NI device port. By convention, the S12 parameter specifies the gain due to the network, and applied to the signal ***b'*** output from the DUT toward the VSA port. NI-RFSA computes the signal at the DUT port using the following formula:

$$b' = \frac{b}{S_{12}}$$

To acquire the output signal of the DUT and not the signal seen at the NI instrument's port, NI-RFSA compensates for the network by amplifying the signal. The driver makes DSP adjustments to compensate for any remaining effects that analog path adjustments do not compensate for. NI-RFSA returns data reflecting the amplitude of the signal at the DUT.

Similarly, when using NI-RFSG scalar de-embedding, the driver computes the output signal at the DUT port using the following formula:

$$a' = S_{21} \times a$$

The receiving port in this case is port2 at the DUT and the input port is port1 at the NI instrument's port. NI-RFSG compensates for the network via analog path adjustments and DSP so that the signal you request arrives at the DUT with the correct amplitude.

Configuring Frequency and Bandwidth for PXIe-5840

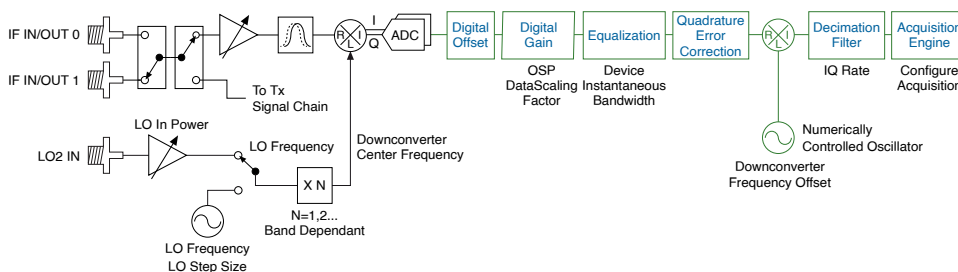
Use the NI-RFSA and NI-RFSG drivers to configure the PXIe-5840 instrument for optimal performance by specifying frequency and bandwidth constraints.

The following table shows the equivalencies between NI-RFSA and NI-RFSG properties mentioned throughout the section.

Table 6. NI-RFSA and NI-RFSG Frequency and Bandwidth Configuration Properties

NI-RFSA Property	NI-RFSG Property
IQ Carrier Frequency	Frequency
Downconverter Center Frequency	Upconverter Center Frequency
Downconverter Frequency Offset	Upconverter Frequency Offset
LO Frequency	LO Frequency
Device Instantaneous Bandwidth	Device Instantaneous Bandwidth
Signal Bandwidth	Signal Bandwidth
IQ Rate	IQ Rate
Downconverter Frequency Offset Mode	Upconverter Frequency Offset Mode

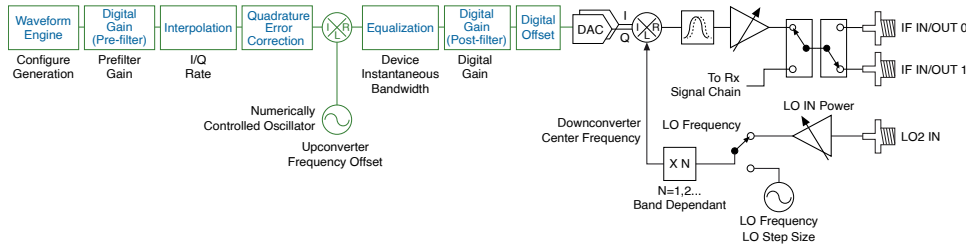
The following block diagram represents the PXIe-5840 RF input connectors and the associated NI-RFSA properties.



Note The names of the input connectors change depending on your

instrument configuration.

The following block diagram represents the PXIe-5840 RF output connectors and the associated NI-RFSG properties.



Note The names of the output connectors change depending on your instrument configuration.

Frequency and Bandwidth Configuration Terminology

Refer to the following list of terms when configuring frequency and bandwidth.

- **I/Q Rate**—The effective sampling rate of the baseband signal chain. Setting a value lower than the maximum will limit the available passband.
- **I/Q Carrier Frequency**—The center frequency of the waveform data acquired or generated.
- **Downconverter Center Frequency**— The frequency present at the mixer during downconversion or upconversion. This frequency is derived from the LO frequency through a series of multipliers. The multiplication factor may be 1, 2, 4, or 8, depending on the target frequency. In a direct conversion architecture, the downconverter center frequency contains LO leakage in the I/Q data.
- **LO Frequency**— The frequency of the local oscillator as present at the LO IN or LO OUT port. This frequency may or may not be equal to the downconverter center frequency depending on the conversion architecture and any frequency multipliers in the LO path. The signal from the onboard LO or the LO IN port passes through signal conditioning circuits and frequency multipliers or dividers to hit the mixer at the required frequency and power.
- **Device Instantaneous Bandwidth**— The total calibrated bandwidth available through the instrument signal path, centered at the downconverter center frequency. For example, if the downconverter center frequency is 6 GHz and the

device instantaneous bandwidth is 1 GHz, an acquisition can contain calibrated data from 5.5 GHz to 6.5 GHz.

- **Signal Bandwidth**—When performing a signal acquisition, **signal bandwidth** is the bandwidth of the signal present at the input port, centered at the I/Q carrier frequency. When performing a signal generation, **signal bandwidth** is the bandwidth of the waveform to be generated, centered at the I/Q carrier frequency.
- **Passband**—The bandwidth able to be acquired based on the I/Q rate, centered at the I/Q carrier frequency. This is usually defined at 80% of the I/Q rate. For example, an I/Q rate of 100 MS/s results in a passband of 80 MHz. Note that the passband edge may fall outside of the device instantaneous bandwidth edge and will, therefore, have aliased or uncalibrated data.
- **LO Step Size**—The quantum at which the LO frequency can be tuned. You can set the LO Step Size property or, on supported instruments, the VCO Step Size property to control the step size at the mixer or on the onboard LO (before multipliers), respectively, to achieve different hardware performance.

For example, assume the LO step size for an instrument is 2 MHz and the downconverter center frequency is set to 5,001.5 MHz. The downconverter center frequency will be coerced to 5,002 MHz, and the remaining 500 kHz shift will be applied digitally.

- **LO Power**—When using an external LO, the power of the LO is important for maintaining good image and LO leakage performance because the impairments correction is calibrated for a specific LO power at the mixer. Based on the LO IN power, NI-RFSA configures the LO signal path to achieve a mixer power close to the mixer power used during impairment calibration. You can also set the LO OUT power to apply gain to the output signal to avoid power loss when in an LO daisy-chain configuration.

Frequency and Bandwidth Selection to Optimize Performance

You can configure frequency and bandwidth settings of an NI VST to optimize measurement performance for different types of applications.



Note This information illustrates frequency and bandwidth concepts by portraying a generic example instrument of 1 GHz bandwidth; values and

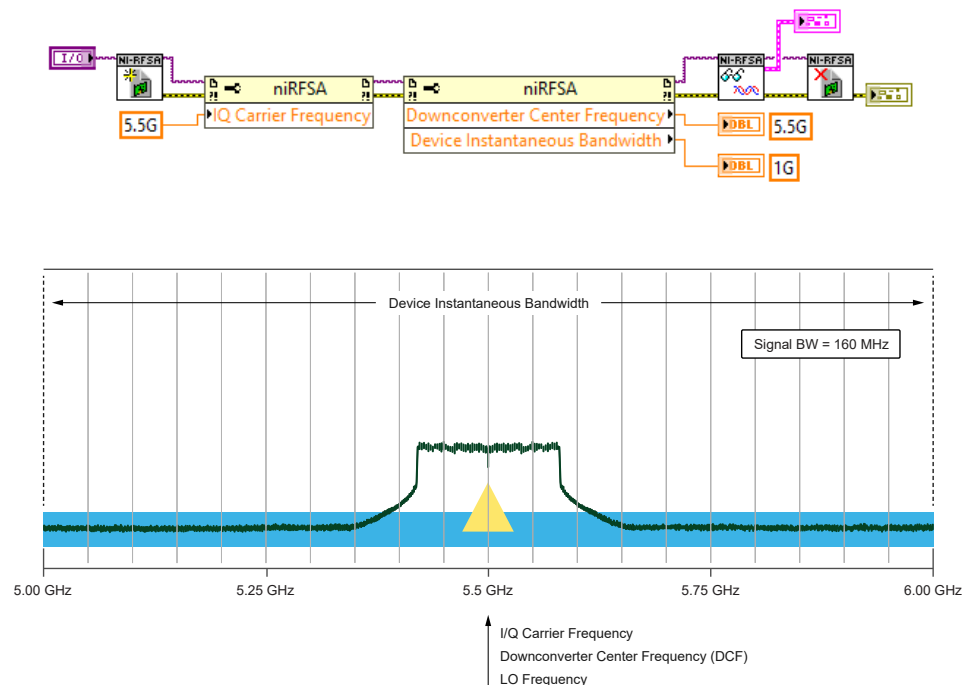
figures may not necessarily reflect the frequencies, bandwidth, or LO step size of your instrument.

Basic Behavior

For a simple acquisition, you can set the I/Q carrier frequency and the I/Q rate. When you do not specify a bandwidth constraint, NI-RFSA selects the widest filter for the given frequency region. You can obtain the bandwidth of the instrument for this configuration by querying the Device Instantaneous Bandwidth property. To determine the center of the device instantaneous bandwidth, you can query the Downconverter Center Frequency property.

You can specify the I/Q rate, which configures the decimation filter and, as a result, configures the available passband. When oversampling, the passband is often greater than the actual signal bandwidth present at the port, so specifying the Signal Bandwidth property gives the driver additional information about the requested bandwidth.

The following example illustrates the default behavior.

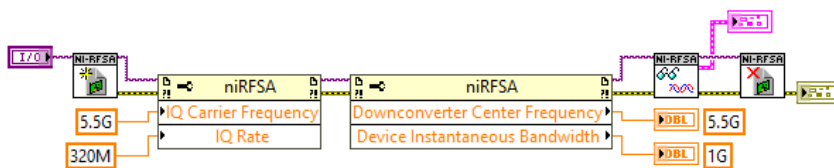


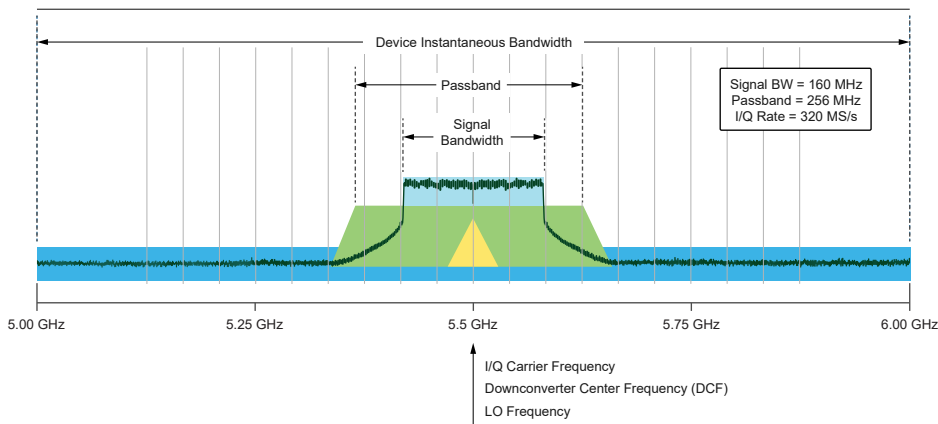
Specifying Device Instantaneous Bandwidth

In some cases, the default behavior may not be optimal. You can improve the default behavior by providing NI-RFSA with more information about the system. By setting the Device Instantaneous Bandwidth property, you are specifying how much instrument bandwidth is required. The instrument bandwidth is used in filter selection and is only coerced up, so the filters chosen will always yield a bandwidth as wide or wider than requested. You can always read back the coerced or actual device instantaneous bandwidth to find out how much bandwidth is available in the given configuration. For example, if only 160 MHz of bandwidth is needed from an instrument and the next largest filter for that instrument is 1 GHz, NI-RFSA chooses the 1 GHz filter.

Oversampling

In the following example, the I/Q rate is set to 320 MS/s, even though the waveform signal bandwidth is only 160 MS/s. This is referred to as **oversampling**. The passband is 80% of the I/Q rate, or 256 MHz. In this example, because the passband extends outside the device instantaneous bandwidth, frequency content outside the device instantaneous bandwidth will be present in the time-domain data. This frequency content is usually filtered out by demodulation algorithms but may be problematic if you are analyzing the time-domain data manually, and there is a strong interfering signal in that region.





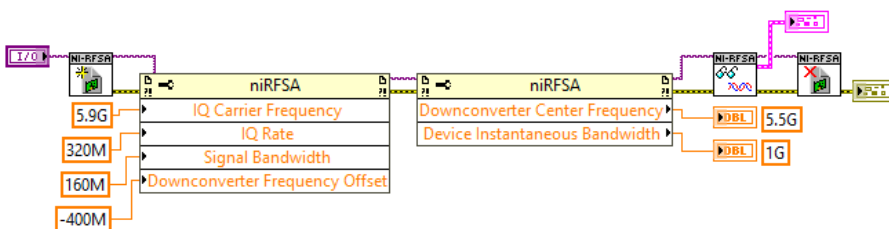
Specifying a Frequency Offset

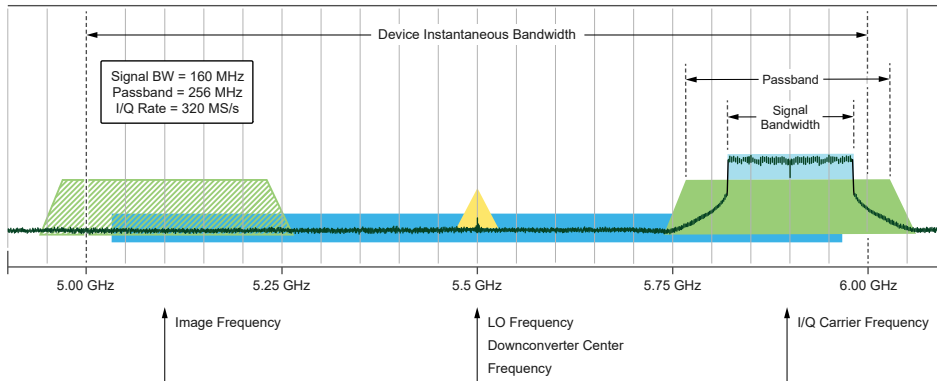
To avoid LO leakage present in the passband, you can apply a frequency offset by setting the NI-RFSADownconverter Frequency Offset property or the NI-RFSGUpconverter Frequency Offset property. This property maintains a constant offset if you vary the I/Q center frequency. You can always read back the actual device instantaneous bandwidth and downconverter center frequency.

Specifying Signal Bandwidth

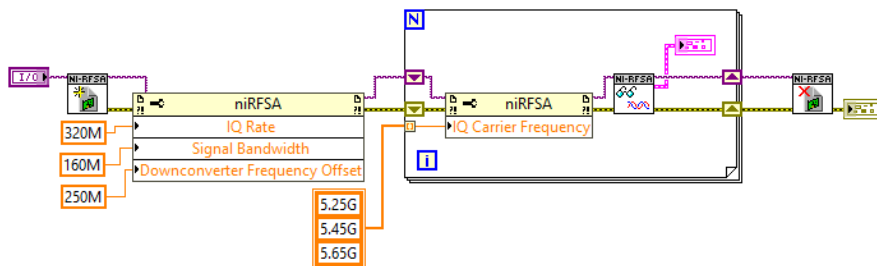
Another way to provide bandwidth information to the instrument driver is to specify the signal bandwidth. Previously, it was noted that the device instantaneous bandwidth is centered at the downconverter center frequency. **Signal bandwidth**, however, is centered at the I/Q carrier frequency, which may be more useful for some applications as it follows the signal of interest. Similarly, you can specify the downconverter frequency offset instead of the downconverter center frequency if it is more intuitive for the application.

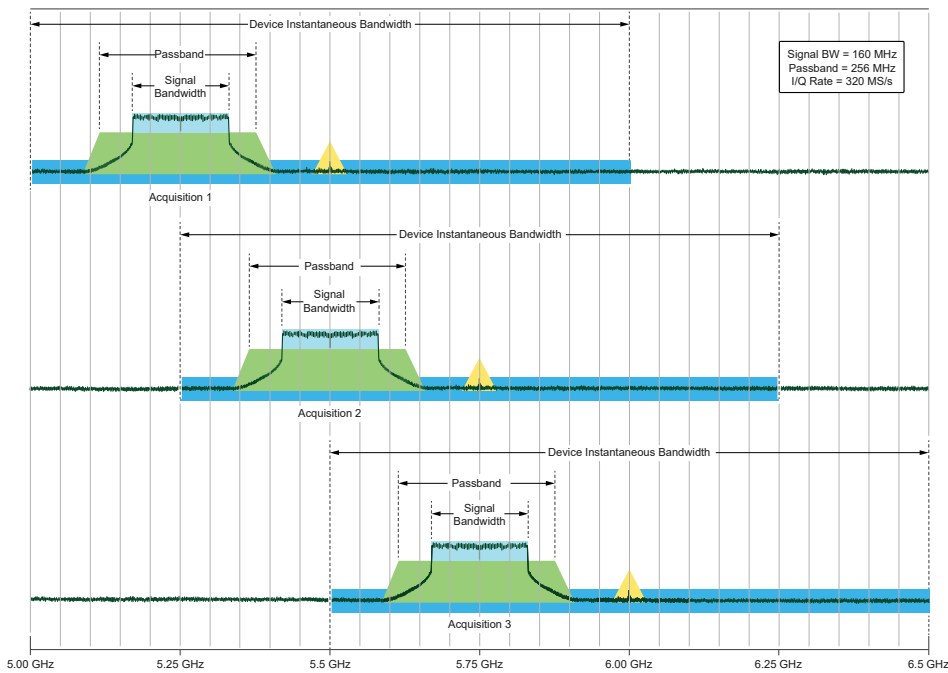
The following example shows how to programmatically specify the signal bandwidth.





Note that setting the signal bandwidth does not necessarily avoid hardware reconfigurations during in-band retuning, but the settings stay relative to the I/Q carrier frequency, so it may be easier to manage in your application. The following example shows three acquisitions with the same I/Q rate, signal bandwidth, and downconverter frequency and only changes the I/Q carrier frequency for each acquisition.





Automatic Frequency Offset

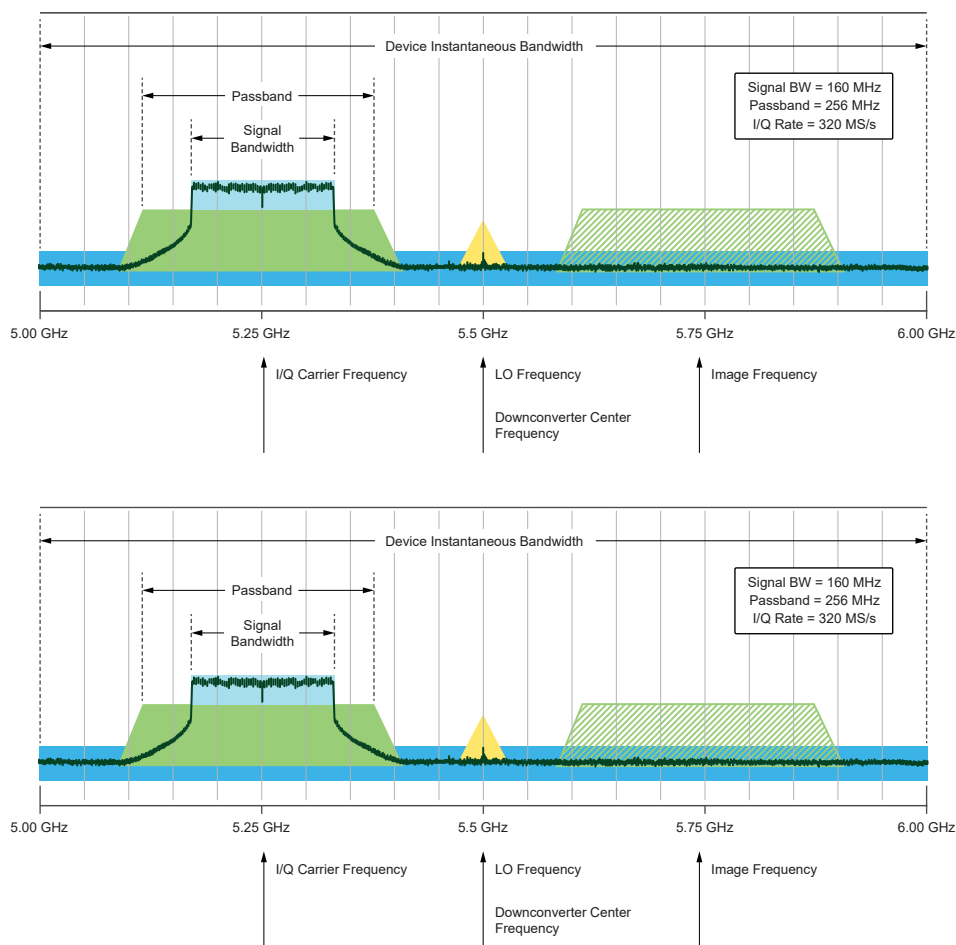
The PXle-5840 can automatically offset the downconverter center frequency from the carrier frequency when sufficient instrument bandwidth is available. For example, the signal must fit within half (the device instantaneous bandwidth minus the LO guard band). A table of the maximum available bandwidth for a given I/Q frequency when using automatic frequency offset is available in the device specifications. In auto-offset mode, the NI-RFSG filters are scaled so that a CW tone will not overflow if the frequency is within the maximum available bandwidth or ± 50 MHz, whichever is less. To prevent an overflow at any offset, you can set Prefilter Gain to less than or equal to -2.0. Outside of auto-offset mode, the filters are scaled so that no CW tone will overflow, even with Prefilter Gain equal to 0.0.

The actual frequency offset applied can be determined by reading the coerced downconverter center frequency. For Automatic Offset mode to function, you must specify the signal bandwidth. Additionally, when the downconverter frequency offset mode is enabled and the signal bandwidth is known, NI-RFSA can further optimize the dynamic range of the instrument. Using the instrument when downconverter frequency offset mode is enabled also ensures the gain accuracy is maintained, as noted in the device specifications. Otherwise, using the user-defined offset mode, the gain accuracy at an offset is limited to the amplitude accuracy specification $\pm$ the frequency response specification.



Note To use automatic frequency offset with an external LO, including sharing an LO between acquisition and generation, refer to the **Using an External LO** section.

The following example shows how to programmatically set the PXIe-5840 to automatically offset the downconverter center frequency from the carrier frequency, if possible. Refer to the Downconverter Frequency Offset Mode and Upconverter Frequency Offset Mode properties for more information.



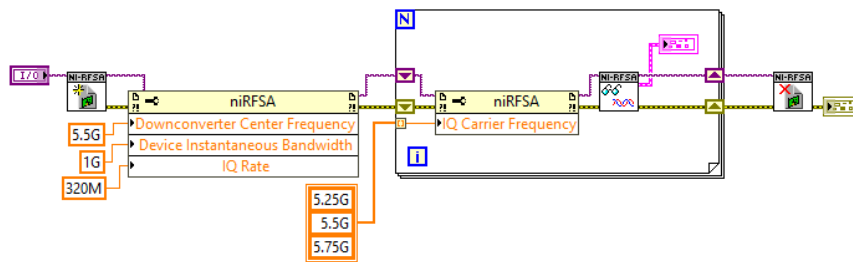
In-Band Retuning

In-band retuning allows the instrument to quickly tune between signals of interest or generation within a given device instantaneous bandwidth using digital upconversion or downconversion to digitally tune the I/Q carrier frequency. The advantages of in-band retuning include reduced settling time for both frequency and amplitude.

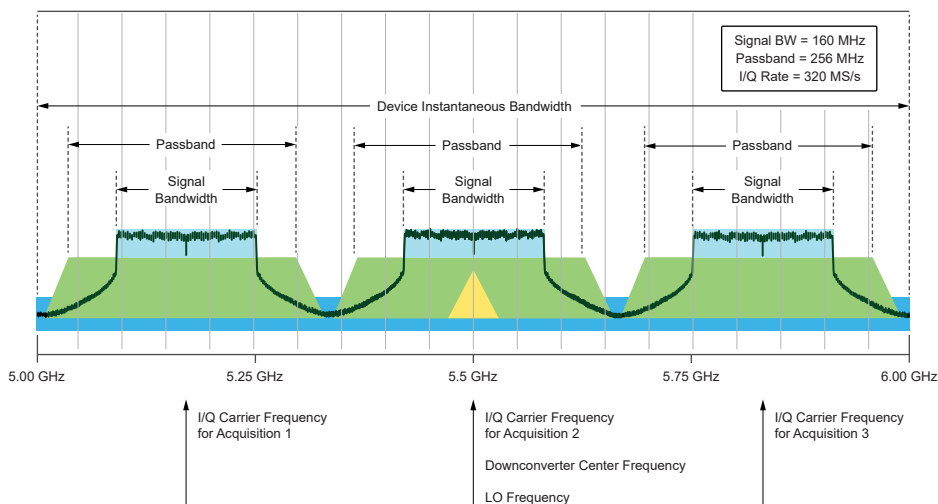
However, in-band retuning can only occur within the supported instantaneous bandwidth of the instrument. You can use digital tuning in combination with LO tuning to more efficiently sweep over a spectrum for supported applications.

You can use in-band retuning by setting the device instantaneous bandwidth and leaving the downconverter center frequency fixed, which significantly reduces reconfiguration and settling times.

The following example shows how to programmatically set the PXle-5840 for in-band retuning.



The following figure shows three acquisitions with only digital frequency shift reconfigurations.



Using an External LO

Complete the following steps when using an external LO.

Cabling

When using an external LO, first ensure that the reference clocks are shared either by using the PXI backplane clock or by exporting the reference clock from the LO by completing the following steps.

1. Connect the external LO's REF OUT connector to the REF IN connector.
2. Specify REF IN as the Reference Clock source using the NI-RFSA or NI-RFSGConfigure Ref Clock VI or function.
3. Connect the output of the external LO to the LO IN connector.

Specifying LO Frequency With Automatic Frequency Offset

To use automatic offset with an external LO, you should provide a frequency as requested by the NI-RFSA or NI-RFSG driver.

When writing your application, complete the following steps to specify the LO frequency in case the driver applies frequency offset as described in the ***Automatic Frequency Offset*** section.

1. Set all the properties for the acquisition or generation, including the NI-RFSA I/Q Carrier Frequency property or the NI-RFSG Frequency property.



Note Do not set the LO Frequency property. If you previously set the LO Frequency property, reset it.

2. Set the LO Source property to LO IN
3. (Optional) Set the Bandwidth Selection property if you want to apply automatic frequency offset.
 - a. (Optional) Set the NI-RFSA Downconverter Frequency Offset Mode property or the NI-RFSG Upconverter Frequency Offset Mode property to Enabled, or query that they are already set to Enabled.



Note For a given RF frequency, NI-RFSA and NI-RFSG use the same automatic offsets for the PXIe-5840. Therefore, if the LO IN source for NI-RFSA is the LO OUT from NI-RFSG on the same device, you can skip steps 3 through 5.

4. Query the LO Frequency to get the expected frequency.
5. Set the frequency of your LO source to the expected frequency.
6. Set the LO Frequency property to the actual frequency of your LO source in case the source does any rounding.

Specifying LO Power When Using an External LO

To achieve better image and LO leakage performance with an external LO, set the LO IN power level of the PXIe-5840 to the actual output power level of the external LO.

1. Query the actual output power level of the external LO.
2. Set the NI-RFSA or NI-RFSG LO IN Power Level property to the value returned in the previous step.

Calibration

The PXIe-5840 supports external adjustment of the following parameters:

- Frequency reference
- Internal LO path gain
- External LO path gain
- RF input gain
- RF output gain

Refer to the **PXIe-5840 Calibration Procedure** available at ni.com/manuals for more information about calibrating the preceding parameters or information about calibrating additional specifications.

Self-Calibration

Temperature drift and other environmental changes can lead to performance degradation for several PXIe-5840 specifications. Self-calibration adjusts the PXIe-5840 for variations in the module environment using an onboard high-precision calibration tone.

Perform self-calibration to compensate and optimize the performance of the PXIe-5840 for a given ambient temperature and operating environment.

The PXIe-5840 is calibrated at the factory; however, you should perform a self-calibration in any of the following situations:

- After first installing your PXIe-5840 into your chassis
- After any module in the chassis is added, moved, or removed
- When the system is in an environment where the ambient temperature varies
- If the module temperature has drifted more than ± 5 °C from the last performed self-calibration

In addition to the preceding scenarios, performing proactive and regular self-calibration helps control the effects of aging-related drifts.



Note Allow the module to warm up for 30 minutes after the PXI Express chassis has been powered on and the operating system has completely loaded. If the temperature drifts significantly during self-calibration, the self-calibration exits with an error.



Note The onboard temperature may fluctuate despite consistent ambient operating temperature. For optimum performance, NI recommends that you periodically verify onboard temperature, especially after changes to the device configuration, and perform self-calibration as necessary. Refer to the **PXIe-5840 Specifications** for more information about operating temperature specifications.

Self-calibration adjusts the following parameters of the PXIe-5840 to facilitate temperature correction:

- LO path gain
- RF input gain
- RF output gain
- RF input residual LO power
- RF output residual LO power
- RF input residual sideband image
- RF output residual sideband image
- RF input flatness
- RF output flatness



Note RF residual LO power and RF residual sideband images are only adjustable in self-calibration and cannot be corrected for during external adjustment. Self-calibration must be successfully executed after an external adjustment to ensure warranted performance.



Note NI recommends that no external signals are transmitted to the RF input port during the self-calibration.

Self-Calibrating the PXIe-5840 with InstrumentStudio

NI recommends you perform an initial self-calibration using InstrumentStudio.



Note Ensure that any connected external hardware is in an idle state and not transmitting during self-calibration. It is not recommended to perform self-calibration while connected in direct loopback configurations.

NI VSTs are represented in InstrumentStudio as a vector signal analyzer and a vector signal generator. Performing self-calibration with either representation of the PXIe-5840 accomplishes the same self-calibration, so it is not necessary to use both when you self-calibrate the PXIe-5840.

Complete the following steps to self-calibrate your VST with InstrumentStudio:

1. To ensure specifications before you use the instrument or perform self-calibration, allow the instrument to warm up.
 - a. If it is not powered already, provide power to the instrument:
 - : first provide power to the remote measurement module using the power adapter, and then power on the PXI Express chassis
 - All other PXIe-5840 instruments: power on the PXI Express chassis
 - b. Wait for the operating system to completely load.
 - c. Allow the instrument to warm up for 30 minutes.
2. Launch InstrumentStudio by navigating to **Start » National Instruments » InstrumentStudio**.
3. Click **File » New » RF Signal Analyzer** to create an analyzer panel for the PXIe-5840.
4. Click the tab created for the PXIe-5840 and click the gear icon (⚙) in the upper right corner of the right sidebar.
5. Hover over **Device Slot » Calibration** and click **Self-Calibrate....**
6. Click **Continue** to proceed.

The PXIe-5840 stores the new calibration data in its nonvolatile memory if the self-calibration is performed successfully.

Partial Self-Calibration

The partial self-calibration feature self-calibrates all configurations within the specified

frequency and reference level limits of the PXIe-5840.

For best results, NI recommends that you perform partial self-calibration without omitting any steps. However, if certain aspects of performance are less important for your application, you can omit the following steps for faster execution:

- LO Self Cal—Omits the LO path gain adjustment.
- Amplitude Accuracy—Omits the RF absolute amplitude accuracy adjustment.
- Residual LO Power—Omits the RF residual LO power adjustment.
- Image Suppression—Omits the RF residual sideband suppression adjustment.



Note The default partial self-calibration does not omit any steps.

Performing Partial Self-Calibration Using LabVIEW

To perform a partial self-calibration when using LabVIEW, use the niRFSA Self Calibrate Range VI or the niRFSG Self Calibrate Range VI.



Note The niRFSA Self Calibrate Range VI does not perform any RF output calibration steps and the niRFSG Self Calibrate Range VI does not perform any RF input calibration steps.



Note Do not access the RF input, RF output, or basecard clock circuitry while either of these VIs are executing.



Notice Resetting the driver results in the loss of any stored partial self-calibration data. Restarting the computer typically resets the driver.



Note NI recommends that no external signals are transmitted to the RF input port during the partial self-calibration.

For more information about calibration, contact NI or visit ni.com/calibration. You can obtain the calibration certificate for your product at ni.com/calibration.

Related concepts:

- [Device Warm-Up](#)

NI-TClk Manual Calibration Using NI-RFSA

Complete the following steps to improve the synchronization accuracy by lowering skew and minimizing jitter of NI-TClk synchronized devices using manual calibration.

1. Connect the external signal to the VSTs. For best performance, minimize unnecessary skew by using matched length cables.
2. Configure the VST for acquisition using NI-TClk. If using LabVIEW, use the `RFSA Synchronization (TClk, Shared LO and Reference Clock) (5840).vi` example.
3. Start the acquisition and measure the skew between devices, noting the amount of jitter.
4. Read the value from the Absolute Delay property. Stop the acquisition, modify the value, and write it back to apply skew correction.
5. Repeat steps 3 and 4 until you achieve the appropriate synchronization results.
6. Read the value from the Absolute Delay property and store the value for future synchronization sessions.

To apply the manual calibration synchronization results, write the stored value to the Absolute Delay property before calling the `NI-TClkSynchronize`.

NI-TClk Manual Calibration Using NI-RFSG

Complete the following steps to improve the synchronization accuracy by lowering skew and minimizing jitter of NI-TClk synchronized devices using manual calibration.

1. Connect the RF output connector on the vector signal transceivers (VSTs) to a multi-channel signal analyzer. For best performance, minimize unnecessary skew by using matched length cables.
2. Configure the VST for generation using NI-TClk. If using LabVIEW, use the example.
3. Start the generation and measure the skew between devices, noting the amount of jitter.
4. Read the value from the Absolute Delay property. Stop the generation, modify the value, and write it back to apply skew correction.
5. Repeat steps 3 and 4 until you achieve the appropriate synchronization results.

6. Read the value from the Absolute Delay property and store the value for future synchronization sessions.

To apply the manual calibration synchronization results, write the stored value to the Absolute Delay property before calling NI-TClkSynchronize.

Unsupported NI-RFSG Features

The following NI-RFSG features are not supported on the PXIe-5840:

- Pulse shaping

Restrictions on Scripts

- `if else` is not supported.
- `break` instruction is not supported.
- `stream` instruction is not supported.
- The maximum compiled script size is 6,100 instructions. Each script language instruction requires roughly one compiled instruction, plus one instruction for each marker.
- Nested repeats are only allowed if the outer `repeat` is a `repeat forever` instruction, and there are no other instructions preceding it or past the end of the `repeat` block. You can only use a single nesting level.
- Markers are allowed in `generate` and `finite wait` instructions. They are not allowed in `conditional wait` instructions.