CALIBRATION PROCEDURE

PXIe-5645

Reconfigurable 6 GHz RF Vector Signal Transceiver with I/Q Interface

This document contains the verification and adjustment procedures for the PXIe-5645 vector signal transceiver.

Refer to *ni.com/calibration* for more information about calibration solutions.

Caution Do not disconnect the cable that connects CAL IN to CAL OUT. Removing the cable from or tampering with the CAL IN or CAL OUT front panel connectors voids the product calibration and specifications are no longer warranted.

Contents

NATIONAL INSTRUMENTS

Required Software

Calibrating the PXIe-5645 requires you to install the following software on the calibration system:

- LabVIEW 2012.1 Base/Full/Pro or later
- PXIe-5644/5645 Instrument Design Libraries 2012.1 or later

- NI-RFSA version 2.7 or later
- NI-RFSG version 1.9 or later
- Modulation Toolkit version 4.3.3 or later
- Spectral Measurements Toolkit version 2.6.3 or later
- PXIe-5645 Calibration Fixture API

You can download all required software, other than the PXIe-5645 Calibration Fixture API, from *ni.com/downloads*.

Related Documentation

For additional information, refer to the following documents as you perform the calibration procedure:

- *PXIe-5645 Getting Started Guide*
- *NI RF Vector Signal Transceivers Help*
- *PXIe-5645 Specifications*

Visit *ni.com/manuals* for the latest versions of these documents.

Test Equipment

RF Test Equipment

National Instruments recommends that you use particular equipment for the RF performance verification and adjustment procedures.

If the recommended equipment is not available, select a substitute using the minimum requirements listed in the following table.

Table 1. Required Equipment Specifications for PXIe-5645 RF Calibration

Equipment	Recommended Model	Where Used	Minimum Requirements
Frequency reference	Symmetricom 8040 Rubidium Frequency Standard	Verifications: • Internal frequency reference • Nonharmonic spurs • Spectral purity • IMD3 • IMD2 • Output noise density • Output second harmonics Adjustments: • Absolute amplitude accuracy • Output power level accuracy	Frequency: 10 MHz Frequency accuracy: ≤±1E-9 Output mode: sinusoid
Power sensor	Rohde & Schwarz (R&S) NRP-Z91	Test system characterization Verifications: • Absolute amplitude accuracy • Frequency response • Output power level accuracy • LO OUT (RF IN 0 and RF OUT 0) Adjustments: • Absolute amplitude accuracy • Output power level accuracy • LO OUT (RF IN 0 and RF OUT 0)	Range: -67 dBm to +23 dBm Frequency range: 65 MHz to 6 GHz Absolute uncertainty: 0.174 dB Power linearity: <0.1 dB VSWR: <1.2:1 up to 6 GHz

Table 1. Required Equipment Specifications for PXIe-5645 RF Calibration (Continued)

Equipment	Recommended Model	Where Used	Minimum Requirements
Vector signal generator	PXIe-5673E	Test system characterization Verifications: • Internal frequency reference • Absolute amplitude accuracy • Frequency response • Input nonharmonic spurs • Input IMD3 • Input EVM • Input IMD2 Adjustments: • Internal frequency reference • Absolute amplitude accuracy • LO OUT (RF IN 0 and RF OUT 0)	Frequency range: 65 MHz to 6 GHz Frequency resolution: <5 Hz Amplitude range: -70 dBm to 5 dBm Instantaneous bandwidth: 50 MHz

Table 1. Required Equipment Specifications for PXIe-5645 RF Calibration (Continued)

Equipment	Recommended Model	Where Used	Minimum Requirements
Spectrum analyzer or vector signal analyzer	PXIe-5665	Test system characterization Verifications: • Spectral purity • Output power level accuracy • Output frequency response • Output noise density • Output second harmonics • Output nonharmonic spurs • Output IMD3 • Output EVM Adjustments: • Output power level accuracy	Frequency range: 65 MHz to 12 GHz Instantaneous bandwidth: 50 MHz Phase noise at 20 kHz offset: <-125 dBm/Hz
Preamplifier	PXI-5691	Output noise density verification	Frequency range: 65 MHz to 8 GHz Noise floor at 6 GHz: <-158 dBm/Hz

Table 1. Required Equipment Specifications for PXIe-5645 RF Calibration (Continued)

Equipment	Recommended Model	Where Used	Minimum Requirements
Power splitter	Aeroflex/Weinschel 1593	Test system characterization Verifications: • Frequency response • Absolute amplitude accuracy • Output power level accuracy Adjustments: • Absolute amplitude accuracy • Output power level accuracy	VSWR: ≤1.25:1 up to 18 GHz Amplitude tracking: <0.25 dB
6 dB attenuator (x2)	Anritsu 41KB-6 or Mini-Circuits	Test system characterization Verifications: • Frequency response • Absolute amplitude accuracy • Output power level accuracy Adjustments: • Absolute amplitude accuracy • Output power level accuracy	Frequency range: DC to 6 GHz VSWR: ≤1.1:1
50 Ω SMA terminator	—	Test system characterization Average noise density verification	Frequency range: DC to 6 GHz VSWR: ≤1.1:1

Table 1. Required Equipment Specifications for PXIe-5645 RF Calibration (Continued)

Equipment	Recommended Model	Where Used	Minimum Requirements
SMA (m)-to-SMA (m) cable	—	All procedures	Frequency range: DC to 6 GHz Impedance: 50 Ω
SMA (m)-to-N (f) adapter	Huber+Suhner 32_SMA_N-50-1/1-_UE	Test system characterization Verifications: • Frequency response • Absolute amplitude accuracy • Output power level accuracy • LO OUT (RF IN 0 and RF OUT 0) Adjustments: • Absolute amplitude accuracy • Output power level accuracy • LO OUT (RF IN 0 and RF OUT 0)	Frequency range: DC to 6 GHz Impedance: 50 Ω Return loss: ≥23 dB
SMA (f)-to-N (f) adapter	Huber+Suhner 31_N-SMA-50-1/1-_UE	Test system characterization	Frequency range: DC to 6 GHz Impedance: 50 Ω Return loss: ≥23 dB

Table 1. Required Equipment Specifications for PXIe-5645 RF Calibration (Continued)

Equipment	Recommended Model	Where Used	Minimum Requirements
3.5 mm (m)-to-3.5 mm (m) adapter	Huber+Suhner 32_PC35-50-0-2/199_NE	Test system characterization Verifications: • Frequency response • Absolute amplitude accuracy • Output power level accuracy Adjustments: • Absolute amplitude accuracy • Output power level accuracy	Frequency range: DC to 6 GHz Impedance: 50 Ω Return loss: ≥30 dB
3.5 mm (f)-to-3.5 mm (f) adapter	Huber+Suhner 32_PC35-50-0-1/199_UE	Test system characterization	Frequency range: DC to 6 GHz Impedance: 50 Ω Return loss: ≥30 dB

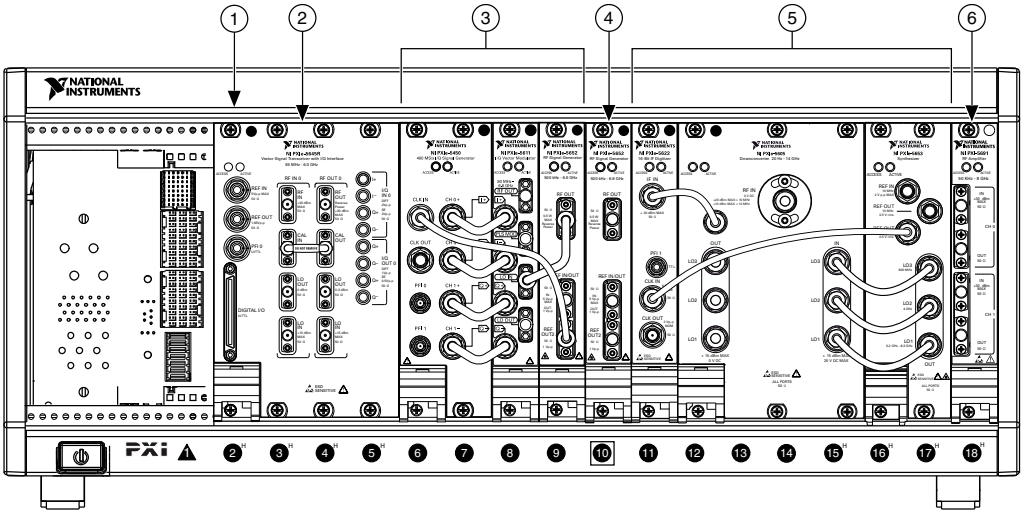
The following table lists equipment required to perform optional verification for non warranted RF specifications of the PXIe-5645.

Table 2. Required Equipment Specifications for Optional PXIe-5645 RF Verification

Equipment	Recommended Model	Where Used	Minimum Requirements
CW signal generator	PXIe-5652	Input IMD3 Input IMD2	Frequency range: 65 MHz to 6 GHz Frequency resolution: <5 Hz Amplitude range: -30 dBm to 0 dBm
Power splitter	Mini-Circuits ZFRSC-123+	Input IMD3 Input IMD2	>20 dB reverse isolation at 6 GHz
SMA (m)-to-SMA (m) cable (x2)	—	Input IMD3 Input IMD2	Frequency range: DC to 6 GHz
Frequency reference	Symmetricom 8040 Rubidium Frequency Standard	Input IMD3 Input IMD2	Frequency: 10 MHz Frequency accuracy: ≤±1E-9
Two-port vector network analyzer (VNA)	PXIe-5630	Return loss	Frequency range: 65 MHz to 6 GHz

The following figure shows a recommended RF calibration system configuration for the PXIe-5645.

Figure 1. Recommended PXIe-5645 RF Calibration System



1. PXIe-1075 Chassis
2. Slots 2 through 5: PXIe-5645 (Device Under Test)
3. Slots 6 and 7: PXIe-5673E Vector Signal Generator
4. Slot 10: PXI-5652 RF Analog Signal Generator and CW Source or PXIe-5652 RF Analog Signal Generator and CW Source
5. Slots 11 through 17: PXIe-5665 Vector Signal Analyzer
6. Slot 18: PXI-5691 RF Amplifier

I/Q Test Equipment

National Instruments recommends that you use particular equipment for the I/Q interface performance verification and adjustment procedures.

If the recommended equipment is not available, select a substitute using the minimum requirements listed in the following table.

Table 3. Required Equipment Specifications for PXIe-5645 I/Q Calibration

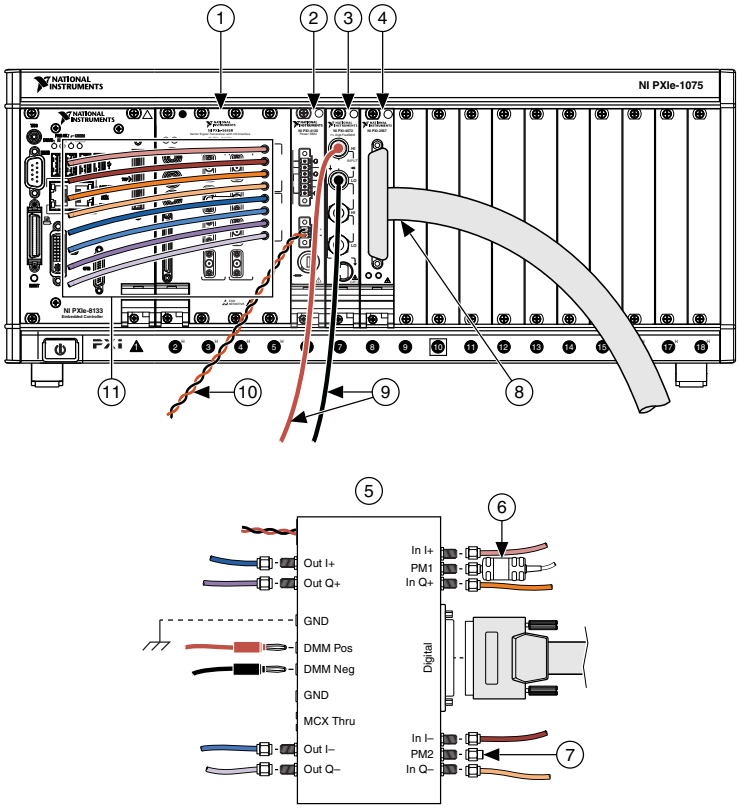
Equipment	Recommended Model	Where Used	Minimum Requirements
(2x) Calibration fixtures; one for verifications, one for adjustments	PXIe-5645 I/Q Calibration Fixture (calibration fixture), 782452-01	I/Q test system characterization I/Q verifications I/Q adjustments	—
Source measure unit (SMU)	PXI-4130	I/Q test system characterization I/Q verifications I/Q adjustments	DC voltage: 6 V DC current: 2A
Relay driver	PXI-2567	I/Q test system characterization I/Q verifications I/Q adjustments	—
Digital multimeter (DMM)	PXI-4072	I/Q test system characterization I/Q verifications I/Q adjustments	Digits of precision: 6½
Power sensor	Rohde & Schwarz (R&S) NRP-Z91	I/Q test system characterization I/Q verifications I/Q adjustments	Range: -67 dBm to +23 dBm Frequency range: 65 MHz to 6 GHz Accuracy: 0.5% VSWR: <1.2:1 at 6 GHz
(8x) MCX (m)-to-SMA (m) cables	188377-01	I/Q test system characterization I/Q verifications I/Q adjustments	Frequency range: DC to 6 GHz Impedance: 50 Ω

Table 3. Required Equipment Specifications for PXIe-5645 I/Q Calibration (Continued)

Equipment	Recommended Model	Where Used	Minimum Requirements
78-pin DSUB cable	Included with relay driver module	I/Q test system characterization I/Q verifications I/Q adjustments	—
(2x) SMA (m)-to-N (f) adapter	Huber+Suhner 32_SMA_N-50-1/1-_UE	I/Q test system characterization I/Q verifications I/Q adjustments	Frequency range: DC to 6 GHz Impedance: 50 Ω Return loss: ≥23 dB
(3x) MCX terminations	Johnson Components 133-3801-801	I/Q test system characterization	Impedance: 50 Ω Frequency range: DC to 1 GHz

I/Q verification procedures and I/Q adjustment procedures each use a different calibration fixture; however, the calibration system configuration is identical for both verification and adjustment. The following figure shows a recommended PXIe-5645 I/Q calibration system.

Figure 2. Recommended PXIe-5645 I/Q Calibration System



1. PXIe-5645
2. PXI-4130 SMU
3. PXI-4072 DMM
4. PXI-2567 Relay Driver
5. PXIe-5645 I/Q Calibration Fixture (one of two)
6. Power Meter 1
7. MCX Termination
8. 78-Pin D-SUB Cable
9. Banana Cables
10. Twisted-Pair Cable
11. MCX (m)-to-SMA (m) Cables

Test Conditions

The following setup and environmental conditions are required to ensure the PXIe-5645 meets published specifications.

- Keep cabling as short as possible. Long cables act as antennas, picking up extra noise that can affect measurements.
- Verify that all connections to the PXIe-5645, including front panel connections and screws, are secure.

- Maintain an ambient temperature of 23 °C ± 5 °C.
- Keep relative humidity between 10% and 90%, noncondensing.
- Allow a warm-up time of at least 30 minutes after the chassis is powered on and PXIe-5644/5645 Instrument Design Libraries is loaded and recognizes the PXIe-5645. The warm-up time ensures that the PXIe-5645 and test instrumentation are at a stable operating temperature.
- In each verification procedure, insert a delay between configuring all devices and acquiring the measurement. This delay may need to be adjusted depending on the instruments used but should always be at least 1,000 ms for the first iteration, 1,000 ms when the power level changes, and 100 ms for each other iteration.
- Ensure that the PXI chassis fan speed is set to HIGH, that the fan filters, if present, are clean, and that the empty slots contain filler panels. For more information about cooling, refer to the *Maintain Forced-Air Cooling Note to Users* document available at *ni.com/manuals*.

Initial Setup

Refer to the *PXIe-5645 Getting Started Guide* for information about how to install the software and the hardware and how to configure the device in Measurement & Automation Explorer (MAX).

RF Test System Characterization

The following procedures characterize the test equipment used during RF verification and RF adjustment.

Caution The connectors on the device under test (DUT) and test equipment are fragile. Perform the steps in these procedures with great care to prevent damaging any DUTs or test equipment.

Zeroing the Power Sensor

1. Ensure that the power sensor is not connected to any signals.
2. Zero the power sensor using the built-in function, according to the power sensor documentation.

Characterizing Power Splitter Balance

You must zero the power sensor as described in the *Zeroing the Power Sensor* section prior to starting this procedure.

This procedure characterizes the balance between the two output terminals of the splitter, where the second terminal is terminated into an attenuator. The following procedures require the power splitter balance data:

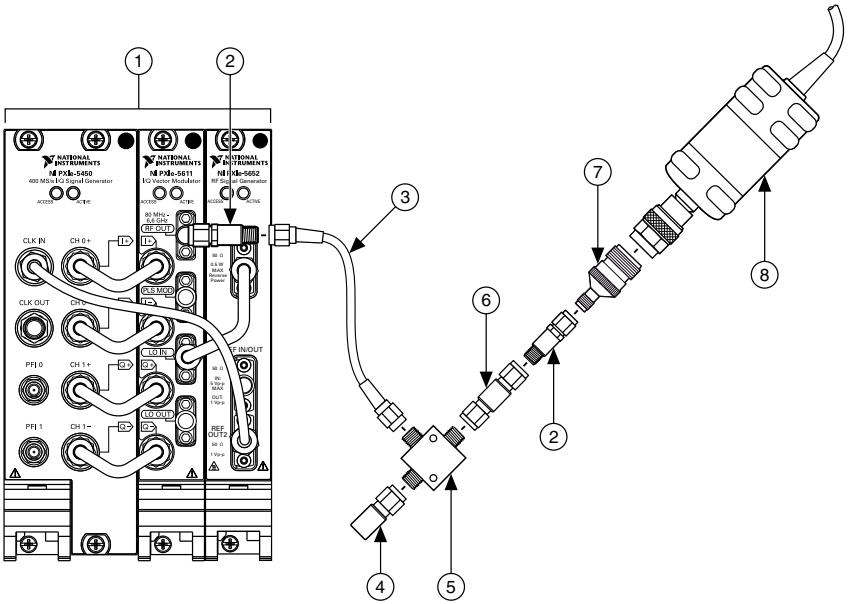
- *Verifying Input Absolute Amplitude Accuracy*
- *Verifying Input Frequency Response*
- *Adjusting Input Absolute Amplitude Accuracy*

The verification and adjustment procedures use different test points for the splitter balance characterization. For characterization used in a verification procedure, use the test points in the *Characterization Test Points for Verification Procedures* table. For characterization used in an adjustment procedure, use 65 MHz to 6 GHz in 5 MHz steps for the test points.

1. Connect the SMA (m) connector of the 6 dB attenuator to the RF OUT front panel connector of the vector signal generator.
2. Connect the SMA (f) connector of the 6 dB attenuator to the input port of the power splitter using an SMA (m)-to-SMA (m) cable.
3. Connect the 50 Ω (m) terminator to one of the power splitter output ports. Refer to this port as *splitter output 1*.
4. Connect the other power splitter output to the SMA (f) connector of the second 6 dB attenuator using a 3.5 mm (m)-to-3.5 mm (m) adapter. Refer to the combined power splitter output and 6 dB attenuator as *splitter output 2*.
5. Connect the power sensor to splitter output 2 using the SMA (f)-to-N (f) adapter.

   The following figure illustrates the hardware setup.

Figure 3. Connection Diagram for Measuring at Splitter Output 2



1. Vector Signal Generator
2. 6 dB Attenuator
3. SMA (m)-to-SMA (m) Cable
4. 50 Ω Terminator
5. Power Splitter
6. 3.5 mm (m)-to-3.5 mm (m) Adapter
7. SMA (f)-to-N (f) Adapter
8. Power Sensor

6. Configure the vector signal generator using the following settings:
   - Center frequency: For characterization used in a verification procedure, use the first test point in the following table. For characterization used in an adjustment procedure, use 65 MHz. For either procedure type, store as *frequency*.
   - Power level: 0 dBm

Table 4. Characterization Test Points for Verification Procedures

Test Points (MHz)	Step Size (MHz)
80 to 100	5
250	—
290 to 310	5
350 to 400	50
410 to 490	5
500	—

Table 4. Characterization Test Points for Verification Procedures (Continued)

Test Points (MHz)	Step Size (MHz)
510 to 690	5
700 to 750	50
760 to 840	5
850 to 900	50
910 to 1,090	5
1,160 to 1,240	5
1,400	—
1,510 to 1,690	5
1,800	—
1,960 to 2,040	5
2,200 to 2,600	200
2,610 to 2,790	5
2,800	—
2,960 to 3,040	5
3,200 to 3,600	200
3,760 to 3,840	5
3,910 to 4,090	5
4,200	—
4,460 to 4,540	5
4,600 to 4,800	200
4,910 to 5,090	5
5,200 to 5,400	200
5,460 to 5,540	5
5,600 to 5,800	200
5,910 to 5,990	5
6,000	—

7. Configure the power sensor to correct for *frequency* using the power sensor frequency correction function.
8. Use the power sensor to measure the power at the *frequency* from step 6.

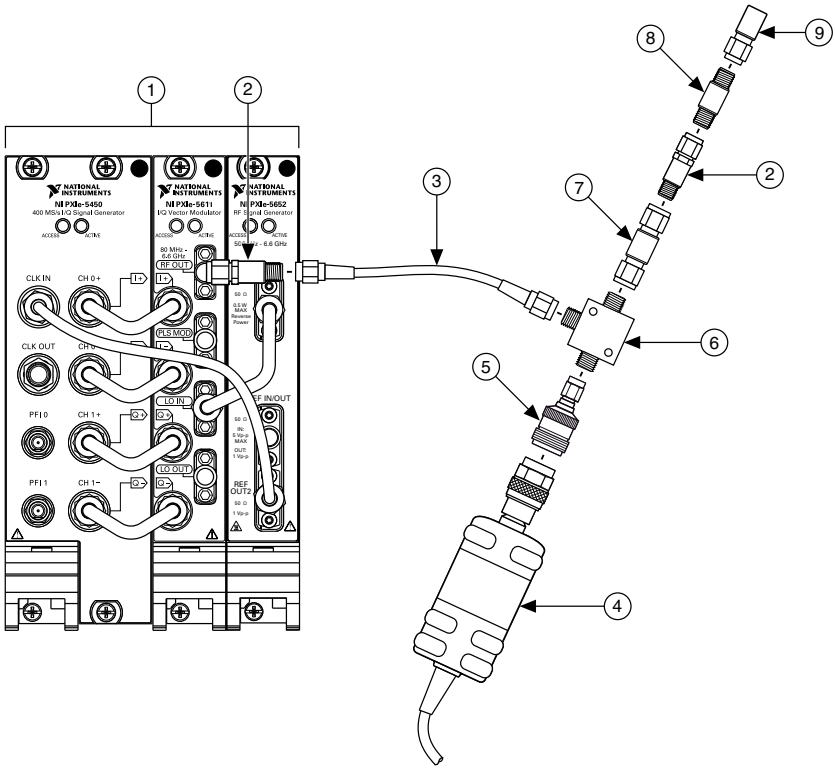
9. Repeat steps 6 through 8 by updating *frequency*. For characterization used in a verification procedure, use the test points in the *Characterization Test Points for Verification Procedures* table. For characterization used in an adjustment procedure, use 65 MHz to 6 GHz in 5 MHz steps for the test points.

   Record the resulting measurements as *splitter output 2 power*. Each frequency should have a corresponding value.

10. Disconnect the power sensor and 50 Ω terminator from the power splitter.
11. Connect the power sensor to splitter output 1 using an SMA (m)-to-N (f) adapter.
12. Connect the 50 Ω terminator to splitter output 2 using an SMA (f)-to-SMA (f) adapter.

The following figure illustrates the hardware setup.

Figure 4. Connection Diagram for Measuring at Splitter Output 1



1. Vector Signal Generator
2. 6 dB Attenuator
3. SMA (m)-to-SMA (m) Cable
4. Power Sensor
5. SMA (m)-to-N (f) Adapter
6. Power Splitter
7. 3.5 mm (m)-to-3.5 mm (m) Adapter
8. 3.5 mm (f)-to-3.5 mm (f) Adapter
9. 50 Ω Terminator

13. Configure the vector signal generator using the following settings:
    - Center frequency: For characterization used in a verification procedure, use the first test point in the *Characterization Test Points for Verification Procedures* table. For characterization used in an adjustment procedure, use 65 MHz. For either procedure type, store as *frequency*.
    - Power level: 0 dBm
14. Configure the power sensor to correct for *frequency* using the power sensor frequency correction function.
15. Use the power sensor to measure the power.
16. Repeat steps 13 through 15 by updating *frequency*. For characterization used in a verification procedure, use the test points in the *Characterization Test Points for Verification Procedures* table. For characterization used in an adjustment procedure, use 65 MHz to 6 GHz in 5 MHz steps for the test points.

    Record the resulting measurements as *splitter output 1 power*. Each frequency should have a corresponding value.
17. Calculate the splitter balance for each frequency point using the following equation:

    splitter balance = splitter output 2 power - splitter output 1 power

Characterizing Power Splitter Loss

This procedure characterizes the loss through the power splitter.

You must zero the power sensor as described in the *Zeroing the Power Sensor* section prior to starting this procedure.

The following procedures require the power splitter loss data:

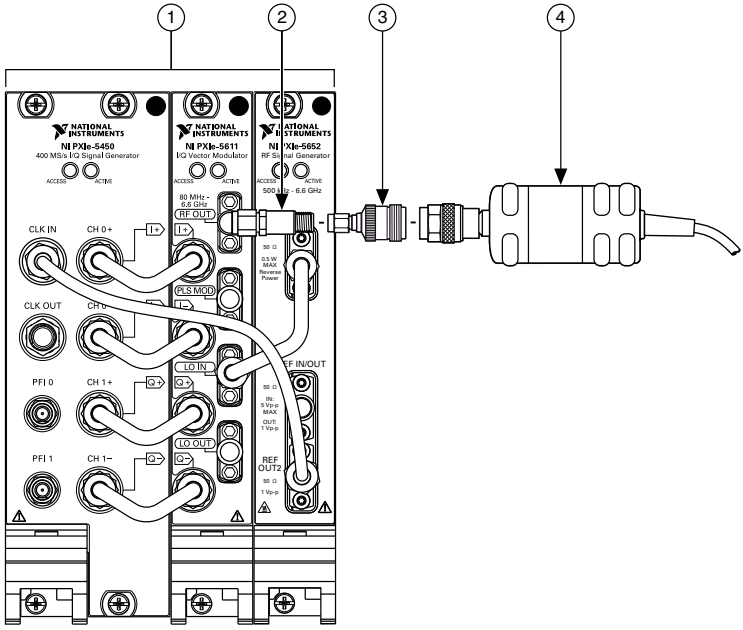
- *Verifying Output Power Level Accuracy*
- *Verifying Output Frequency Response*
- *Adjusting Output Power Level Accuracy*

The verification and adjustment procedures use different test points for the splitter loss characterization. For characterization used in a verification procedure, use the test points in the *Characterization Test Points for Verification Procedures* table. For characterization used in an adjustment procedure, use 65 MHz to 6 GHz in 5 MHz steps for the test points.

1. Connect the SMA (m) connector of the 6 dB attenuator to the RF OUT front panel connector of the vector signal generator.
2. Connect the SMA (f) connector of the 6 dB attenuator to the power sensor using an SMA (m)-to-N (f) adapter.

   The following figure illustrates the hardware setup.

Figure 5. Connection Diagram for Measuring Splitter Input Power



1. Vector Signal Generator
2. 6 dB Attenuator
3. SMA (m)-to-N (f) Adapter
4. Power Sensor

3. Configure the vector signal generator to generate a tone using the following settings:
   - Center frequency: For characterization used in a verification procedure, use the first test point in the *Characterization Test Points for Verification Procedures* table in the *Characterizing Power Splitter Balance* section. For characterization used in an adjustment procedure, use 65 MHz.
   - Power level: Configured output power from transfer function A in the following table.
   - Tone offset: 3.75 MHz

Table 5. Accuracy Transfer Definitions

Transfer Function	Supported Output Power Level (dBm)	Configured Output Power (dBm)	Configured Reference Level (dBm)
A	+10 to -20	0	10
B	-20 to -40	-15	-30

4. Configure the power sensor to correct for the center frequency from step 3 using the power sensor frequency correction function.
5. Use the power sensor to measure the output power.

6. Repeat steps 3 through 5 for the remaining frequencies. For characterization used in a verification procedure, use the test points from the *Characterization Test Points for Verification Procedures* table in the *Characterizing Power Splitter Balance* section. For characterization used in an adjustment procedure, use 65 MHz to 6 GHz in 5 MHz steps for the test points.

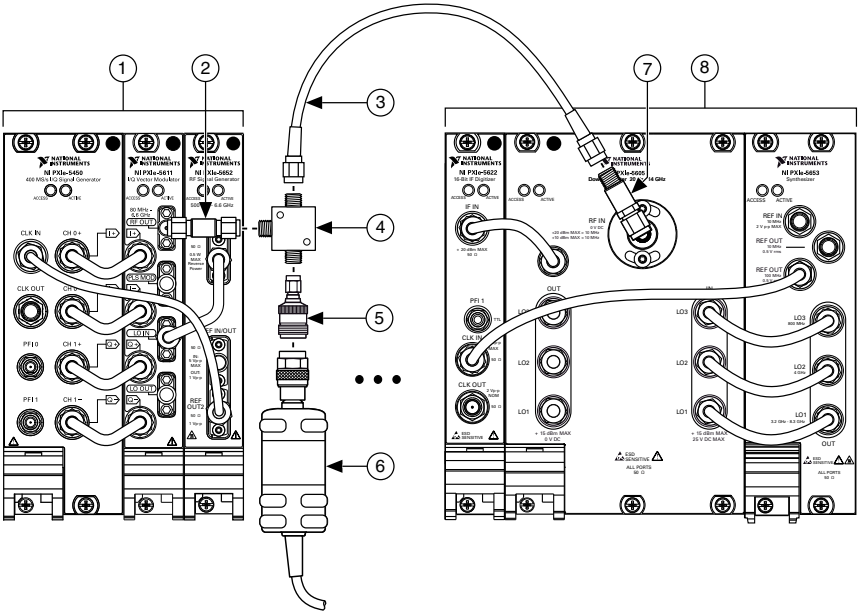
   Record the resulting measurements as *splitter input power*. Each frequency should have a corresponding value.
7. Disconnect the power sensor from the 6 dB attenuator.
8. Connect the power splitter input port to the SMA (f) port of the 6 dB attenuator using an SMA (m)-to-SMA (m) adapter.
9. Connect the power sensor to one of the splitter output ports using the SMA (m)-to-N (f) adapter.

   Refer to this port as *splitter output 1* for the remainder of this procedure and all tests that use the resulting characterization data.
10. Connect the other output of the power splitter to the SMA (f) connector of a second 6 dB attenuator using an SMA (m)-to-SMA (m) cable.
11. Connect the SMA (m) connector of the second 6 dB attenuator to the RF IN front panel port of the spectrum analyzer.

    Refer to this port as *splitter output 2* for the remainder of this procedure and all tests that use the resulting characterization data.

    The following figure illustrates the hardware setup.

Figure 6. Connection Diagram for Measuring Splitter Output 1 Power



1. Vector Signal Generator
2. 6 dB Attenuator
3. SMA (m)-to-SMA (m) Adapter
4. Power Splitter
5. SMA (m)-to-N (f) Adapter
6. Power Sensor
7. SMA (m)-to-SMA (m) Cable
8. Spectrum Analyzer

Note If you use the PXIe-5665, as recommended, for the spectrum analyzer, disable the preamplifier and preselector options and set the FFT window type to Flat Top.

12. Configure the vector signal generator to generate a tone using the following settings:
    - Center frequency: *Center frequency* from step 3.
    - Power level: *Configured output power* from transfer function A in the *Accuracy Transfer Definitions* table.
13. Configure the spectrum analyzer using the following settings:
    - Center frequency: Center frequency of the vector signal generator + *tone offset* from step 3.
    - Reference level: Configured reference level from transfer function A in the *Accuracy Transfer Definitions* table.
    - Span: 250 kHz
    - Resolution bandwidth: 4 kHz
    - Averaging mode: RMS
    - Number of averages: 10
14. Use the spectrum analyzer to acquire the signal.

15. Measure the peak output power present in the signal from step 14. Store this value as *splitter output 2 power*.
16. Configure the power sensor to correct for the frequency from step 12 using the power sensor frequency correction function.
17. Use the power sensor to measure the output power. Store this value as *splitter output 1 power*.
18. Repeat steps 12 through 17 for the remaining frequencies. For characterization used in a verification procedure, use the test points from the *Characterization Test Points for Verification Procedures* table in the *Characterizing Power Splitter Balance* section. For characterization used in an adjustment procedure, use 65 MHz to 6 GHz in 5 MHz steps for the test points.
19. Repeat steps 12 through 18 for transfer function B from the *Accuracy Transfer Definitions* table.
20. Calculate a table of splitter loss values for each frequency of each transfer function using the following equation:

    splitter loss = splitter output 1 power - splitter input power

    Store the results in a *Splitter Loss* table.
21. Calculate the accuracy transfer result for each frequency of each transfer function using the following equation:

    accuracy transfer result = splitter output 1 - splitter output 2

    Store the results in an *RF Output Transfer Result* table.

I/Q Test System Characterization

The following procedures characterize the I/Q calibration fixtures used during I/Q verification and I/Q adjustment.

I/Q verification procedures and I/Q adjustment procedures each use a different calibration fixture; however, the characterization is identical for both calibration fixtures. The I/Q calibration fixture characterization produces data required to perform verifications and adjustments. You must characterize the designated I/Q calibration fixture once, prior to performing all verifications or adjustments.

The I/Q calibration fixture characterization procedures automatically execute for the permutations of calibration fixture settings defined in the following tables. For each procedure, actions are performed based on the current permutation. For example, for each physical connection, iterate through all signal path configurations, for each signal path configuration, iterate through all terminations, and so on. The following list shows the hierarchy of settings.

- Iterate physical connection
  - Iterate signal path configuration
    - Iterate termination
      - Iterate DMM source

Table 6. Physical Connection Iterations

Iteration	Physical Connection
0	Power meter direct
1	No connect
2	No connect (cable measurements)[1]
3	Power meter to I
4	Power meter to Q
5	Swapped[2]
6	Thru[3]

Table 7. Signal Path Configuration Iterations

Iteration	Signal Path	Terminal Configuration
0	No connect	Single-ended
1	No connect	Differential
2	Terminated	Differential
3	Terminated	Single-ended
4	Inline	Single-ended
5	Inline	Differential
6	Cross	Differential
7	Cross	Single-ended
8	Absolute I	Single-ended
9	Absolute I	Differential
10	Absolute Q	Differential
11	Absolute Q	Single-ended
12	Splitter I	Single-ended
13	Splitter I	Differential

[1] Use this connection only for the cable impedance characterization.
[2] PXIe-5645 I+/- input to Q+/- output and Q+/- input to I+/- output.
[3] PXIe-5645 I+/- input to I+/- output and Q+/- input to Q+/- output.

Table 7. Signal Path Configuration Iterations (Continued)

Iteration	Signal Path	Terminal Configuration
14	Splitter Q	Differential
15	Splitter Q	Single-ended

Table 8. Termination Iterations

Iteration	Termination
0	False (unterminated)
1	True (terminated)

Table 9. DMM Source Iterations

Iteration	DMM Source
0	None differential
1	None single-ended
2	I In differential
3	I In single-ended
4	Q In differential
5	Q In single-ended
6	I Out differential
7	I Out single-ended
8	Q Out differential
9	Q Out single-ended
10	Power meter differential
11	Power meter single-ended
12	I to I+
13	I to Q+
14	I to power meter+
15	I to I-
16	I to Q-
17	I to power meter-

Table 9. DMM Source Iterations (Continued)

Iteration	DMM Source
18	Q to I+
19	Q to Q+
20	Q to power meter+
21	Q to I-
22	Q to Q-
23	Q to power meter-

I/Q Calibration Fixture Connections

Specific calibration fixture connections vary according to the current iteration of the I/Q calibration fixture characterization procedure.

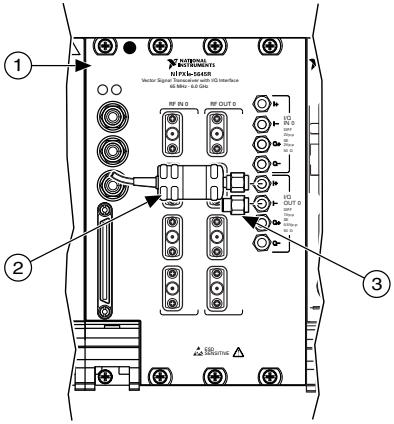
The following cabling diagrams correspond to the iteration values for *Physical Connection* in the *Physical Connection Iterations* table in the *I/Q Test System Characterization* section.

Power Meter Direct Connections

1. Connect power meter 1 to I+ (I/Q OUT 0) on the PXIe-5645.
2. Connect an MCX termination to I- (I/Q OUT 0) on the PXIe-5645.

   The following figure illustrates the hardware setup.

Figure 7. Power Meter Direct Cabling Diagram



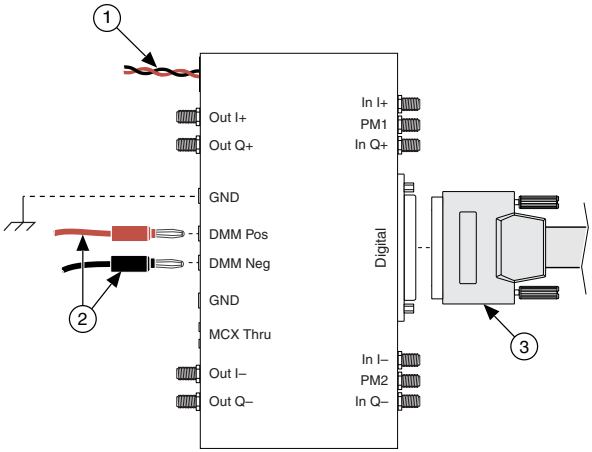
1. PXIe-5645
2. Power Meter 1
3. MCX Termination

No Connect Connections

1. Connect the PXI-4130 to the calibration fixture.
2. Connect the PXI-4072 to the DMM Pos and DMM Neg connectors on the calibration fixture.
3. Connect the PXI-2567 to the Digital connector on the calibration fixture.

The following figure illustrates the hardware setup.

Figure 8. No Connect Cabling Diagram



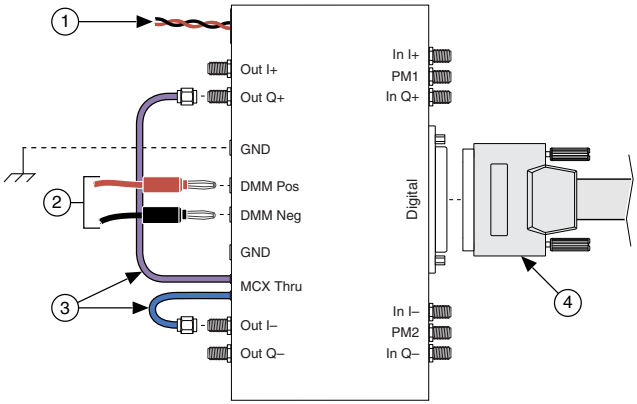
1. PXI-4130 Connection
2. PXI-4072 Connection
3. PXI-2567 Connection

Cable Measurements Connections

1. Connect the PXI-4130 to the calibration fixture.
2. Connect the PXI-4072 to the DMM Pos and DMM Neg connectors on the calibration fixture.
3. Connect an MCX (m)-to-SMA (m) cable from the Out Q+ connector to the nearest MCX Thru connector on the calibration fixture.
4. Connect an MCX (m)-to-SMA (m) cable from the Out I- connector to the nearest MCX Thru connector on the calibration fixture.
5. Connect the PXI-2567 to the Digital connector on the calibration fixture.

The following figure illustrates the hardware setup.

Figure 9. Cable Measurements Cabling Diagram



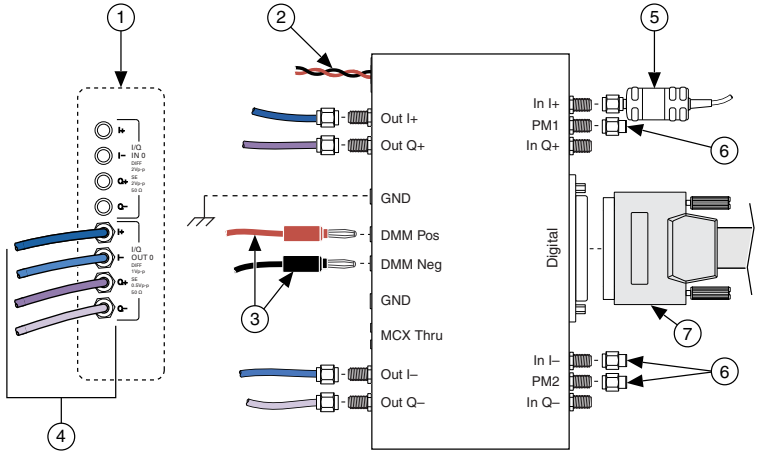
1. PXI-4130 Connection
2. PXI-4072 Connection
3. MCX (m)-to-SMA (m) Cable Connections
4. PXI-2567 Connection

Power Meter to I Connections

1. Connect the PXI-4130 to the calibration fixture.
2. Connect the PXI-4072 to the DMM Pos and DMM Neg connectors on the calibration fixture.
3. Connect Out I+ on the calibration fixture to I+ (I/Q OUT 0) on the PXIe-5645.
4. Connect Out Q+ on the calibration fixture to Q+ (I/Q OUT 0) on the PXIe-5645.
5. Connect Out I- on the calibration fixture to I- (I/Q OUT 0) on the PXIe-5645.
6. Connect Out Q- on the calibration fixture to Q- (I/Q OUT 0) on the PXIe-5645.
7. Connect power meter 1 to In I+ on the calibration fixture.
8. Connect MCX terminations to PM1, In I-, and PM2 on the calibration fixture.
9. Connect the PXI-2567 to the Digital connector on the calibration fixture.

   The following figure illustrates the hardware setup.

Figure 10. Power Meter to I Cabling Diagram



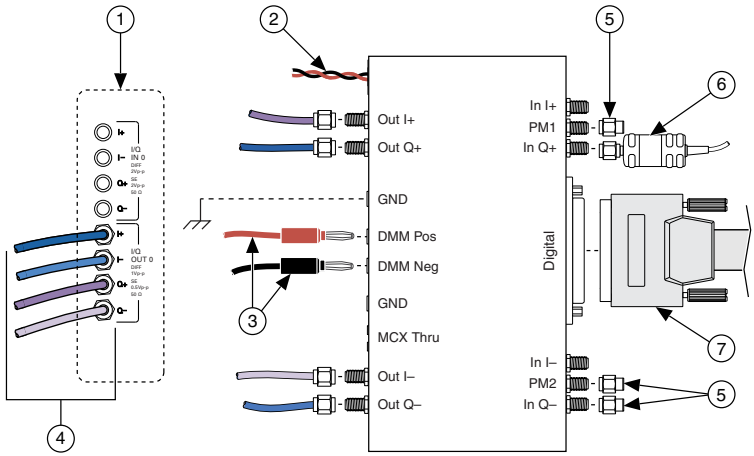
1. Zoomed View of PXIe-5645 I/Q Connectors
2. PXI-4130 Connection
3. PXI-4072 Connection
4. MCX (m)-to-SMA (m) Cables
5. Power Meter 1
6. MCX Terminations
7. PXI-2567 Connection

Power Meter to Q Connections

1. Connect the PXI-4130 to the calibration fixture.
2. Connect the PXI-4072 to the DMM Pos and DMM Neg ports of the calibration fixture.
3. Connect I+ (I/Q OUT 0) on the PXIe-5645 to Out I+ on the calibration fixture.
4. Connect Q+ (I/Q OUT 0) on the PXIe-5645 to Out Q+ on the calibration fixture.
5. Connect I- (I/Q OUT 0) on the PXIe-5645 to Out I- on the calibration fixture.
6. Connect Q- (I/Q OUT 0) on the PXIe-5645 to Out Q- on the calibration fixture.
7. Connect power meter 1 to In Q+ on the calibration fixture.
8. Connect MCX terminations to PM1, PM2, and In Q- on the calibration fixture.
9. Connect the PXI-2567 to the Digital connector on the calibration fixture.

   The following figure illustrates the hardware setup.

Figure 11. Power Meter to Q Cabling Diagram



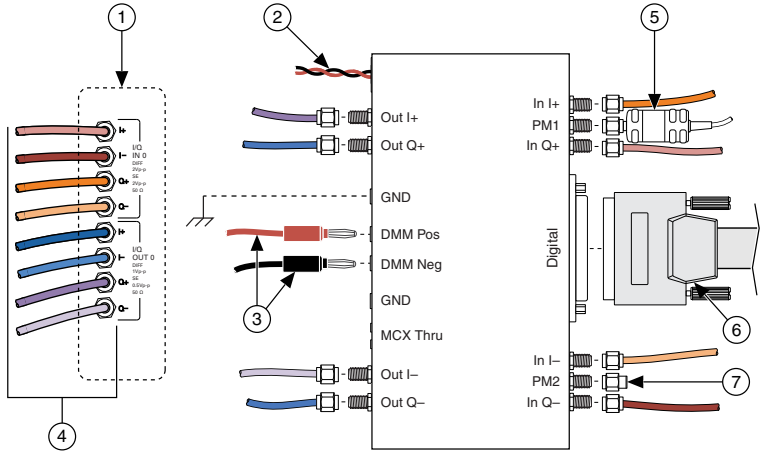
1. Zoomed View of PXIe-5645 I/Q Connectors
2. PXI-4130 Connection
3. PXI-4072 Connection
4. MCX (m)-to-SMA (m) Cables
5. MCX Terminations
6. Power Meter 1
7. PXI-2567 Connection

Swapped Connections

1. Connect the PXI-4130 to the calibration fixture.
2. Connect the PXI-4072 to the DMM Pos and DMM Neg connectors on the calibration fixture.
3. Connect I+ (I/Q IN 0) on the PXIe-5645 to In Q+ on the calibration fixture.
4. Connect I- (I/Q IN 0) on the PXIe-5645 to In I- on the calibration fixture.
5. Connect Q+ (I/Q IN 0) on the PXIe-5645 to In I+ on the calibration fixture.
6. Connect Q- (I/Q IN 0) on the PXIe-5645 to In Q- on the calibration fixture.
7. Connect I+ (I/Q OUT 0) on the PXIe-5645 to Out Q+ on the calibration fixture.
8. Connect I- (I/Q OUT 0) on the PXIe-5645 to Out Q- on the calibration fixture.
9. Connect Q+ (I/Q OUT 0) on the PXIe-5645 to Out I+ on the calibration fixture.
10. Connect Q- (I/Q OUT 0) on the PXIe-5645 to Out I- on the calibration fixture.
11. Connect power meter 1 to PM1 on the calibration fixture.
12. Connect an MCX termination to PM2 on the calibration fixture.
13. Connect the PXI-2567 to the Digital connector on the calibration fixture.

The following figure illustrates the hardware setup.

Figure 12. Swapped Cabling Diagram



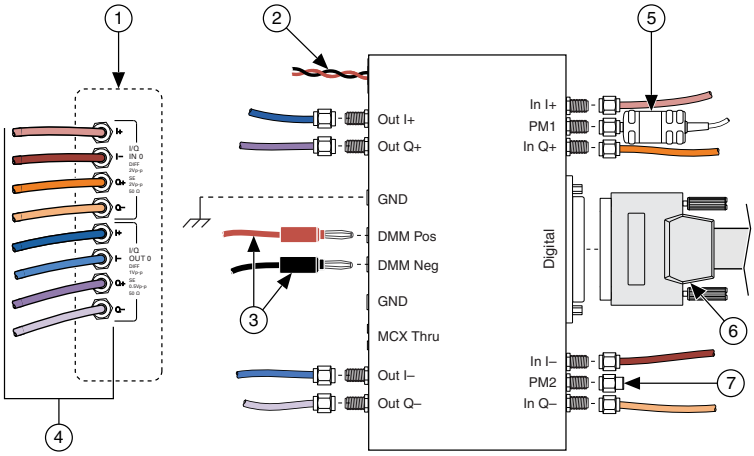
1. Zoomed View of PXIe-5645 I/Q Connectors
2. PXI-4130 Connection
3. PXI-4072 Connection
4. MCX (m)-to-SMA (m) Cables
5. Power Meter 1
6. PXI-2567 Connection
7. MCX Termination

Thru Connections

1. Connect the PXI-4130 to the calibration fixture.
2. Connect the PXI-4072 to the DMM Pos and DMM Neg connectors on the calibration fixture.
3. Connect I+ (I/Q IN 0) on the PXIe-5645 to In I+ on the calibration fixture.
4. Connect I- (I/Q IN 0) on the PXIe-5645 to In I- on the calibration fixture.
5. Connect Q+ (I/Q IN 0) on the PXIe-5645 to In Q+ on the calibration fixture.
6. Connect Q- (I/Q IN 0) on the PXIe-5645 to In Q- on the calibration fixture.
7. Connect I+ (I/Q OUT 0) on the PXIe-5645 to Out I+ on the calibration fixture.
8. Connect I- (I/Q OUT 0) on the PXIe-5645 to Out I- on the calibration fixture.
9. Connect Q+ (I/Q OUT 0) on the PXIe-5645 to Out Q+ on the calibration fixture.
10. Connect Q- (I/Q OUT 0) on the PXIe-5645 to Out Q- on the calibration fixture.
11. Connect power meter 1 to PM1 on the calibration fixture.
12. Connect an MCX termination to PM2 on the calibration fixture.
13. Connect the PXI-2567 to the Digital connector on the calibration fixture.

The following figure illustrates the hardware setup.

Figure 13. Thru Cabling Diagram



1. Zoomed View of PXIe-5645 I/Q Connectors
2. PXI-4130 Connection
3. PXI-4072 Connection
4. MCX (m)-to-SMA (m) Cables
5. Power Meter 1
6. PXI-2567 Connection
7. MCX Termination

Characterizing Relay Impedance

This procedure measures the resistance of each relay pair of the I/Q calibration fixture for a given measurement.

1. If the current iteration has the following values, continue to step 2. Otherwise, proceed to the next characterization.
   - Connection configuration: No connect
   - Signal path: No connection or terminated
   - Terminal configuration: Differential or single-ended
   - DMM source: I In, I Out, Q In, or Q Out
2. Ensure the calibration fixture is connected to the appropriate instrumentation based on the value of *connection configuration* in step 1 for the current iteration.
3. Use the following settings to configure the DMM for impedance measurements:
   - Function: 2-wire resistance
   - Digits of precision: 6 1/2
   - Range: 150 Ω
   - Aperture: 0.1 seconds
   - Auto zero: On
   - Offset compensated Ohms: On
   - Number of averages: 1
   - Powerline frequency: 60 Hz

4. Call the InitializeRelayCal VI and configure it using the following parameters:
   - **connection**: Current iteration value for *connection configuration*
   - **signal path**: Current iteration value for *signal path*
   - **terminal configuration**: Current iteration value for *terminal configuration*
   - **DMM source name**: Current iteration value for *DMM source*
5. Configure the I/Q calibration fixture based on the **IQ cal fixture cal** output of the IntializeRelayCal VI in step 4.
6. Measure the impedance using the DMM.
7. Pass the following values to the AdjustRelayCal VI:
   - **relay measurement type**: **relay measurement type** output of the IntializeRelayCal VI in step 4
   - **impedance**: Impedance value from step 6

Characterizing Cable Impedance

This procedure removes the impedance of each of the connected cables and measures impedance of the cable pairs I Out, Q Out, I In, and Q In.

1. If the current iteration has the following values, continue to step 2. Otherwise, proceed to the next characterization.
   - Connection configuration: No connect
   - Signal path: No connection
   - Terminal configuration: N/A
   - DMM source: I In, I Out, Q In, or Q Out
2. Ensure the calibration fixture is connected to the appropriate instrumentation based on the value of *connection configuration* in step 1 for the current iteration.
3. Use the following settings to configure the DMM for impedance measurements:
   - Function: 2-wire resistance
   - Digits of precision: 6 1/2
   - Range: 150 Ω
   - Aperture: 0.1 seconds
   - Auto zero: On
   - Offset compensated Ohms: On
   - Number of averages: 1
   - Powerline frequency: 60 Hz
4. Call the InitializeCableCal VI and configure it using the following parameters:
   - **connection**: Current iteration value for *connection configuration*
   - **signal path**: Current iteration value for *signal path*
   - **terminal configuration**: Current iteration value for *terminal configuration*
   - **DMM source name**: Current iteration value for *DMM source*
5. Configure the I/Q calibration fixture based on the **IQ cal fixture cal** output of the IntializeCableCal VI in step 4.
6. Measure the impedance using the DMM.
7. Pass the impedance value from step 6 to the **impedance** input of the AdjustCableCal VI.

8. Repeat steps 2 through 7 for the remaining cable pairs: Q Out+/Q Out-, I In+/I In-, and Q In+/Q In -.

Characterizing Impedance

This procedure measures the impedance for the input and output ports of the PXIe-5645 I/Q calibration fixture.

1. If the current iteration has the following values, continue to step 2, otherwise proceed to the next characterization.
   - Connection configuration: Thru
   - Signal path: No connection, inline, cross, absolute I, absolute Q, splitter I to I and power meter, or splitter I to Q and power meter
   - Terminal configuration: Differential or single-ended
   - DMM source: I In, I Out, Q In, or Q Out
2. Ensure the calibration fixture is connected to the appropriate instrumentation based on the value of *connection configuration* in step 1 for the current iteration.
3. Use the following settings to configure the DMM for impedance measurements:
   - Function: 2-wire resistance
   - Digits of precision: 6 1/2
   - Range: 150 Ω
   - Aperture: 0.1 seconds
   - Auto zero: On
   - Offset compensated Ohms: On
   - Number of averages: 1
   - Powerline frequency: 60 Hz
4. Call the InitializeImpedanceCal VI and configure it using the following parameters:
   - **connection**: Current iteration value for *connection configuration*
   - **signal path**: Current iteration value for *signal path*
   - **terminal configuration**: Current iteration value for *terminal configuration*
   - **DMM source name**: Current iteration value for *DMM source*
5. Configure the I/Q calibration fixture based on the **IQ cal fixture cal** output of the IntializeImpedanceCal VI in step 4.
6. Measure the impedance using the DMM.
7. Pass the impedance value from step 6 to the **impedance** input of the AdjustCableCal VI.
8. Repeat steps 3 through 7 for the remaining cable pairs: Q Out+/Q Out-, I In+/I In-, and Q In+/Q In -.

Characterizing Flatness

This procedure measures the flatness of the PXIe-5645 I/Q calibration fixture.

1. If the current iteration has the following values, continue to step 2, otherwise proceed to the next characterization.
   - Connection configuration:
     - Power meter on I Out
     - Power meter on I In
     - Power meter on Q In
     - Swapped
     - Thru
   - Signal path:
     - Inline
     - Cross
     - Absolute I
     - Absolute Q
     - Splitter I to I and power meter
     - Splitter I to Q and power meter
   - Terminal configuration: Differential or single-ended
   - DMM source: None
2. Ensure the calibration fixture is connected to the appropriate instrumentation based on the value of *connection configuration* in step 1 for the current iteration.
3. Call the InitializeFlatnessCal VI and configure it using the following parameters:
   - **connection**: Current iteration value for *connection configuration*
   - **signal path**: Current iteration value for *signal path*
   - **terminal configuration**: Current iteration value for *terminal configuration*
4. Configure the I/Q calibration fixture based on the **IQ cal fixture cal** output of the IntializeFlatnessCal VI in step 3.
5. Configure the PXIe-5645 to generate a -3 dBFS signal at a specified frequency offset signal using the following settings.
   - Level (V_{pk-pk}): 1 if *terminal configuration* is differential, otherwise 0.5
   - Tone amplitude: -3 dBFS
   - Tone frequency: 500 kHz
   - Offset (V): 0
   - Common-mode (V): 0
   - Load impedance: Default
6. Configure the power sensor to correct for the frequency from step 5 using the power sensor frequency correction function.
7. Measure the output power of the generated signal using the power sensor.

   Store the result as *fixture flatness* (*f*), where *f* is the frequency generated in step 5.
8. Repeat steps 5 through 7 for the remaining frequencies from 500 kHz to 42.5 MHz in 1 MHz steps.

9. Call the AdjustFlatnessCal VI. Pass the *fixture flatness* versus frequency from step 8 to the **flatness measurement** input.

Characterizing Matching

This procedure measures the gain imbalance and phase matching for the input and output ports of the PXIe-5645 I/Q calibration fixture.

1. If the current iteration has the following values, continue to step 2, otherwise proceed to the next characterization.
   - Connection configuration: Swapped or thru
   - Signal path: Inline or cross
   - Terminal configuration: Differential or single-ended
   - DMM source: None
2. Ensure the calibration fixture is connected to the appropriate instrumentation based on the value of *connection configuration* in step 1 for the current iteration.
3. Call the InitializeMatchingCal VI and configure it using the following parameters:
   - **connection**: Current iteration value for *connection configuration*
   - **signal path**: Current iteration value for *signal path*
   - **terminal configuration**: Current iteration value for *terminal configuration*
4. Configure the I/Q calibration fixture based on the **IQ cal fixture cal** output of the IntializeMatchingCal VI in step 3.
5. Use the following settings to configure the PXIe-5645 to generate a -3 dBFS signal at a specified frequency offset signal:
   - Level (V_{pk-pk}): 1 if *terminal configuration* is differential, otherwise 0.5
   - Tone amplitude: -3 dBFS
   - Tone frequency: *start frequency* from the following table
   - Offset (V): 0
   - Common-mode (V): 0
   - Load impedance: Default

Table 10. Matching Characterization Test Frequencies

Signal Path	Start Frequency (MHz)	Stop Frequency (MHz)	Step Size (kHz)
Inline	-40.5	40.5	500
Cross	40.5	-40.5	500

6. Use the following settings to configure the PXIe-5645 I/Q input to acquire a signal:
   - Level (V_{pk-pk}): 0.8 if *terminal configuration* is differential, otherwise 0.4
   - Sample rate: 120 MS/s
   - Acquisition size: 15,000 samples
7. Measure the resulting generated signal using the PXIe-5645 I/Q input. Store the following values from the measurement:

   Fixture Gain Imbalance = $I_{magnitude}(f)/Q_{magnitude}(f)$

   Fixture Phase Mismatch = $I_{phase}(f) - Q_{phase}(f)$

8. Repeat steps 5 through 7 for the remaining frequencies listed in the previous table for the current iteration.
9. Call the AdjustMatchingCal VI. Pass the *Fixture Gain Imbalance* versus frequency from step 8 to the **gain imbalance** input. Pass the *Fixture Phase Mismatch* versus frequency from step 8 to the **phase skew** input.

Characterizing Gain

This procedure measures the gain for the input and output ports of the PXIe-5645 I/Q calibration fixture.

1. If the current iteration has the following values, continue to step 2, otherwise proceed to the next characterization.
   - Connection configuration: Thru
   - Signal path:
     - Inline
     - Cross
     - Absolute I
     - Absolute Q
     - Splitter I to I and power meter
     - Splitter I to Q and power meter
   - Terminal configuration: Differential, or single-ended
   - DMM source: I In, I Out, Q In, Q Out, or power meter
2. Ensure the calibration fixture is connected to the appropriate instrumentation based on the value of *connection configuration* in step 1 for the current iteration.
3. Call the InitializeGainCal VI and configure it using the following parameters:
   - **connection**: Current iteration value for *connection configuration*
   - **signal path**: Current iteration value for *signal path*
   - **terminal configuration**: Current iteration value for *terminal configuration*
   - **DMM source name**: Current iteration value for *DMM source*
4. Use the following settings to configure the DMM for a voltage measurement:
   - Function: DC Volts
   - Digits of precision: 6 1/2
   - Range: 2 Volts
   - Aperture: 0.1 seconds
   - Auto zero: On
   - Offset compensated Ohms: On
   - Number of averages: 2
   - Powerline frequency: 60 Hz
5. Use the following settings to configure the PXIe-5645 I/Q output to generate a DC value of 1 V:
   - Level (V_{pk-pk}): 1 if *Terminal Configuration* is differential, otherwise 0.5
   - DC level: 1
   - Offset (V): 0

- Common-mode voltage: 0
- Load impedance: Default

6. Measure the resulting signal using the DMM.
7. Use the following settings to configure the PXIe-5645 I/Q output to generate a DC value of -1 V:
   - Level (V_{pk-pk}): 1 if *Terminal Configuration* is differential, otherwise 0.5
   - DC level: -1
   - Offset (V): 0
   - Common-mode voltage: 0
   - Load impedance: Default
8. Measure the resulting signal using the DMM.
9. Call the AdjustGainCal VI and pass (result of step 8 - result of step 5) to the **DMM measurement** input.

Self-Calibrating the PXIe-5645

Allow a 30-minute warm-up time before you begin self-calibration.

Note The warm-up time begins after the PXI Express chassis is powered on and the operating system completely loads.

The PXIe-5645 includes precise internal circuits and references used during self-calibration to adjust for any errors caused by short-term fluctuations in the environment. You must call the self-calibration function to validate the specifications in the *Verification* section.

1. Perform self-calibration using the installed self-calibration executable or the niVST Self-Calibrate VI. Open one of the following self-calibration tools:
   - Navigate to **Start»All Programs»National Instruments»Vector Signal Transceivers»VST Self-Calibrate** or `<Program Files>\National Instruments\NI VST\Self Calibration` to launch the self-calibration executable.
   - Add the niVST Self-Calibrate VI, located on the **Functions»Instrument I/O»Instrument Drivers»NI VST Calibration** palette, to a block diagram.
2. Run the self-calibration executable or VI.

As-Found and As-Left Limits

The as-found limits are the published specifications for the PXIe-5645. NI uses these limits to determine whether the PXIe-5645 meets the specifications when it is received for calibration. Use the as-found limits during initial verification.

The as-left calibration limits are equal to the published NI specifications for the PXIe-5645, less guard bands for measurement uncertainty, temperature drift, and drift over time. NI uses these limits to reduce the probability that the instrument will be outside the published specification limits at the end of the calibration cycle. Use the as-left limits when performing verification after adjustment.

RF Verification

The performance verification procedures assume that adequate traceable uncertainties are available for the calibration references.

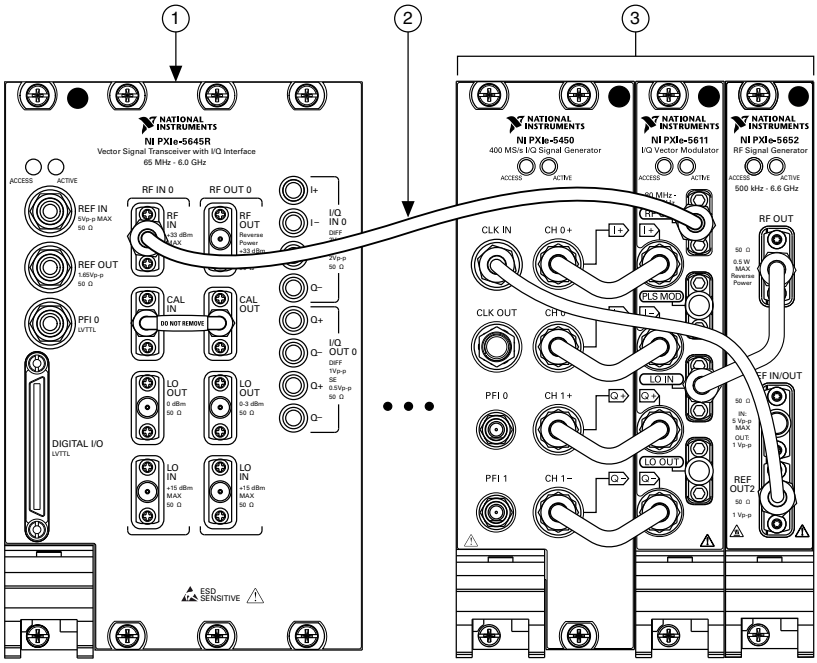
Verifying Internal Frequency Reference

This procedure verifies the frequency accuracy of the PXIe-5645 onboard frequency reference using a vector signal generator.

1. Connect the vector signal generator RF OUT front panel connector to the PXIe-5645 RF IN front panel connector.

   The following figure illustrates the hardware setup.

Figure 14. Internal Frequency Reference Verification Cabling Diagram



1. PXIe-5645
2. SMA (m)-to-SMA (m) Cable
3. Vector Signal Generator

2. Connect an available 10 MHz rubidium frequency reference output to the vector signal generator REF IN front panel connector.

3. Configure the vector signal generator to generate a 2.22 GHz signal with a 0 dBm average output power, using the following settings:
   - Center frequency: 2.22 GHz
   - Output power: 0 dBm
   - Reference Clock source: External
4. Configure the PXIe-5645 to acquire and measure the signal generated in step 3, using the following settings:
   - Center frequency: 2.22 GHz
   - Reference level: +10 dBm
   - Resolution bandwidth: 100 Hz
   - Span: 100 kHz
   - FFT window: Hanning
   - Averaging type: RMS
   - Number of averages: 20
   - Reference Clock source: Onboard
5. Measure the frequency of the peak acquired tone.
6. Calculate the deviation using the following equation:

$$\Delta f = \left| \frac{f_{measured\mathrm{GHz}} - 2.2\mathrm{GHz}}{2.2\mathrm{GHz}} \right|$$

7. The result in step 6 should be less than the result of the following equation:

   initial accuracy + *aging* + *temperature stability*
   where
   initial accuracy = ±200 * 10^{-9}
   aging = ±1 * 10^{-6} */year* * *number of years since last adjustment*
   temperature stability = ±1 * 10^{-6}

Note You can determine number of years since last adjustment programmatically using the PXIe-5644/5645 Instrument Design Libraries.

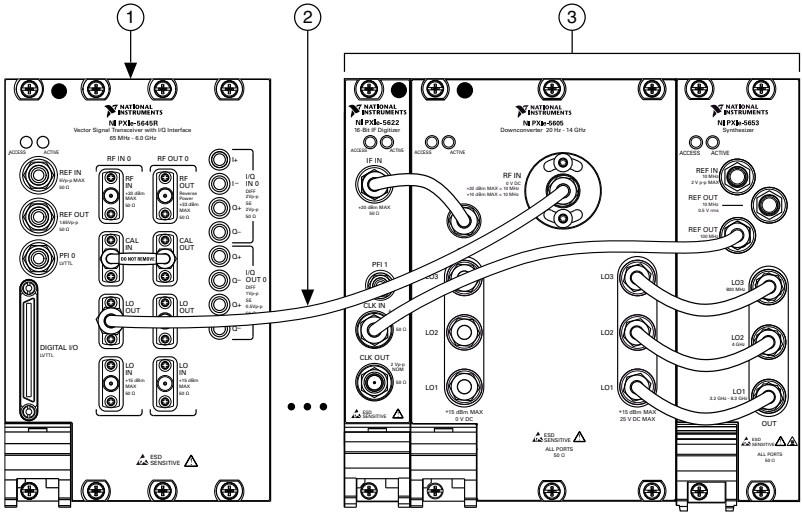
Verifying RF Input Spectral Purity

This procedure verifies the RF input spectral purity of the PXIe-5645.

1. Connect the PXIe-5645 LO OUT (RF IN 0) front panel connector to the RF IN front panel connector of the spectrum analyzer.

   The following figure illustrates the hardware setup.

Figure 15. RF Input Spectral Purity Verification Cabling Diagram



1. PXIe-5645
2. SMA (m)-to-SMA (m) Cable
3. Spectrum Analyzer

2. Connect an available 10 MHz rubidium frequency reference output to the PXIe-5645 REF IN front panel connector.
3. Connect an available 10 MHz rubidium frequency reference output to the spectrum analyzer REF IN front panel connector.
4. Configure the PXIe-5645 to export the LO using the following settings:
   - Center frequency: 1 GHz
   - LO OUT: Enabled
   - Reference Clock source: REF IN
5. Configure the spectrum analyzer to acquire a spectrum using the following settings:
   - Center frequency: 1 GHz
   - Reference level: 0 dBm
   - Span: 100 Hz
   - Resolution bandwidth: 10 Hz
   - Reference Clock source: External
   - Averaging type: RMS
   - Number of averages: 20
6. Measure the peak power at the center frequency.

   The measured value is the power, in dBm, of the generated tone.

7. Configure the spectrum analyzer to acquire a spectrum using the following settings:
   - Center frequency: *Center frequency* from step 4 + 20 kHz
   - Reference level: 0 dBm
   - Span: 100 Hz
   - Resolution bandwidth (RBW): 10 Hz
   - Reference Clock source: External
   - Averaging type: RMS
   - Number of averages: 20
8. Measure the power at a 20 kHz offset. Normalize the result to 1 Hz bin width by subtracting 10 * log (RBW), where RBW is the setting specified in step 7.

   The result of this step is in dBm/Hz.
9. Calculate the relative difference between the signal and noise using the following equation:

   SSB Phase Noise at 20 kHz (dBc/Hz) = *step 8 measurement* (dBc/Hz) - *step 6 measurement* (dBm)

   The result of this step is in dBc/Hz.
10. Compare the results of step 9 to the specified limits in the following table.

Table 11. SSB Phase Noise at 20 kHz Offset (Low Loop Bandwidth)

Frequency	As-Found Limit (dBc/Hz)	As-Left Limit (dBc/Hz)
<3 GHz	-99	-99
3 GHz to 4 GHz	-91	-91
>4 GHz to 6 GHz	-93	-93

11. Repeat steps 4 through 10 for the following frequencies:
    - 1 GHz
    - 1.9 GHz
    - 2.4 GHz
    - 3 GHz
    - 4.4 GHz
    - 5.8 GHz
12. Repeat steps 4 through 11 for the configurations specified in the following tables.

Table 12. SSB Phase Noise at 20 kHz Offset (Medium-Loop Bandwidth)

Frequency	As-Found Limit (dBc/Hz)	As-Left Limit (dBc/Hz)
<3 GHz	-99	-99
3 GHz to 4 GHz	-93	-93
>4 GHz to 6 GHz	-93	-93

Table 13. SSB Phase Noise at 20 kHz Offset (High-Loop Bandwidth)

Frequency	As-Found Limit (dBc/Hz)	As-Left Limit (dBc/Hz)
<3 GHz	-94	-94
3 GHz to 4 GHz	-91	-91
>4 GHz to 6 GHz	-87	-87

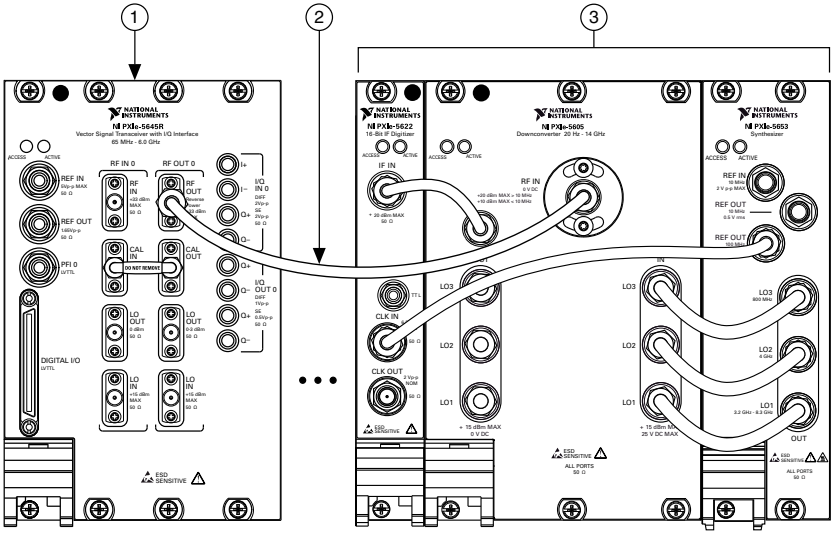
Verifying RF Output Spectral Purity

This procedure verifies the RF output spectral purity of the PXIe-5645.

1. Connect the PXIe-5645 RF OUT (RF IN 0) front panel connector to the RF IN front panel connector of the spectrum analyzer.

   The following figure illustrates the hardware setup.

Figure 16. RF Output Spectral Purity Verification Cabling Diagram



1. PXIe-5645
2. SMA (m)-to-SMA (m) Cable
3. Spectrum Analyzer

2. Connect an available 10 MHz rubidium frequency reference output to the PXIe-5645 REF IN front panel connector.
3. Connect an available 10 MHz rubidium frequency reference output to the spectrum analyzer REF IN front panel connector.
4. Configure the PXIe-5645 to generate an offset CW tone using the following settings:
   - Center frequency: 1 GHz
   - Output power: 0 dBm

- Tone offset: 3.75 MHz
- I/Q rate: 10 MS/s
- Loop bandwidth: Low
- Fractional mode: Enabled
- Step size: 200 kHz
- Reference Clock source: REF IN

5. Configure the spectrum analyzer to acquire a spectrum using the following settings:
   - Center frequency: 1 GHz + 3.75 MHz
   - Reference level: 0 dBm
   - Span: 100 Hz
   - Resolution bandwidth: 10 Hz
   - Reference Clock source: External
   - Averaging type: RMS
   - Number of averages: 20
6. Measure the peak power at the center frequency.

   The measured power should match the power, in dBm, of the generated tone.
7. Configure the spectrum analyzer to acquire a spectrum using the following settings:
   - Center frequency: *Center frequency* from step 5 + 20 kHz
   - Reference level: 0 dBm
   - Span: 100 Hz
   - Resolution bandwidth: 10 Hz
   - Reference Clock source: External
   - Averaging type: RMS
   - Number of averages: 20
8. Measure the power at a 20 kHz offset. Normalize the result to 1 Hz bin width by subtracting 10 * log (RBW), where RBW is the setting specified in step 7.

   The result of this step is in dBm/Hz.
9. Calculate the relative difference between the signal and noise using the following equation:

   SSB Phase Noise at 20 kHz (dBm/Hz) = *step 8 measurement* (dBm/Hz) - *step 6 measurement* (dBm)

   The result of this step is in dBm/Hz.
10. Compare the results of step 9 to the specified limits in the following table.

Table 14. SSB Phase Noise at 20 kHz Offset (Low-Loop Bandwidth)

Frequency	As-Found Limit (dBc/Hz)	As-Left Limit (dBc/Hz)
<3 GHz	-99	-99
3 GHz to 4 GHz	-91	-91
>4 GHz to 6 GHz	-93	-93

11. Repeat steps 4 through 10 for the following frequencies:
    - 1 GHz
    - 1.9 GHz
    - 2.4 GHz
    - 3 GHz
    - 4.4 GHz
    - 5.8 GHz
12. Repeat steps 4 through 11 for the configurations specified in the following tables.

Table 15. SSB Phase Noise at 20 kHz Offset (Medium-Loop Bandwidth)

Frequency	As-Found Limit (dBc/Hz)	As-Left Limit (dBc/Hz)
<3 GHz	-99	-99
3 GHz to 4 GHz	-93	-93
>4 GHz to 6 GHz	-93	-93

Table 16. SSB Phase Noise at 20 kHz Offset (High-Loop Bandwidth)

Frequency	As-Found Limit (dBc/Hz)	As-Left Limit (dBc/Hz)
<3 GHz	-94	-94
3 GHz to 4 GHz	-91	-91
>4 GHz to 6 GHz	-87	-87

Verifying Input Absolute Amplitude Accuracy

This procedure verifies the absolute amplitude accuracy of the PXIe-5645 input channels.

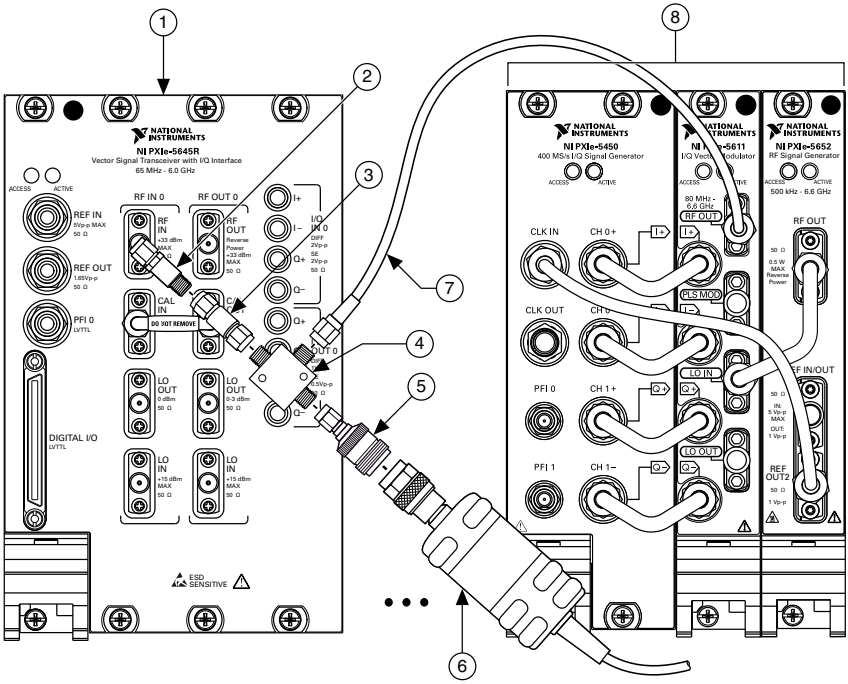
This procedure requires the same attenuator and splitter positioning as used during the *Test System Characterization* procedures, as well as the data collected in the *Characterizing Power Splitter Balance* section. You must characterize the power splitter balance before running this procedure. Ensure you use the characterization data derived from test points in the *Characterization Test Points for Verification Procedures* table in the *Characterizing Power Splitter Balance* section.

You must zero the power sensor as described in the *Zeroing the Power Sensor* section prior to starting this procedure.

1. Connect the vector signal generator RF OUT front panel connector to the input terminal of the power splitter using a SMA (m)-to-SMA (m) cable.
2. Connect splitter output 1 directly to the power sensor input connector using the SMA (m)-to-N (f) adapter.
3. Connect splitter output 2 to the SMA (f) end of the 6 dB attenuator using a 3.5 mm (m)-to-3.5 mm (m) adapter.
4. Connect the remaining 6 dB attenuator SMA (m) connector directly to the PXIe-5645 RF IN front panel connector.

The following figure illustrates the complete hardware setup.

Figure 17. Input Absolute Amplitude Accuracy Verification Cabling Diagram



1. PXIe-5645
2. 6 dB Attenuator
3. 3.5 mm (m)-to-3.5 mm (m) Adapter
4. Power Splitter
5. SMA (m)-to-N (f) Adapter
6. Power Sensor
7. SMA (m)-to-SMA (m) Cable
8. Vector Signal Generator

5. Configure the PXIe-5645 to acquire a signal at 500 MHz, using the following settings:
   - Center frequency: 500 MHz
   - Reference level: 30 dBm

   Note Steps 6 through 10 create correction factors that transfer the accuracy of the power sensor to the vector signal generator. Record the results from these steps in a lookup table called *Accuracy Transfer Results*.

6. Configure the vector signal generator to generate a 76.25 MHz tone, using the following settings:
   - Center frequency: 76.25 MHz
   - Tone offset: 3.75 MHz
   - I/Q rate: 10 MS/s
   - Output power: *Configured output power* from transfer row A in the following table.

Table 17. RF Input Accuracy Transfers

Transfer	Supported Reference Levels (dBm)	Configured Output Power (dBm)	Start Frequency (MHz)	Stop Frequency (MHz)	Frequency Step Size (MHz)
A	30 to -10	0	76.25	101.25	5
			146.25	946.25	50
			996.25	5,996.25	200
B	<-10 to -30	-20	76.25	101.25	5
			146.25	946.25	50
			996.25	5,996.25	200

7. Configure the power sensor to correct for the (*center frequency* + *tone offset*) from step 6 using the power sensor frequency correction function.
8. Measure the power of the signal present at the reference output of the power splitter using the power sensor.

   Record the results from this step as *accuracy transfer result*.
9. Repeat steps 6 through 8 for the remaining frequencies listed in transfer row A in the previous table.
10. Repeat steps 6 through 9 for transfer row B in the previous table. Create a table and include a value for each test point, *transfer* versus *frequency*.
11. Configure the PXIe-5645 to acquire a signal at 80 MHz, using the following settings:
    - Center frequency: 80 MHz
    - Reference level: 30 dBm
    - Span: 10 MHz
    - Resolution bandwidth: 1 kHz
    - Averaging type: RMS
    - Number of averages: 10
    - FFT window: Flat Top
12. Configure the vector signal generator to generate a signal at the *center frequency* specified in step 11 with a 3.75 MHz signal offset, using the following settings:
    - Center frequency: *Center frequency* from step 11
    - Tone offset: 3.75 MHz
    - Power level: *Configured output power* from the transfer row in the previous table that supports the *reference level* from step 11.
    - I/Q rate: 10 MS/s
    - Digital gain: (*reference level* from step 11 - *power level* from step 12) or 0 dB, whichever is less.
13. Calculate the *transfer input power* using the following equation:

transfer input power = *accuracy transfer result* + *digital gain* from step 12

Note Determine the *accuracy transfer result* by interpolating between the data points in the *Accuracy Transfer Results* table.

14. Calculate the *corrected input power* using the following equation:

    corrected input power = *transferred input power* + *splitter balance*

    Note Determine the *splitter balance* by interpolating between data points derived using test points in the *Characterization Test Points for Verification Procedures* table in the *Characterizing Power Splitter Balance* section.

15. Configure the PXIe-5645 using the settings from step 11, perform an acquisition, and measure the tone present at the offset of 3.75 MHz.
16. Calculate the *absolute amplitude accuracy* using the following equation:

    absolute amplitude accuracy = PXIe-5645 *input power* - *corrected input power*

17. Repeat steps 11 through 16 for the remaining frequencies in the previous table.
18. Repeat steps 11 through 17 for the remaining reference levels from 30 dBm to -30 dBm in 10 dB increments.
19. Compare the *absolute amplitude accuracy* values measured to the verification test limits in the following table.

Table 18. Input Absolute Amplitude Accuracy Verification Test Limits

Frequency	As-Found Limit (dB)	As-Left Limit (dB)
65 MHz to <375 MHz	±0.70	±0.55
375 MHz to <2 GHz	±0.65	±0.45
2 GHz to <4 GHz	±0.70	±0.40
4 GHz to 6 GHz	±0.90	±0.55

Verifying Input Frequency Response

This procedure verifies the frequency response of the PXIe-5645 input channels.

This procedure requires the same attenuator and splitter positioning as used during the *Test System Characterization* procedures, as well as the data collected in the *Characterizing Power Splitter Balance* section. You must characterize the power splitter balance before running this procedure. Ensure you use the characterization data derived from test points in the *Characterization Test Points for Verification Procedures* table in the *Characterizing Power Splitter Balance* section.

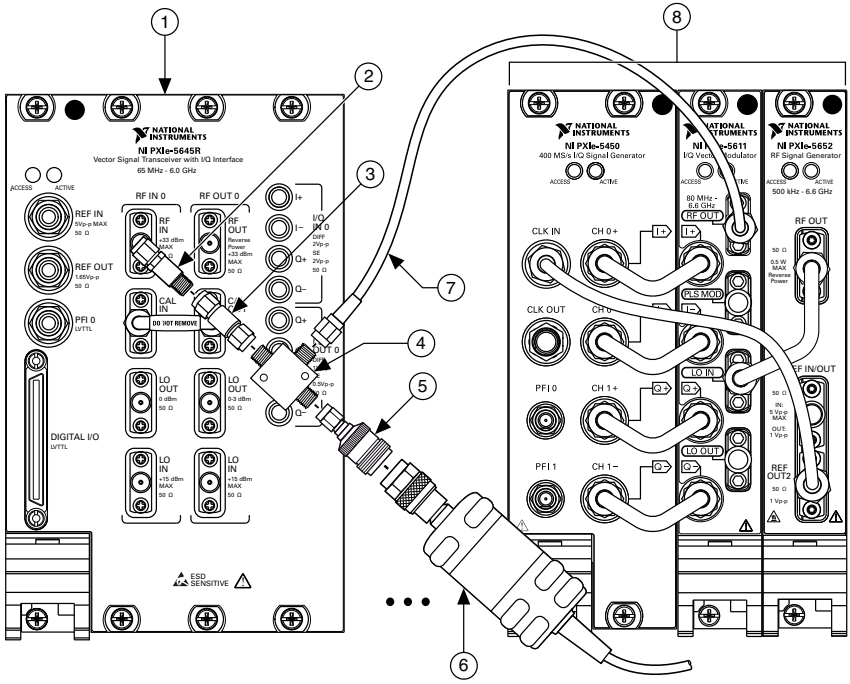
You must zero the power sensor as described in the *Zeroing the Power Sensor* section prior to starting this procedure.

1. Connect the vector signal generator RF OUT front panel connector to the input terminal of the power splitter using an SMA (m)-to-SMA (m) cable.
2. Connect splitter output 1 directly to the power sensor input connector using the SMA (m)-to-N (f) adapter.

3. Connect splitter output 2 to the SMA (f) end of the 6 dB attenuator using a 3.5 mm (m)-to-3.5 mm (m) adapter.
4. Connect the remaining 6 dB attenuator SMA (m) connector directly to the PXIe-5645 RF IN front panel connector.

The following figure illustrates the complete hardware setup.

Figure 18. Input Frequency Response Verification Cabling Diagram



1. PXIe-5645
2. 6 dB Attenuator
3. 3.5 mm (m)-to-3.5 mm (m) Adapter
4. Power Splitter
5. SMA (m)-to-N (f) Adapter
6. Power Sensor
7. SMA (m)-to-SMA (m) Cable
8. Vector Signal Generator

5. Configure the PXIe-5645 to acquire a signal using the following settings:
   - Center frequency: 500 MHz
   - Reference level: 30 dBm

   Note Steps 6 through 11 create correction factors that transfer the accuracy of the power sensor to the vector signal generator. Record the results from these steps in a lookup table called *Accuracy Transfer Results*.
6. Configure the vector signal generator to generate a 300 MHz tone, using the following settings:
   - Center frequency: 300 MHz
   - Tone offset: -(*test bandwidth*/2) MHz, where *test bandwidth* is the value specified in the *Input Frequency Response Test Points* table.

- I/Q rate: 10 MS/s
- Output power: Configured output power from the transfer A row in the following table.

Table 19. Frequency Response Accuracy Transfers

Transfer	Supported Reference Levels (dBm)	Configured Output Power (dBm)
A	30 to -10	0
B	-10 to -30	-20

7. Configure the power sensor to correct for the value of (*center frequency* + *tone offset*) from step 6 using the power sensor frequency correction function.
8. Measure the power of the signal present at splitter output 1 of the power splitter using the power sensor.
9. Repeat steps 6 through 8 by sweeping the vector signal generator tone offset from -(*test bandwidth*/2) to +(*test bandwidth*/2) in 5 MHz steps, where *test bandwidth* is the value specified in the following table.

Table 20. Input Frequency Response Test Points

Test Bandwidth (MHz)	Test Points (MHz)				
20	300				
80	450	550	600	650	800
	950	1,000	1,050	1,200	1,550
	1,600	1,650	2,000	2,650	2,700
	2,750	3,000	3,800	3,950	4,000
	4,050	4,500	4,950	5,000	5,050
	5,500	5,950			

10. Repeat steps 6 through 9 for the remaining frequencies listed in the previous table.
11. Repeat steps 6 through 10 for transfer B in the *Frequency Response Accuracy Transfers* table.
12. Configure the PXIe-5645 to acquire a signal at 300 MHz, using the following settings:
    - Center frequency: 150 MHz
    - Reference level: 30 dBm
    - Span: *Test bandwidth* from the *Input Frequency Response Test Points* table
    - Resolution bandwidth: 1 kHz
    - Averaging type: RMS
    - Number of averages: 10
    - FFT window: Flat Top

13. Configure the vector signal generator to generate a signal at the *center frequency* specified in step 12 - (*test bandwidth*/2) MHz, where *test bandwidth* is the value specified in the previous table, using the following settings:
    - Center frequency: *Center frequency* from step 12
    - Tone offset: -(*test bandwidth*/2) MHz
    - Power level: *Configured output power* from the transfer row in the *Accuracy Transfer Definitions* table from the *Characterizing Power Splitter Loss* section that supports the *reference level* from step 12.
    - I/Q rate: 10 MS/s
    - Digital gain: (*reference level* from step 10 - *power level* from step 13 or 0 dB, whichever is less.
14. Calculate the *transfer input power* using the following equation:

    transfer input power = *accuracy transfer result* + *digital gain* from step 13

    Note Find the *accuracy transfer result* by interpolating between the data points in the *Accuracy Transfer Results* table.
15. Calculate the *corrected input power* using the following equation:

    corrected input power = *transferred input power* + *splitter balance*

    Note Determine the *splitter balance* by interpolating between data points derived using test points in the *Characterization Test Points for Verification Procedures* table in the *Characterizing Power Splitter Balance* section.
16. Configure the PXIe-5645 using the settings from step 12, perform an acquisition, and measure the tone present at the (*center frequency* + *tone offset*) from step 13.
17. Calculate the *absolute amplitude accuracy* using the following equation:

    absolute amplitude accuracy = PXIe-5645 *input power* - *corrected input power*
18. Repeat steps 13 through 17 by sweeping the vector signal generator tone offset from -(*test bandwidth*/2) to +(*test bandwidth*/2) in 5 MHz steps, where *test bandwidth* is the value specified in the *Input Frequency Response Test Points* table.
19. Determine the positive and negative frequency response results for the center frequency from step 12 by completing the following steps.
    a) Subtract the median *absolute power level accuracy* from the maximum *absolute power level accuracy* to determine the positive (+) *frequency response*.
    b) Subtract the minimum *absolute power level accuracy* from the median *absolute power level accuracy* to determine the negative (-) *frequency response*.
20. Repeat steps 12 through 19 for the remaining frequencies in the *Input Frequency Response Test Points* table.
21. Repeat steps 12 through 20 for the remaining reference levels between 0 dBm and -30 dBm in 10 dB steps.
22. Compare the ± *frequency response* values measured to the verification test limits in the following table.

Table 21. Input Frequency Response Test Limits

Frequency	Equalized Bandwidth (MHz)	As-Found Limit (dB)	As-Left Limit (dB)
>109 MHz to 375 MHz	20	±0.5	±0.5
>375 MHz to 6 GHz	80	±0.5	±0.5

Verifying Input Average Noise Density

This procedure verifies the average noise level of the PXIe-5645.

1. Connect a 50 Ω terminator to the PXIe-5645 RF IN front panel connector.
2. Configure the PXIe-5645 to acquire a signal at 100 MHz center frequency, using the following settings:
   - Center frequency: 100 MHz
   - Reference level: -50 dBm
   - Span: 1 MHz
   - Resolution bandwidth: 1 kHz
   - Averaging type: RMS
   - Number of averages: 50
   - FFT window: Flat Top
3. Read the power spectral density from the PXIe-5645.
4. Convert the sorted spectrum magnitude values from decibel milliwatts (dBm) to watts (W), calculate the mean, and convert the result back to dBm. The result is the *average noise* based on the configuration in step 2. Convert *average noise* to *average noise density* by normalizing to 1 Hz using the following equation:

   average noise density = *average noise* - 10 * log(*resolution bandwidth* from step 2)

   Record the result.
5. Repeat steps 2 through 4 for the remaining frequencies from 100 MHz to 6 GHz in 590 MHz steps.
6. Change the reference level to -10 dBm and repeat steps 2 through 5.
7. Compare the PXIe-5645 *average noise density* to the verification test limits listed in the following tables.

Table 22. Average Noise Density Test Limits (-50 dBm Reference Level)

Frequency	As-Found Limit (dBm/Hz)	As-Left Limit (dBm/Hz)
65 MHz to 4 GHz	-159	-159
>4 GHz to 6 GHz	-156	-156

Table 23. Average Noise Density Test Limits (-10 dBm Reference Level)

Frequency	As-Found Limit (dBm/Hz)	As-Left Limit (dBm/Hz)
65 MHz to 4 GHz	-145	-145
>4 GHz to 6 GHz	-144	-144

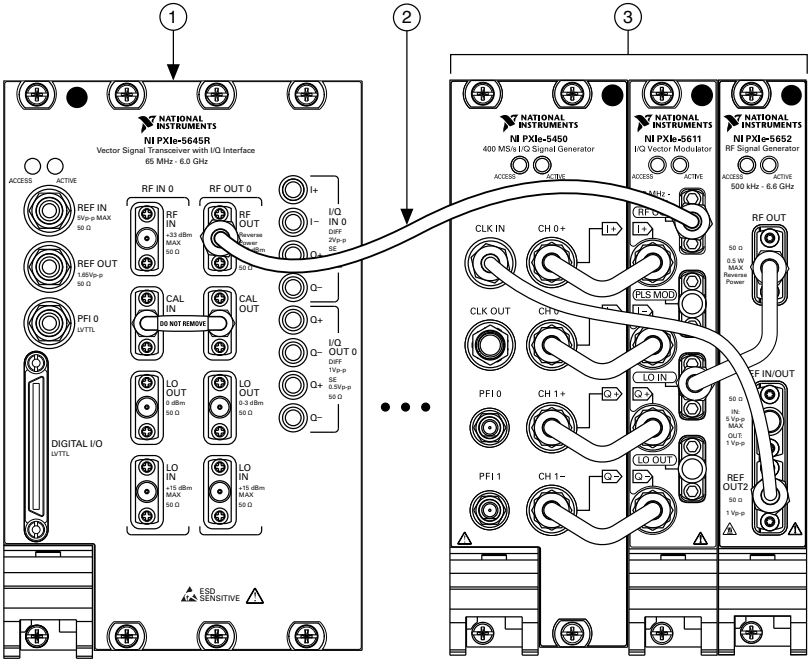
Verifying Input Nonharmonic Spurs

This procedure verifies the nonharmonic spurs in the presence of an external signal.

1. Connect the vector signal generator RF OUT connector to the RF IN front panel connector of the PXIe-5645.

   The following figure illustrates the hardware setup.

Figure 19. Input Nonharmonic Spurs Verification Cabling Diagram



1. PXIe-5645
2. SMA (m)-to-SMA (m) Cable
3. Vector Signal Generator

2. Connect an available 10 MHz rubidium frequency reference output to the PXIe-5645 REF IN front panel connector.
3. Connect an available 10 MHz rubidium frequency reference output to the vector signal generator REF IN front panel connector.

4. Configure the PXIe-5645 to acquire an 80 MHz-wide signal, using the following settings:
   - Center frequency: 144.2 MHz
   - Reference level: 0 dBm
   - Span: 80 MHz
   - Resolution bandwidth: 1 kHz
   - Averaging type: RMS
   - Number of averages: 10
   - FFT window: Flat Top
5. Configure the vector signal generator to generate a single -1 dBr tone at the *center frequency* specified in step 4.

   Note The following steps provide a general method for validating the nonharmonic spurs. For an improved measurement, use a peak-detect method to differentiate spurious content from noise.
6. Acquire an 80 MHz-wide spectrum using the PXIe-5645.
7. Measure the peak power within 100 kHz to 1 MHz offset of the tone on either side of the carrier frequency from the data acquired in step 6.

   Record the maximum value for comparison to the >100 kHz offset limits.
8. Measure the peak power at a >1 MHz offset of the tone on either side of the carrier frequency from the data acquired in step 6.

   Record the maximum value for comparison to the >1,000 kHz offset limits.
9. Repeat steps 4 through 8 for the remaining test points listed in the following table.

Table 24. Input Nonharmonic Spurs Test Points

Frequency (MHz)				
144.2	264.2	504.2	1,008.2	2,016.2
2,502.2	3,024.2	4,008.2	5,016.2	—

10. Compare the results from steps 7 through 9 to the test limits in the following table.

Table 25. Input Nonharmonic Spurs Test Limits

Frequency	Offset (kHz)	As-Found Limit (dBc)	As-Left Limit (dBc)
65 MHz to 3 GHz	>100	-60	-60
	>1,000	-75	-75
>3 GHz to 6 GHz	>100	-55	-55
	>1,000	-70	-70

Verifying Output Power Level Accuracy

This procedure verifies the power level accuracy of the PXIe-5645 RF output channel.

This procedure requires the test setup and data collected in the *Characterizing Power Splitter Loss* section. You must characterize the power splitter loss before running this procedure.

Ensure you use the characterization data derived from test points in the *Characterization Test Points for Verification Procedures* table in the *Characterizing Power Splitter Balance* section.

You must zero the power sensor as described in the *Zeroing the Power Sensor* section prior to starting this procedure.

This procedure references the following tables you created when you characterized the power splitter loss:

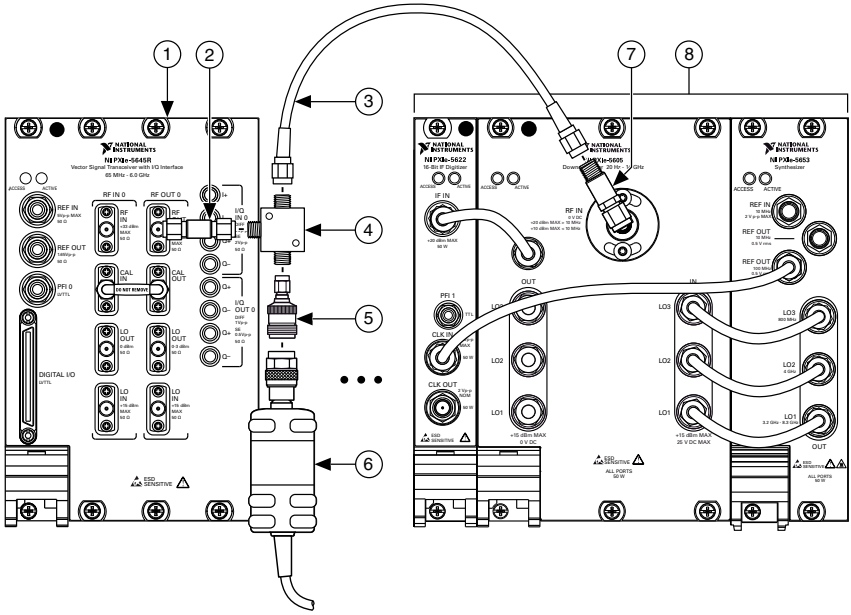
- *Splitter Loss*
- *RF Output Accuracy Transfer Result*

Note If you use the PXIe-5665, as recommended, for the spectrum analyzer, disable the preamplifier and preselector options and set the FFT window type to Flat Top.

1. Connect the PXIe-5645 RF OUT front panel connector to the input terminal of the power splitter using a 3.5 mm (m)-to-3.5 mm (m) adapter.
2. Connect splitter output 1 directly to the power sensor using the SMA (m)-to-N (f) adapter.
3. Connect the remaining power splitter output to one end of the 6 dB attenuator using an SMA (m)-to-SMA (m) cable.
4. Connect the other port of the 6 dB attenuator directly to the spectrum analyzer RF IN front panel connector.

   The following figure illustrates the complete hardware setup.

Figure 20. Output Power Level Accuracy Verification Cabling Diagram



1. PXIe-5645
2. 3.5 mm (m)-to-3.5 mm (m) Adapter
3. SMA (m)-to-SMA (m) Cable
4. Power Splitter
5. SMA (m)-to-N (f) Adapter
6. Power Sensor
7. 6 dB Attenuator
8. Spectrum Analyzer

5. Configure the PXIe-5645 to generate a tone using the following settings:
   - Center frequency: 76.25 MHz
   - Output power: 10 dBm
   - Tone offset: 3.75 MHz
   - I/Q rate: 10 MS/s
6. Configure the spectrum analyzer to acquire a signal at the *center frequency* specified in step 5 using the following settings:
   - Center frequency: (*Center frequency* + *tone offset*) from step 5
   - Reference level: *Configured reference level* from the transfer row in the *RF Output Accuracy Transfer Result* table from the *Characterizing Power Splitter Loss* section that supports the *output power* from step 5.
   - Span: *Span* from the following table
   - Resolution bandwidth: *RBW* from the following table
   - Averaging type: RMS
   - Number of averages: *Number of averages* from the following table

Table 26. Advanced Spectrum Analyzer Settings

Supported Output Power Levels	Span (kHz)	RBW	Number of Averages
x > -70 dBm	250	4 kHz	10
-70 dBm ≥ x > -100 dBm	250	900 Hz	20
x ≤ -100 dBm	250	900 Hz	100

7. Acquire the signal with the spectrum analyzer and measure the tone power located at the value of (*center frequency* + *tone offset*) from step 5. This value is the *measured tone power*.
8. Calculate the *transferred output power* using the following equation:

   transferred output power = *accuracy transfer result* + *measured tone power*

   Note Determine the *accuracy transfer result* by interpolating between the data points in the *RF Output Transfer Result* table you created in step 21 of the *Characterizing Power Splitter Loss* section. Ensure you use the characterization data derived from test points in the *Characterization Test Points for Verification Procedures* table in the *Characterizing Power Splitter Balance* section.
9. Calculate the *corrected output power* using the following equation:

   corrected output power = *transferred output power* + *splitter loss*

   Note Determine the *splitter loss* by interpolating between the data points in the *Splitter Loss* table you created in step 20 of the *Characterizing Power Splitter Loss* section. Ensure you use the characterization data derived from test points in the *Characterization Test Points for Verification Procedures* table in the *Characterizing Power Splitter Balance* section. Choose the appropriate value based on the transfer function used from the *Accuracy Transfer Definitions* table in the *Characterizing Power Splitter Loss* section.
10. Calculate the *absolute power level accuracy* using the following equation:

    absolute power level accuracy = *device output power* - *corrected output power*
    Where *device output power* is the configured output power of the PXIe-5645 RF output path.
11. Repeat steps 5 through 10 for the remaining frequencies listed in the following table.

Table 27. Output Power Level Accuracy Test Points

Start Frequency (MHz)	Stop Frequency (MHz)	Frequency Step Size (MHz)
76.25	101.25	5
125.25	225.25	20
246.25	946.25	50
996.25	5,996.25	200

12. Repeat steps 5 through 11 for the remaining power levels between 10 dBm and -70 dBm in 10 dB steps.

13. Compare the *absolute power level accuracy* values measured to the test limits in the following table.

Table 28. Output Power Level Accuracy Test Limits

Frequency	As-Found Limit (dB)	As-Left Limit (dB)
65 MHz to <109 MHz	±0.70	±0.40
109 MHz to <270 MHz	±0.75	±0.45
270 MHz to <375 MHz	±0.70	±0.40
375 MHz to <2 GHz	±0.75	±0.40
2 GHz to <4 GHz	±0.75	±0.45
4 GHz to 6 GHz	±1.00	±0.55

Note The as-left limits are not listed in the published specifications for the PXIe-5645. These limits are based on published *PXIe-5645 Specifications*, less guard bands for measurement uncertainty, temperature drift, and drift over time.

Verifying Output Frequency Response

This procedure verifies the frequency response of the PXIe-5645 outputs.

This procedure requires the test setup and data collected in the *Characterizing Power Splitter Loss* section. You must characterize the power splitter loss before running this procedure. Ensure you use the characterization data derived from test points in the *Characterization Test Points for Verification Procedures* table in the *Characterizing Power Splitter Balance* section.

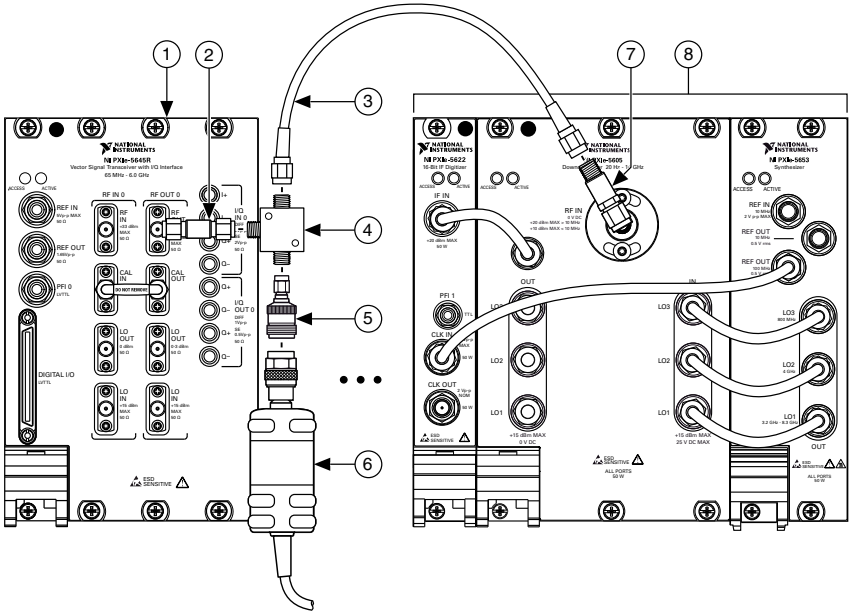
You must zero the power sensor as described in the *Zeroing the Power Sensor* section prior to starting this procedure.

Note If you use the PXIe-5665, as recommended, for the spectrum analyzer, disable the preamplifier and preselector options and set the FFT window type to Flat Top.

1. Connect the PXIe-5645 RF OUT front panel connector to the input terminal of the power splitter using a 3.5 mm (m)-to-3.5 mm (m) adapter.
2. Connect splitter output 1 directly to the power sensor using the SMA (m)-to-N (f) adapter.
3. Connect the remaining power splitter output to one end of the 6 dB attenuator using an SMA (m)-to-SMA (m) cable.
4. Connect the other port of the 6 dB attenuator directly to the spectrum analyzer RF IN front panel connector.

   The following figure illustrates the complete hardware setup.

Figure 21. Output Frequency Response Verification Cabling Diagram



1. PXIe-5645
2. 3.5 mm (m)-to-3.5 mm (m) Adapter
3. SMA (m)-to-SMA (m) Cable
4. Power Splitter
5. SMA (m)-to-N (f) Adapter
6. Power Sensor
7. 6 dB Attenuator
8. Spectrum Analyzer

5. Configure the PXIe-5645 to generate a signal at 300 MHz with a tone at -(*test bandwidth*/2) MHz offset, where *test bandwidth* is the value specified in the following table, using the following settings:
   - Center frequency: 300 MHz
   - Tone offset: -(*test bandwidth*/2) MHz
   - I/Q rate: 120 MS/s
   - Output power: 0 dBm

Table 29. Output Frequency Response Test Points

Test Bandwidth (MHz)	Test Points (MHz)				
20	300				
80	450	550	600	650	800
	950	1,000	1,050	1,200	1,550
	1,600	1,650	2,000	2,650	2,700
	2,750	3,000	3,800	3,950	4,000
	4,050	4,500	4,950	5,000	5,050
	5,500	5,950			

6. Configure the spectrum analyzer to acquire a signal at the tone frequency of step 5, using the following settings:
   - Center frequency: (*Center frequency* + *tone offset*) from step 5, in MHz
   - Reference level: Configured reference level (dBm) from the transfer row in the *Accuracy Transfer Definitions* table in the *Characterizing Power Splitter Loss* section that supports the *output power* from step 5.
   - Span: *Span* from the following table
   - Resolution bandwidth: *RBW* from the following table
   - Averaging type: RMS
   - Number of averages: *Number of averages* from the following table

Table 30. Advanced Spectrum Analyzer Settings

Supported Output Power Levels	Span (kHz)	RBW	Number of Averages
$x >$ -70 dBm	250	4 kHz	10
-70 dBm $\geq x >$ -100 dBm	250	900 Hz	20
$x \leq$ -100 dBm	250	900 Hz	100

7. Acquire the signal with the spectrum analyzer and measure the tone power located at the value of (*center frequency* + *tone offset*) from step 5. This value is the *measured tone power*.
8. Calculate the *transferred output power* using the following equation:

   transferred output power = accuracy transfer result + measured tone power

   Note Find the *accuracy transfer result* by interpolating between the data points in the *RF Output Transfer Result* table you created in step 21 of the*Characterizing Power Splitter Loss* section. Ensure you use the characterization data derived from test points in the *Characterization Test Points for Verification Procedures* table in the *Characterizing Power Splitter Balance* section.
9. Calculate the *corrected output power* using the following equation:

corrected output power = transferred output power + splitter loss

Note Find the *splitter loss* by interpolating between the data points in the *Splitter Loss* table you created in step 20 of the *Characterizing Power Splitter Loss* section. Ensure you use the characterization data derived from test points in the *Characterization Test Points for Verification Procedures* table in the *Characterizing Power Splitter Balance* section. Choose the appropriate value based on the transfer function used from the *Accuracy Transfer Definitions* table in the *Characterizing Power Splitter Loss* section.

10. Calculate the *absolute power level accuracy* using the following equation:

    absolute power level accuracy = device output power - corrected output power
    Where *device output power* is the configured output power of the PXIe-5645 RF output path.
11. Repeat steps 5 through 10 by sweeping the tone offset from -(*test bandwidth*/2) to +(*test bandwidth*/2) in 5 MHz steps, where *test bandwidth* is the value specified in the *Output Frequency Response Test Points* table.
12. Determine the positive and negative frequency response results for the *center frequency* from step 5 by completing the following steps.
    a) positive (+) *frequency response* = maximum *absolute power level accuracy* - median *absolute power level accuracy*
    b) negative (-) *frequency response* = median *absolute power level accuracy* - minimum *absolute power level accuracy*
13. Repeat steps 5 through 12 for the remaining center frequencies listed in the *Output Frequency Response Test Points* table.
14. Repeat steps 5 through 13 for power levels 0 dBm to -30 dBm in 10 dB steps.
15. Compare the ± *frequency response* values measured to the test limits in the following table.

Table 31. Output Frequency Response Test Limits

Frequency	Equalized Bandwidth (MHz)	As-Found Limit (dB)	As-Left Limit (dB)
>109 MHz to 375 MHz	20	±0.5	±0.5
>375 MHz to 6 GHz	80	±0.5	±0.5

Verifying Output Noise Density

This procedure verifies the generated noise density of the PXIe-5645 outputs.

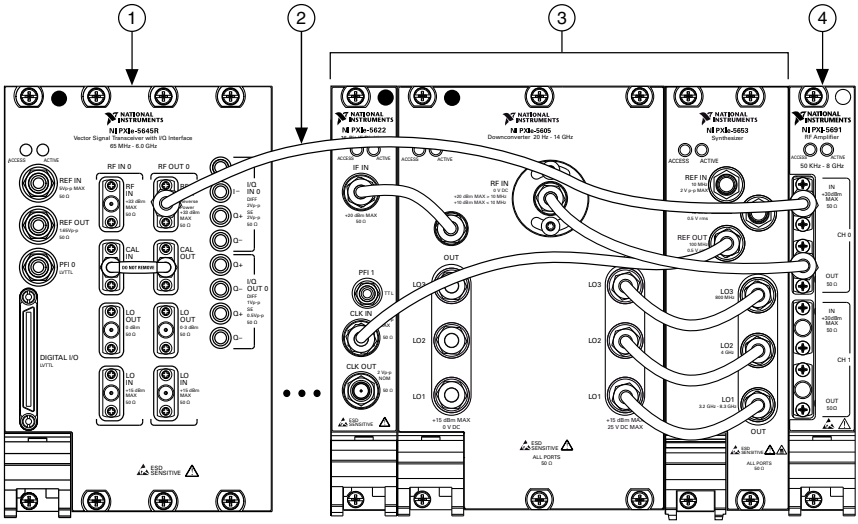
Note This measurement requires a measuring instrument with an average noise density better than -158 dBm/Hz. You may need an external preamplifier if your spectrum analyzer does not have an internal gain mode that can meet this requirement. If you are using an external preamplifier, begin with step 1, otherwise begin with step 3.

1. Connect the PXIe-5645 RF OUT front panel connector to the input connector of the external preamplifier.

2. Connect the preamplifier output to the RF IN front panel connector of the spectrum analyzer.

   The following figure illustrates the hardware setup.

Figure 22. Output Noise Density Verification Cabling Diagram



1. PXIe-5645
2. SMA (m)-to-SMA (m) Cable
3. Spectrum Analyzer
4. Preamplifier

3. Connect an available 10 MHz rubidium frequency reference output to the PXIe-5645 REF IN front panel connector.
4. Connect an available 10 MHz rubidium frequency reference output to the spectrum analyzer REF IN front panel connector.
5. Generate a 1 MHz tone arbitrary waveform using the following settings:
   - Center frequency: 110 MHz
   - I/Q rate: 120 MS/s
   - Tone offset frequency: 1 MHz
   - Tone full scale: -40 dBFS
   - Power level: 10 dBm
   - Reference Clock source: REF IN
6. Measure the output noise floor 4 MHz offset from the generated tone using the spectrum analyzer and the following settings:
   - Center frequency: *Center frequency* from step 5 + 5 MHz
   - Reference level: -10 dBm
   - Frequency span: 1 MHz
   - Number of averages: 200
   - Reference Clock source: External

- Attenuation: 0 dB
- Resolution bandwidth: 500 Hz

7. Convert the sorted spectrum magnitude values from decibel milliwatts (dBm) to watts (W), calculate the mean, and convert the result to decibel milliwatts. This value is the *average noise*. Convert *average noise* to *average noise density* by normalizing to 1 Hz using the following equation:

   average noise density = *average noise* - 10 * log (*resolution bandwidth* from step 6)

   Record the result.
8. Repeat steps 5 through 7 for the remaining RF frequencies between 110 MHz and 6 GHz in 589 MHz steps.
9. Repeat steps 5 through 8 for the 0 dBm output power level for frequencies between 510 MHz and 6 GHz in 589 MHz steps.
10. Compare the results of this procedure to the specified limits in the following tables.

Table 32. Output Noise Density Test Limits (10 dBm Power Level)

Frequency	As-Found Limit (dBm/Hz)	As-Left Limit (dBm/Hz)
65 MHz to 500 MHz	-136	-136
>500 MHz to 2.5 GHz	-141	-141
>2.5 GHz to 3.5 GHz	-139	-139
>3.5 GHz to 6 GHz	-136	-136

Table 33. Output Noise Density Test Limits (0 dBm Power Level)

Frequency	As-Found Limit (dBm/Hz)	As-Left Limit (dBm/Hz)
>500 MHz to 2.5 GHz	-150	-150
>2.5 GHz to 3.5 GHz	-149	-149
>3.5 GHz to 6 GHz	-147	-147

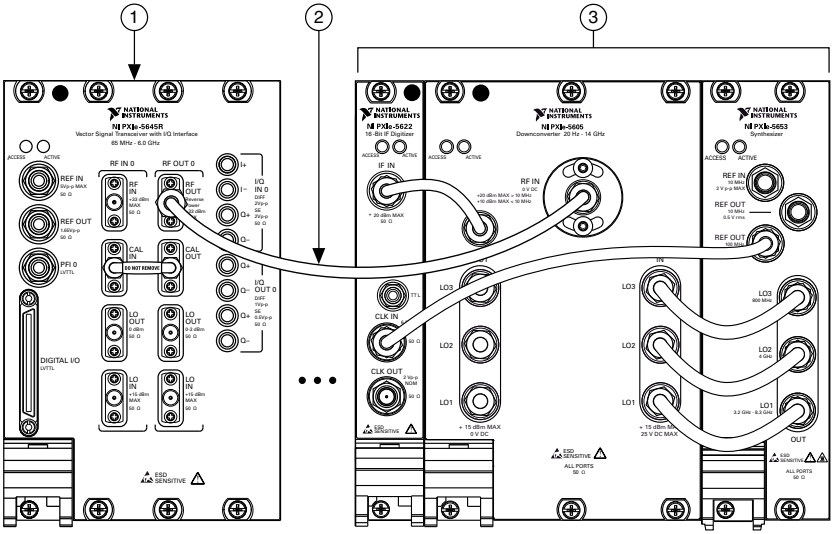
Verifying Output Second Harmonics

This procedure verifies the generated harmonics of the PXIe-5645 outputs.

1. Connect the PXIe-5645 RF OUT front panel connector to the spectrum analyzer RF IN front panel connector.

   The following figure illustrates the hardware setup.

Figure 23. Output Second Harmonics Verification Cabling Diagram



1. PXIe-5645
2. SMA (m)-to-SMA (m) Cable
3. Spectrum Analyzer

2. Connect an available 10 MHz rubidium frequency reference output to the PXIe-5645 REF IN front panel connector.
3. Connect an available 10 MHz rubidium frequency reference output to the spectrum analyzer REF IN front panel connector.
4. Configure the PXIe-5645 to generate a signal using the following settings:
   - Frequency: 100 MHz
   - Power level: 7 dBm
   - I/Q rate: 10 MS/s
   - Tone offset: 1 MHz
   - Tone digital gain: -1 dBFS
   - Reference Clock source: REF IN
   - Reference Clock frequency: 10 MHz
5. Use the spectrum analyzer to measure the fundamental tone power using the following settings:
   - Center frequency: (*frequency* + *tone offset*) from step 4
   - Reference level: +20 dBm
   - Frequency span: 100 kHz
   - Resolution bandwidth: 1 kHz
   - Reference Clock source: REF IN
   - Reference Clock frequency: 10 MHz

6. Use the spectrum analyzer to measure the second harmonic power level using the following settings:
   - Center frequency: 2 * *center frequency* from step 5
   - Reference level: 0 dBm
   - Frequency span: 100 kHz
   - Resolution bandwidth: 1 kHz
   - Reference Clock source: REF IN
   - Reference Clock frequency: 10 MHz
7. Calculate the distortion level in dBc by subtracting the fundamental power from the second harmonic power.
8. Repeat steps 4 through 7 for the remaining frequencies from 100 MHz to 6 GHz in 590 MHz steps.
9. Compare the values calculated in step 7 and 8 to the corresponding limits in the following table.

Table 34. Second Harmonics Test Limits

Frequency	As-Found Limit (dBc)	As-Left Limit (dBc)
65 MHz to 3.5 GHz	-27	-27
>3.5 GHz to 4.5 GHz	-26.3	-26.3
>4.5 GHz to 6 GHz	-28.9	-28.9

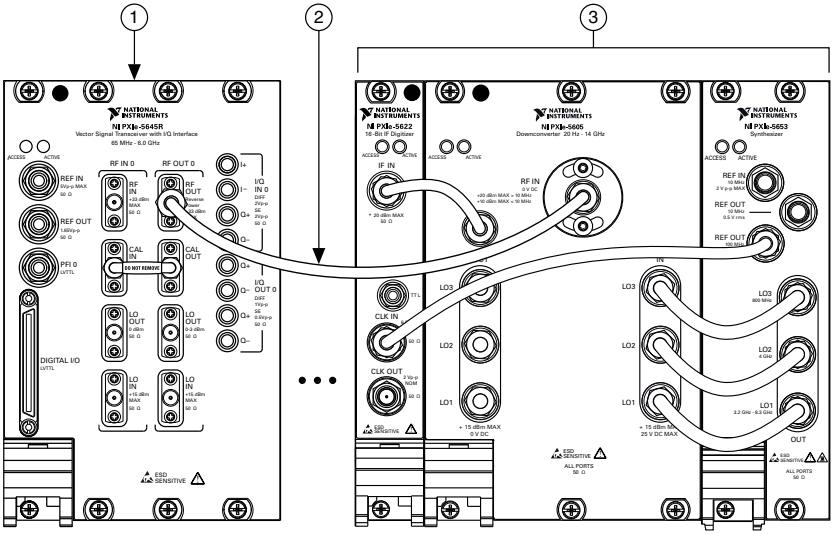
Verifying Output Nonharmonic Spurs

This procedure verifies the nonharmonic spurs generated by the PXIe-5645 RF output.

1. Connect the PXIe-5645 RF OUT front panel connector to the RF IN connector of the spectrum analyzer.

   The following figure illustrates the hardware setup.

Figure 24. Output Nonharmonic Spurs Verification Cabling Diagram



1. PXIe-5645
2. SMA (m)-to-SMA (m) Cable
3. Spectrum Analyzer

2. Connect an available 10 MHz rubidium frequency reference output to the PXIe-5645 REF IN front panel connector.
3. Connect an available 10 MHz rubidium frequency reference output to the spectrum analyzer REF IN front panel connector.
4. Configure the PXIe-5645 to generate a CW tone using the following settings:
   - Center frequency: 144.2 MHz
   - Power level: 0 dBm
   - I/Q rate: 10 MS/s
   - Digital gain: -1 dB
   - Reference Clock source: REF IN
   - Reference Clock frequency: 10 MHz
5. Configure the spectrum analyzer to acquire a spectrum using the following settings:
   - Center frequency: *Center frequency* from step 4
   - Reference level: 0 dBm
   - Span: 80 MHz
   - Resolution bandwidth: 1 kHz
   - Averaging type: RMS
   - Number of averages: 20
   - Reference Clock source: REF IN
   - Reference Clock frequency: 10 MHz

6. Measure the peak power within 100 kHz to 1 MHz offset of the tone on either side of the carrier frequency from the data acquired in step 5.

   Record the maximum value for comparison to the >100 kHz offset limits.

7. Measure the peak power at >1 MHz offset of the tone on either side of the carrier frequency from the data acquired in step 5. Record the maximum value.

   Record the maximum value for comparison to the >1,000 kHz offset limits.

8. Repeat steps 4 through 7 for the remaining test points listed in the following table.

Table 35. Output Nonharmonics Test Points

Frequency (MHz)				
144.2	264.2	504.2	1,008.2	2,016.2
2,520.2	3,024.2	4,008.2	5,016.2	

9. Compare the results from steps 6 through 8 to the test limits in the following table.

Table 36. Output Nonharmonics Test Limits

Frequency	Offset (kHz)	As-Found Limit (dBc)	As-Left Limit (dBc)
65 MHz to 3 GHz	>100	-62	-62
	>1,000	-75	-75
>4 GHz to 6 GHz	>100	-57	-57
	>1,000	-70	-70

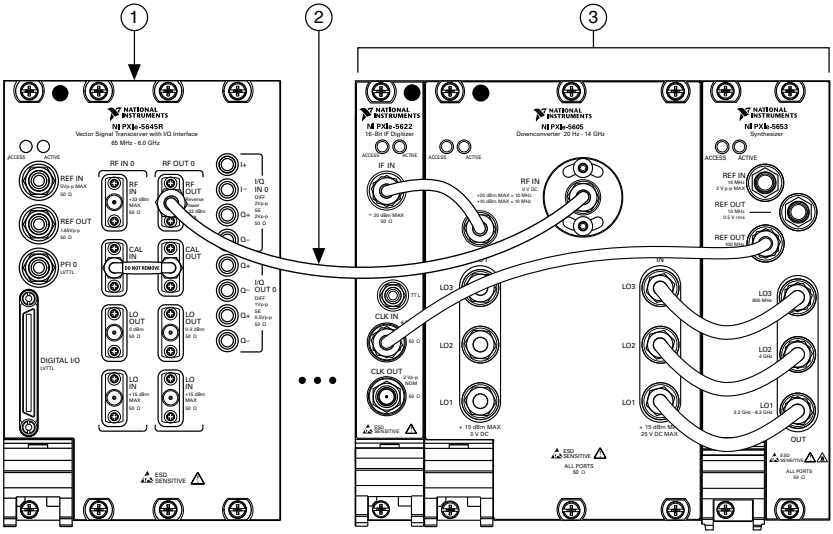
Verifying Third-Order Output Intermodulation (IMD3)

This procedure verifies the nonlinear performance of the output channel at several output levels.

1. Connect the PXIe-5645 RF OUT front panel connector to the spectrum analyzer RF IN front panel connector.

   The following figure illustrates the hardware setup.

Figure 25. Output IMD3 Verification Cabling Diagram



1. PXIe-5645
2. SMA (m)-to-SMA (m) Cable
3. Spectrum Analyzer

2. Connect an available 10 MHz rubidium frequency reference output to the PXIe-5645 REF IN front panel connector.
3. Connect an available 10 MHz rubidium frequency reference output to the spectrum analyzer REF IN front panel connector.
4. Configure the PXIe-5645 to generate two single sideband tones simultaneously at 2 MHz (f_1) and 2.5 MHz (f_2) offset from the carrier, using the following settings:
   - Center frequency: 100 MHz
   - Power level (dBm): 0 dBm
   - I/Q rate: 10 MS/s
   - Reference Clock source: REF IN
   - Relative tone power (dB): -6 dB
5. Use the spectrum analyzer to measure the generated signal using the following settings:
   - Center frequency: (*Center frequency* + (f_1+ f_2)/2) from step 4
   - Reference level: *Power level* from step 4 + 10 dB
   - Span: 5 MHz
   - Resolution bandwidth: 100 Hz
   - Averaging type: RMS
   - Number of averages: 10

6. Measure and record the peak power of the following tones and distortion locations:
   - Center frequency + f_1, record as *fundamental tone*$_1$
   - Center frequency + f_2, record as *fundamental tone*$_2$
   - Center frequency + $2f_2$ - f_1, record as *IMD tone*$_1$
   - Center frequency + $2f_1$ - f_2, record as *IMD tone*$_2$
7. Calculate the output IMD using the following equation:

   output IMD = maximum *(IMD tone)* - minimum *(fundamental tone)*
8. Repeat steps 4 through 7 for the remaining frequencies from 100 MHz to 6 GHz in 590 MHz steps.
9. Repeat steps 4 through 8 for the tone output power level -36 dBm.
10. Compare the output IMD values calculated in steps 7 through 9 to the corresponding limits in the following tables.

Table 37. IMD3 (dBc) -6 dBm Tones

Frequency	As-Found Limit (dBc)	As-Left Limit (dBc)
65 MHz to 1.5 GHz	-50	-50
>1.5 GHz to 3.5 GHz	-54	-54
>3.5 GHz to 5 GHz	-50	-50
>5 GHz to 6 GHz	-47	-47

Table 38. IMD3 (dBc) -36 dBm Tones

Frequency	As-Found Limit (dBc)	As-Left Limit (dBc)
65 MHz to 200 MHz	-52	-52
>200 MHz to 6 GHz	-52	-52

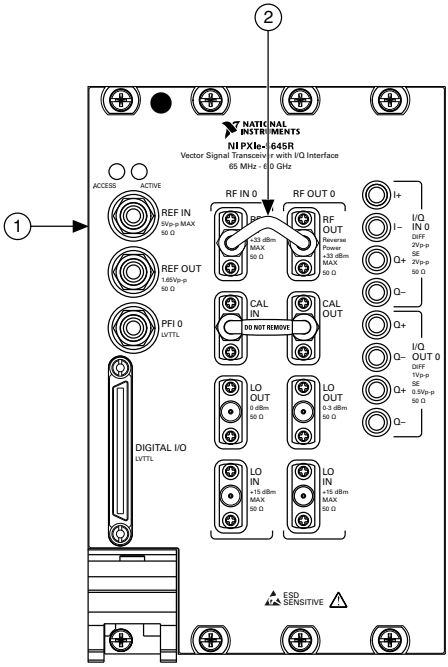
Verifying Residual LO Power and Residual Sideband Image

This procedure verifies the residual LO power and residual sideband image suppression of the PXIe-5645.

1. Connect the PXIe-5645 RF IN front panel connector to the PXIe-5645 RF OUT front panel connector.

   The following figure illustrates the complete hardware setup.

Figure 26. Residual LO Power and Residual Sideband Image Verification Cabling Diagram



1. PXIe-5645
2. SMA (m)-to-SMA (m) Cable

2. Configure the PXIe-5645 to acquire a spectrum at 80 MHz using the following settings:
   - Center frequency: 80 MHz
   - Reference level: 0 dBm
   - Span: 20 MHz
   - Resolution bandwidth: 1 kHz
   - Averaging type: RMS
   - Number of averages: 10
   - Window type: Flat Top
3. Configure the PXIe-5645 to generate a single sideband tone at an offset from the center frequency listed in step 2 using the following settings:
   - Center frequency: 80 MHz + *LO offset*
   - LO offset: 200 kHz
   - Power level: *Reference level* from step 2 or 0 dBm, whichever is less.
   - I/Q rate: 120 MS/s
   - Tone offset: -(*span* from step 2)/2
4. Acquire the signal using the PXIe-5645.

5. Measure the following tones:
   - Generated tone power. Record as *fundamental tone*.
   - *Center frequency* from step 2. Record as *RF input residual LO*.
   - *Center frequency* from step 3. Record as *RF output residual LO*.
   - Image of tone relative to *center frequency* from step 2. Record as *RF input image*.
   - Image of tone relative to *center frequency* from step 3. Record as *RF output image*.
6. Repeat steps 2 through 5 for the remaining tone offsets from -*span*/2 to +*span*/2 in 5 MHz steps, where *span* is the value listed in the following table.

Table 39. Measurement Span Over Center Frequency

Frequency	Measurement Span
≤109 MHz	20 MHz
>109 MHz to 375 MHz	40 MHz
>375 MHz to <6 GHz	80 MHz

Note Skip the case where the tone offset is equal to zero.

7. Calculate the *RF input residual sideband image supression* using the following equation:

   RF input residual sideband image = maximum *(RF input image) - fundamental tone*
8. Calculate the *RF output residual sideband image supression* using the following equation:

   RF output residual sideband image = maximum *(RF output image) - fundamental tone*
9. Calculate the *RF input residual LO power* using the following equation:

   RF input residual LO power = maximum *(RF input residual LO) - reference level* from step 2.
10. Calculate the *RF output residual LO power* using the following equation:

    RF output residual LO power = maximum *(RF output residual LO) - reference level* from step 2
11. Repeat steps 2 through 10 for the remaining center frequencies from 80 MHz to 6 GHz in 296 MHz steps.
12. Repeat steps 2 through 11 for the remaining reference levels from 0 dBm to -30 dBm in 10 dB steps.
13. Compare the results from this procedure to the limits listed in the following tables.

Table 40. Residual LO Power Test Limits

Frequency	RF Input		RF Output	
	As-Found Limit (dBc)	As-Left Limit (dBc)	As-Found Limit (dBc)	As-Left Limit (dBc)
≤109 MHz	-62	-67	-50	-55
>109 MHz to 375 MHz	-58	-61	-45	-50
>375 MHz to 2 GHz	-58	-61	-55	-60
>2 GHz to 3 GHz	-55	-58	-50	-53
>3 GHz to 5 GHz	-45	-48	-55	-58
>5 GHz to 6 GHz	-45	-48	-50	-55

Note The as-left limits are not listed in the published specifications for the PXIe-5645. As-left limits are based on the published *PXIe-5645 Specifications*, less guard bands for measurement uncertainty, temperature drift, and drift over time.

Table 41. Residual Sideband Image Test Limits

Frequency	RF Input		RF Output	
	As-Found Limit (dBc)	As-Left Limit (dBc)	As-Found Limit (dBc)	As-Left Limit (dBc)
≤109 MHz	-40	-50	-40	-45
>109 MHz to 375 MHz	-40	-45	—	—
>375 MHz to 500 MHz	-40	-45	-60	-65
>500 MHz to 2 GHz	-65	-70	-60	-65
>2 GHz to 3 GHz	-65	-70	-50	-55
>3 GHz to 4 GHz	-55	-60	-50	-55
>4 GHz to 5 GHz	-55	-60	-40	-50
>5 GHz to 6 GHz	-60	-65	-40	-50

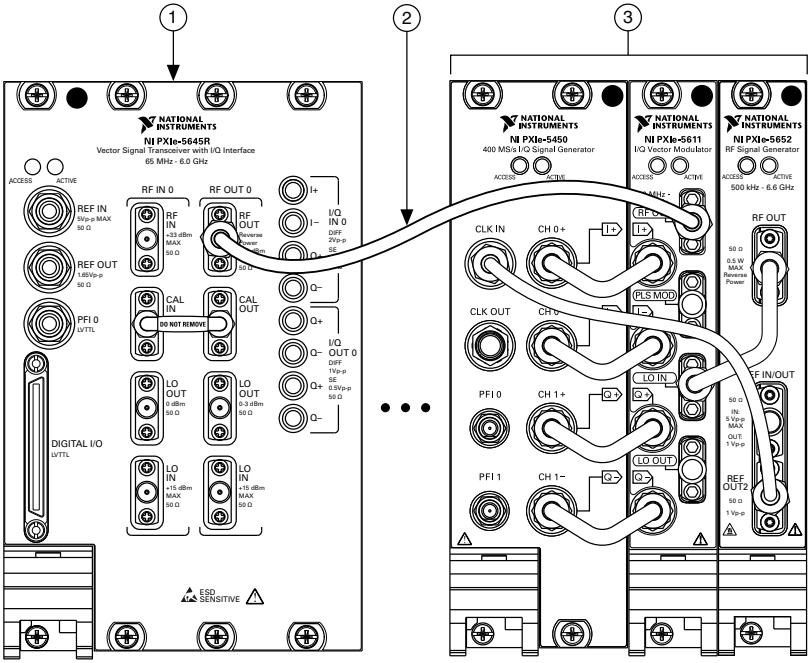
Verifying RF Input EVM (Functional Test)

This procedure verifies the demodulation performance of the PXIe-5645.

1. Connect the PXIe-5645 RF IN front panel connector to the RF OUT front panel connector of the vector signal generator using an SMA (m)-to-SMA (m) cable.

   The following figure illustrates the complete hardware setup.

Figure 27. RF Input EVM Verification Cabling Diagram



1. PXIe-5645
2. SMA (m)-to-SMA (m) Cable
3. Vector Signal Generator

2. Configure the PXIe-5645 to acquire a complex modulated signal at 400 MHz using the following settings:
   - Center frequency: 400 MHz
   - Reference level: -10 dBm
   - I/Q rate: 120 MS/s
   - Record length: 300 µs
3. Configure the vector signal generator to generate a complex modulated signal at the *center frequency* specified in step 2 using the following settings:
   - Power level: -10 dBm
   - I/Q rate: 120 MS/s
4. Configure the modulated waveform signal with the Modulation Toolkit using the following settings:
   - QAM: 64
   - Symbol rate: 16 MSymbols/s
   - Samples per symbol: 4
   - Pulse shape filtering: Root-raised-cosine, 0.25 alpha
   - PN sequence order: 14

5. Download the waveform from step 4 to the vector signal generator and generate the modulated signal.
6. Acquire the signal with the PXIe-5645 and demodulate it with the Modulation Toolkit using the settings from step 4.
7. Measure and record the RMS EVM in dB.
8. Repeat steps 2 through 7 for frequencies from 400 MHz to 6 GHz in 200 MHz steps.
9. Compare the results from this procedure to the specified limits:
   - As-found: -40 dB
   - As-left: -40 dB

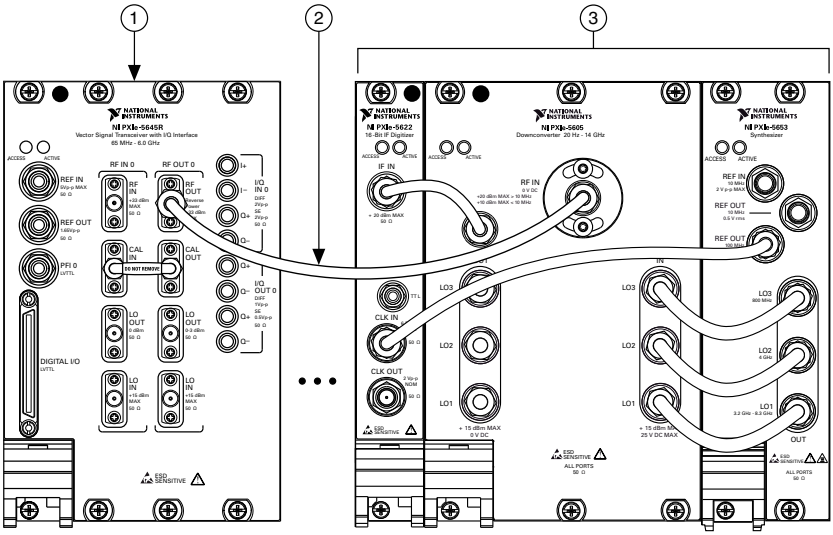
Verifying RF Output EVM (Functional Test)

This procedure verifies the modulation performance of the PXIe-5645.

1. Connect the RF OUT front panel connector of the PXIe-5645 to the RF IN front panel connector of the vector signal analyzer.

   The following figure illustrates the complete hardware setup.

Figure 28. RF Output EVM Verification Cabling Diagram



1. PXIe-5645
2. SMA (m)-to-SMA (m) Cable
3. Spectrum Analyzer

2. Configure the vector signal analyzer to acquire a complex modulated signal at 400 MHz using the following settings:
   - Center frequency: 400 MHz
   - Reference level: -10 dBm

- I/Q rate: 50 MS/s
- Record length: 300 µs

3. Configure the PXIe-5645 to generate a complex modulated signal at the *center frequency* specified in step 2 using the following settings:
   - Power level: -10 dBm
   - I/Q rate: 120 MS/s
4. Configure the modulated waveform signal with the Modulation Toolkit using the following settings:
   - QAM: 64
   - Symbol rate: 16 MSymbols/s
   - Samples per symbol: 4
   - Pulse shape filtering: Root raise cosine, 0.25 alpha
   - PN sequence order: 14
5. Download the waveform from step 4 to the PXIe-5645 and generate the modulated signal.
6. Acquire the signal with the vector signal analyzer and demodulate it with the Modulation Toolkit using the settings from step 4.
7. Measure and record the RMS EVM in dB.
8. Repeat steps 2 through 7 for frequencies from 400 MHz to 6 GHz in 200 MHz steps.
9. Compare the results from this procedure to the specified limits:
   - As-found: -40 dB
   - As-left: -40 dB

Verifying LO OUT (RF IN 0 and RF OUT 0) (Functional Test)

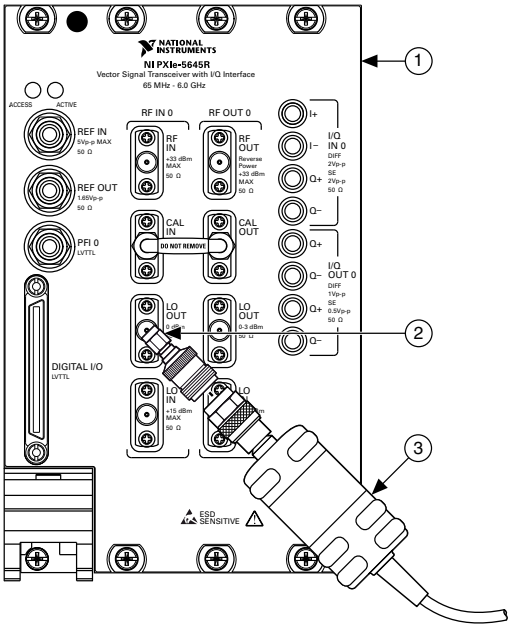
This procedure verifies the power level of the local oscillator (LO) for the input and output channels of the PXIe-5645.

You must zero the power sensor as described in the *Zeroing the Power Sensor* section prior to starting this procedure.

1. Connect the PXIe-5645 LO OUT (RF IN 0) front panel connector to the power sensor using the SMA (m)-to-N (f) adapter.

   The following figure illustrates the complete hardware setup.

Figure 29. LO OUT (RF IN 0) Verification Cabling Diagram



1. PXIe-5645
2. SMA (m)-to-N (f) Adapter
3. Power Sensor

2. Configure the PXIe-5645 RF IN channel to export the local oscillator, using the following settings:
   - Center frequency: 100 MHz
   - LO OUT enabled: Enabled
3. Configure the power sensor to correct for the *center frequency* from step 2 using the power sensor frequency correction function.
4. Use the power sensor to measure the signal power at the LO OUT (RF IN 0) connector.
5. Compare the measured LO OUT (RF IN 0) output power to the limits listed in the following table.

Table 42. LO OUT Power Test Limits

Frequency	LO OUT Power		As-Found Limit (dB)	As-Left Limit (dB)
	LO OUT (RF IN 0) (dBm)	LO OUT (RF OUT 0) (dBm)		
65 MHz to <3.6 GHz	0	0	± 2.0	± 2.0
≥3.6 GHz to 6 GHz[4]	0	3.0	± 2.0	± 2.0
The limits in this table are *typical* values. Typical values describe useful product performance beyond specifications that are not covered by warranty and do not include guardbands for measurement uncertainty or drift.				

6. Repeat steps 2 through 5 for the remaining frequencies between 100 MHz and 1 GHz, in 100 MHz steps.
7. Repeat steps 2 through 5 for the remaining frequencies between 1.5 GHz and 6 GHz, in 500 MHz steps.
8. Move the power sensor from the LO OUT (RF IN 0) connector to the LO OUT (RF OUT 0) connector, then repeat steps 1 through 7 for the LO OUT (RF OUT 0) connector.

I/Q Verification

The performance verification procedures assume that adequate traceable quantities are available for the calibration references.

Before performing any I/Q verifications, characterize the I/Q calibration fixture designated for verifications once, as described in the *I/Q Test System Characterization* section.

Verifying I/Q Input DC Gain Error

This procedure verifies the I/Q input absolute gain error of the PXIe-5645 for differential input.

Characterize the I/Q calibration fixture designated for verifications once prior to performing any verifications.

1. Connect the PXIe-5645, calibration fixture, and calibration standards as shown in the *I/Q Test Equipment* topic.
2. Configure the calibration fixture using the following settings:
   - Signal path: Inline
   - DMM path: I In
   - Terminal configuration: Differential

[4] The expected output power of the LO OUT (RF OUT 0) is 3 dBm at frequencies ≥ 3.6 GHz

3. Configure the DMM using the following settings:
   - Function: DC Volts
   - Resolution: 6 1/2 digits
   - Auto range: Enabled
   - Aperture time: 1 PLC
   - Auto zero: On
   - Number of averages: 48
4. Configure the PXIe-5645 output using the following settings:
   - Terminal configuration: Differential
   - Voltage: 2 $V_{pk\text{-}pk}$
   - Offset: 0 V
   - Common mode offset: 0 V
   - Load impedance: I/Q calibration fixture I Out impedance
   - Waveform: DC tone with amplitude of 0.99
5. Configure the PXIe-5645 input to acquire a signal using the following settings:
   - Terminal configuration: Differential
   - Level: 2 $V_{pk\text{-}pk}$
   - I/Q rate: 120 Ms/s
   - Acquisition size: 1.5E+6 samples
6. Generate a +1 V DC signal on the I channel.
7. Measure the I/Q Out DC voltage using the DMM and correct this value using the following equation.

$$PosVoltage = step7Measurement * \left(\frac{ImpedanceIIn - (CableImpedance + RelayImpedance)}{ImpedanceIIn}\right)$$

   Store this value as the *Pos Voltage*.
8. Measure the I/Q output DC voltage using the PXIe-5645 I/Q input.

   Store this value as *Acquired Pos Voltage*.
9. Generate a -1 V DC signal on the I channel.
10. Measure the I/Q output DC voltage using the DMM and correct this value using the following equation.

$$NegVoltage = step10Measurement * \left(\frac{ImpedanceIIn - (CableImpedance + RelayImpedance)}{ImpedanceIIn}\right)$$

    Store this value as *Neg Voltage*.
11. Measure the I/Q output DC voltage using the PXIe-5645 I/Q input.

    Store this value as *Acquired Neg Voltage*.

12. Calculate the DC gain error using the following equation:

$$GainAccuracy(\%) = 100 * \frac{(Acquired\ PosVoltage - Acquired\ NegVoltage) - (PosVoltage - NegVoltage)}{(PosVoltage - NegVoltage)}$$

Compare the results to the following limits:

- As-found: ±1.75 %
- As-left: ±1.75 %

13. Repeat steps 4 through 12 for the remaining I/Q input voltage levels from 2 V_{pk-pk} to 0.5 V_{pk-pk} in 250 mV steps. In step 4, set the I/Q output voltage to match the I/Q input level being verified.
14. Repeat steps 2 through 13 for the Q channel by configuring the DMM path of the calibration fixture to Q In.

Verifying I/Q Input DC Offset Error

This procedure verifies the I/Q input DC offset error of the PXIe-5645 for differential input.

Characterize the calibration fixture once prior to performing any verifications.

1. Connect the PXIe-5645, calibration fixture, and calibration standards as shown in the *I/Q Test Equipment* topic.
2. Configure the calibration fixture using the following settings:
   - Signal path: Terminated
   - DMM path: I In
   - Terminal configuration: Differential
3. Configure the DMM using the following settings:
   - Function: DC Volts
   - Resolution: 6 1/2 digits
   - Auto range: Enabled
   - Aperture time: 1 PLC
   - Auto zero: On
   - Number of averages: 48
4. Configure the PXIe-5645 output using the following settings:
   - Terminal configuration: Differential
   - Voltage: 0.1 V_{pk-pk}
   - Offset: 0 V
   - Common mode offset: 2 V
   - Load impedance: I/Q calibration fixture I Out impedance
   - Waveform: 0.99 amplitude DC tone
5. Configure the PXIe-5645 input to acquire using the following settings:
   - Terminal configuration: Differential
   - Level: 2 V_{pk-pk}

- I/Q rate: 120 Ms/s
- Acquisition size: 1.5E+6 samples

6. Measure the I/Q output DC voltage using the DMM. Store this value as *Offset.*
7. Measure the I/Q output DC voltage using the PXIe-5645 I/Q Input. Store this value as *Acquired Offset.*
8. Calculate the DC offset error using the following equation.

   Offset Error (V) = Acquired Offset - Offset

   Compare the resulting offset error to the following limits:
   - As-found: ±15 mV
   - As-left: ±15 mV
9. Repeat steps 4 through 8 for the remaining I/Q voltage levels from 2 V_{pk-pk} to 0.5 V_{pk-pk} in 250 mV steps.
10. Repeat steps 4 through 8 for the remaining I/Q output common mode voltages: 2 V, 0 V, -2 V.
11. Repeat steps 2 through 10 for the Q channel by configuring the DMM path of the calibration fixture to Q In.

Verifying I/Q Input AC Gain Accuracy and Passband Flatness

This procedure verifies the I/Q input AC gain accuracy and passband flatness of the PXIe-5645 for differential input.

Characterize the calibration fixture once prior to performing any verifications.

This procedure verifies absolute AC gain accuracy and passband flatness only for the I channel. By design, the Q channel is matched to the I channel to a level specified by the channel-to-channel gain imbalance.

1. Connect the PXIe-5645, calibration fixture, and calibration standards as shown in the *I/Q Test Equipment* topic.
2. Configure the calibration fixture using the following settings:
   - Signal path: Splitter I
   - DMM path: None
   - Terminal configuration: Differential
3. Configure the PXIe-5645 using the following settings:
   - Terminal configuration: Differential
   - Voltage: 1 V_{pk-pk}
   - Offset: 0 V
   - Common mode offset: 0 V
   - Load impedance: I/Q calibration fixture I Out impedance
4. Configure the PXIe-5645 I/Q input to acquire a signal using the following settings:
   - Terminal configuration: Differential
   - Voltage range: 1 V_{pk-pk}

- I/Q rate: 120 Ms/s
- Acquisition size: 1.5E+5 samples

5. Generate a 500 kHz signal with an amplitude of -1 dBFS.
6. Configure the power sensor to correct for the frequency specified in step 5.
7. Measure the signal power with power meter 1 at PM+ and correct the result using the following equation.

   Absolute Level = step 7 Measurement + Gain PM + Absolute Cal Gain at 500 kHz

   Store this value as the *Absolute Level*.
8. Measure the signal power with the PXIe-5645 I/Q input. Store this value as *Acquired Absolute Level*.
9. Generate a 1 MHz signal with an amplitude of -1 dBFS.
10. Configure the power sensor to correct for the frequency specified in step 7.
11. Measure the signal power with the power meter and correct this value using the following equation.

    Relative Response (f) = step 11 Measurement + Gain PM + Absolute Cal Gain at *f*

    where *f* is the frequency specified in step 9

    Record the result as *Relative Response* versus frequency.
12. Measure the signal power with the PXIe-5645 I/Q input.

    Record the result as *Acquired Relative Response* .
13. Repeat steps 9 though 12 for the following test frequencies:

Table 43. Input AC Gain Accuracy and Passband Flatness Test Points

Frequency (MHz)				
1	5	10	15	20
25	30	35	40	

14. Compare the *Absolute Level* from step 7 to the specified signal level using the following equation.

    AC Gain Accuracy (dB) = Acquired Absolute Level - Absolute Level

    Compare the *AC Gain Accuracy* to the limits in the *Input AC Gain Accuracy and Passband Flatness Test Limits* table.
15. Compare the PXIe-5645 input measurement to the external standard using the following equation.

    Passband Flatness at f (dB) = Acquired Relative Response - Relative Response

    Compare the *Passband Flatness* to the limits in the *Input AC Gain Accuracy and Passband Flatness Test Limits* table.
16. Repeat steps 3 through 15 for the remaining I/Q input voltage levels: 1 V_{pk-pk}, 0.5 V_{pk-pk}, 0.1 V_{pk-pk}. Set the I/Q output voltage level in step 3 to the same value as the I/Q input voltage level.

Table 44. Input AC Gain Accuracy and Passband Flatness Test Limits

Specification	As-Found Limit (dB)	As-Left Limit (dB)
Absolute AC Gain Accuracy at 1.0 V_{pk-pk}	0.42	0.42
Absolute AC Gain Accuracy at 0.5 V_{pk-pk}	0.41	0.41
Absolute AC Gain Accuracy at 0.1 V_{pk-pk}	0.52	0.52
20 MHz Passband Flatness	0.43	0.43
40 MHz Passband Flatness	0.52	0.52

Verifying I/Q Output DC Gain Error

This procedure verifies the I/Q output absolute gain error of the PXIe-5645 for differential output.

Characterize the calibration fixture once prior to performing any verifications.

1. Connect the PXIe-5645, calibration fixture, and calibration standards as shown in the *I/Q Test Equipment* topic.
2. Configure the calibration fixture using the following settings:
   - Signal path: No connection
   - DMM path: I Out
   - Terminal configuration: Differential
3. Configure the DMM using the following settings:
   - Function: DC Volts
   - Resolution: 6 1/2 digits
   - Auto range: Enabled
   - Aperture time: 1 PLC
   - Auto zero: On
   - Number of averages: 48
4. Configure the PXIe-5645 using the following settings:
   - Terminal configuration: Differential
   - Voltage: 2 V_{pk-pk}
   - Offset: 0 V
   - Common mode offset: 0 V
   - Load impedance: I/Q calibration fixture I Out impedance
   - Waveform: 0.99 amplitude DC tone
5. Generate a +1 V DC signal on the I channel.
6. Measure the I/Q output DC voltage using the DMM. Store this value as the *Positive Voltage*.
7. Generate a -1 V DC signal on I channel.
8. Measure the I/Q output DC voltage using the DMM. Store this value as the *Negative Voltage*.

9. Calculate the DC gain error using the following equation:

$$Gain\ Accuracy(\%) = 100 * \frac{step4Voltage - (PositiveVoltage - NegativeVoltage)}{(PositiveVoltage - NegativeVoltage)}$$

10. Repeat steps 4 through 9 for the remaining I/Q output voltage levels from 2 V_{pk-pk} to 0.25 V_{pk-pk} in 250 mV steps.
11. Repeat steps 2 through 10 for the Q channel by configuring the DMM path of the calibration fixture to Q Out.

Table 45. Output DC Gain Error Test Settings

PXIe-5645 Settings			Calibration Fixture Settings		
Port	**Terminal Configuration**	**Load Impedance**	**Signal Path**	**DMM Path**	**Terminal Configuration**
I	Differential	High impedance	No connection	I Out	Differential
Q	Differential	High impedance	No connection	Q Out	DIfferential

12. Compare the results from this procedure to the following limits:
    - As-found: ±1.12 %
    - As-left: ±1.12 %

Verifying I/Q Output DC Offset Error

This procedure verifies the I/Q output DC offset error of the PXIe-5645 configured for differential output.

Characterize the calibration fixture once prior to performing any verifications.

1. Connect the PXIe-5645, calibration fixture, and calibration standards as shown in the *I/Q Test Equipment* topic.
2. Configure the calibration fixture using the following settings:
    - Signal path: No connection
    - DMM path: I Out
    - Terminal configuration: Differential
3. Configure the DMM using the following settings:
    - Function: DC Volts
    - Resolution: 6 1/2 digits
    - Auto range: Enabled
    - Aperture time: 1 PLC
    - Auto zero: On
    - Number of averages: 48
4. Configure the PXIe-5645 using the following settings:
    - Terminal configuration: Differential
    - Voltage: 2 V_{pk-pk}
    - Offset: 0 V

- Common mode offset: 2 V
- Load impedance: I/Q calibration fixture I Out impedance

5. Generate a 0 V DC signal on the I channel.
6. Measure the I/Q output DC voltage using the DMM. Store this value as the *Positive Voltage*.
7. Repeat steps 4 through 6 for the remaining common mode offset from 2 V to - 2 V in 1 V steps.
8. Repeat steps 4 through 7 for the remaining I/Q output voltage levels from 2 V_{pk-pk} to 0.25 V_{pk-pk} in 250 mV steps.
9. Repeat steps 2 through 8 for the Q channel by configuring the DMM path of the calibration fixture to Q Out.

Table 46. Output DC Offset Error Test Settings

PXIe-5645 Settings			Calibration Fixture Settings		
Port	**Terminal Configuration**	**Load Impedance**	**Signal Path**	**DMM Path**	**Terminal Configuration**
I	Differential	High impedance	Disconnected	I Out	Differential
Q	Differential	High impedance	Disconnected	Q Out	Differential

10. Compare the results from this procedure to the following limits:
    - As-found: ±3.6 mV
    - As-left: ±3.6 mV

Verifying I/Q Output AC Gain Accuracy and Passband Flatness

This procedure verifies the I/Q output absolute AC gain accuracy and passband flatness of the PXIe-5645 for differential output.

Characterize the calibration fixture once prior to performing any verifications.

This procedure verifies absolute AC gain accuracy and passband flatness only for the I channel. By design, the Q channel is matched to the I channel to a level specified by the channel-to-channel gain imbalance.

1. Connect the PXIe-5645, calibration fixture, and calibration standards as shown in the *I/Q Test Equipment* topic.
2. Configure the calibration fixture using the following settings:
    - Signal path: Absolute I
    - DMM path: None
    - Terminal configuration: Differential
3. Configure the PXIe-5645 using the following settings:
    - Terminal configuration: Differential
    - Voltage: 1 V_{pk-pk}

- Offset: 0 V
- Common mode offset: 0 V
- Load impedance: I/Q calibration fixture I Out impedance

4. Generate a 500 kHz signal with an amplitude of -1 dBFS.
5. Configure the power sensor to correct for the frequency specified in step 4.
6. Measure the signal power with the power meter. Store this value as the *Absolute Level*.
7. Generate a 1 MHz signal with an amplitude of -1 dBFS.
8. Configure the power sensor to correct for the frequency specified in step 7.
9. Measure the signal power with the power meter.
10. Repeat steps 7 though 9 for the following frequencies:

Table 47. Output AC Gain Accuracy and Passband Flatness Test Points

Frequency (MHz)				
1	5	10	15	20
25	30	35	40	

Record the results as *Relative Response* versus frequency.

11. Compare the *Absolute Level* from step 6 to the specified signal level using the following equation:

$$ACGainAccuracy(dB) = AbsoluteLevel(dBm) - \left[10 * \log\left(\left(\frac{step3VoltageRange}{50 * 2\sqrt{2}}\right)^2\right)dBm + 30dB - 1dB\right]$$

Compare the *AC Gain Accuracy* to the limits in the *Output AC Gain Accuracy and Passband Flatness Test Limits* table.

12. Compare the *Relative Response* from step 10 to the *Absolute Level* from step 6 using the following equation:

Passband Flatness at *f* (dB) = *Relative Response* (*f*) - *Absolute Level*

Compare the *Passband Flatness* to the limits in the *Output AC Gain Accuracy and Passband Flatness Test Limits* table.

13. Repeat steps 3 through 12 for the remaining I/Q output voltage levels: $1V_{pk\text{-}pk}$, $0.5\ V_{pk\text{-}pk}$, $0.1\ V_{pk\text{-}pk}$

Table 48. Output AC Gain Accuracy and Passband Flatness Test Limits

Specification	As-Found Limit (dB)	As-Left Limit (dB)
Absolute AC Gain Accuracy at -1.0 $V_{pk\text{-}pk}$	0.48	0.48
Absolute AC Gain Accuracy at -0.5 $V_{pk\text{-}pk}$	0.47	0.47

Table 48. Output AC Gain Accuracy and Passband Flatness Test Limits (Continued)

Specification	As-Found Limit (dB)	As-Left Limit (dB)
Absolute AC Gain Accuracy at -0.1 V_{pk-pk}	0.57	0.57
20 MHz Passband Flatness	0.42	0.42
40 MHz Passband Flatness	0.43	0.43

Updating Calibration Date and Time

This procedure updates the date and time of the last calibration of the PXIe-5645.

Prior to updating the calibration date and time on the PXIe-5645, you must successfully complete all required verifications or successfully complete reverification following adjustment.

Note You do not need to complete the optional verification procedures to update the calibration date and time.

1. Call the Update External Calibration Last Date and Time VI.
2. Call the Update External Calibration Temp VI.

Optional Verification

Use the following procedures to verify nonwarranted specifications for the PXIe-5645.

Verifying RF Input and RF Output Return Loss

This procedure verifies the return loss, also referred to as the voltage standing wave ratio (VSWR), of the PXIe-5645 RF input and output.

1. Calibrate the VNA for an S11 (return loss) measurement using the following settings:
   - Calibration: Short, open, load (SOL)
   - Sweep: 65 MHz to 6 GHz
   - Points: 801
   - IF bandwidth: 3 kHz
   - Power: 5 dBm
   - Connection: Male SMA
2. Connect the PXIe-5645 RF IN front panel connector to the calibrated PORT 1 of the VNA using an SMA (m)-to-SMA (m) cable.
3. Configure the PXIe-5645 receiver for 350 MHz with a -10 dBm reference level.
4. Perform an S11 measurement sweep using the following settings:
   - Center frequency: 350 MHz
   - Reference level: 0 dBm

5. Record the minimum absolute return loss value between the start and stop frequency listed for the specified carrier frequency in step 3. Compare the results with the appropriate limits listed in the following table.

Table 49. RF Input Return Loss Test Limits

Frequency	As-Found Limit (dB)	As-Left Limit (dB)
109 MHz ≤ *f* < 2.4 GHz	13	13
2.4 GHz ≤ *f* < 4 GHz	11	11
4 GHz ≤ *f* < 6 GHz	10	10

Note The as-found and as-left limits are not listed in the published specifications for the PXIe-5645. As-left limits are based on the published *PXIe-5645 Specifications*, less guard bands for measurement uncertainty, temperature drift, and drift over time.

6. Repeat steps 3 through 5 for the remaining configurations listed in the following table.

Table 50. Return Loss Test Points

Configured Frequency (MHz)	Measurement Start Frequency (MHz)	Measurement Stop Frequency (MHz)
350	109	<600
800	600	<1,000
1,200	1,000	<1,600
2,000	1,600	<2,700
3,000	2,700	<4,000
4,500	4,000	<5,000
5,500	5,000	6,000

7. Connect the PXIe-5645 RF OUT front panel connector to the calibrated PORT 1 of the VNA using an SMA (m)-to-SMA (m) cable.
8. Configure the PXIe-5645 to generate a -30 dBm CW tone at 350 MHz.
9. Perform an S11 measurement sweep. Record the minimum absolute return loss value between the start and stop frequency listed for the specified carrier frequency in step 3. Compare the results with the appropriate limits listed in the following table.

Table 51. RF Output Return Loss Test Limits

Frequency	As-Found Limit (dB)	As-Left Limit (dB)
109 MHz ≤ *f* < 2 GHz	16	16
2 GHz ≤ *f* < 5 GHz	13	13
5 GHz ≤ *f* < 6 GHz	9	9

Note The as-found and as-left limits are not listed in the published specifications for the PXIe-5645. As-left limits are based on the published *PXIe-5645 Specifications*, less guard bands for measurement uncertainty, temperature drift, and drift over time.

10. Repeat steps 8 and 9 for the remaining configured frequencies listed in the *Return Loss Test Points* table.

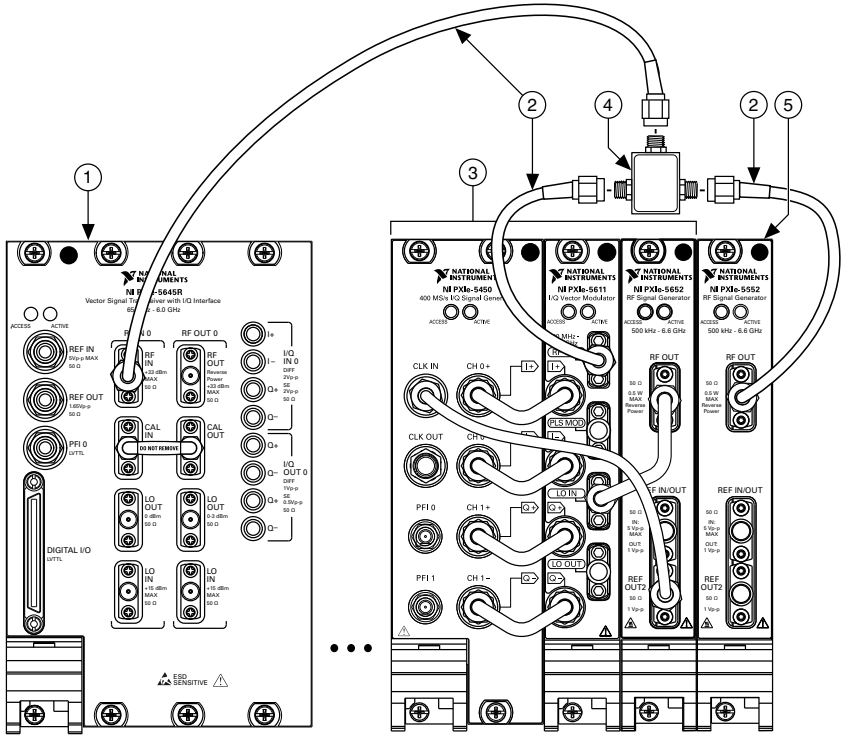
Verifying RF Input IMD3 and Second-Order Input Intermodulation (IMD2)

This procedure verifies the IMD3 and IMD2 distortion products of the PXIe-5645.

1. Connect the RF OUT ports of the vector signal generator and CW generator to the input ports of the power combiner.
2. Connect the output of the power combiner to the PXIe-5645 RF IN front panel connector.

   The following figure illustrates the complete hardware setup.

Figure 30. RF Input IMD3 and IMD2 Verification Cabling Diagram



1. NI 5645R
2. SMA (m)-to-SMA (m) Cable
3. Vector Signal Generator
4. Power Combiner
5. CW Signal Generator

3. Connect an available 10 MHz rubidium frequency reference output to the PXIe-5645 REF IN front panel connector.
4. Connect an available 10 MHz rubidium frequency reference output to the vector signal generator REF IN front panel connector.
5. Connect an available 10 MHz rubidium frequency reference output to the CW generator REF IN front panel connector.
6. Configure the PXIe-5645 for a center frequency of 65 MHz, using the following settings:
   - Center frequency: 65 MHz
   - Reference level: *Configured reference level* from the *IIP3 Test Limits* table that corresponds to the *center frequency*
   - Span: 20 MHz
   - Resolution bandwidth: 1 kHz
   - Averaging mode: RMS
   - Number of averages: 10

- Window type: Flat Top
- Reference Clock source: REF IN
- Reference Clock frequency: 10 MHz

Note Steps 7 and 8 configure the vector signal generator at a 2 MHz (f_1) and the CW generator at a 2.7 MHz (f_2) offset from the center frequency. The spacing of the two tones is the same for all iterations of this procedure.

7. Configure the vector signal generator for a frequency offset of f_1 from the *center frequency* in step 6, using the following settings:
   - Center frequency: *Center frequency* from step 6 + f_1
   - Power level: *Reference level* from step 6
   - Reference Clock source: REF IN
   - Reference Clock frequency: 10 MHz
8. Configure the CW generator for a frequency offset of f_2 from the *center frequency* in step 6, using the following settings:
   - Center frequency: *Center frequency* from step 6 + f_2
   - Power level: *Reference level* from step 6
   - Reference Clock source: REF IN
   - Reference Clock frequency: 10 MHz
9. Acquire a spectrum of the combined signal from steps 7 and 8 using the PXIe-5645.
10. Measure the power at expected distortion frequencies using the following settings:
    - *Center frequency* from step 6 + f_1, record as *fundamental tone*$_1$
    - *Center frequency* from step 6 + f_2, record as *fundamental tone*$_2$
    - Center frequency + ($2f_1$ - f_2), record as *IMD3 tone*
    - Center frequency + ($2f_2$ - f_1), record as *IMD3 tone*
    - Center frequency + (f_2 - f_1), record as *IMD2 tone*
    - Center frequency + (f_2 + f_1), record as *IMD2 tone*
11. Calculate *input IMD3* and *input IP3* using the following equations.

    input IMD3 = *maximum* (*IMD3 tone power*) - *minimum* (*fundamental tone*)

    input IP3 = *maximum* (*IMD3 tone power*) + (*IMD3*) / 2

    Record the *input IP3* value.
12. Calculate *input IMD2* and *input IP2* using the following equations.

    input IMD2 = *maximum* (*IMD2 Tone*) - *minimum* (*fundamental tone*)

    input IP2 = 2 * maximum (*IMD3 tone power*) + *IMD2*

    Record the *input IP2* value.
13. Repeat steps 6 through 12 for the remaining frequencies from 65 MHz to 6 GHz in 90 MHz steps.
14. Compare the calculated *input IP3* and *input IP2* with the specified limits in the following tables.

Table 52. IIP3 Test Limits

Frequency	Configured Reference Level (dBm)	As-Found Limit (dBm)	As-Left Limit (dBm)
65 MHz to 1.5 GHz	-5	19	19
>1.5 GHz to 4 GHz	-5	20	20
>4 GHz to 6 GHz	-2	20	20

Table 53. IIP2 Test Limits

Frequency	Configured Reference Level (dBm)	As-Found Limit (dBm)	As-Left Limit (dBm)
65 MHz to 1.5 GHz	-5	69	69
>1.5 GHz to 4 GHz	-5	58	58
>4 GHz to 6 GHz	-2	52	52

RF Adjustment

This section describes the steps needed to adjust the PXIe-5645 to meet published RF specifications.

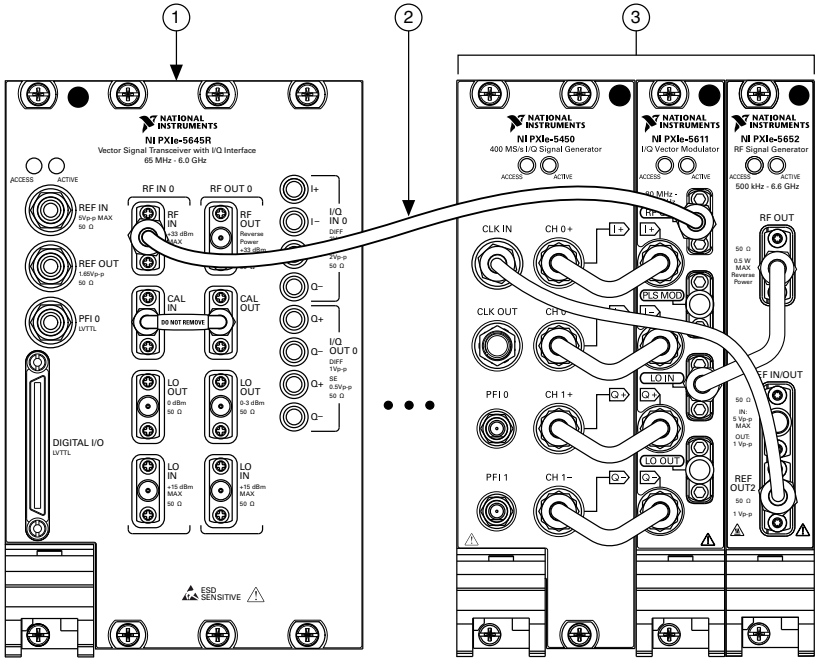
Adjusting RF Internal Frequency Reference

This procedure measures the accuracy of the internal frequency reference, which you use to realign the internal frequency reference to a value within warranted specifications.

1. Connect the vector signal generator RF OUT front panel connector to the PXIe-5645 RF IN front panel connector.

   The following figure illustrates the complete hardware setup.

Figure 31. Internal Frequency Reference Adjustment Cabling Diagram



1. PXIe-5645
2. SMA (m)-to-SMA (m) Cable
3. Vector Signal Generator

2. Connect an available 10 MHz rubidium frequency reference output to the vector signal generator REF IN front panel connector.
3. Configure the vector signal generator to generate a 2.22 GHz signal with a 0 dBm average output power, using the following settings:
   - Center frequency: 2.22 GHz
   - Output power: 0 dBm
   - Reference Clock source: External
4. Call the niVST Initialize External Calibration VI.
5. Call the niVST Reference Clock Cal VI. Wire the frequency of the vector signal generator to the **actual frequency** input.
6. Call the niVST Close External Calibration VI. Set the **write calibration to hardware?** input to TRUE to store the results to the EEPROM on the PXIe-5645.

Adjusting Input Absolute Amplitude Accuracy

This procedure measures the response of the RF IN signal path of the PXIe-5645. The response receives external signals at the RF IN front panel connector at a higher accuracy and optimized dynamic range.

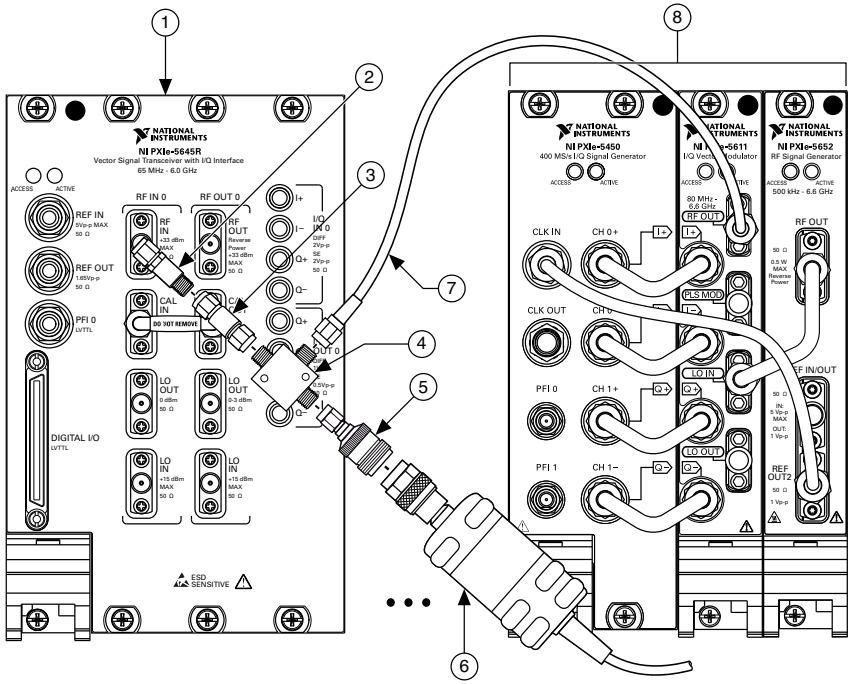
This procedure requires the test setup and data collected in the *Characterizing Power Splitter Balance* section. You must characterize the power splitter balance before running this procedure. Ensure you use the characterization data derived from test points 65 MHz to 6 GHz, in 5 MHz steps

You must zero the power sensor as described in the *Zeroing the Power Sensor* section prior to starting this procedure.

1. Connect the vector signal generator RF OUT front panel connector to the input terminal of the power splitter using a SMA (m)-to-SMA (m) cable.
2. Connect splitter output 1 directly to the power sensor input connector using an SMA (m)-to-N (f) adapter.
3. Connect the splitter output 2 to the SMA (f) end of the 6 dB attenuator using a 3.5 mm (m)-to-3.5 mm (m) adapter.
4. Connect the remaining 6 dB attenuator SMA (m) connector directly to the PXIe-5645 RF IN front panel connector.

   The following figure illustrates the hardware setup.

Figure 32. Absolute Amplitude Accuracy Adjustment Cabling Diagram



1. PXIe-5645
2. 6 dB Attenuator
3. 3.5 mm (m)-to-3.5 mm (m) Adapter
4. Power Splitter
5. SMA (m)-to-N (f) Adapter
6. Power Sensor
7. SMA (m)-to-SMA (m) Cable
8. Vector Signal Generator

5. Connect an available 10 MHz rubidium frequency reference output to the PXIe-5645 REF IN front panel connector.
6. Connect an available 10 MHz rubidium frequency reference output to the vector signal generator REF IN front panel connector.
7. Configure the PXIe-5645 to acquire a signal at 500 MHz using the following settings:
   - Center frequency: 500 MHz
   - Reference level: 30 dBm

   Note Steps 8 through 12 create correction factors that transfer the accuracy of the power sensor to the generator. Record the results from these steps in a lookup table called *Accuracy Transfer Results*.
8. Configure the vector signal generator to generate a tone using the following settings:
   - Center frequency: 65 MHz
   - Tone offset: 3.75 MHz
   - Power level: *Configured output power* from transfer row A of the following table
   - Reference Clock source: REF IN

Table 54. Absolute Amplitude Accuracy Adjustment Transfer Table

Transfer	Supported Output Power Levels	Configured Output Power (dBm)	Start Frequency (MHz)	Stop Frequency (GHz)	Frequency Step Size (MHz)
A	>-20 dBm to 0 dBm	0	65	6	5
B	≤-20 dBm	-20	65	6	5

9. Configure the power sensor to correct for the *center frequency* listed in step 7 using the power sensor frequency correction function.
10. Measure the power of the signal present at splitter output 1 of the power splitter using the power sensor.
11. Repeat steps 8 through 10 for the remaining frequencies listed in transfer row A of the previous table.
12. Repeat steps 8 through 11 for transfer row B of the previous table. Record the results from this step as *accuracy transfer result*. Create a table and include a value for each test point, *transfer* versus *frequency*.
13. Call the niVST Initialize External Calibration VI.
14. Call the niVST RF Input Gain Cal Initialize VI. Wire a Ref In constant to the **reference clock source** input.
15. Call the niVST RF Input Gain Cal Configure VI.
16. Configure the vector signal generator to generate a tone using the following settings:
    - Center frequency: **frequency to generate** output from step 15 - 3.75 MHz
    - Tone offset: 3.75 MHz
    - Power level: *Configured output power* from the transfer row of the previous table that supports the result of the following expression:
      (*power to generate* from step 15 + 10 dB) or 0 dBm, whichever is less
    - I/Q rate: 10 MS/s
    - Digital gain: ((*power to generate* from step 15 + 10 dB) - *power level* from step 16) or 0 dB, whichever is less.
    - Reference Clock source: REF IN
17. Calculate the *transfer input power* using the following equation:

    transfer input power = *accuracy transfer result* + *digital gain* from step 16

    Note Determine the *accuracy transfer result* by interpolating between the data points in the accuracy transfer results row based on step 16.
18. Calculate the *corrected input power* using the following equation:

    corrected input power = *transferred input power* + *splitter balance*

    Note Determine the *splitter balance* by interpolating between data points from the *Characterizing Power Splitter Balance* section. Ensure you use the characterization data derived from test points 65 MHz to 6 GHz, in 5 MHz steps.

19. Call the niVST RF Input Gain Cal Adjust VI.
    a) Wire the *corrected input power* from step 18 to the **actual power** input.
    b) Wire the value of (*center frequency* of the vector signal generator from step 16 + 3.75 MHz) to the **actual frequency** input.
20. Repeat steps 15 through 19 until the **RF input gain calibration complete** output of the niVST RF Input Gain Cal Adjust VI returns a value of TRUE.
21. Call the niVST Close External Calibration VI. Set the **write calibration to hardware?** input to TRUE to store the results to the EEPROM on the PXIe-5645.

Adjusting Output Power Level Accuracy

This procedure measures the response of the RF OUT signal path of the PXIe-5645. The response generates accuracy signals at the RF OUT front panel connector.

This procedure requires the test setup and data collected in the *Characterizing Power Splitter Loss* section. You must characterize the power splitter loss before running this procedure. Ensure you use the characterization data derived from test points 65 MHz to 6 GHz, in 5 MHz steps.

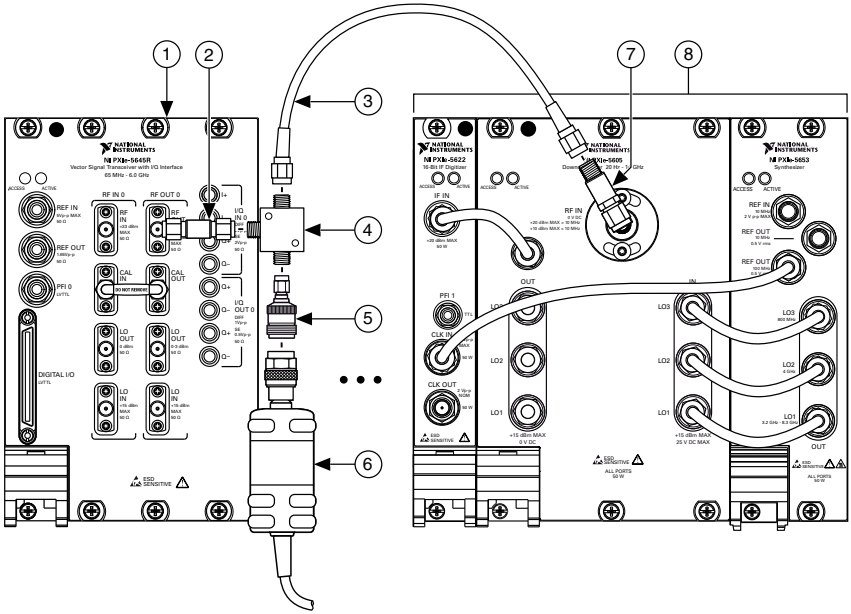
You must zero the power sensor as described in the *Zeroing the Power Sensor* section prior to starting this procedure.

1. Connect the PXIe-5645 RF OUT front panel connector to the input terminal of the power splitter using a 3.5mm (m)-to-3.5mm (m) adapter.
2. Connect splitter output 1 directly to the power sensor using the SMA (m)-to-N (f) adapter.
3. Connect the remaining power splitter output to one end of the 6 dB attenuator using an SMA (m)-to- SMA (m) cable.
4. Connect the other port of the 6 dB attenuator directly to the spectrum analyzer RF IN front panel connector.

   The following figure illustrates the complete hardware setup.

Note If you use the PXIe-5665, as recommended, for the spectrum analyzer, disable the preamplifier and preselector options and set the FFT window type to Flat Top.

Figure 33. Output Power Level Accuracy Adjustment Cabling Diagram



1. PXIe-5645
2. 3.5 mm (m)-to-3.5 mm (m) Adapter
3. SMA (m)-to-SMA (m) Cable
4. Power Splitter
5. SMA (m)-to-N (f) Adapter
6. Power Sensor
7. 6 dB Attenuator
8. Spectrum Analyzer

5. Connect an available 10 MHz rubidium frequency reference output to the PXIe-5645 REF IN front panel connector.
6. Connect an available 10 MHz rubidium frequency reference output to the vector signal analyzer REF IN front panel connector.
7. Call the niVST Initialize External Calibration VI.
8. Call the niVST RF Output Gain Cal Initialize VI. Wire a RefIn constant to the **reference clock source** input.
9. Call the niVST RF Output Gain Cal Configure VI.
10. Configure the spectrum analyzer to acquire a signal with the following settings:
    - Center frequency: **frequency to measure** output of the niVST RF Output Gain Cal Configure VI
    - Reference level: *Configured reference level* specified in the *Accuracy Transfer Definitions* table from the *Characterizing Power Splitter Loss* section that supports the result of the following expression:
      expected power output from step 9 - 12 dB
    - Span: *Span* from the following table that corresponds to the *reference level* from this step
    - Resolution bandwidth: *RBW* from the following table that corresponds to the *reference level* from this step

- Averaging mode: RMS
- Number of averages: *Number of averages* from the following table that corresponds to the reference level from this step

Table 55. Advanced Spectrum Analyzer Settings

Supported Output Power Levels	Span (kHz)	RBW	Number of Averages
$x >$ -70 dBm	250	4 kHz	10
-70 dBm $\geq x >$ -100 dBm	250	900 Hz	20
$x \leq$ -100 dBm	250	900 Hz	100

11. Acquire the signal with the spectrum analyzer and measure the peak tone power.
12. Calculate the *transferred output power* using the following equation:

    transferred output power = accuracy transfer result + measured tone power

    Note Determine the *accuracy transfer result* by interpolating between the data points in the *RF Output Accuracy Transfer Results* table you created in step 21 of the *Characterizing Power Splitter Loss* section. Ensure you use the characterization data derived from test points 65 MHz to 6 GHz, in 5 MHz steps. Choose the value that corresponds to the transfer used.
13. Calculate the *corrected output power* using the following equation:

    corrected output power = transferred output power + splitter loss

    Note Determine the *splitter loss* by interpolating between the data points in the *Splitter Loss* table you created in step 20 of the *Characterizing Power Splitter Loss* section. Ensure you use the characterization data derived from test points 65 MHz to 6 GHz, in 5 MHz steps. Choose the value that corresponds to the transfer used.
14. Call the niVST RF Output Gain Cal Adjust VI. Wire the *corrected output power* from step 13 to the **measured power** input.
15. Repeat steps 9 through 14 until the **RF output gain calibration complete** output of the niVST RF Output Gain Cal Adjust VI returns a value of TRUE.
16. Call the niVST Close External Calibration VI. Set the **write calibration to hardware?** input to TRUE to store the results to the EEPROM on the PXIe-5645.

Adjusting LO OUT (RF IN 0 and RF OUT 0)

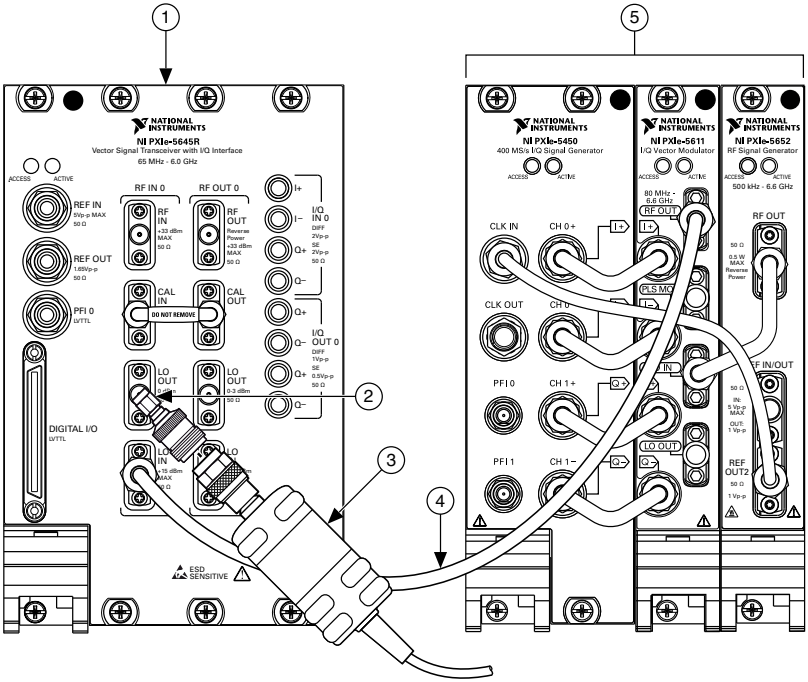
This procedure measures the PXIe-5645 LO Power Sensor response. The internal power sensor ensures that the internal LO power level is correct at the mixing stages for the RF IN and RF OUT channels.

You must zero the power sensor as described in the *Zeroing the Power Sensor* section prior to starting this procedure.

1. Connect the power sensor to the PXIe-5645 RF IN 0 LO OUT front panel with the SMA (m)-to-N (f) adapter.
2. Connect the vector signal generator RF OUT front panel connector to the PXIe-5645 RF IN 0 LO IN front panel connector with an SMA (m)-to-SMA (m) cable.

The following figure illustrates the complete hardware setup.

Figure 34. LO OUT Adjustment Cabling Diagram



1. PXIe-5645
2. SMA (m)-to-N (f) Adapter
3. Power Sensor
4. SMA (m)-to-SMA (m) Cable
5. Vector Signal Generator

3. Call the niVST Initialize External Calibration VI.
4. Call the niVST LO Cal Initialize VI. Wire an RF In constant to the **port type** input.
5. Call the niVST LO Cal Configure VI.
6. Configure the vector signal generator to generate a tone with the following settings:
   - Center frequency: **frequency to generate** output specified by the niVST LO Cal Configure VI.
   - Power level: **power to generate** output specified by the niVST LO Cal Configure VI.
   - Reference Clock source: Onboard
7. Configure the power meter to correct for the **frequency to generate** output specified by the niVST LO Cal Configure VI.
8. Measure the power of the signal present at the RF IN 0 LO OUT front panel connector using the power sensor.
9. Call the niVST LO Cal Adjust VI. Wire the measured value from step 8 to the **measured LO Out power** input.

10. Repeat steps 5 through 9 until the **LO calibration complete** output of the niVST LO Cal Adjust VI returns a value of TRUE.
11. Call the niVST Close External Calibration VI. Set the **write calibration to hardware?** input to TRUE to store the results to the EEPROM on the PXIe-5645.
12. Repeat steps 1 to 11 for RF OUT 0 LO OUT to adjust the LO power sensor of the PXIe-5645 RF OUT channel.

I/Q Adjustment

This section describes the steps needed to adjust the PXIe-5645 to meet published I/Q specifications.

Before performing any I/Q adjustments, characterize the I/Q calibration fixture designated for adjustments once, as described in the *I/Q Test System Characterization* section.

Adjusting I/Q Input DC Gain

This procedure adjusts the differential and single-ended I/Q input DC gain for the PXIe-5645 to meet published specifications.

Characterize the I/Q calibration fixture designated for adjustments once prior to performing any adjustments.

1. Set up the hardware as illustrated in the *I/Q Test Equipment* section.
2. Configure the calibration fixture using the following settings:
   - Signal path: Inline
   - DMM source: I In
   - Terminal configuration: Differential
3. Call the niVST Initialize External Calibration VI.
4. Call the niVST IQ In DC Gain Cal Initialize VI and configure the following inputs of the VI:
   - **port**: I
   - **terminal configuration**: Differential
5. Configure the DMM with the following settings:
   - Measurement digits: 6 ½
   - Function: DC Volts
   - Digits: 6 ½
   - Range: Automatic
   - Aperture: 0.1 seconds
   - Auto zero: On
   - Offset compensated Ohms: On
   - Number of averages: 1
   - Power line frequency: 60 Hz
6. Call the niVST IQ In DC Gain Cal Configure VI.

7. Configure the PXIe-5645 I/Q output with the following settings:
   - Frequency offset: 0 Hz
   - Terminal configuration: Terminal configuration setting from step 4
   - Level ($_{pk\text{-}pk}$): **voltage to generate** output from the niVST IQ In DC Gain Cal Configure VI
   - Load impedance: I and Q load impedance values from the *I/Q Test System Characterization*
   - Use correction filter: TRUE
8. Measure the DC voltage using the DMM.
9. Correct the measurement from step 8 by normalizing the measured result to the impedance network using the following equation.

   Corrected DMM Measurement (V) = *DMM Measurement from step 8* * ((*Impedance*$_{DMM\ Source}$ - *Impedance*$_{Cable}$ + *Impedance*$_{Relay}$)/*Impedance*$_{DMM\ Source}$)
10. Call the niVST IQ in DC Gain Cal Adjust VI. Wire the corrected result from step 9 to the **actual voltage generated** input of the VI.
11. Repeat steps 5 through 10 until the **DC gain calibration complete** output of the niVST IQ In DC Gain Cal Adjust VI returns TRUE.
12. Call the niVST Close External Calibration VI. Set the **write calibration to hardware?** input to TRUE to store the results to the EEPROM of the PXIe-5645.
13. Repeat steps 2 through 12 for the remaining configurations in the following table.

Table 56. I/Q Input DC Gain Adjustment Settings

PXIe-5645 Settings			Calibration Fixture Settings		
Port	**Terminal Configuration**	**Port Type**	**Signal Path**	**DMM Source**	**Terminal Configuration**
I	Differential	I/Q Out	Inline	I In	Differential
I	Single-ended	I/Q Out	Inline	I In	Single-ended
Q	Differential	I/Q Out	Inline	Q In	Differential
Q	Single-ended	I/Q Out	Inline	Q In	Single-ended

Adjusting I/Q Input DC Offset

This procedure adjusts the differential and single-ended I/Q input DC offset for the PXIe-5645 to meet published specifications.

Characterize the I/Q calibration fixture designated for adjustments once prior to performing any adjustments.

1. Set up the hardware as illustrated in the *I/Q Test Equipment* section.

2. Configure the calibration fixture using the following settings:
   - Signal path: Terminated
   - DMM source: None
   - Terminal configuration: Differential
3. Call the niVST Initialize External Calibration VI.
4. Call the niVST IQ In DC Offset Cal VI. Set the **port** input of the VI to I.
5. Call the niVST Close External Calibration VI. Set the **write calibration to hardware?** input to TRUE to store the results to the EEPROM of the PXIe-5645.
6. Repeat steps 2 through 5 for the Q port of the PXIe-5645:
   - Signal path: Terminated
   - DMM source: None
   - Terminal configuration: Differential

Adjusting I/Q Input Passband Flatness

This procedure adjusts the differential and single-ended I/Q input passband flatness for the PXIe-5645 to meet published specifications.

Characterize the I/Q calibration fixture designated for adjustments once prior to performing any adjustments.

1. Set up the hardware as illustrated in the *I/Q Test Equipment* section.
2. Configure the calibration fixture using the following settings:
   - Signal path: Splitter I
   - DMM source: None
   - Terminal configuration: Differential
3. Call the niVST Initialize External Calibration VI.
4. Call the niVST IQ In Flatness Cal Initialize VI, and set the **terminal configuration** input to Differential.
5. Call the niVST IQ In Flatness Cal Configure VI.
6. Configure the PXIe-5645 I/Q output using the following settings:
   - Terminal configuration: Terminal configuration from Step 2
   - Output level: The result of the following expression:
     $$\frac{voltagetogenerateoutput\ of the\ niVST\ IQ\ InFlatnessCalConfigure\ VI}{nominal\ splitter gain}$$
   - Tone frequency: **frequency to generate** output of the niVST IQ In Flatness Cal Configure VI
7. Measure the output signal using power sensor 1. Configure the power sensor to compensate for the signal frequency specified in step 6.

   Store the output signal as $+Power_{diff}$ in watts.
8. Measure the output signal using power sensor 2. Configure the power sensor to compensate for the signal frequency specified in step 6.

   Store the output signal as $-Power_{diff}$ in watts.
9. Calculate $Power_{diff}$ using the following equation:

$$Power_{diff} = \left(+Power_{diff}\right) + \left(-Power_{diff}\right) + \left(2 * \sqrt{\left(+Power_{diff}\right) * \left(-Power_{diff}\right)}\right)$$

10. Convert $Power_{diff}$ to dBm using the following equation:

$$Power(dBm) = 10 * \log\left(Power_{diff} * 1000\right)$$

11. Correct the result of step 10 by adding the loss of the calibration fixture at the frequency specified in step 6.
12. Call the niVST IQ In Flatness Cal Adjust VI, and complete the following steps:
    a) Set the **actual frequency** input of the VI to the value of the **frequency to generate** output of the niVST IQ In Flatness Cal Configure VI.
    b) Wire the corrected measurement from step 11 to the **measured power** input.
13. Repeat steps 5 through 12 until the **flatness calibration complete** output of the niVST IQ In Flatness Cal Adjust VI returns TRUE.
14. Call the niVST Close External Calibration VI. Set the **write calibration to hardware?** input to TRUE to store the results to the EEPROM of the PXIe-5645.
15. Repeat steps 2 through 14 with the terminal configuration set to single-ended.

Adjusting I/Q Input Gain and Phase Matching

This procedure adjusts the differential and single-ended I/Q input gain and phase matching for the PXIe-5645 to meet published specifications.

Characterize the I/Q calibration fixture designated for adjustments once prior to performing any adjustments.

1. Set up the hardware as illustrated in the *I/Q Test Equipment* section.
2. Configure the calibration fixture using the following settings:
    - Signal path: Inline
    - DMM source: None
    - Terminal configuration: Differential
3. Call the niVST Initialize External Calibration VI.
4. Call the niVST IQ Matching Cal VI. Configure the following inputs of the VI:
    - **cable configuration**: Inline
    - **IQ terminal configuration**: Differential
    - **cable impairments**: *cable impairments* from calibration fixture characterization
5. Call the niVST Close External Calibration VI. Set the **write calibration to hardware?** input to TRUE to store the results to the EEPROM of the PXIe-5645.
6. Repeat steps 2 through 5 for the remaining configurations in the following table.

Table 57. I/Q Input Gain and Phase Matching Adjustment Settings

PXIe-5645 Settings		Calibration Fixture Settings		
Cable Configuration	**Terminal Configuration**	**Signal Path**	**DMM Source**	**Terminal Configuration**
Inline	Differential	Inline	None	Differential
Cross	Differential	Cross	None	Differential
Inline	Single-ended	Inline	None	Single-ended
Cross	Single-ended	Cross	None	Single-ended

Adjusting I/Q Input Impedance

This procedure adjusts the differential and single-ended I/Q input impedance for the PXIe-5645 to meet published specifications.

Characterize the I/Q calibration fixture designated for adjustments once prior to performing any adjustments.

1. Set up the hardware as illustrated in the *I/Q Test Equipment* section.
2. Configure the calibration fixture using the following settings:
   - Signal path: No connection
   - DMM source: I In
   - Terminal configuration: Differential
3. Call the niVST Initialize External Calibration VI.
4. Call the niVST IQ Impedance Cal Initialize VI and configure the following inputs of the VI:
   - **terminal configuration**: Differential
   - **port**: I
   - **port type**: IQ In
5. Call the niVST IQ Impedance Cal Configure VI.
6. Measure the impedance of the current PXIe-5645 configuration using the DMM with the following settings:
   - Function: 2-Wire resistance
   - Digits: 6 ½
   - Range: 200 Ω
   - Aperture: 0.1 seconds
   - Auto zero: On
   - Offset compensated Ohms: On
   - Number of averages: 1
   - Power line frequency: 60 Hz
7. Correct the result of step 6 using the following equation:

   corrected impedance = measured impedance - (*I/Q calibration fixture relay impedance* + *cable impedance*)

8. Call the niVST IQ Impedance Cal Adjust VI, and wire the *corrected impedance* from step 7 to the **measured impedance** input.
9. Repeat steps 5 through 8 until the **impedance cal complete** output of the niVST IQ Impedance Cal Adjust VI returns TRUE.
10. Call the nIVST Close External Calibration VI. Set the **write calibration to hardware?** input to TRUE to store the results to the EEPROM of the PXIe-5645.
11. Repeat steps 2 through 10 for the remaining configurations listed in the following table.

Table 58. I/Q Input Impedance Adjustment Settings

PXIe-5645 I/Q Settings			Calibration Fixture Settings		
Port	**Terminal Configuration**	**Port Type**	**Signal Path**	**DMM Source**	**Terminal Configuration**
I	Differential	I/Q In	No connection	I In	Differential
I	Single-ended	I/Q In	No connection	I In	Single-ended
Q	Differential	I/Q In	No connection	Q In	Differential
Q	Single-ended	I/Q In	No connection	Q In	Single-ended

Adjusting I/Q Output Gain and Offset

This procedure adjusts the differential and single-ended I/Q output gain and offset for the PXIe-5645 to meet published specifications.

Characterize the I/Q calibration fixture designated for adjustments once prior to performing any adjustments.

1. Set up the hardware as illustrated in the *I/Q Test Equipment* section.
2. Configure the calibration fixture using the following settings:
   - Signal path: No Connection
   - DMM source: I Out
   - Terminal configuration: Differential
3. Call the niVST Initialize External Calibration VI.
4. Call the niVST IQ Out DC Gain and Offset Cal Initialize VI and configure the following inputs of the VI:
   - **port**: I
   - **terminal configuration**: Differential
   - **load impedance**: High impedance
5. Configure the DMM with the following settings
   - Function: DC Volts
   - Digits: 6 ½
   - Range: Auto
   - Aperture: 0.1 seconds
   - Auto zero: On

- Offset compensated Ohms: On
- Number of averages: 1
- Power line frequency: 60 Hz

6. Call the nIVST IQ Out DC Gain and Offset Cal Configure VI.
7. Measure the I/Q output DC voltage using the DMM.
8. Call the niVST IQ Out DC Gain and Offset Cal Adjust VI. Wire the result from step 8 to the **measured output** input.
9. Repeat steps 5 through 9 until the **DC gain and offset calibration complete** output of the niVST IQ Out DC Gain and Offset Cal Adjust VI returns TRUE.
10. Call the niVST Close External Calibration VI. Set the **write calibration to hardware?** input to TRUE to store the results to the EEPROM of the PXIe-5645.
11. Repeat steps 2 through 11 for the remaining configurations in the following table.

Table 59. I/Q Output Gain and Offset Adjustment Settings

PXIe-5645 Settings			Calibration Fixture Settings		
Port	**Terminal Configuration**	**Load Impedance**	**Signal Path**	**DMM Source**	**Terminal Configuration**
I	Differential	High impedance	No connection	I Out	Differential
I	Single-ended	High impedance	No connection	I Out	Single-ended
Q	Differential	High impedance	No connection	Q Out	Differential
Q	Single-ended	High impedance	No connection	Q Out	Single-ended

Adjusting I/Q Output Passband Flatness

This procedure adjusts the differential and single-ended passband flatness for the PXIe-5645 to meet published specifications.

Characterize the I/Q calibration fixture designated for adjustments once prior to performing any adjustments.

1. Set up the hardware as illustrated in the *I/Q Test Equipment* section.
2. Configure the calibration fixture using the following settings:
   - Signal path: Absolute I
   - DMM source: None
   - Terminal configuration: Differential
3. Call the niVST Initialize External Calibration VI.
4. Call the niVST IQ Out Flatness Cal Initialize VI. Set the **terminal configuration** to differential.
5. Call the niVST IQ Out Flatness Cal Configure VI.

6. Measure the output signal using power sensor 1. Configure the power sensor to compensate for the signal frequency specified by the output of the niVST IQ Out Flatness Cal Configure VI.

   Store the output signal as $+Power_{diff}$ in watts.

7. Measure the output signal using power sensor 2. Configure the power sensor to compensate for the signal frequency specified by the output of the niVST IQ Out Flatness Cal Configure VI.

   Store the output signal as $-Power_{diff}$ in watts.

8. Calculate $Power_{diff}$ using the following equation:

$$Power_{diff} = \left(+Power_{diff}\right) + \left(-Power_{diff}\right) + \left(2 * \sqrt{\left(+Power_{diff}\right) * \left(-Power_{diff}\right)}\right)$$

9. Convert $Power_{diff}$ to dBm using the following equation:

$$Power(dBm) = 10 * \log\left(Power_{diff} * 1000\right)$$

10. Correct the result of step 9 by adding the loss of the calibration fixture at the frequency specified by the output of the niVST IQ Out Flatness Cal Configure VI to *Power*(*dBm*).
11. Call the niVST IQ Out Flatness Cal Adjust VI. Wire the result of step 10 to the **measured power** input of the VI.
12. Repeat steps 5 through 11 until the **flatness calibration complete** output of the niVST IQ Out Flatness Cal Adjust VI returns TRUE.
13. Call the niVST Close External Calibration VI. Set the **write calibration to hardware?** input to TRUE to store the results to the EEPROM of the PXIe-5645.
14. Repeat steps 2 through 13 with the terminal configuration set to single-ended.

Adjusting I/Q Output Impedance

This procedure adjusts the differential and single-ended I/Q output impedance for the PXIe-5645 to meet published specifications.

Characterize the I/Q calibration fixture designated for adjustments once prior to performing any adjustments.

1. Set up the hardware as illustrated in the *I/Q Test Equipment* section.
2. Configure the calibration fixture using the following settings:
   - Signal path: No connection
   - DMM source: I Out
   - Terminal configuration: Differential
3. Call the niVST Initialize External Calibration VI.

4. Call the niVST IQ Impedance Cal Initialize VI and configure the following inputs of the VI:
   - **terminal configuration**: Differential
   - **port**: I
   - **port type**: IQ Out
5. Call the niVST IQ Impedance Cal Configure VI.
6. Measure the impedance of the current PXIe-5645 configuration using the DMM with the following settings:
   - Function: 2-Wire resistance
   - Digits: 6 ½
   - Range: 200 Ω
   - Aperture: 0.1 seconds
   - Auto zero: On
   - Offset compensated Ohms: On
   - Number of averages: 1
   - Power line frequency: 60 Hz
7. Correct the result of step 6 using the following equation:

   corrected impedance = measured impedance - (*I/Q calibration fixture relay impedance + cable impedance*)
8. Call the niVST IQ Impedance Cal Adjust VI and wire the *corrected impedance* from step 7 to the **measured impedance** input.
9. Repeat steps 5 through 8 until the **impedance cal complete** output of the niVST IQ Impedance Cal Adjust VI returns TRUE.
10. Call the nIVST Close External Calibration VI. Set the **write calibration to hardware?** input to TRUE to store the results to the EEPROM of the PXIe-5645.
11. Repeat steps 2 through 10 for the remaining configurations listed in the following table.

Table 60. I/Q Output Impedance Adjustment Settings

PXIe-5645 I/Q Settings			Calibration Fixture Settings		
Port	**Terminal Configuration**	**Port Type**	**Signal Path**	**DMM Source**	**Terminal Configuration**
I	Differential	I/Q Out	No connection	I Out	Differential
I	Single-ended	I/Q Out	No connection	I Out	Single-ended
Q	Differential	I/Q Out	No connection	Q Out	Differential
Q	Single-ended	I/Q Out	No connection	Q Out	Single-ended

EEPROM Update

When an adjustment procedure completes, the PXIe-5645 internal calibration memory, stored in the EEPROM, immediately updates.

If you do not want to perform an adjustment, you can update the calibration date and onboard calibration temperature without making any adjustments by performing an external calibration in software.

Reverification

Repeat the *Verification* section to determine the as-left status of the PXIe-5645.

Note If any test fails reverification after performing an adjustment, verify that you have met the test conditions before returning your PXIe-5645 to NI. Refer to the *Worldwide Support and Services* section for information about support resources or service requests.

Worldwide Support and Services

The NI website is your complete resource for technical support. At *ni.com/support*, you have access to everything from troubleshooting and application development self-help resources to email and phone assistance from NI Application Engineers.

Visit *ni.com/services* for NI Factory Installation Services, repairs, extended warranty, and other services.

Visit *ni.com/register* to register your NI product. Product registration facilitates technical support and ensures that you receive important information updates from NI.

A Declaration of Conformity (DoC) is our claim of compliance with the Council of the European Communities using the manufacturer's declaration of conformity. This system affords the user protection for electromagnetic compatibility (EMC) and product safety. You can obtain the DoC for your product by visiting *ni.com/certification*. If your product supports calibration, you can obtain the calibration certificate for your product at *ni.com/calibration*.

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