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# Understanding FlexRIO Integrated I/O Features

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# Power On, Download, and Reset Conditions

Your FlexRIO with Integrated I/O device applies default conditions after powering on the device, restarting the device, or downloading a new FPGA VI to the device. Find the default conditions for your module listed below.

## PXle-5763, PXle-5764, PXle-5775

- ADC resets to its default operating mode.
- Clocking is reset to the internal clock and backplane reference.
- Phase DAC value resets to minimum.

## PXle-5745

- DAC resets to its default operating mode: 3.2 GS/s dual-channel, inverse sinc filter disabled
- Clocking is reset to the internal clock and backplane reference.
- Phase DAC value resets to minimum.

## PXle-5785

- ADC resets to its default operating mode: 3.2 GS/s dual-channel
- DAC resets to its default operating mode: 3.2 GS/s dual-channel, inverse sinc filter disabled
- Clocking is reset to the internal clock and backplane reference.
- Phase DAC value resets to minimum.

# PXI Express FPGA Module Functions Supported by FlexRIO Integrated I/O Devices

Your FlexRIO Integrated I/O device supports the following LabVIEW FPGA functions:

## Arbitration

Determines which object can access the resource if multiple objects request access at the same time. Configure the arbitration settings for the channels of this device in the FPGA I/O Properties dialog box for the FPGA I/O item you are using.

## FPGA Base Clocks

Refer to the FPGA Target Properties Dialog Box topic in the LabVIEW FPGA Help for more information about configuring base clocks.

## Single-Cycle Timed Loop

Enables implementation of multiple clock domains in an FPGA VI.

## Peer-to-Peer Streaming

Enables peer-to-peer data streaming. Use LabVIEW FPGA to configure your FlexRIO with Integrated I/O device to set up a peer-to-peer streaming session.

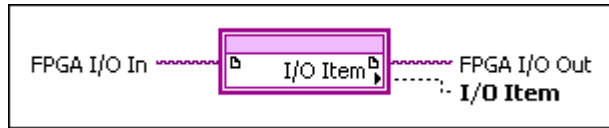
## FlexRIO Peer-to-Peer Resource Availability

Enables Peer to Peer Reader and Peer to Peer Writer streams. The following table lists the stream types available for FlexRIO PXI Express devices.

FIFO Type	Description
DMA input	Reads data into the FIFO from the VI.
DMA output	Writes data from the FIFO into the VI.
P2P Writer	Writes data to the peer-to-peer reader device.
P2P Reader	Reads data from the peer-to-peer writer device.

# PXI/PXIe FPGA I/O Items

**Figure 1.** FPGA I/O Node



You can use an FPGA I/O Node, configured for reading and writing, with your FlexRIO Integrated I/O device. The FPGA I/O Node is located on the FPGA I/O Functions palette and performs specific FPGA I/O operations on your FPGA target.

You can select the following PXI/PXI Express FPGA I/O items for the FlexRIO with Integrated I/O devices.

**Table 2.** PXI/PXIe FPGA I/O Items

FPGA I/O Item	Description
PXI_Clk10	Controls the 10 MHz clock on the PXI backplane. You can use this clock to synchronize multiple PXI modules. Use an FPGA I/O Node configured for reading across this channel.

**Table 2.** PXI Express FPGA I/O Items

Terminal	Description
PXIe_DStarB	Controls the differential star trigger that creates connections between a PXI Express system timing module and a peripheral device. PXIe_DStarB distributes trigger signals from the system timing slot to the peripherals (input). Use an FPGA I/O Node configured for reading to access this channel.
PXIe_DStarC	Controls the differential star trigger that creates connections between a PXI Express system timing module and a peripheral device. PXIe_DStarC sends trigger or clock signals from the peripherals to the system timing slot (output). Use an FPGA I/O Node configured for writing to access this channel.

Terminal	Description
PXIe_Sync100	Controls the reference signal that is synchronous to the rising edge of PXIe_CLK100. Use PXIe_Sync100 to synchronize multiple modules in a PXI Express system. Use an FPGA I/O Node configured for reading to access this channel.

# FPGA Base Clock Resources for FlexRIO with Integrated I/O

A base clock is a digital signal existing in hardware that you can use as a clock for an FPGA application.

You can use the following base clock resources for FlexRIO with Integrated I/O devices:

## 80 MHz Clock

The 80 MHz Onboard Clock is the default clock in your LabVIEW FPGA project. This clock can be used as a top-level clock for running your LabVIEW FPGA VI. The top-level clock on an FPGA target determines the execution time of the individual functions and VIs on the FPGA VI block diagram. If you change the frequency of the top-level clock, you also change the execution speed of functions on the block diagram and the execution rate of the FPGA VI.

## PXle\_Clk100

PXle\_Clk100 can be used as a source for running your LabVIEW FPGA VI.

## 300 MHz Clock

The 300 MHz Clock can be used as a source for running your LabVIEW FPGA VI. Refer to the FPGA Base Clock Properties Dialog Box topic of the **LabVIEW FPGA Module Help** for more information about configuring base clocks on your FPGA target.

## DRAM Clock

The DRAM Clock drives the DRAM interface. Refer to the FPGA Base Clock Properties Dialog Box topic in the **LabVIEW FPGA Module Help** for more information about configuring base clocks on your FPGA target.





**Note** Some FlexRIO with Integrated I/O FPGA variants do not have onboard DRAM. The DRAM clock is only available on variants that include onboard DRAM.

# CLIP File and Adapter Module Configuration File Locations

To access CLIP files and adapter module configuration files, open `<NISharedDir>/FlexRIO IO Sockets/FlexRIOIoSocketType1/<Device name>/`.



**Note** All FlexRIO with Integrated I/O targets parse only the .fam files in the subdirectory determined by their target name independent of their bus type or FPGA variant. For example, the targets PXIe-5763 - KU060 and PXIe-5763 - KU040 both parse the folder NI-5763.

# Configuring FlexRIO I/O in LabVIEW

The FlexRIO I/O module provides the interface to the physical I/O signals in your system.

1. Right-click the target and select **Properties** to configure the type of I/O module used in your system.
2. In the IO Module Properties window, select the **General** heading under the **Category** column.
3. Check the **Enable IO Module** box to enable the use of an I/O module with your device.
4. Select your I/O module from the **IO Modules** list, then select the I/O module's CLIP from the **Component Level IP** list.
5. Click **OK**.
6. Select **Clock Selections** from the **Category** column.
7. Select **Clocks** and click **Create Necessary Clocks**.
8. Click **OK**.



**Note** Select **Details** from the **Category** list for more information about the I/O module in your system.

# Socketed Component-Level IP (CLIP) by Module Name

The following tables provide the Socketed CLIP signals for your FlexRIO Integrated I/O Module.



**Notice** You can create custom CLIP items for your FlexRIO Integrated I/O module. If you choose to develop a custom CLIP item for your application, NI recommends using the CLIP provided with in the LabVIEW example for your module as a template, while referring to the specifications for your module to ensure you maintain the proper electrical characteristics. Failure to adhere to the specified electrical requirements and signal directions may result in device damage. NI is not liable for any damage resulting from such misuse.

## PXle-5745 Socketed CLIP Signals

The PXle-5745 CLIP provides access to two AC-coupled 12-bit 3.2 GS/s analog input channels and eight bidirectional DIO channels.

CLIP Signal Name	Direction	Data Type	Description
Data Clock	From CLIP	Boolean	FPGA clock used to sample analog input data.
Data Clock 2x	From CLIP	Boolean	FPGA clock that samples analog input data at twice the rate of Data Clock.
AO Ready for Input	From CLIP	Boolean	Indicates whether the AO link is ready for data.
AO 0 Data N	To CLIP	fixed-point <±12,1>	Sends analog output samples through the AO 0 front panel connector.
AO 0 Data N-1			
AO 0 Data N-2			
AO 0 Data N-3			

CLIP Signal Name	Direction	Data Type	Description
AO 0 Data N-4			
AO 0 Data N-5			
AO 0 Data N-6			
AO 0 Data N-7			
AO 0 Data N-8			
AO 0 Data N-9			
AO 0 Data N-10			
AO 0 Data N-11			
AO 0 Data N-12			
AO 0 Data N-13			
AO 0 Data N-14			
AO 0 Data N-15			
Ao 1 Data N	To CLIP	fixed-point <±12,1>	Sends analog output samples through the AO 1 front panel connector.
AO 1 Data N-1			
AO 1 Data N-2			
AO 1 Data N-3			
AO 1 Data N-4			
AO 1 Data N-5			
AO 1 Data N-6			
AO 1 Data N-7			
AO 1 Data N-8			
AO 1 Data N-9			
AO 1 Data N-10			
AO 1 Data N-11			
AO 1 Data N-12			
AO 1 Data N-13			
AO 1 Data N-14			
AO 1 Data N-15			
IO Error	From CLIP	i32	Returns IO module errors, to be reported by the driver.

CLIP Signal Name	Direction	Data Type	Description
IO Ready	From CLIP	Boolean	Indicates successful configuration of the IO module devices with the current clocking mode settings.

## PXle-5785 Socketed CLIP Signals

The PXle-5785 CLIP provides access to two AC-coupled 12-bit 3.2 GS/s analog input channels, two AC-coupled 12 bit 3.2 GS/s analog output channels, and eight bidirectional DIO channels.

CLIP Signal Name	Direction	Data Type	Description
Data Clock	From CLIP	Boolean	FPGA clock used to sample analog input data.
Data Clock 2x	From CLIP	Boolean	FPGA clock that samples analog input data at twice the rate of Data Clock.
AI Data Valid	From CLIP	Boolean	Indicates whether AI sample data is valid.
AI 0 Data N	From CLIP	fixed-point $\langle \pm 12, 1 \rangle$	Returns analog input data through the AI 0 front panel connector.
AI 0 Data N-1			
AI 0 Data N-2			
AI 0 Data N-3			
AI 0 Data N-4			
AI 0 Data N-5			
AI 0 Data N-6			
AI 0 Data N-7			
AI 0 Data N-8			
AI 0 Data N-9			
AI 0 Data N-10			
AI 0 Data N-11			
AI 0 Data N-12			

CLIP Signal Name	Direction	Data Type	Description
AI 0 Data N-13			
AI 0 Data N-14			
AI 0 Data N-15			
AI 1 Data N	From CLIP	fixed-point < $\pm 12,1$ >	Returns analog input data through the AI 1 front panel connector.
AI 1 Data N-1			
AI 1 Data N-2			
AI 1 Data N-3			
AI 1 Data N-4			
AI 1 Data N-5			
AI 1 Data N-6			
AI 1 Data N-7			
AI 1 Data N-8			
AI 1 Data N-9			
AI 1 Data N-10			
AI 1 Data N-11			
AI 1 Data N-12			
AI 1 Data N-13			
AI 1 Data N-14			
AI 1 Data N-15			
AO Ready for Input	From CLIP	Boolean	Indicates whether the AO link is ready for data.
AO 0 Data N	To CLIP	fixed-point < $\pm 12,1$ >	Sends analog output samples through the AO 0 front panel connector.
AO 0 Data N-1			
AO 0 Data N-2			
AO 0 Data N-3			
AO 0 Data N-4			
AO 0 Data N-5			
AO 0 Data N-6			
AO 0 Data N-7			
AO 0 Data N-8			
AO 0 Data N-9			

CLIP Signal Name	Direction	Data Type	Description
AO 0 Data N-10			
AO 0 Data N-11			
AO 0 Data N-12			
AO 0 Data N-13			
AO 0 Data N-14			
AO 0 Data N-15			
AO 1 Data N	To CLIP	fixed-point <±12,1>	Sends analog output samples through the AO 1 front panel connector.
AO 1 Data N-1			
AO 1 Data N-2			
AO 1 Data N-3			
AO 1 Data N-4			
AO 1 Data N-5			
AO 1 Data N-6			
AO 1 Data N-7			
AO 1 Data N-8			
AO 1 Data N-9			
AO 1 Data N-10			
AO 1 Data N-11			
AO 1 Data N-12			
AO 1 Data N-13			
AO 1 Data N-14			
AO 1 Data N-15			
IO Error	From CLIP	I32	Returns IO module errors, to be reported by the driver.
IO Ready	From CLIP	Boolean	Indicates successful configuration of the IO module devices with the current clocking mode settings.



## PXle-5763 Socketed CLIP Signals

The PXle-5763 CLIP provides access to four AC-coupled and DC-coupled 16-bit 500 MS/s analog input channels and eight bidirectional DIO channels.

CLIP Signal Name	Direction	Data Type	Description
Data Clock	From CLIP	Boolean	FPGA clock used to sample analog input data.
Data Clock 2x	From CLIP	Boolean	FPGA clock that samples analog input data at twice the rate of Data Clock.
AI 0 Data N	From CLIP	fixed-point $\langle \pm 16, 1 \rangle$	Returns analog input data through the AI 0 front panel connector. Each sample is a left-justified 16-bit data type.
AI 0 Data N-1			
AI 0 Data N-2			
AI 0 Data N-3			
AI 1 Data N	From CLIP	fixed-point $\langle \pm 16, 1 \rangle$	Returns analog input data through the AI 1 front panel connector. Each sample is a left-justified 16-bit data type.
AI 1 Data N-1			
AI 1 Data N-2			
AI 1 Data N-3			
AI 2 Data N	From CLIP	fixed-point $\langle \pm 16, 1 \rangle$	Returns analog input data through the AI 2 front panel connector. Each sample is a left-justified 16-bit data type.
AI 2 Data N-1			
AI 2 Data N-2			
AI 2 Data N-3			
AI 3 Data N	From CLIP	fixed-point $\langle \pm 16, 1 \rangle$	Returns analog input data through the AI 3 front panel connector. Each sample is a left-justified 16-bit data type.
AI 3 Data N-1			
AI 3 Data N-2			
AI 3 Data N-3			

## PXle-5764 Socketed CLIP Signals

The PXle-5764 CLIP provides access to four AC-coupled and DC-coupled 14-bit 1 GS/s analog input channels and eight bidirectional DIO channels.

CLIP Signal Name	Direction	Data Type	Description
Data Clock	From CLIP	Boolean	FPGA clock used to sample analog input data.
Data Clock 2x	From CLIP	Boolean	FPGA clock that samples analog input data at twice the rate of Data Clock.
AI 0 Data N	From CLIP	fixed-point <±16,1>	Returns analog input data through the AI 0 front panel connector. Each sample is a left-justified 16 data type.
AI 0 Data N-1			
AI 0 Data N-2			
AI 0 Data N-3			
AI 0 Data N-4			
AI 0 Data N-5			
AI 0 Data N-6			
AI 0 Data N-7			
AI 1 Data N	From CLIP	fixed-point <±16,1>	Returns analog input data through the AI 1 front panel connector. Each sample is a left-justified 16 data type.
AI 1 Data N-1			
AI 1 Data N-2			
AI 1 Data N-3			
AI 1 Data N-4			
AI 1 Data N-5			
AI 1 Data N-6			
AI 1 Data N-7			
AI 2 Data N	From CLIP	fixed-point <±16,1>	Returns analog input data through the AI 2 front panel connector. Each sample is a left-justified 16 data type.
AI 2 Data N-1			
AI 2 Data N-2			
AI 2 Data N-3			
AI 2 Data N-4			
AI 2 Data N-5			
AI 2 Data N-6			
AI 2 Data N-7			

CLIP Signal Name	Direction	Data Type	Description
AI 3 Data N	From CLIP	fixed-point <±16,1>	Returns analog input data through the AI 3 front panel connector. Each sample is a left-justified I16 data type
AI 3 Data N-1			
AI 3 Data N-2			
AI 3 Data N-3			
AI 3 Data N-4			
AI 3 Data N-5			
AI 3 Data N-6			
AI 3 Data N-7			

## PXIe-5775 Socketed CLIP Signals

The PXIe-5775 CLIP provides access to two AC-coupled 12-bit 3.2 GS/s analog input channels and eight bidirectional DIO channels.

CLIP Signal Name	Direction	Data Type	Description
Data Clock	From CLIP	Boolean	FPGA clock used to sample analog input data.
Data Clock 2x	From CLIP	Boolean	FPGA clock that samples analog input data at twice the rate of Data Clock.
AI Data Valid	From CLIP	Boolean	Indicates whether AI sample data is valid.
AI 0 Data N	From CLIP	fixed-point <±12,1>	Returns analog input data through the AI 0 front panel connector.
AI 0 Data N-1			
AI 0 Data N-2			
AI 0 Data N-3			
AI 0 Data N-4			
AI 0 Data N-5			
AI 0 Data N-6			
AI 0 Data N-7			
AI 0 Data N-8			
AI 0 Data N-9			

CLIP Signal Name	Direction	Data Type	Description
AI 0 Data N-10			
AI 0 Data N-11			
AI 0 Data N-12			
AI 0 Data N-13			
AI 0 Data N-14			
AI 0 Data N-15			
AI 1 Data N	From CLIP	fixed-point <±12,1>	Returns analog input data through the AI 1 front panel connector.
AI 1 Data N-1			
AI 1 Data N-2			
AI 1 Data N-3			
AI 1 Data N-4			
AI 1 Data N-5			
AI 1 Data N-6			
AI 1 Data N-7			
AI 1 Data N-8			
AI 1 Data N-9			
AI 1 Data N-10			
AI 1 Data N-11			
AI 1 Data N-12			
AI 1 Data N-13			
AI 1 Data N-14			
AI 1 Data N-15			
IO Error	From CLIP	I32	Returns IO module errors, to be reported by the driver.
IO Ready	From CLIP	Boolean	Indicates successful configuration of the IO module devices with the current clocking mode settings.

## Configuring the DIO Voltage

1. In the DIO Voltage Properties dialog box, select **General** from the Category list to display the DIO Voltage General Properties page.
2. Specify the DIO Voltage.



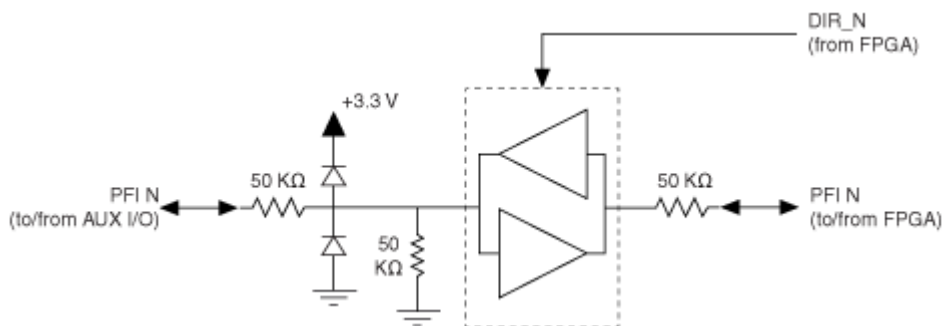
**Note** The default DIO Voltage is 3.3 V. To enable DIO voltage configuration through the DIO Voltage API property, select **Software Controlled**.

# FlexRIO Integrated I/O DIO Connector

The DIO front panel connector includes 8 general purpose digital lines and 4 MGT lanes. You can connect to these resources using a supported cable and accessory, such as the NI SCB-19 (NI part number 156053A-01). These signals are 3.3V LVCMOS bidirectional digital signals and may be used in a variety of applications. Direction is controlled independently for each channel through the LabVIEW FPGA Module diagram.

The PFI signals are connected to the FPGA through 3.3 V LVCMOS buffers. These buffers allow for direction control, isolation to protect the FPGA from overvoltage conditions, and excellent signal quality through the matched 50  $\Omega$  output impedance. For exact I/O levels and input and output impedances, refer to the device specifications.

The digital lines are protected against overvoltage conditions. The device provides this protection through a combination of diode clamps to the +3.3 V and GND lines and a positive temperature coefficient resistor for impedance matching.



**Note** The interface from the PFI LVCMOS buffer to and from the FPGA is bidirectional. To guarantee that this line is not double-driven by both the FPGA and the buffer at the same time, the FPGA implements a direction control latency. This latency is an explicit delay between enabling the FPGA I/O buffer and setting the direction of the PFI. For more information on direction control latency, refer to the device specifications.



**Note** The PXIe-7911 does not include a DIO front panel connector.

# FlexRIO MGT DIO General Properties Page

Enter a short description of your concept here (optional).

This socket connects the user diagram with the DIO MGTs, Reference Clocks, and support signals. Reference Clock IBUFGTs are already instantiated and should not be added in the CLIP.

This page includes the following components:

- Socketed Component-Level IP Declaration—Specifies the socketed CLIP to use. Socketed CLIP allows your IP to communicate with both the FPGA VI and the I/O module connector interface.



# Signal and Trigger Routing

Enter a short description of your concept here (optional).

FlexRIO devices with integrated I/O can send and receive signals through the front panel connectors and the PXI trigger bus. The front panel connectors provide connectivity for the input and output signals and for the control lines that send and receive clocks, triggers, and events. You can use the PXI trigger bus to send and receive events and triggers.

## PXI Trigger Lines

FlexRIO devices with integrated I/O support sharing signals with other devices via the PXI trigger bus. Host software connects a logical device terminal to a specific PXI Trigger line or to a terminal on another device. An FPGA I/O Node can then read or write the logical signal from the FPGA diagram. FlexRIO devices with integrated I/O provide 32 logical sources (Source0 through Source31) that can drive signals on the PXI trigger bus, and 32 logical destinations (Destination0 through Destination31) that can receive signals from the PXI trigger bus. Use FPGA I/O nodes to write to and read from these sources and destinations. These logical sources and destinations are not connected to the PXI trigger bus until host software creates an appropriate route. You can create a route by using [niFlexRIO\\_RouteSignal](#) or by providing a terminal name as a routing property.

## Terminal Names and Aliasing

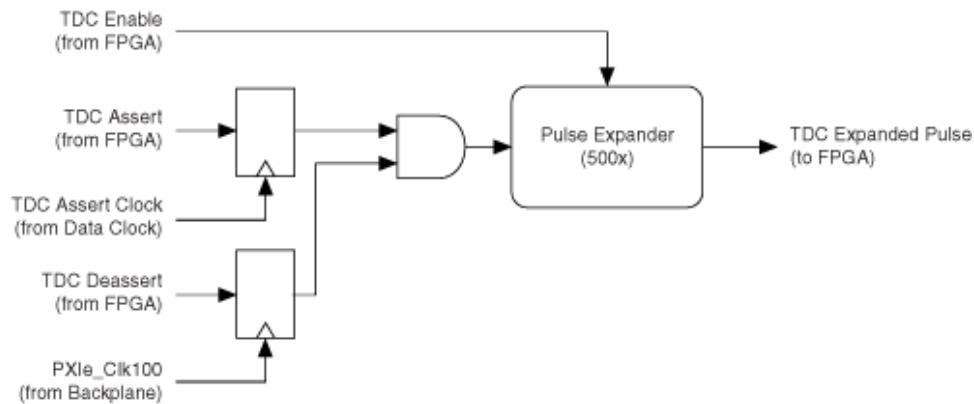
A terminal name is a unique identifier that refers to a physical terminal in your system. To guarantee the uniqueness of a terminal name across multiple devices, terminal names begin with a forward slash, followed by the name of the device as configured in MAX, such as Dev1. A forward slash and the name of the terminal, such as PFI1, follow the device identifier. For example, the fully qualified terminal name for PFI1 on Dev1 is /Dev1/PFI1.

Each of the routing matrix's 32 Source signals and 32 Destination signals can be assigned an alias by renaming the I/O item in the LabVIEW FPGA Project. These

aliases become valid terminal names once the bitfile has been opened on the device, and can be used wherever a terminal name is expected.

# Time-to-Digital Converter

The FlexRIO Integrated I/O devices have a Time-to-Digital Converter (TDC) subsystem that allows the device to measure time between an event asserted in the Sample Clock domain and an event asserted on the PXIe\_Clk100 domain. This measurement may be useful for evaluating the relative timing between synchronous events and is a useful component for multi-board synchronization. A functional illustration of the TDC is shown below.



# Viewing FPGA Target VI Dependencies

1. Right-click **Dependencies**.
2. Select **Refresh** from the shortcut menu.

Refer to Managing Dependencies in LabVIEW Projects in the **LabVIEW Help** for more information about using dependencies.

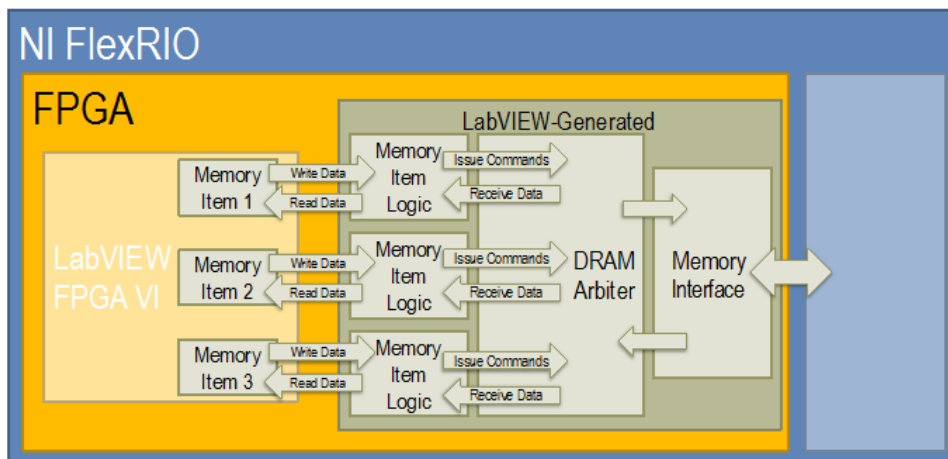
## Configuring DRAM with FPGA Memory Items

Use the FPGA memory item interface to use DRAM in the same way that you use block memory and look-up tables (LUT). DRAM memory items appear in the Project Explorer window under the FPGA target. The FPGA memory item interface allows you to partition the physical DRAM banks into multiple memory items. You can create target-scoped or VI-defined memory items.



**Note** A memory item targets a single DRAM bank. If you only select one memory item, this memory item can be as large as the entire bank. You can use memory items to divide the full DRAM space into smaller memories that you can access independently from different sections of the LabVIEW FPGA code.

Figure 2. DRAM Bank Access Logic Generated by LabVIEW

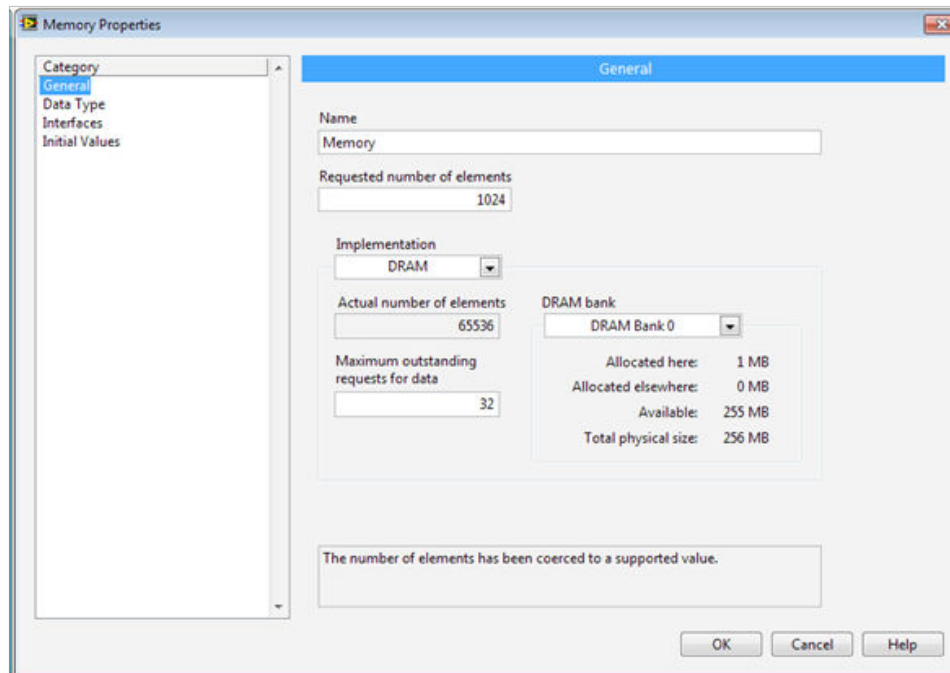


To configure DRAM with FPGA memory items, complete the following steps.

1. Determine whether you want to create a target-scoped memory item or a VI-defined memory item.
  - To create a target-scoped memory item, which you can access in the entire FPGA VI hierarchy, right-click the FPGA target in the Project Explorer window and select **New»Memory** from the shortcut menu. The Memory Properties dialog box appears.

- To create a VI-defined memory item, place a VI-defined Memory Configuration node on the block diagram, right-click the node, and select Configure from the shortcut menu. The Memory Properties dialog box appears.

Figure 3. Memory Properties Window



2. Configure the memory item in the Memory Properties dialog box. Click **OK**. The memory item is now populated in the Project Explorer window under the target.



**Note** If you use a Memory Method Node in a single-cycle Timed Loop, make sure the corresponding arbitration option is Arbitrate if Multiple Requestors Only or Never Arbitrate.

3. Use the memory item in an FPGA VI.