Manufacturer: National Instruments

Board Assembly Part Numbers (Refer to Procedure 1 for identification procedure):

Part Number and Revision	Description
146638A-01L or later	PXIE-5745, FLEXRIO SIGNAL GENERATOR, KU035 FPGA
146638A-02L or later	PXIE-5745, FLEXRIO SIGNAL GENERATOR, KU040 FPGA, 4 GB DRAM
146638A-03L or later	PXIE-5745, FLEXRIO SIGNAL GENERATOR, KU060 FPGA, 4 GB DRAM
146638A-04L or later	PXIE-5745, FLEXRIO SIGNAL GENERATOR W/AO FLTR, KU035 FPGA
146638A-05L or later	PXIE-5745, FLEXRIO SIGNAL GENERATOR W/AO FLTR, KU040 FPGA, 4 GB DRAM
146638A-06L or later	PXIE-5745, FLEXRIO SIGNAL GENERATOR W/AO FLTR, KU060 FPGA, 4 GB DRAM

Part Number and Revision	Description
146637A-01L or later	PXIE-5775, FLEXRIO DIGITIZER, KU035 FPGA
146637A-02L or later	PXIE-5775, FLEXRIO DIGITIZER, KU040 FPGA, 4GB DRAM
146637A-03L or later	PXIE-5775, FLEXRIO DIGITIZER, KU060 FPGA, 4GB DRAM

Part Number and Revision	Description
146636A-01L or later	PXIE-5785, FLEXRIO IF TRANSCEIVER, KU035 FPGA
146636A-02L or later	PXIE-5785, FLEXRIO IF TRANSCEIVER, KU040 FPGA, 4GB DRAM
146636A-03L or later	PXIE-5785, FLEXRIO IF TRANSCEIVER, KU060 FPGA, 4GB DRAM
146636A-04L or later	PXIE-5785, FLEXRIO IF TRANSCEIVER W/AO FLTR, KU035 FPGA
146636A-05L or later	PXIE-5785, FLEXRIO IF TRANSCEIVER W/AO FLTR, KU040 FPGA, 4GB DRAM
146636A-06L or later	PXIE-5785, FLEXRIO IF TRANSCEIVER W/AO FLTR, KU060 FPGA, 4GB DRAM

Volatile Memory

Target Data	*Type*	*Size*	*Battery Backup*	*User[1] Accessible*	*System Accessible*	*Sanitization Procedure*
Data storage (PN -02, -03, -05 and -06 only)	DRAM	4 GB	No	Yes	Yes	Cycle power
User FPGA bitstream storage	SDRAM	32 MB	No	Yes	Yes	Cycle power
User bitstream	FPGA	Xilinx KU035, KU040 or KU060	No	Yes	Yes	Cycle power

Non-Volatile Memory (*incl. Media Storage*)

Target Data	*Type*	*Size*	*Battery Backup*	*User Accessible*	*System Accessible*	*Sanitization Procedure*
Adapter module ID	EEPROM	32 KB	No	No	Yes	None
FPGA configuration logic	CPLD	Altera 10M04SAU169	No	No	Yes	None
User persistent FPGA Image	FLASH	64 MB	No	No	Yes	None

[1] Refer to *Terms and Definitions* section for clarification of *User* and *System Accessible*

Default persistent FPGA image	FLASH	64 MB	No	No	Yes	None
Golden FPGA image	FLASH	64 MB	No	No	Yes	None
Calibration constants	EEPROM	1 KB	No	Yes	Yes	Procedure 2

Procedures

Procedure 1 – Board Assembly Part Number identification:
To determine the Board Assembly Part Number and Revision, refer to the label applied to the surface of your product. The Assembly Part Number should be formatted as "P/N: 146636a-xxL", "P/N: 146637a-xxL", or "P/N: 146638a-xxL" where "a" is the letter revision of the assembly (e.g. A, B, C…) and "xx" describes the product version.

Procedure 2 – Calibration Constants EEPROM:
Requirements: LabVIEW 2018 or later and FlexRIO 18.7 or later

The calibration constants EEPROM can be cleared by using the FlexRIO API to overwrite the memory space with arbitrary values. To clear the storage through LabVIEW, complete the following steps:

1. Find and open the example LabVIEW Project "Read-Write Calibration Data" at "C:\<Program Files>\National Instruments\<LabVIEW>\examples\FlexRIO\System Calibration\" (replace <LabVIEW> with version of LabVIEW running on system).
    a. Alternatively, create a new VI and drop the "Write Calibration Data" VI from the FlexRIO API palette.
2. Select your FlexRIO device from **FPGA Resource** dropdown and set **Calibration Operation** to **Write**.
3. Run VI with **Calibration Data** set to 0, or other arbitrary value, to clear values in flash memory.
4. Repeat Step 3 for entire memory space to clear entire EEPROM memory. Set the **Read** option for the **Calibration Operation** to verify data has been cleared or to check sections of memory for other unintended values.

This memory space is also exposed to the C API. Use the following code as reference to clear it:

```
// Open session to the resource
niFlexRIO_OpenSession(resource, bitfile, 0, &session)
// Determine calibration storage size
niFlexRIO_GetAttributeInt32(session, NULL, kFlexRIO_CalibrationStorageSize, &size)
// Allocate byte buffer of zeros
zeros = calloc(size, 1);
// Write zeros to the device
niFlexRIO_WriteCalibrationData(session, 0, zeros, size)
```

Terms and Definitions

Cycle Power:
The process of completely removing power from the device and its components and allowing for adequate discharge. This process includes a complete shutdown of the PC and/or chassis containing the device; a reboot is not sufficient for the completion of this process.

Volatile Memory:
Requires power to maintain the stored information. When power is removed from this memory, its contents are lost. This type of memory typically contains application specific data such as capture waveforms.

Non-Volatile Memory:
Power is not required to maintain the stored information. Device retains its contents when power is removed. This type of memory typically contains information necessary to boot, configure, or calibrate the product or may include device power up states.

User Accessible:
The component is read and/or write addressable such that a user can store arbitrary information to the component from the host using a publicly distributed NI tool, such as a Driver API, the System Configuration API, or MAX.

System Accessible:
The component is read and/or write addressable from the host without the need to physically alter the product.

Clearing:
Per *NIST Special Publication 800-88 Revision 1*, "clearing" is a logical technique to sanitize data in all User Accessible storage locations for protection against simple non-invasive data recovery techniques using the same interface available to the user; typically applied through the standard read and write commands to the storage device.

Sanitization:
Per *NIST Special Publication 800-88 Revision 1*, "sanitization" is a process to render access to "Target Data" on the media infeasible for a given level of effort. In this document, clearing is the degree of sanitization described.