PXIe-6569

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Contents

PXIe-6569 Specifications

These specifications apply to the following variants of the PXIe-6569:

- PXIe-6569 with 32 LVDS Out, 32 LVDS In
- PXIe-6569 with 64 LVDS In
- PXIe-6569 with 64 LVDS Out

Note In this document, all variants are referred to inclusively as the PXIe-6569.

Definitions

Warranted specifications describe the performance of a model under stated operating conditions and are covered by the model warranty.

Characteristics describe values that are relevant to the use of the model under stated operating conditions but are not covered by the model warranty.

- **Typical** specifications describe the performance met by a majority of models.
- **Nominal** specifications describe an attribute that is based on design, conformance testing, or supplemental testing.
- **Measured** specifications describe the measured performance of a representative model.

Conditions

Specifications are valid under the following conditions unless otherwise noted.

- Ambient temperature of 0 °C to 55 °C
- Installed in chassis with slot cooling capacity ≥38 W

Digital I/O

Connector	SAMTEC SEARAY™

Table 1. Digital I/O Signal Characteristics

PXIe-6569 Variant	Signal	Type	Direction
32 LVDS Out, 32 LVDS In	PFI <0...7>	Single-ended	Bidirectional
	DIFF PFI +/- <0, 1>	Differential	Bidirectional
	DI +/- <0...31>	Differential	Input
	DO +/- <0...31>	Differential	Output
	GND	Ground	—
64 LVDS In	PFI <0...7>	Single-ended	Bidirectional
	DIFF PFI +/- <0, 1>	Differential	Bidirectional
	DI +/- <0...63>	Differential	Input
	GND	Ground	—
64 LVDS Out	PFI <0...7>	Single-ended	Bidirectional
	DIFF PFI +/- <0, 1>	Differential	Bidirectional
	DO +/- <0...63>	Differential	Output
	GND	Ground	—

Digital I/O PFI Channels

Part number for I/O PFI buffers	Texas Instruments, SN74AVC2T245
Number of channels	8
Signal type	Single-ended
Voltage families	3.3 V, 2.5 V, 1.8 V, 1.5 V, 1.2 V
Input impedance	50 kΩ

Output impedance	56 Ω
Direction control	Per pin
Minimum required direction change latency	13 ns

Table 2. Digital I/O PFI Characteristics

Voltage Family	V_{IL}	V_{IH}	V_{OL} (100µA load)	V_{OH} (100µA load)	Maximum DC Drive Strength	Digital Data Rate
3.3 V	0.8 V	2.0 V	0.2 V	3.0 V	24 mA	300 Mbps
2.5 V	0.7 V	1.6 V	0.2 V	2.2 V	18 mA	300 Mbps
1.8 V	0.62 V	1.29 V	0.2 V	1.5 V	16 mA	300 Mbps
1.5 V	0.51 V	1.07 V	0.2 V	1.2 V	12 mA	280 Mbps
1.2 V	0.42 V	0.87 V	0.2 V	0.9 V	6 mA	240 Mbps

LVDS Channels

Part number for LVDS buffers	Texas Instruments, DS25BR440
Input impedance	100 Ω
Output impedance	100 Ω
Onboard pulls	4.12 kΩ to 3.3 V on the inverted pins, and 2.32 kΩ to GND on the non-inverted pins
Maximum line rate	
LVDS lines	1.25 Gbps
DIFF PFI lines	300 Mbps

Bus Interface

Card edge form factor	PCI Express Gen-3 x8

Reconfigurable FPGA

PXIe-6569 modules are available with two FPGA options. The following table lists the FPGA specifications for the PXIe-6569 FPGA options.

Table 3. Reconfigurable FPGA Characteristics

FPGA Characteristics	KU035	KU060
LUTs	203,128	331,680
DSP48 slices (25 × 18 multiplier)	1,700	2,760
Embedded block RAM	19.0 Mb	38.0 Mb
Data transfers	DMA, interrupts, programmed I/O	
Default timebase	80 MHz	
Timebase reference sources	PXI Express 100 MHz (PXIe_CLK100)	
Number of DMA channels	60	

Note The Reconfigurable FPGA Characteristics table depicts the total number of FPGA resources available on the part. The number of resources available to the user is slightly lower, as some FPGA resources are consumed by board-interfacing IP for PCI Express, device configuration, and various board I/O. For more information, contact NI support.

Note For FPGA designs using the majority of KU035 or KU060 FPGA resources while running at high clock rates, the module may require more power than is available. If the module attempts to draw more than allowed per its specification, the module protects itself and reverts to a default FPGA personality. Refer to the getting started guide for your module or contact NI support for more information.

Onboard DRAM

Table 4. Onboard DRAM Specifications

DRAM Characteristics	KU035	KU060
Memory size	2 GB (2 banks of 1 GB)	4 GB (2 banks of 2 GB)
DRAM clock rate	1064 MHz	
Physical bus width	32 bit	
LabVIEW FPGA DRAM clock rate	267 MHz	
LabVIEW FPGA DRAM bus width	256 bit per bank	
Maximum theoretical data rate	17 GB/s (8.5 GB/s per bank)	

Environmental Characteristics

Temperature	
Operating	0 °C to 55 °C
Storage	-40 °C to 71 °C
Humidity	
Operating	10% to 90%, noncondensing
Storage	5% to 95%, noncondensing
Pollution Degree	2
Maximum altitude	2,000 m (800 mbar) (at 25 °C ambient temperature)
Shock and Vibration	
Operating vibration	5 Hz to 500 Hz, 0.3 g RMS
Non-operating vibration	5 Hz to 500 Hz, 2.4 g RMS

Operating shock	30 g, half-sine, 11 ms pulse

Maximum Power Requirements

Note Power requirements are dependent on the contents of the LabVIEW FPGA VI used in your application.

+3.3 V	2.0 A
+12 V	4.0 A
Maximum total power	58 W

Note For applications requiring >38 W, the PXIe-6569 must be installed in a ≥58 W-capable chassis.

Physical Characteristics

Dimensions	2.0 cm × 12.9 cm × 20.0 cm (0.8 in. × 5.1 in. × 7.9 in.)
Weight	495 g (17.5 oz)

CLOCK IN

Frequency	10 MHz
Signal type	LVDS

Table 5. Clock Configuration Options

Clock Configuration	Clocking IC	Clocking IC Resolution	Description
Si514	Si514	0.1 Hz	The internal Sample Clock is provided by the Si514. The Si514 clock cannot be locked to external references. The FlexRIO driver may limit the Si514 frequency range to be compatible with the CLIP in use.
Internal PXI_CLK10 + LMK04832	LMK04832	<10 kHz	The internal Sample Clock locks to the PXI 10 MHz Reference Clock, which is provided through the FPGA baseboard.
External Reference Clock Input + LMK04832	LMK04832	<10 kHz	The internal Sample Clock locks to the External 10 MHz Reference Clock, which is provided through the front panel connector.
External Sample/ Reference Clock Output	LMK04832	—	The External Sample/ Reference Clock Output is sourced by the LMK04832. The LMK04832 hardware architecture places restrictions on the relationship between the internal Sample Clock and the External Sample/ Reference Clock Output as these must be related through divisors available in the chip.

Clock Configuration	Clocking IC	Clocking IC Resolution	Description
			The FlexRIO driver manages checking this relationship.

NI-TClk

Note The NI-TClk synchronization method is only supported on output channels of the PXIe-6569.

You can use the NI-TClk synchronization method and the NI-TClk driver to align the Sample Clocks on any number of supported devices in one or more chassis. For more information about TClk synchronization, refer to the **NI-TClk Synchronization Help** within the **FlexRIO Help**. For other configurations, including multichassis systems, contact NI Technical Support at ni.com/support.

Intermodule Synchronization Using NI-TClk for Identical Modules

Note For more information about TClk synchronization, refer to the **NI-TClk Synchronization Help**, located in the **LabVIEW Help** at **LabVIEW Help** » **FPGA Module** » **FlexRIO Help** » **NI-TClk Synchronization Help**.

Synchronization specifications are valid under the following conditions:

- All modules are installed in one PXI Express chassis.
- The NI-TClk driver is used to align the Sample Clocks of each module.
- All parameters are set to identical values for each module.
- Modules are synchronized without using an external Sample Clock.
- The LMK04832 clocking IC is used as the clock source.
- The internal sample clock, sourced by the LMK04832, must be ≥30 MHz.

- NI-TClk synchronization can be used to align digital outputs across several PXIe-6569 modules with sample-level accuracy. The PXIe-6569 output delay adjustments can be used for fine-tuning the skew after TClk adjustment is complete. NI-TClk synchronization supports only PXIe-6569 digital outputs. Digital input channels are not supported.

Note Most, but not all, internal sample clock rates will work with TClk. TClk is available on a frequency within 50 kHz of all internal sample clock frequencies between 30 MHz and 156.25 MHz. The NI-TClk API will report whether the clock rate is valid.

Note These specifications apply only to synchronizing identical modules.

Skew	400 ps, peak-to-peak, measured
Transmit clock phase DAC adjustment resolution	0.7 ps

IO Delay Adjustment

IDELAY/ODELAY chain resolution	2.5 ps to 15 ps
IDELAY/ODELAY minimum guaranteed span	1.25 ns