

Calibration Procedure

PXIe-6571

8-Channel

July 2025

379117A-01

Instructions on how to complete the performance verification and adjustment of your instrument.

This document contains the verification and adjustment procedures for the NI PXIe-6571 (8-channel) 100MVector/s PXI digital pattern instrument with PPMU. Use the procedures in this document to automate calibration or to conduct manual calibration. Review and become familiar with the entire procedure before beginning the calibration process.



Note

Refer to the *Revision History* section of this document for updates since the previous revision of this document.

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1. Terms and Definitions

DUT DUT is an acronym for Device Under Test and refers to the NI product being calibrated. For this procedure, DUT refers to the NI PXIe-6571 (8-channel).

As-Found Limits These limits are derived from the published specifications for the DUT. NI uses these limits to determine if the DUT is performing within the recommended calibration interval specifications at the time of calibration and before any adjustment is performed.

As-Left Limits	These limits are derived from the published specifications for the DUT minus guardband to ensure a high probability that the DUT will meet its specifications over the next recommended calibration interval.
Functional Test	Functional Tests determine whether the DUT is operating correctly. Functional tests are not directly related to performance specifications.
Verification	Verification evaluates the measured calibration results against the defined As-Found Limits. The result of the evaluation is expressed as a Pass/Fail condition in the calibration certificate using an established evaluation formula.
Adjustment	Adjustment performs a set of operations on the DUT to optimize the measurement performance and conform it to the assigned calibrated values.
Reverification	Reverification evaluates the measured calibration results against the As-Left limits after adjustment. The As-Left limits may be tighter than the As-Found limits.
Recommended Calibration Interval	This interval indicates the recommended period between each round of verification and adjustment of the DUT. There is a high probability that, within this interval, the DUT will remain within the published warranted performance specifications. Some measurement DUTs have warranted specifications for different calibration intervals, for example: 24 hours, 90 days, 1 year, and 2 years. In this case, the specification depends on the calibration cycle chosen by the user.

2. Calibration Overview

Recommended Calibration Interval

1 year

Password

NATI



Note

This is the default password for all password-protected operations. This password is site-specific.

Task	Estimated Test Time	Operator Connections	Test Points
Setup	20 minutes	—	—
Warm Up	30 minutes	—	—
Verify, Adjust, and Reverify	155 minutes	18	18
Verify Only	40 minutes	6	6
Adjust Only	75 minutes	6	6



Note
This DUT requires special considerations when calculating the total warm up time for the system. Refer to the Warm Up section in this document for more information.



Note
Estimated test times assume the user is conducting a manual calibration. For most procedures, automating the calibration significantly reduces test times.

Environmental Conditions	Verification	Adjustment
Ambient temperature	23 °C ± 5 °C	23 °C ± 1 °C
Internal DUT temperature range ¹	Tcal ± 1 °C	Tcal ± 1 °C
Relative humidity	Between 10% and 80%, noncondensing	

¹ The internal temperature of the DUT is greater than the ambient temperature.

2.1. Calibration Condition Guidelines

- Keep cabling as short as possible. Long cables act as antennas, picking up extra noise that can affect measurements.
- Verify that all connections to the DUT are secure, including front panel connections and screws, are secure.
- Use shielded VHDCI cable when connecting to the DUT front panel. Use twisted pair copper cabling for connecting between SCB-68 HSDIO and TB-2636. Use twisted pair copper cabling for connecting between the TB-2636 and the SMU / DMM.
- Allow adequate warm up time for all components of the calibration system.
- Make all connections as shown in diagrams.
- Use shielded copper wire for all cable connections to the DUT.
- Use twisted-pair wires to eliminate noise and thermal offsets.

Ensure that the PXI/PXI Express chassis fan speed is set to HIGH, that the fan filters (if present) are clean, and that the empty slots contain filler panels. For more information, refer to the Maintain Forced-Air Cooling Note to Users document available at ni.com/manuals.

- If a DUT fails reverification after adjustment, ensure that the Test Conditions have been met before returning the DUT to NI.

3. Calibration Resources

3.1. Required Software

**Note**

Ensure that the most recent version of the required driver software is installed before conducting the calibration.

Install the following software on the calibration system:

- LabVIEW version 2022 SPI Base/Full/Pro or later
- NI-Digital Pattern Driver version 2024 Q3 or greater

3.2. Recommended Documentation

Go to ni.com/docs to locate the following documentation for more information when performing this calibration:

- PXIe-6571 Specifications
- PXIe-6571 User Manual
- PXIe-6571 Getting Started Guide

3.3. Test Equipment

This section details the equipment NI recommends for each test performed as part of this calibration procedure.



NI Calibration Executive Users

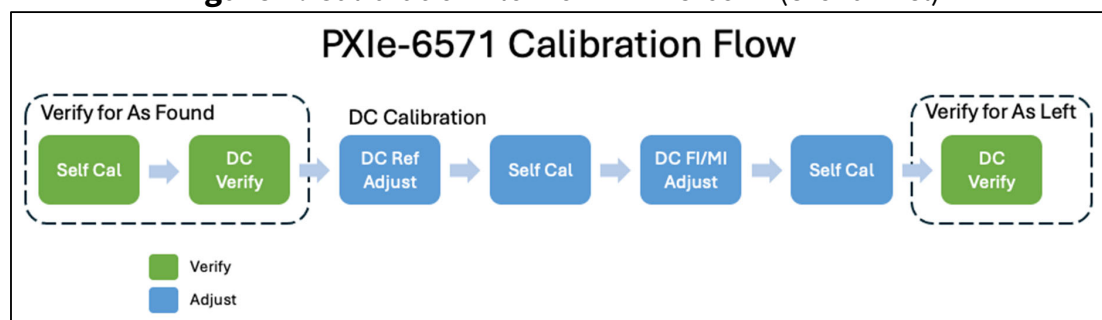
Refer to the Calibration Executive Help to find an updated list of test equipment for this calibration procedure.

Standard	Recommended Model	Where Used	Functional Requirement(s)
Digital Multimeter (DMM)	PXI-4081	DC Verification DC Adjustment	DC Voltage
Source Measurement Unit (SMU)	PXIe-4143	DC Verification DC Adjustment	DC Current Source and Sink DC Voltage
DC Switch Matrix	PXIe-2529	DC Verification DC Adjustment	Enough columns to contain 32 PXIe-6571 channels. (Enough rows to contain 3 instrumentation channels)
Shielded Single-ended Cable	NI SHC68-C68- D4L	DC Verification DC Adjustment	Shielded 50 Ω coaxial cable (68-pin VHDCI connector)
DC Test Fixture for NI PXIe-6570/1	NI PN: 790411 -01	DC Verification DC Adjustment	Test fixture interface for 6571 channels and DMM, SMU. (Test fixture includes TB-2636)
58W Cooling PXI Chassis	PXIe-1095	DC Verification DC Adjustment	PXIe-6571 (8-channel) requires a PXI chassis capable of 58 W of power and cooling

3.4. Calibration Summary

Figure 1 shows the recommended sequence for calibration of the PXIe-6571 (8-channel) module. This sequence is followed by the NI Calibration Executive routine. Using this sequence minimizes the number of cable-swaps needed during the calibration procedure.

Figure 1. Calibration Flow of NI PXIe-6571 (8-channel)



4. Warm Up the DUT

Warm up time starts after the installed DUT is powered on in the chassis. Warm up time resets after the DUT is removed from the chassis. This DUT requires 30 minutes to warm up prior to conducting any tests.



Note

Observe adequate Warm up time for all components of the calibration system.

4.1. Perform Self-Calibration

Self-calibration should be performed after the DUT has warmed up for the recommended time period. This function measures the onboard references of the DUT and adjusts the self-calibration constants to account for any errors caused by short-term fluctuations in the environment.

If cables remain connected during self-calibration, ensure there are no fast-transient signals such as digital drivers, frequency generators, or noise sources driving into the digital pattern instrument.



Note

NI recommends disconnecting all external signals before beginning self-calibration.

Complete the following steps to conduct self-calibration using Measurement & Automation Explorer (MAX).

1. Wait for DUT to be fully warmed up.
2. Launch MAX.
3. Select **My System»Devices and Interfaces» NI PXIe-6571 (8CH)**.
4. Start self-calibration using one of the following methods:

5. Click **Self-Calibrate** in the upper right corner of MAX.
6. Right-click the name of the DUT in the MAX configuration tree and select **Self-Calibrate** from the drop-down menu.

Complete the following steps to conduct self-calibration using LabVIEW programming environment.

1. Wait for DUT to be fully warmed up.
2. Initialize a session.
3. Call the **niDigital Self Calibrate** function.
4. Close the session.

5. Perform Verification

5.1. Digital Pins Definitions

- V_{IH} – Specifies the voltage that the instrument applies to the input of the DUT when the instrument drives a logic high (1).
- V_{IL} – Specifies the voltage that the instrument applies to the input of the DUT when the instrument drives a logic low (0).
- V_{OH} – Specifies the DUT output voltage above which the comparator on the instrument pin interprets a logic high (H).
- V_{OL} – Specifies the DUT output voltage below which the comparator on the instrument pin interprets a logic low (L).
- V_{TERM} – Specifies the termination voltage the instrument applies during non-drive cycles when the termination mode is set VTERM. The instrument applies the termination voltage through a 50 Ω parallel termination resistance.

5.2. Driver Voltage Level Accuracy Verification

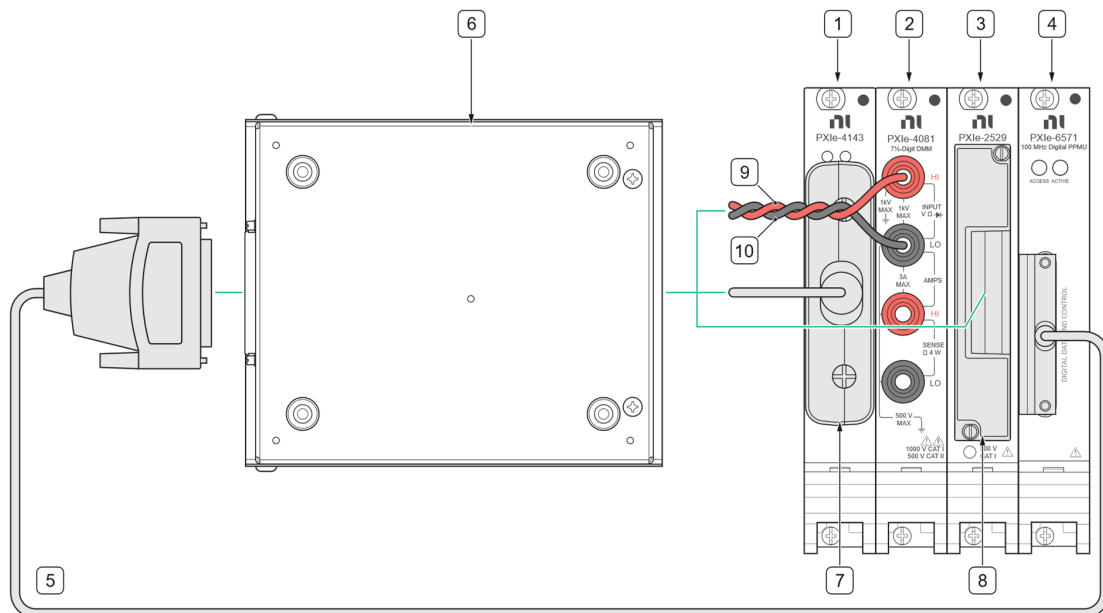
5.2.1. Verification Test Limits

Table 1: Driver Voltage Accuracy Verification Test Limits

Voltage Level Range	Test Voltage	DC Voltage Measurement	As-Found Test Limit	
			Lower Limit	Upper Limit
– 2 V to 6 V	– 2 V	Voltage Input Level High (V_{IH})	– 15 mV	15 mV
	– 0.857 V		– 15 mV	15 mV
	2.571 V		– 15 mV	15 mV
	6 V		– 15 mV	15 mV
– 2 V to 6 V	– 2 V	Voltage Input Level Low (V_{IL})	– 15 mV	15 mV
	– 0.857 V		– 15 mV	15 mV
	2.571 V		– 15 mV	15 mV
	6 V		– 15 mV	15 mV
– 2 V to 6 V	– 2 V	Termination Voltage (V_{TERM})	– 15 mV	15 mV
	– 0.857 V		– 15 mV	15 mV
	2.571 V		– 15 mV	15 mV
	6 V		– 15 mV	15 mV

5.2.2. Initial Test Connection

Figure 2. Initial Connection for Driver Voltage Accuracy Verification Procedure



- | | |
|-------------------------|----------------------------------|
| 1. SMU | 6. SCB-68 Terminal Block |
| 2. DMM | 7. PXIe-414x Terminal Block |
| 3. Switch Module | 8. TB-2636 Terminal Block |
| 4. DUT | 9. Red Banana Cable to DMM HI |
| 5. VHDCI-to-VHDCI Cable | 10. Black Banana Cable to DMM LO |

5.2.3. Verification Procedure

1. Initialize a session and reset the device.
2. Configure the DMM according to the following settings:
 - a. Function: **DC Volts**
 - b. Range: **10 V**
 - c. Digits of resolution: **6 ½ Digits**
 - d. Input Impedance: **10 MΩ**
 - e. Power line Frequency: **50 Hz or 60 Hz**, depending on your country

Repeat 8 times, once for each DUT channel.

3. Connect channel to be measured of the DUT to the DMM through the switch matrix.
 - a. Increment and iterate through all channels of DUT from 0 to 7.
4. Set DUT channel to be measured to **Digital**.

Repeat 4 times, once for each test voltage.

5. Set DUT to correct test voltage. Starting with the lowest test voltage and incrementing voltage value per iteration of loop. Refer to **Table 1**.

Repeat 3 times, once for each measurement type (V_{IH} , V_{IL} , and V_{TERM}).

6. Set DUT to correct state depending on measurement type:
 - a. To verify V_{IH} : Set the DUT **state** to '1'. Refer to **Table 1**.
 - b. To verify V_{IL} : Set the DUT **state** to '0'. Refer to **Table 1**.
 - c. To verify V_{TERM} :
 1. Set DUT termination mode to V_{TERM} .
 2. Set the DUT **state** to 'X'. Refer to **Table 1**.
7. Commit changes to DUT.
8. Wait 4 ms for the output to settle, and measure the voltage on channel 0 of the DUT using the DMM.
9. Record the output voltage measurement and calculate the error value to be compared against the limits in **Table 1**.

$$V_{error} = V_{setpoint} - V_{measured}$$

10. Disconnect the DUT from the DMM using the switch matrix.
11. Close the session to the DUT.

5.3. Comparator Voltage Level Accuracy Verification

The Driver Voltage Level accuracy test will determine the DC accuracy of the internal comparator thresholds used to acquire digital data on the D_{OUT} pin. There are two comparators internal to the pin electronics channel, V_{OH} and V_{OL} . Both comparators must be tested to ensure both meet their DC accuracy specifications.

The internal voltage thresholds used by the comparators can't be measured directly, since there is no way to export them from the pin electronics chip without adding a significant amount of error. The thresholds can be tested by providing a stimulus voltage into each comparator, then seeing if the comparator returns a high or low comparison. For instance, if a low voltage was applied and the comparator returned "LOW", then the voltage threshold is above the applied voltage stimulus. If a high voltage was applied and the comparator returned "HIGH", the voltage threshold is below the applied voltage stimulus. By providing a wide sweep of stimulus voltages, the exact voltage threshold that defines the boundary between "LOW" and "HIGH" comparisons can be defined allowing the stimulus voltage to be measured instead of having to directly measure the threshold voltage.

The noise on the comparator voltage threshold can be determined, when the correct stimulus voltage is applied to find the threshold. Noise on the threshold and stimulus voltage will cause a random distribution of "HIGH" and "LOW" comparisons. The comparator threshold voltage will be bounded by two measurements, an upper bound and a lower bound for each threshold. These bounds are effectively the DC comparator threshold voltage plus any additional noise/repeatability in the test setup. The lower bound defines the point at which the comparator transitions from always returning "LOW" comparisons to returning at least one "HIGH" comparison. The upper bound defines the point at which the comparator transitions from returning at least one "LOW" comparison to always returning "HIGH" comparisons. To determine the worst case threshold accuracy, the worse of the two bounding measurements is taken as the

comparator voltage threshold accuracy to be compared against the specifications.

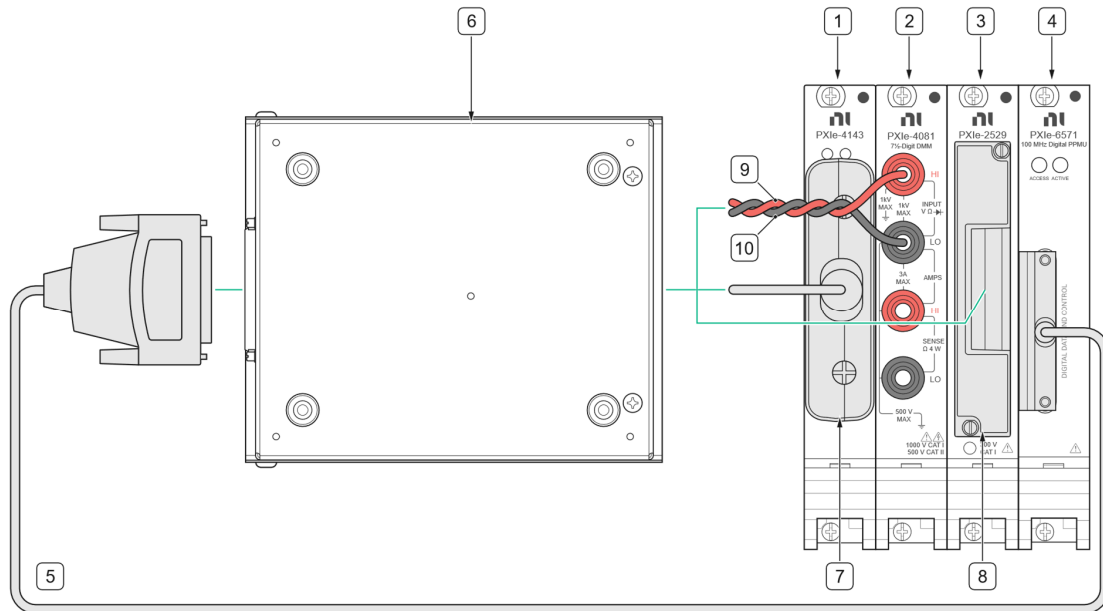
5.3.1. Verification Test Limits

Table 2: Comparator Threshold Accuracy Verification Test Limits

Voltage Level Range	Test Voltage	DC Voltage Measurement	As-Found Test Limit	
			Lower Limit	Upper Limit
– 2 V to 6 V	– 1.5 V	Voltage Output Level High (V _{OH})	– 25 mV	25 mV
	0.1 V		– 25 mV	25 mV
	3.9 V		– 25 mV	25 mV
	5.8 V		– 25 mV	25 mV
– 2 V to 6 V	– 1.5 V	Voltage Output Level Low (V _{OL})	– 25 mV	25 mV
	0.1 V		– 25 mV	25 mV
	3.9 V		– 25 mV	25 mV
	5.8 V		– 25 mV	25 mV

5.3.2. Test Connection

Figure 3. Initial Connection for Comparator Voltage Level Accuracy Verification Procedure



- | | |
|-------------------------|----------------------------------|
| 1. SMU | 6. SCB-68 Terminal Block |
| 2. DMM | 7. PXIe-414x Terminal Block |
| 3. Switch Module | 8. TB-2636 Terminal Block |
| 4. DUT | 9. Red Banana Cable to DMM HI |
| 5. VHDCI-to-VHDCI Cable | 10. Black Banana Cable to DMM LO |

5.3.3. Verification Procedure

1. Initialize a session and reset the device.
2. Configure the DMM according to the following settings:
 - a. Function: **DC Volts**
 - b. Range: **10 V**
 - c. Digits of resolution: **6 ½ Digits**

- d. Input Impedance: **10 M Ω**
- e. Power line Frequency: **50 Hz or 60 Hz**, depending on your country
3. Disconnect all channels of DUT from the DMM using the switch matrix.

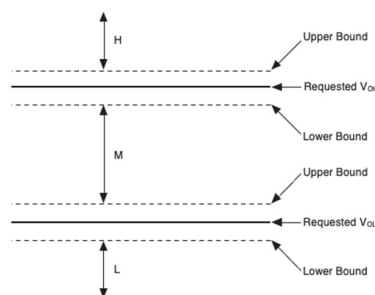
Repeat 8 times, once for each DUT channel.

4. Disconnect channel to be measured of the DUT to the DMM through the switch matrix.
 - a. Increment and iterate through all channels of DUT from 0 to 7.
5. Set DUT channel to be measured to **Digital**.

Repeat 4 times, once for each test voltage.

6. Set DUT to correct test voltage. Starting with the lowest test voltage and incrementing per iteration of loop. Refer to **Table 2**.
7. Set DUT digital voltage levels, refer to **Figure 4**.
 - a. V_{OL} to the test voltage. Refer to **Table 2**.
 - b. V_{OH} to the range maximum of **6 V**.
 - c. V_{IH} **0.1 V** lower than the test voltage.

Figure 4. Digital Voltage Levels



8. Commit the changes.
9. Write a static '**1**' to the channel being tested.
10. Wait 2 ms.

Repeat 11 times, changing the step size by $\frac{1}{2}$ each time.

11. Each value of loop will decrease the step size of how V_{OL} is modified. (0.2 V, 0.1 V, 0.05 V, etc.)

Repeat up to 50 times, until 'M' is returned.

12. Read static channel information.
13. Store all the data returned to be analyzed outside of loop.
14. Determine step size value of V_{OL} .
 - a. If 'M' is not returned by any of the samples in the array, increase the value of V_{OL} by loop step size value starting with 0.2 V.
 - b. If 'M' is returned by any of the samples in the array, decrease the value of V_{OL} by loop step size value starting with 0.2 V.
15. Set DUT channel's new value for V_{OL} .
16. Commit changes.
17. Connect DUT channel to DMM using switch matrix.
18. Wait 2 ms.
19. Using the DMM, measure the lower boundary voltage for V_{OL} .
20. Disconnect the DUT channel from the DMM using the switch matrix.
21. Set the V_{IH} to 0.1 V higher than the test voltage. Refer to **Figure 4** and **Table 2**.
22. Write a static '1' to the channel being tested.
23. Commit the changes.
24. Wait 2 ms.

Repeat 11 times, changing the step size by $\frac{1}{2}$ each time.

25. Each value of loop will decrease the step size of how V_{IH} is modified. (0.2 V, 0.1 V, 0.05 V, etc.)

Repeat 50 times.

26. Read static channel information.
27. Store all the data returned to be analyzed outside of loop.
28. Determine step size value of V_{OL} .
 - a. If only 'M' is returned by any of the samples in the array, decrease the value of V_{OL} by loop step size value starting with 0.2 V.
 - b. If 'M' is returned by any of the samples in the array, increase the value of V_{OL} by loop step size value starting with 0.2 V.
29. Set DUT channel's new value for V_{OL} .
30. Commit changes.
31. Connect DUT channel to DMM using switch matrix.
32. Wait 2 ms.
33. Using the DMM, measure the upper boundary voltage for V_{OL} .
34. Disconnect the DUT channel from the DMM using the switch matrix.
35. Set DUT digital voltage levels, refer to **Figure 4**.
 - a. V_{OL} to the range minimum of **-2 V**.
 - b. V_{OH} to the test voltage. Refer to **Table 2**.
 - c. V_{IH} **0.1 V** lower than the test voltage.
36. Commit the changes.
37. Write a static '1' to the channel being tested.
38. Wait 2 ms.

Repeat 11 times, changing the step size by $\frac{1}{2}$ each time.

39. Each value of loop will decrease the step size of how V_{OL} is modified. (0.2 V, 0.1 V, 0.05 V, etc.)

Repeat 50 times.

40. Read static channel information.
41. Store all the data returned to be analyzed outside of loop.
42. Determine step size value of V_{OH} .
 - a. If 'H' is not returned by any of the samples in the array, increase the value of V_{OH} by loop step size value starting with 0.2 V.
 - b. If 'H' is returned by any of the samples in the array, decrease the value of V_{OH} by loop step size value starting with 0.2 V.
43. Set DUT channel's new value for V_{OH} .
44. Commit changes.
45. Connect DUT channel to DMM using switch matrix.
46. Wait 2 ms.
47. Using the DMM, measure the lower boundary voltage for V_{OH} .
48. Disconnect the DUT channel from the DMM using the switch matrix.
49. Set the V_{IH} to 0.1 V higher than the test voltage. Refer to **Figure 4** and **Table 2**.
50. Write a static '**1**' to the channel being tested.
51. Commit the changes.
52. Wait 2 ms.

Repeat 11 times, changing the step size by $\frac{1}{2}$ each time.

53. Each value of loop will decrease the step size of how V_{IH} is modified. (0.2 V, 0.1 V, 0.05 V, etc.)
- Repeat 50 times.
54. Read static channel information.
55. Store all the data returned to be analyzed outside of loop.
56. Determine step size value of V_{OH} .
 - a. If only 'H' is returned by any of the samples in the array, decrease the value of V_{OH} by loop step size value starting with 0.2 V.
 - b. If 'H' is returned by any of the samples in the array, increase the value of V_{OH} by loop step size value starting with 0.2 V.
57. Set DUT channel's new value for V_{IH} .
58. Commit changes.
59. Connect DUT channel to DMM using switch matrix.
60. Wait 2 ms.
61. Using the DMM, measure the upper boundary voltage for V_{OH} .
62. Disconnect channel to be measured of the DUT to the DMM through the switch matrix.
63. Compare V_{OL} and V_{OH} upper as well as lower bounds against limits in **Table 2** for each test voltage.
64. Close the session to the DUT.

5.4. Force Voltage Accuracy and Measure Voltage Accuracy Verification

5.4.1. Verification Test Limits

Table 3: Force Voltage Accuracy and Measure Voltage Accuracy Verification Test Limits

Voltage Level Range	Test Voltage	DC Voltage Measurement	As-Found Test Limit	
			Lower Limit	Upper Limit
– 2 V to 6 V	– 2 V	PPMU Force	– 15 mV	15 mV
	– 0.857 V		– 15 mV	15 mV
	4.857 V		– 15 mV	15 mV
	6 V		– 15 mV	15 mV
– 2 V to 6 V	– 2 V	PPMU Measure	– 5 mV	5 mV
	– 0.857 V		– 5 mV	5 mV
	4.857 V		– 5 mV	5 mV
	6 V		– 5 mV	5 mV

- d. Input Impedance: **10 MΩ**
- e. Power line Frequency: **50 Hz or 60 Hz**, depending on your country

Repeat 8 times, once for each DUT channel.

3. Connect channel to be measured of the DUT to the DMM through the switch matrix.
 - a. Increment and iterate through all channels of DUT from 0 to 7.
4. Set DUT channel to be measured to **PPMU**.

Repeat 4 times, once for each test voltage.

5. Set DUT channel with the following PPMU settings:
 - a. Set current limit range to **32 mA**.
 - b. Set output function to **DC Voltage**.
 - c. Configure the voltage to the correct test voltage. Starting with the lowest test voltage and incrementing voltage value per iteration of loop. Refer to **Table 3**.
6. Commit changes to DUT.
7. Source PPMU.
8. Wait 4 ms for the output to settle and measure the voltage on channel 0 of the DUT using the DMM.
9. Calculate the force voltage error by comparing the test voltage ideal value against the DMM measurement, then compare against the limits in **Table 3**.
 - a. $V_{PPMU_force_error} = V_{DMM_Measure} - V_{Ideal_Test_Voltage}$
10. Set the PPMU Aperture time to **1/60 second** for 60 Hz PLC or **1/50 second** for 50 Hz PLC.

11. Measure the PPMU from the DUT and calculate the voltage error using the measurement from the DMM, then compare against the limits in **Table 3**.
 - a. $V_{PPMU_Measure_error} = V_{DMM_Measure} - V_{DUT_Measure}$
12. Disconnect the DUT from the DMM using the switch matrix.
13. Close the session to the DUT.

5.5. Force Current Accuracy and Measure Current Accuracy (Zone 1) Verification

5.5.1. Verification Test Limits

Table 4: Force Current Accuracy and Measure Current Accuracy (Zone 1) Verification Test Limits

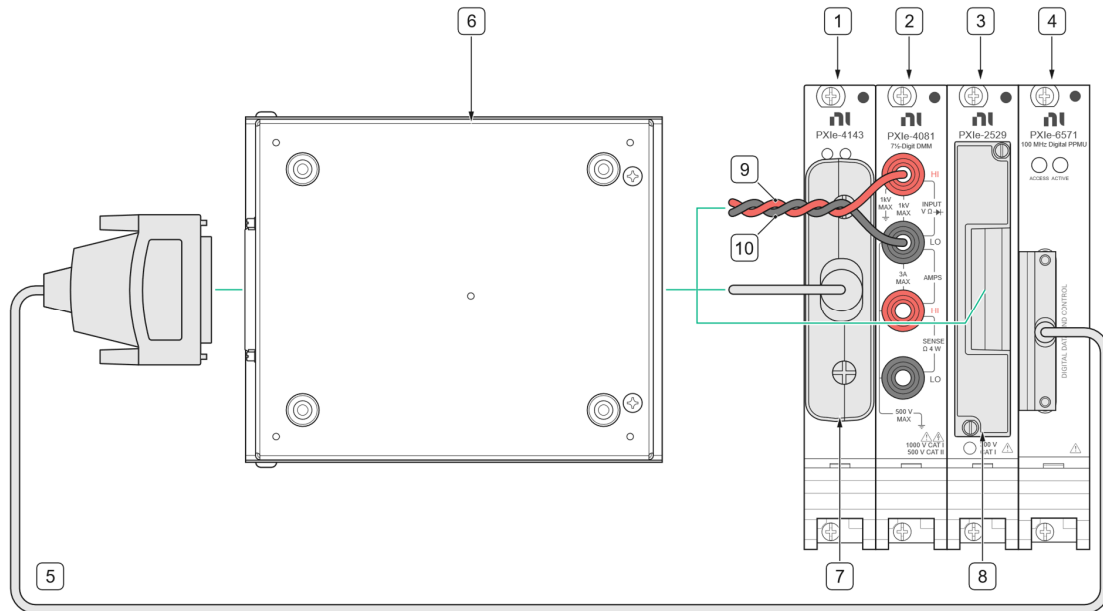
PPMU Current	PPMU Current Range	SMU Test Voltage	PPMU Function	As-Found Test Limit	
				Lower Limit	Upper Limit
32 mA	-100% of current range	5 V	Force Current	- 1%	1%
	100% of current range	5 V		- 1%	1%
	-30% of current range	-1 V		- 1%	1%
	-100% of current range	1.25 V		- 1%	1%
	100% of current range	-1 V		- 1%	1%
2 mA	-100% of current range	5 V	Force Current	- 1%	1%
	100% of current range	5 V		- 1%	1%
	-30% of current range	-1 V		- 1%	1%
	-100% of current range	1.25 V		- 1%	1%
	100% of current range	-1 V		- 1%	1%

128 μ A	-100% of current range	5 V	Force Current	- 1%	1%
	100% of current range	5 V		- 1%	1%
	-30% of current range	-1 V		- 1%	1%
	-100% of current range	1.25 V		- 1%	1%
	100% of current range	-1 V		- 1%	1%
32 μ A	-100% of current range	5 V	Force Current	- 1%	1%
	100% of current range	5 V		- 1%	1%
	-30% of current range	-1 V		- 1%	1%
	-100% of current range	1.25 V		- 1%	1%
	100% of current range	-1 V		- 1%	1%
2 μ A	-100% of current range	5 V	Force Current	- 1%	1%
	100% of current range	5 V		- 1%	1%
	-30% of current range	-1 V		- 1%	1%
	-100% of current range	1.25 V		- 1%	1%
	100% of current range	-1 V		- 1%	1%
32 mA	-100% of current range	5 V	Measure Current	- 1%	1%
	100% of current range	5 V		- 1%	1%
	-30% of current range	-1 V		- 1%	1%
	-100% of current range	1.25 V		- 1%	1%
	100% of current range	-1 V		- 1%	1%
2 mA	-100% of current range	5 V	Measure Current	- 1%	1%
	100% of current range	5 V		- 1%	1%
	-30% of current range	-1 V		- 1%	1%
	-100% of current range	1.25 V		- 1%	1%
	100% of current range	-1 V		- 1%	1%
	-100% of current range	5 V		- 1%	1%

128 μ A	100% of current range	5 V	Measure Current	– 1%	1%
	-30% of current range	-1 V		– 1%	1%
	-100% of current range	1.25 V		– 1%	1%
	100% of current range	-1 V		– 1%	1%
32 μ A	-100% of current range	5 V	Measure Current	– 1%	1%
	100% of current range	5 V		– 1%	1%
	-30% of current range	-1 V		– 1%	1%
	-100% of current range	1.25 V		– 1%	1%
	100% of current range	-1 V		– 1%	1%
2 μ A	-100% of current range	5 V	Measure Current	– 1%	1%
	100% of current range	5 V		– 1%	1%
	-30% of current range	-1 V		– 1%	1%
	-100% of current range	1.25 V		– 1%	1%
	100% of current range	-1 V		– 1%	1%

5.5.2. Initial Test Connection

Figure 6. Initial Connection for Force Current Accuracy and Measure Current Accuracy (Zone 1) Verification Procedure



- | | |
|-------------------------|----------------------------------|
| 1. SMU | 6. SCB-68 Terminal Block |
| 2. DMM | 7. PXIe-414x Terminal Block |
| 3. Switch Module | 8. TB-2636 Terminal Block |
| 4. DUT | 9. Red Banana Cable to DMM HI |
| 5. VHDCI-to-VHDCI Cable | 10. Black Banana Cable to DMM LO |

5.5.3. Verification Procedure

1. Initialize a session and reset the device.
2. Configure the SMU according to the following settings:
 - a. Source mode: **Single Point**
 - b. Output function: **DC Voltage**
 - c. Sense: **Local**

- d. Voltage range: **10 V**
- e. Aperture time: **1 PLC**
- f. Power line Frequency: **50 Hz or 60 Hz**, depending on your country
- g. Current limit auto range: **Off**
3. Configure the DUT to source current according to the following settings:
 - a. Upper voltage limit: **6 V**
 - b. Lower voltage limit: **-2 V**
 - c. Select function: **PPMU**
 - d. Aperture time: **16.667 ms** (60 Hz) or **20 ms** (50 Hz), depending on your country

Repeat 8 times, once for each DUT channel.

4. Connect channel to be measured of the DUT to the SMU through the switch matrix.
 - a. Increment and iterate through all channels of DUT from 0 to 7.

Repeat 4 times, once for each SMU Test Voltage.

5. Set DUT PPMU settings according to **Table 4**.
 - a. **Current Level**
 - b. **Current Range**
6. Set the current limit range and current limit of the SMU to the appropriate value for current being measured. The SMU current limit must always be at least 10% larger than the PPMU current range being tested.

7. Set the voltage level of the SMU to the correct output voltage. Starting with the lowest test voltage and incrementing voltage value per iteration of loop. Refer to **Table 4**.
8. Enable SMU output and initiate SMU generation.
9. Set DUT PPMU to source test current.
10. Wait 30 ms for SMU, cabling, and DUT to settle.
11. Measure current using the SMU and store value. Negate measurement to make the measurement related to if PPMU sinking or sourcing. When the SMU is sinking, the PPMU is sourcing, and vice versa.
12. Measure current using PPMU and store value.
13. Calculate the force current error, then compare against the limits in **Table 4**.
 - a.
$$Force_{Current_error} = \frac{100 * (SMU_{measurement} - SMU_{Test_Point})}{Current_{Range}}$$
14. Calculate the measure current error, then compare against the limits in **Table 4**.
 - a.
$$Measure_{Current_error} = \frac{100 * (PPMU_{measurement} - SMU_{measurement})}{Current_{Range}}$$
15. Set DUT channel to **Disconnect** state.
16. Abort the SMU voltage source and set to **0 V**. This prevents hot switching as channel is disconnected using the switch matrix.
17. Disconnect the DUT from the SMU using the switch matrix.
18. Close the session to the DUT.

5.6. Measure Current Accuracy and Force Voltage Quadrant (Zone 2) Verification

5.6.1. Verification Test Limits

Table 5: Measure Current Accuracy and Force Voltage Quadrant (Zone 2) Verification Test Limits

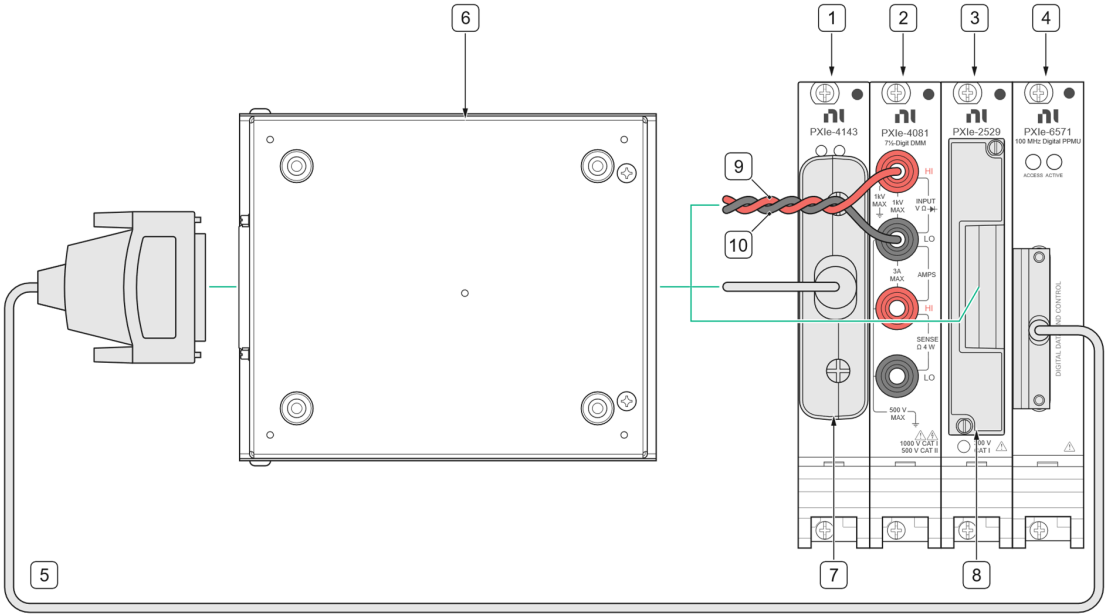
FVMI Quadrant	PPMU Current Range	SMU Test Voltage	PPMU Function	As-Found Test Limit	
				Lower Limit	Upper Limit
32 mA	0% of current range	-2 V	Measure Current	- 1.5%	1.5%
	-100% of current range	1.25 V		- 1%	1%
	100% of current range	-2 V		- 1.5%	1.5%
	100% of current range	6 V		- 1.5%	1.5%
	-100% of current range	6 V		- 1.5%	1.5%
2 mA	0% of current range	-2 V	Measure Current	- 1.5%	1.5%
	-100% of current range	1.25 V		- 1%	1%
	100% of current range	-2 V		- 1.5%	1.5%
	100% of current range	6 V		- 1.5%	1.5%
	-100% of current range	6 V		- 1.5%	1.5%
128 μ A	0% of current range	-2 V	Measure Current	- 1.5%	1.5%
	-100% of current range	1.25 V		- 1%	1%
	100% of current range	-2 V		- 1.5%	1.5%
	100% of current range	6 V		- 1.5%	1.5%
	-100% of current range	6 V		- 1.5%	1.5%
32 μ A	0% of current range	-2 V	Measure Current	- 1.5%	1.5%
	-100% of current range	1.25 V		- 1%	1%
	100% of current range	-2 V		- 1.5%	1.5%

	100% of current range	6 V		- 1.5%	1.5%
	-100% of current range	6 V		- 1.5%	1.5%
2 μ A	0% of current range	-2 V	Measure Current	- 1.5%	1.5%
	-100% of current range	1.25 V		- 1%	1%
	100% of current range	-2 V		- 1.5%	1.5%
	100% of current range	6 V		- 1.5%	1.5%
	-100% of current range	6 V		- 1.5%	1.5%
32 mA	0% of current range	-2 V	Force Voltage	- 15 mV	15 mV
	-100% of current range	1.25 V		- 15 mV	15 mV
	100% of current range	-2 V		- 15 mV	15 mV
	100% of current range	6 V		- 15 mV	15 mV
	-100% of current range	6 V		- 15 mV	15 mV
2 mA	0% of current range	-2 V	Force Voltage	- 15 mV	15 mV
	-100% of current range	1.25 V		- 15 mV	15 mV
	100% of current range	-2 V		- 15 mV	15 mV
	100% of current range	6 V		- 15 mV	15 mV
	-100% of current range	6 V		- 15 mV	15 mV
128 μ A	0% of current range	-2 V	Force Voltage	- 15 mV	15 mV
	-100% of current range	1.25 V		- 15 mV	15 mV
	100% of current range	-2 V		- 15 mV	15 mV
	100% of current range	6 V		- 15 mV	15 mV
	-100% of current range	6 V		- 15 mV	15 mV
32 μ A	0% of current range	-2 V	Force Voltage	- 15 mV	15 mV
	-100% of current range	1.25 V		- 15 mV	15 mV
	100% of current range	-2 V		- 15 mV	15 mV
	100% of current range	6 V		- 15 mV	15 mV

	-100% of current range	6 V		- 15 mV	15 mV
2 μ A	0% of current range	-2 V	Force Voltage	- 15 mV	15 mV
	-100% of current range	1.25 V		- 15 mV	15 mV
	100% of current range	-2 V		- 15 mV	15 mV
	100% of current range	6 V		- 15 mV	15 mV
	-100% of current range	6 V		- 15 mV	15 mV

5.6.2. Initial Test Connection

Figure 7. Initial Connection for Measure Current Accuracy and Force Quadrant (Zone 2) Verification Procedure



- | | |
|-------------------------|----------------------------------|
| 1. SMU | 6. SCB-68 Terminal Block |
| 2. DMM | 7. PXIe-414x Terminal Block |
| 3. Switch Module | 8. TB-2636 Terminal Block |
| 4. DUT | 9. Red Banana Cable to DMM HI |
| 5. VHDCl-to-VHDCl Cable | 10. Black Banana Cable to DMM LO |

5.6.3. Verification Procedure

1. Initialize a session and reset the device.
2. Configure the SMU according to the following settings:
 - a. Source mode: **Single Point**
 - b. Output function: **DC Current**
 - c. Sense: **Local**
 - d. Voltage limit range: **6.5 V**
 - e. Voltage limit: **6.5 V**
 - f. Current limit range: **32 mA**
 - g. Current level: **32 mA**
 - h. Aperture time: **1 PLC**
 - i. Power line Frequency: **50 Hz or 60 Hz**, depending on your country
 - j. Current limit auto range: **Off**
3. Configure the DUT to source current according to the following settings:
 - a. Select function: **PPMU**
 - b. Aperture time: **16.667 ms** (60 Hz) or **20 ms** (50 Hz), depending on your country

Repeat 8 times, once for each DUT channel.

4. Connect channel to be measured of the DUT to the SMU through the switch matrix.
 - a. Increment and iterate through all channels of DUT from 0 to 7.

Repeat 4 times, once for each PPMU Test Voltage.

5. Set DUT PPMU settings according to **Table 5**.
 - a. **Voltage level**
 - b. **Current limit range**
 - c. **Test Current**
6. Commit changes to DUT.
7. Set DUT PPMU source to force requested voltage level.
8. Wait 30 ms for SMU, cabling, and DUT to settle.
9. Measure current with SMU, negate the measurement (invert the sign).
10. Calculate the measure current error, then compare against the limits in **Table 5**.
 - a.
$$Measure_{Current_error} = \frac{100 * (PPMU_{Current_meas} - SMU_{Current_meas})}{Current_{Range}}$$
11. Calculate the measure current error, then compare against the limits in **Table 5**.
 - a.
$$Force_{Voltage_error} = PPMU_{Voltage_meas} - Voltage_{Set_Point}$$
12. Set DUT channel to **Disconnect** state.
13. Abort the SMU voltage source and set to **0 V**. This prevents hot switching as channel is disconnected using the switch matrix.
14. Disconnect the DUT from the SMU using the switch matrix.
15. Close the session to the DUT.

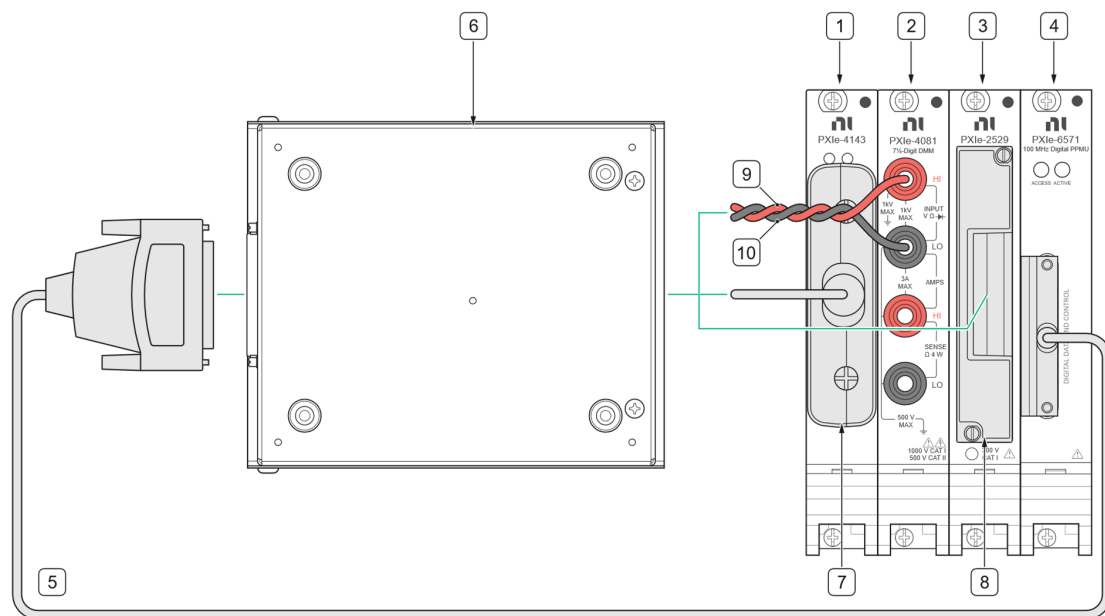
6. Perform Adjustment

Perform an adjustment at least once within the calibration interval. Adjustment automatically updates the calibration constants, the date, and the temperature in the DUT EEPROM. If the DUT passes the verification procedures within the As-Left test limits, an adjustment is not required. Proceed to the *Update the Onboard Calibration Information* section.

6.1. Adjusting Voltage and Resistor References

6.1.1. Initial Test Connection

Figure 8. Initial Connection for Adjusting Voltage and Resistor References



1. SMU

2. DMM

3. Switch Module

4. DUT

5. VHDCI-to-VHDCI Cable

6. SCB-68 Terminal Block

7. PXIe-414x Terminal Block

8. TB-2636 Terminal Block

9. Red Banana Cable to DMM HI

10. Black Banana Cable to DMM LO

6.1.2. Adjustment Procedure

1. Initialize an external calibration session.
2. Configure the DUT Digital Calibration Reference according to the following settings:
 - a. Calibration path: **Voltage Reference**
 - b. Calibration reference: **0 V**
3. Configure the DMM according to the following settings:
 - a. Functions: **DC Volts**
 - b. Range: **100 mV**
 - c. Sense: **Local**
 - d. Digits of resolution: **7 ½ Digits**
 - e. Input Impedance: **> 10 GΩ**
 - f. Power line Frequency: **50 Hz or 60 Hz**, depending on your country

Repeat 8 times, once for each DUT channel.

4. Connect channel to be measured of the DUT to the DMM and SMU through the switch matrix.
 - a. Increment and iterate through all channels of DUT from 0 to 7.
5. Wait 2 seconds for the measurement voltage to settle.

Repeat 8 times, once for each Resistor Reference Current Setpoint in Table 6.

6. Use the DMM to read and save the measurement as **M₀**.
7. Adjust the DUT Digital Calibration Reference according to the following settings:
 - a. Calibration path: **Voltage Reference**

- b. Calibration reference: **0 V**
 - c. Value: **M_0**
8. Configure the DUT Digital Configure Calibration Reference according to the following settings:
 - a. Calibration path: **Voltage Reference**
 - b. Calibration reference: **5 V**
9. Configure DMM range to **10 V**.
10. Wait 2 seconds for the measurement voltage to settle.
11. Use the DMM to read and save the measurement as **M_1** .
12. Adjust the DUT Digital Calibration Reference according to the following settings:
 - a. Calibration path: **Voltage Reference**
 - b. Calibration reference: **5 V**
 - c. Value: **M_1**
13. Configure the SMU according to the following settings:
 - a. Source mode: **Single point**
 - b. Output function: **DC current**
 - c. Sense: **Remote**
 - d. Voltage limit: **8 V**
 - e. Voltage limit range: **8 V**
 - f. Aperture time units: **Power Line Cycles (PLC)**
 - g. Aperture time: **3 PLC**
 - h. Samples to average: **1**
14. Configure the DUT Digital Calibration Reference according to the following settings:

- a. Calibration path: **Sink resistor** or **Source resistor**, based on **Iteration of loop from Table 6.**
- b. Calibration reference: **Resistor (n+1)**, where n= Iteration in **Table 6.**

Table 6. Resistor Reference Current Setpoints and Settling Time

Iteration	Calibration Path	Current Range	First Current	Second Current	Settling Time
0	Sink resistor	10 mA	10 mA	6 mA	1 s
1		1 mA	1 mA	600 μ A	1 s
2		100 μ A	100 μ A	60 μ A	5 s
3		10 μ A	5 μ A	1 μ A	5 s
4	Source resistor	10 mA	– 10 mA	– 6 mA	1 s
5		1 mA	– 1 mA	– 600 μ A	1 s
6		100 μ A	– 100 μ A	– 60 μ A	5 s
7		10 μ A	– 5 μ A	– 1 μ A	5 s

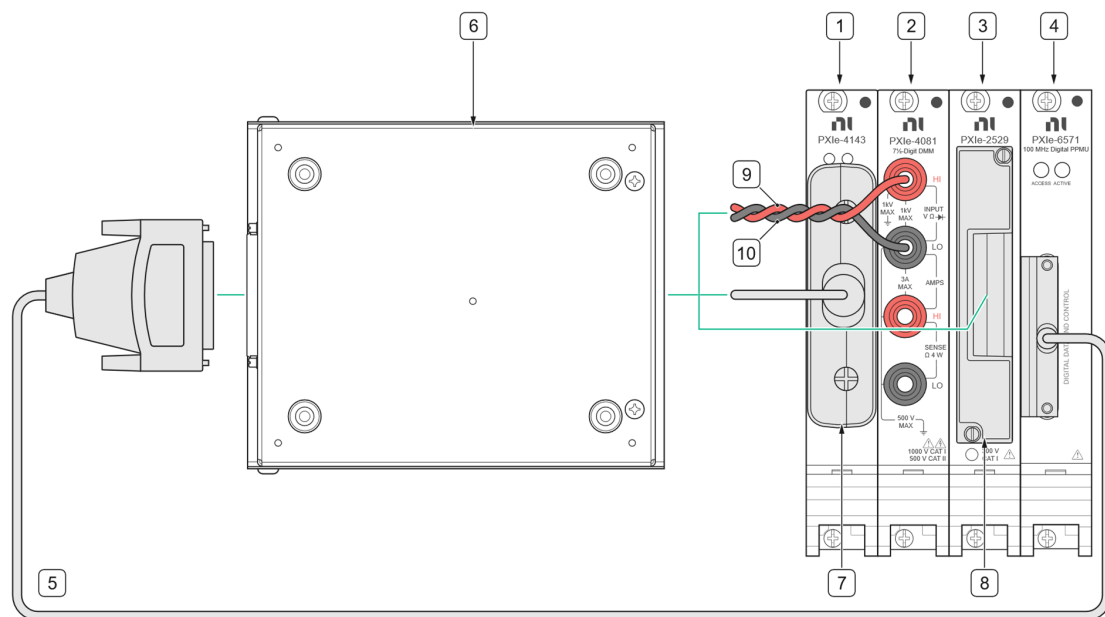
15. Wait for 500 ms for path to settle.
16. Source the first current value for iteration of loop from **Table 6.**
17. Wait for settling time for iteration of loop from **Table 6.**
18. Measure voltage (V_1) and current (I_1) using the SMU.
19. Source the second current value for iteration of loop from **Table 6.**
20. Wait for settling time for iteration of loop from **Table 6.**
21. Measure voltage (V_2) and current (I_2) using the SMU.
22. Calculate the measured resistance.
 - a. $Measured_{Resistance} = \frac{(V_2 - V_1)}{(I_2 - I_1)}$
23. Set the DUT Digital Adjust Calibration Reference according to the following settings:

- a. Calibration path: **Sink resistor** or **Source resistor, based on Iteration of loop from Table 6.**
 - b. Calibration reference: **Resistor (n+1)**, where n= Iteration in **Table 6.**
 - c. Value: **Measured Resistance**
24. Abort the SMU voltage source and set to **0 V**. This prevents hot switching as channel is disconnected using the switch matrix.
25. Disconnect the DUT from the DMM and the SMU using the switch matrix.
26. Clear the calibration state.

6.2. Adjusting Force Current and Measure Current Gain/Offset

6.2.1. Initial Test Connection

Figure 9. Initial Connection for Adjusting Force Current and Measure Current Gain/Offset Procedure



- | | |
|-------------------------|----------------------------------|
| 1. SMU | 6. SCB-68 Terminal Block |
| 2. DMM | 7. PXIe-414x Terminal Block |
| 3. Switch Module | 8. TB-2636 Terminal Block |
| 4. DUT | 9. Red Banana Cable to DMM HI |
| 5. VHDCI-to-VHDCI Cable | 10. Black Banana Cable to DMM LO |

6.2.2. Adjustment Procedure

Repeat 8 times, once for each current range.

1. Initialize an external calibration session.

2. Adjust the Source Gain of the DUT with the following settings:
 - a. Current Range: **32 mA**, refer to **Table 7**
 - b. Adjustments: **1D Array of 8 Doubles each initialized to a value of 1**

Table 7. Adjust Current Ranges

Iteration	Current Range
0	32 mA
1	8 mA
2	2 mA
3	512 μ A
4	128 μ A
5	32 μ A
6	8 μ A
7	2 μ A

3. Adjust the Source Offset of the DUT with the following settings:
 - a. Current Range: **32 mA**, refer to **Table 7**
 - b. Adjustments: **1D Array of 8 Doubles each initialized to a value of 0**
4. Adjust the Measure Gain of the DUT with the following settings:
 - a. Current Range: **32 mA**, refer to **Table 7**
 - b. Adjustments: **1D Array of 8 Doubles each initialized to a value of 1**
5. Adjust the Measure Offset of the DUT with the following settings:
 - a. Current Range: **32 mA**, refer to **Table 7**

- b. Adjustments: **1D Array of 8 Doubles each initialized to a value of 0**
6. Close the external calibration session with the following setting:
 - a. Write Calibration to Hardware: **True**
7. Initialize a session and reset the DUT.
8. Set the DUT to self-calibration.
9. Close the DUT session.

Repeat 8 times, once for each DUT channel.

10. Connect channel to be measured of the DUT to the SMU through the switch matrix.
 - a. Increment and iterate through all channels of DUT from 0 to 7.
11. Initialize a session with the DUT.

Repeat 64 times, once for each Test Current in Table 8.

12. Configure SMU according to the following settings:
 - a. Source mode: **Single point**
 - b. Output function: **DC Voltage**
 - c. Sense: **Local**
 - d. Voltage range: **2 V**
 - e. Voltage level: **2 V**
 - f. Power line Frequency: **50 Hz or 60 Hz**, depending on your country
 - g. Aperture Time: **1 PLC**
 - h. Current limit: Refer to **Table 8**

Table 8. Adjust Current Test Points

SMU Current Limit	DUT Current Range	Test Current Level
10 μ A	2 μ A	0.5 μ A
		1.0 μ A
		1.5 μ A
		2.0 μ A
		– 0.5 μ A
		– 1.0 μ A
		– 1.5 μ A
		– 2.0 μ A
10 μ A	8 μ A	2 μ A
		4 μ A
		6 μ A
		8 μ A
		– 2 μ A
		– 4 μ A
		– 6 μ A
		– 8 μ A
100 μ A	32 μ A	8 μ A
		16 μ A
		24 μ A
		32 μ A
		– 8 μ A
		– 16 μ A
		– 24 μ A

1 mA	128 μ A	- 32 μ A
		32 μ A
		64 μ A
		96 μ A
		128 μ A
		- 32 μ A
		- 64 μ A
		- 96 μ A
		- 128 μ A
1 mA	512 μ A	128 μ A
		256 μ A
		384 μ A
		512 μ A
		- 128 μ A
		- 256 μ A
		- 384 μ A
		- 512 μ A
10 mA	2 mA	0.5 mA
		1.0 mA
		1.5 mA
		2.0 mA
		- 0.5 mA
		- 1.0 mA
		- 1.5 mA
		- 2.0 mA
10 mA	8 mA	2 mA

		4 mA
		6 mA
		8 mA
		– 2 mA
		– 4 mA
		– 6 mA
		– 8 mA
150 mA	32 mA	8 mA
		16 mA
		24 mA
		32 mA
		– 8 mA
		– 16 mA
		– 24 mA
		– 32 mA

13. Initialize generation on the SMU.
14. Configure the PPMU source current of the DUT.
 - a. Current level: **Refer to Table 8**
 - b. Current range: **Refer to Table 8**
 - c. Upper voltage limit (high clamp voltage: **6 V**
 - d. Lower voltage limit (low clamp voltage: **– 2 V**
15. Wait 30 ms for the DUT, SMU, and cabling to settle.
16. Read the current with the SMU and store the value in an array.
17. Configure the DUT PPMU aperture time to **16.667 ms** (60 Hz) or **20 ms** (50 Hz), depending on your country

18. Measure the DUT PPMU current and store the value in an array.
19. Select the disconnect state for the selected DUT channel.
20. Negate (multiple by -1) all SMU measurements. The SMU polarity is opposite the PPMU, and must be the same polarity for the processing of the measurements.
 - a. SMU sources when PPMU sinks
 - b. SMU sinks when PPMU sources
21. Split SMU and DUT PPMU measurements into multiple array based on the DUT ranges.
22. Determine linear fit of the following parameters for each DUT range, hence known as FI gain and offset error.
 - a. Y-values: 1D array of negated measurements from SMU
 - b. X-values: 1D array of test points
 - c. Store gain and offset for each DUT range.
23. Determine linear fit of the following parameters for each DUT range, hence known as MI gain and offset error.
 - a. Y-values: 1D array of DUT PPMU measurements
 - b. X-values: 1D array of negated measurements from SMU
 - c. Store gain and offset for each DUT range.
24. Disable the SMU output and close the SMU session.
25. Close the DUT session.
26. Disconnect the DUT channel from the SMU.
27. Create multiple 1D arrays.
 - a. Using the FI Gain Error obtained from each channel for specific current range. Form a 1D array of 8 doubles consisting of the FI Gain Error for each channel tested. Create a separate 1D array of 8 doubles for every current range.

- b. Using the FI Offset Error obtained from each channel for specific current range. Form a 1D array of 8 doubles consisting of the FI Offset Error for each channel tested. Create a separate 1D array of 8 doubles for every current range.
- c. Using the MI Gain Error obtained from each channel for specific current range. Form a 1D array of 8 doubles consisting of the MI Gain Error for each channel tested. Create a separate 1D array of 8 doubles for every current range.
- d. Using the MI Offset Error obtained from each channel for specific current range. Form a 1D array of 8 doubles consisting of the MI Offset Error for each channel tested. Create a separate 1D array of 8 doubles for every current range.

Repeat 8 times, once for each current range.

28. Initialize an external calibration session.
29. Adjust the Source Gain of the DUT with the following settings:
 - a. Current Range: **32 mA**, refer to **Table 7**
 - b. Adjustments: **1D Array of 8 Doubles from FI Gain Error information**
30. Adjust the Source Offset of the DUT with the following settings:
 - a. Current Range: **32 mA**, refer to **Table 7**
 - b. Adjustments: **1D Array of 8 Doubles from FI Offset Error information**
31. Adjust the Measure Gain of the DUT with the following settings:
 - a. Current Range: **32 mA**, refer to **Table 7**
 - b. Adjustments: **1D Array of 8 Doubles from MI Gain Error information**
32. Adjust the Measure Offset of the DUT with the following settings:
 - a. Current Range: **32 mA**, refer to **Table 7**

- b. Adjustments: **1D Array of 8 Doubles from MI Offset Error information**
- 33. Close the external calibration session with the following setting:
 - a. Write Calibration to Hardware: **True**

7. Perform Reverification

Perform all tests in the Verification section after completing Adjustment. This verification compares the As-Left limits with measurement data collected after the DUT adjustment. The As-Left limits may be tighter than the As-Found limits.

8. Update the Onboard Calibration Information

If the DUT passes all verification procedures successfully, meets the As Left limits, and the adjustment procedure is not going to be executed, then the calibration date can be updated by completing the following steps.



Note

NI recommends following the adjustment procedure in order to update the calibration constants and renew the device calibration interval.

Use either Measurement Automation Explorer (MAX) or NI System Configuration API to set a calibration due date for the DUT or to clear the calibration due date. NI suggests a minimum calibration due date of the date of external calibration plus the recommended external calibration interval.

1. In MAX, navigate to the External Calibration section of the Settings tab to update the Calibration Due Date entry.

- Alternatively, use the Update Calibration vi in the NI System Configuration API to set the calibration due date for a specific date of an interval in months.

9. Revision History

Revision	Section	Changes
379117A-01 July 2025	All	This is the initial release version of the PXIe-6571 (8-channel) Calibration Procedure.

10. NI Services

Visit ni.com/support to find support resources including documentation, downloads, and troubleshooting and application development self-help such as tutorials and examples.

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