PXIe-6674T User Manual

2024-04-16

Contents

Welcome to the PXIe-6674T User Manual

The PXIe-6674T User Manual provides detailed descriptions of product functionality and step-by-step processes for use.

Looking for something else?

For information not found in the User Manual for your product, like specifications or API reference, browse Related Information.

Related information:

- PXIe-6674T Specifications
- PXIe-6674T Calibration Executive Procedure
- NI-Sync
- NI-Sync LabVIEW API Reference
- NI-Sync C API Reference
- NI VISA User Manual
- PXI Specification
- PICMG 2.0 R3.0, CompactPCI Core Specification
- License Setup and Activation
- Software and Driver Downloads
- Release Notes
- NI Learning Center
- Discussion Forums

PXIe-6674T Overview

The PXIe-6674T is a PXI Express timing and synchronization module that can generate and route clocks and triggers between devices in a single PXI Express chassis or across multiple PXI and PXI Express chassis. Use the PXIe-6674T to provide advanced triggering schemes, perform synchronization for multiple devices, and improve measurement accuracy for extremely high-channel-count applications.

Device Capabilities

The PXIe-6674T has the following features and capabilities.

- An onboard precision oven controlled crystal oscillator (OCXO) with an accuracy of 80 parts-per-billion (ppb)
- A built-in clock generation circuitry based on direct digital synthesis (DDS) with an 800 MHz reference phase locked to PXIe_CLK100
- DDS Clock Generation Range: 0.3 Hz to 1 GHz
- DDS Clock Generation Resolution: 2.84 µHz
- Six front-panel SMA connectors, which can be configured as single-ended LVTTL 5 V-tolerant input/output lines, or as LVDS differential signal input/output pairs
- Eight PXI Trigger bidirectional lines
- 13 sets of differential PXIe_DSTAR triggers

Driver Support

NI recommends that you use the newest version of the driver for your module.

Table 1. Earliest Driver Version Support

Driver Name	Earliest Version Support
NI-Sync	3.4.1

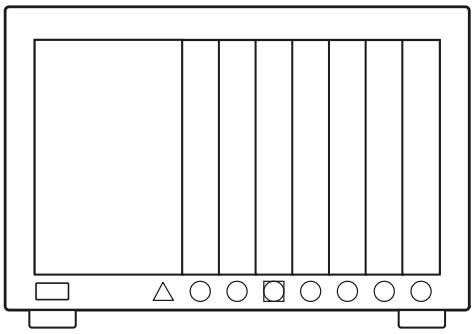
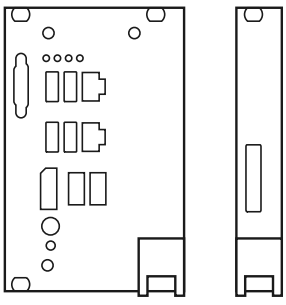
Components of a PXIe-6674T System

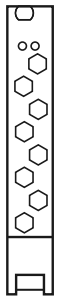
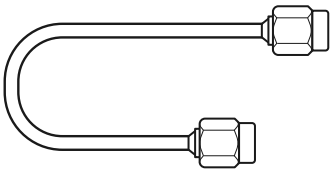
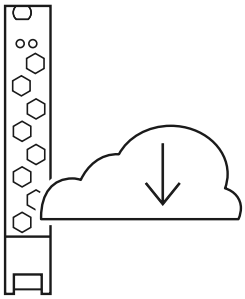
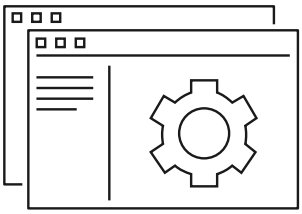
The PXIe-6674T is designed for use in a system that includes other hardware components, drivers, and software.

Notice A system and the surrounding environment must meet the requirements defined in **PXIe-6674T Specifications**.

The following list defines the minimum required hardware and software for a system that includes a PXIe-6674T.

Table 2. System Components

Component	Description and Recommendations
PXI Express Chassis 	A PXI Express chassis houses the PXIe-6674T. **Note** In most PXI Express chassis, the PXIe-6674T must be installed in the system timing slot of the chassis. Some PXI Express chassis can accommodate the PXIe-6674T in other slots, but certain features, such as PXI_CLK10_IN and PXIe_DSTAR lines will not be available.
PXI Express embedded controller or a desktop computer connected to the PXI Express chassis using MXI-Express hardware 	You can install a PXI Express controller or a PXI remote control (MXI) module depending on your system requirements. These components, installed in the same PXI Express chassis as the PXIe-6674T, interface with the instrument using NI device drivers.

Component	Description and Recommendations
Timing and Synchronization Module 	The PXIe-6674T timing and Synchronization module.
Cables and Accessories 	Cables and accessories allow connectivity to/from your instrument for measurements. Refer to **Cables and Accessories** for recommended cables and accessories and guidance.
NI-Sync Driver 	Instrument driver software that provides an API to interact with the PXIe-6674T.
NI Applications 	NI-Sync offers driver support for the following applications: ▪ LabVIEW ▪ LabWindows/CVI ▪ C/C++

Cables and Accessories

NI recommends using the following cables and accessories with your module.

Table 3. Cables and Accessories

Accessory Description	Notes	Part Number
PXI slot blocker	Set of 5	199198-01
PXI EMC filler panel	N/A	778700-01

Additional Cabling and Accessory Guidance

NI recommends the following:

- You can install PXI slot blockers and PXI EMC filler panels in empty slots to improve chassis cooling and control EMC emissions from the chassis. For more information about installing slot blockers and filler panels, go to ni.com/r/pxiblocker.

Programming Options

When programming the PXIe-6674T, you can use NI application development environment (ADE) software such as LabVIEW or LabWindows/CVI, or you can use other ADEs, such as Visual C/C++.

LabVIEW is a programming environment used to create applications using the G programming language. It features a wide range of analysis functions and interactive, programmable display elements. The LabVIEW Data Acquisition VI Library, a series of virtual instruments for using LabVIEW with National Instruments DAQ hardware, is included with LabVIEW.

LabWindows/CVI is a complete ANSI C ADE that features an interactive video interface, code generation tools, and the LabWindows/CVI Data Acquisition and Easy I/O libraries.

PXIe-6674T Theory of Operation

The PXIe-6674T timing and synchronization module performs two broad functions:

- Generating clock and trigger signals.
- Routing internally or externally generated signals from one location to another.

The PXIe-6674T can generate two types of clock signals. The first type of clock signal is generated using the onboard clock generation circuitry based on direct digital synthesis (DDS) with an 800 MHz reference phase locked to PXIe_CLK100. The second type of clock signal is generated with an onboard precision oven controlled crystal oscillator (OCXO). The constant temperature maintained by the OCXO allows it to produce stable 10 MHz clock signals with an accuracy of 80 parts-per-billion (ppb) within one year of calibration. Refer to **Generating and Routing Clocks** for a detailed description of these two types of clock generation.

In terms of routing signals, the PXIe-6674T features six programmable function interface (PFI) pins that can be individually configured for either single-ended operation or low-voltage differential signaling (LVDS) operation. The use of LVDS logic in signal routing allows much faster speeds than can be achieved with the single-ended PFIs. In LVDS mode, the connectors are paired and can be programmatically set as either inputs or outputs, but not both simultaneously. You can also define the source and destination of the signals for each PFI pin.

The PXIe-6674T supports two methods of routing clock and trigger signals: asynchronously or synchronously.

- In asynchronous routing, source signals are transferred to the destinations in multiple modules after different propagation delays.
- In synchronous routing, all destination signals are updated synchronous with a reference clock signal (for example, the PXI_CLK10), and do not directly follow the source signals after the propagation delays. Therefore, the source signals in synchronous routing are received by the destinations at the same time.

You can use the NI-Sync software or the NI-MAX interface to interact with the PXIe-6674T, including configuring the PFI, PXI_STAR, and PXIe_DSTAR terminals, and specifying the frequencies produced by the DDS clock generation circuitry.

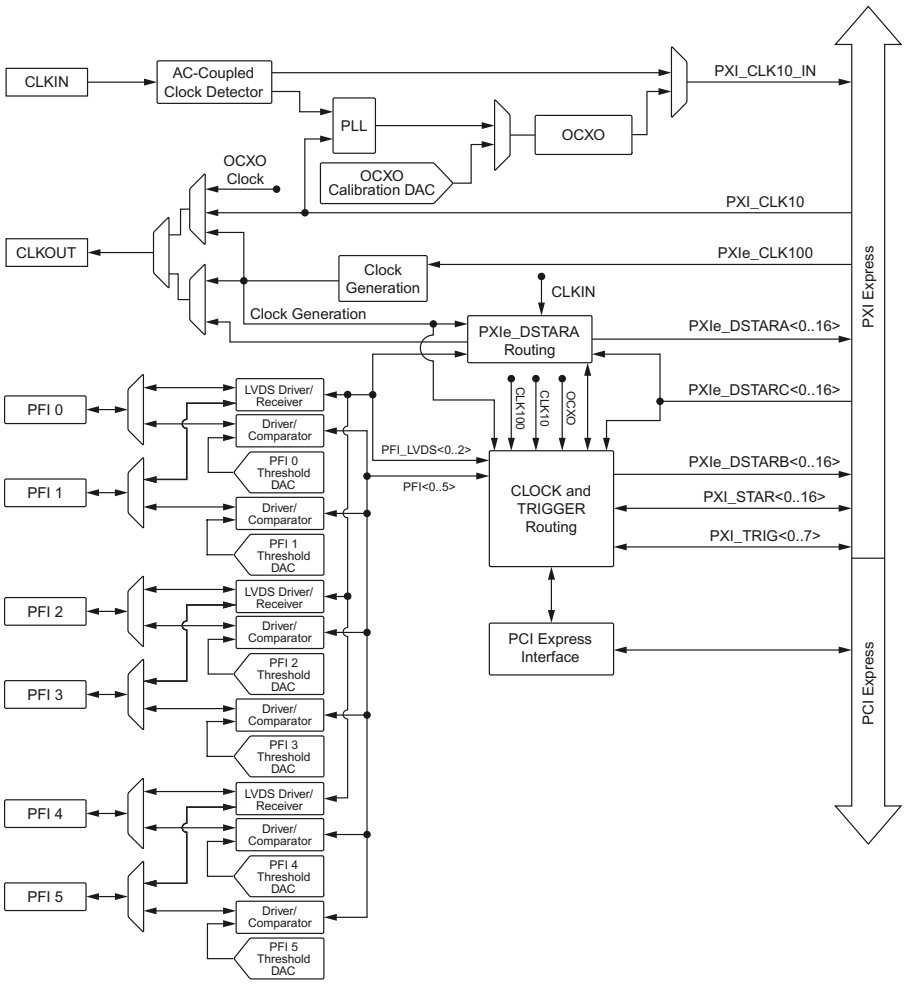
Related concepts:

- Generating and Routing Clocks

PXIe-6674T Block Diagram

The following diagram illustrates the design of the PXIe-6674T.

Figure 1. PXIe-6674T Block Diagram

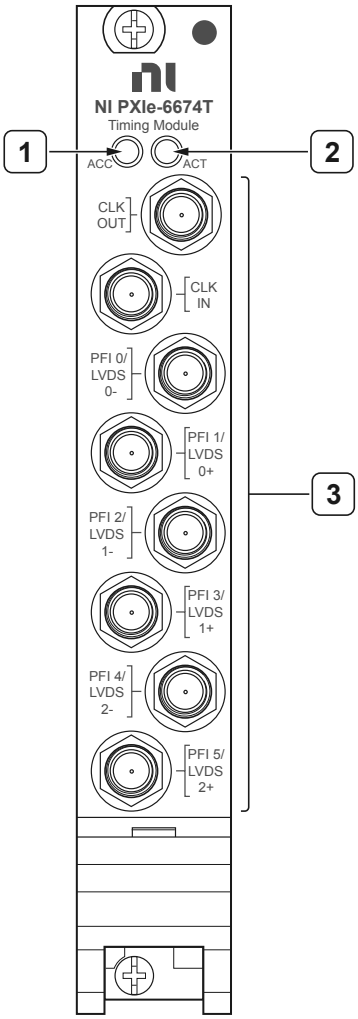


Related concepts:

- Generating and Routing Clocks

PXIe-6674T Front Panel

Figure 2. PXIe-6674T Front Panel



1. Access LED
2. Active LED
3. SMA Connectors

PXIe-6674T Pinout

The following figure shows the terminals on the PXIe-6674T front panel.

Figure 3. PXIe-6674T Connector Pinout

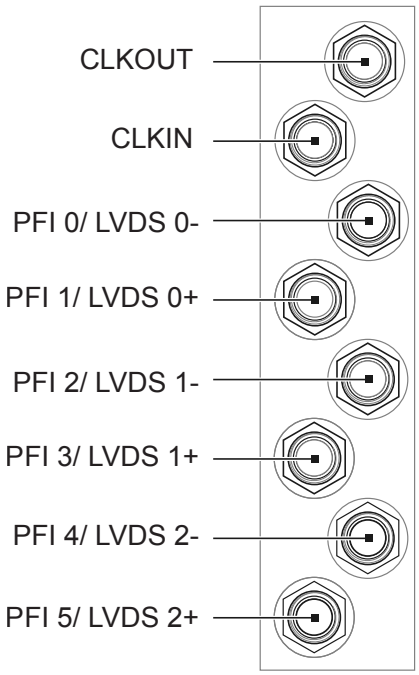


Table 4. Signal Descriptions

Signal	Description
CLKIN	AC-coupled, 50 Ω clock input. CLKIN can be routed directly to PXI_CLK10_IN, to the 10 MHz PLL, to PXIe_DSTARA, or to the FPGA for use as a synchronization clock.
CLKOUT	AC-coupled clock output. CLKOUT can be sourced from the OCXO, PXI_CLK10, Clock Generation, or from the PXIe_DSTARA network.
PFI <0..5>	Single-ended programmable function interface (PFI) pins that can route timing and triggering signals between multiple PXI Express chassis.
PFI_LVDS <0..2>	Pairs of PFI connectors that can be configured to be used as PFI_LVDS. Like the PFI pins, PFI_LVDS pins can route timing and triggering

Signal	Description
	signals between multiple PXI Express chassis. When used in LVDS mode, the connectors are paired and can be programmatically set as either inputs or outputs, but not both simultaneously.

Notice Connections that exceed any of the maximum ratings of input or output signals on the PXIe-6674T can damage the module and the computer. NI is not liable for any damage resulting from such signal connections.

PXIe-6674T LED Indicators

The PXIe-6674T features an Access LED and Active LED.

Access LED

The Access LED, located on the module front panel, indicates module power and access.

The following table lists the Access LED states.

Table 5. Access LED

Color	Status
Off	Module is not yet functional.
Green	Driver has initiated the module.
Amber	Module is being accessed. The Access LED flashes amber for 50 ms when the module is accessed.
Blinking Red	Module has detected an over-temperature condition.
Solid Red	A hardware error has been detected.

Notice If the Access LED is observed to be blinking red, the module has detected an over-temperature condition. Continued use of the PXIe-6674T in this condition is not recommended as product reliability may become compromised.

To identify the cause of an over-temperature condition, investigate the following:

- Check that all chassis covers, filler panels, and/or slot blockers are installed.
- Make sure that the chassis fan speed is set to the highest setting.
- If applicable, check that the chassis fan air intake is not blocked and that the fan filters are clean.

- Make sure that the ambient temperature around the chassis isn't above the rated temperature specifications. If so, move the chassis to a cooler ambient temperature location.

Notice If the Access LED is observed to be solid red, a hardware failure has been detected that may impact the performance of the PXIe-6674T. Contact NI for support.

Active LED

The Active LED indicates an error or phase-locked loop (PLL) activity. You can change the Active LED to amber, unless an error overrides the selection.

Tip Changing the Active LED color to amber is helpful when you want to identify devices in a multichassis configuration or when you want an indication that your application has reached a predetermined section of the code.

The following table lists the Active LED states.

Table 6. Active LED

Active LED Color	Status
Off	The 10 MHz PLL is not in use and no errors are present.
Green	The 10 MHz PLL is active and locked.
Solid Amber	You can set the Active LED to amber through software.
Solid Red	10 MHz PLL is attempting to lock to the reference supplied on CLKIN.

PXIe-6674T Installation and Configuration

Complete the following steps to install the PXIe-6674T into a chassis and prepare it for use.

1. Installing the Software
2. Unpacking the Kit
3. Installing the PXIe-6674T into a Chassis
4. Verifying the Installation in MAX

Installing the Software

You must be an Administrator to install NI software on your computer.

1. Install an ADE, such as LabVIEW or LabWindows™/CVI™.
2. Download the driver software installer from ni.com/downloads.
   NI Package Manager downloads with the driver software to handle the installation. Refer to the NI Package Manager Manual for more information about installing, removing, and upgrading NI software using NI Package Manager.
3. Follow the instructions in the installation prompts.

   Note Windows users may see access and security messages during installation. Accept the prompts to complete the installation.

4. When the installer completes, select **Restart** in the dialog box that prompts you to restart, shut down, or restart later.

Unpacking the Kit

Notice To prevent electrostatic discharge (ESD) from damaging the device, ground yourself using a grounding strap or by holding a grounded object, such as your computer chassis.

1. Touch the antistatic package to a metal part of the computer chassis.
2. Remove the device from the package and inspect the device for loose components or any other sign of damage.

   Notice Never touch the exposed pins of connectors.

   Note Do not install a device if it appears damaged in any way.
3. Unpack any other items and documentation from the kit.

Note Store the device in the antistatic package when the device is not in use.

Kit Contents

Refer to the following figure to identify the contents of the PXIe-6674T kit.

Figure 4. PXIe-6674T Kit Contents

1. PXIe-6674T Module
2. SMA Driver Bit
3. Documentation

Installing the PXIe-6674T into a Chassis

Note

Be sure to install the driver software before installing the PXIe-6674T hardware.

Notice To prevent damage to the PXIe-6674T caused by ESD or contamination, handle the module using the edges or the metal bracket.

The following are general installation instructions. Consult the chassis user manual or technical reference manual for specific instructions and warnings about installing new modules.

1. Power off and unplug the chassis.
2. Locate the system timing slot for your PXI Express chassis. The system timing slot can be identified by the glyph shown in the following figure.

   Figure 5. System Timing Slot Indicator Glyph

   Note The system timing slot glyph for your chassis may include a slot number within the black circle.
3. Remove the filler panel for the system timing slot, if applicable.
4. Ground yourself using a grounding strap or by touching a grounded object. Make sure you follow the ESD protection precautions.
5. Carefully insert the PXIe-6674T into the system timing slot. Make sure you do not scrape the module on any adjacent modules. Use the injector/ejector handle to fully insert the module into the chassis.
6. Screw the front panel of the device to the front panel mounting rail of the chassis.
7. If adjacent slots are not populated, use EMC filler panels to cover the opening.

   Notice

- To ensure the specified EMC performance, you must install PXI EMC filler panels (p/n 778700-01) in all open chassis slots.
- To ensure the specified EMC performance, operate this product only with double-shielded cables and accessories (for example, RG-223 cables).

8. Visually verify the installation. Ensure that the module is fully inserted into the slot.
9. Plug in and power on the chassis.
   The PXIe-6674T is now installed.

Verifying the Installation in MAX

Use Measurement & Automation Explorer (MAX) to configure your NI hardware. MAX informs other programs about which NI hardware products are in the system and how they are configured. MAX is automatically installed with NI-Sync.

1. Launch MAX.
2. In the configuration tree, expand **Devices and Interfaces** to see the list of installed NI hardware.
   Installed modules appear under the name of their associated chassis.
3. Expand your **Chassis** tree item.
   MAX lists all modules installed in the chassis. Your default names may vary.

Note If you do not see your module listed, press <F5> to refresh the list of installed modules. If the module is still not listed, power off the system, ensure the module is correctly installed, and restart.

4. Record the identifier MAX assigns to the hardware. Use this identifier when programming the PXIe-6674T.
5. Self-test the hardware by selecting the item in the configuration tree and clicking **Self-Test** in the MAX toolbar.
   MAX self-test performs a basic verification of hardware resources.

What Should I Do if the PXIe-6674T Does Not Appear in MAX?

1. In the MAX configuration tree, expand **Devices and Interfaces**.
2. Expand the **Chassis** tree to see the list of installed hardware, and press <F5> to refresh the list.
3. If the module is still not listed, power off the system, ensure that all hardware is correctly installed, and restart the system.
4. Navigate to the Device Manager by right-clicking the Start button, and selecting **Device Manager**.
5. Verify the PXIe-6674T appears in the Device Manager.
    a. Under an NI entry, confirm that a PXIe-6674T entry appears.

> **Note** If you are using a PC with a device for PXI remote control system, under **System Devices**, also confirm that no error conditions appear for the **PCI-to-PCI Bridge**.

    b. If error conditions appear, reinstall the NI-Sync driver.

What Should I Do if the PXIe-6674T Fails the Self-Test?

1. Reset the PXIe-6674T through MAX, and then perform the self-test again.
2. Restart the system, and then perform the self-test again.
3. Power off the chassis.
4. Power on the chassis.
5. Perform the self-test again.

PXIe-6674T Signal Description

The following table outlines the function and direction of the signals in the PXIe-6674T.

Table 7. PXIe-6674T Signals

Signal Name	Direction	Description
PXI_CLK10_IN	Out (to chassis)	This is a signal that can be used to provide the backplane with a reference 10 MHz signal from the system timing slot. When a 10 MHz signal is connected to PXI_CLK10_IN, the PXI Express chassis is required to derive PXI_CLK10 and PXIe_CLK100 from this reference. Refer to the user manual for your PXI Express chassis for more information on how it uses PXI_CLK10_IN.
PXI_CLK10	In (from chassis)	This signal is the PXI 10 MHz backplane clock. This signal is the output of the native 100 MHz oscillator in the chassis divided by ten.
PXIe-CLK100	In (from chassis)	This signal is the PXI Express 100 MHz backplane clock. PXIe_CLK100 offers tighter slot to slot timing than PXI_CLK10.
OCXO Clock	Out (internal)	This is the output of the 10 MHz OCXO. The OCXO is an extremely stable and accurate frequency source.
CLKIN	In (from front panel)	CLKIN is the signal connected to the SMA input connector of the same name. CLKIN can be routed directly to PXI_CLK10_IN, to the 10 MHz

Signal Name	Direction	Description
		PLL, to PXIe_DSTARA, or to the FPGA.
CLKOUT	Out (to front panel)	CLKOUT is the signal on the SMA output connector of the same name. CLKOUT can be sourced from the OCXO, PXI_CLK10, Clock Generation, or from the PXIe_DSTARA network.
Clock Generation	Out (internal)	Clock Generation refers to the clock signal coming from the onboard clock generation circuitry of the PXIe-6674T. The clock generation circuitry can generate a clock from sub-1 Hz to 1 GHz with fine granularity and is automatically locked in phase to PXIe_CLK100.
PFI<0..5>	In/Out (to/from front panel)	The single-ended Programmable Function Interface pins on the PXIe-6674T route timing and triggering signals between multiple PXI Express chassis. A wide variety of input and output signals can be routed to or from the PFI lines.
PFI_LVDS<0..2>	In/Out (to/from front panel)	The LVDS Programmable Function Interface can be used to route timing and triggering signals between multiple PXI Express chassis. The use of LVDS logic allows much faster speeds than can be achieved with the single-ended PFIs. When used as outputs, the LVDS PFIs can be sourced from the PXIe_DSTARA network, the FPGA, or the clock generation circuitry. As inputs, the LVDS

Signal Name	Direction	Description
		PFIs can be routed to the PXIe_DSTARA network and to the FPGA.
PXI_TRIG<0..7>	In/Out (to/from chassis)	The PXI trigger bus consists of eight digital lines shared among all slots in the PXI Express chassis. The PXIe-6674T can route a wide variety of signals to and from these lines. **Note** PXI_TRIG<0..5> are also known as RTSI<0..5> in some hardware devices and APIs. However, PXI_TRIG<6..7> are not identical to RTSI<6..7>.
PXI_STAR<0..16>	In/Out (to/from chassis)	The PXI star trigger bus connects the system timing slot to other peripheral slots in a star configuration. The electrical paths of each star line are closely matched to minimize intermodule skew. A PXIe-6674T in the system timing slot can route signals to all available PXI_STAR lines in the PXI Express chassis.
PXIe_DSTARA	Out (to chassis)	The PXIe_DSTARA lines connect the system timing module to each peripheral slot in a PXI Express chassis, allowing the system timing module to distribute a clock signal to every slot. PXIe_DSTARA uses differential LVPECL signaling

Signal Name	Direction	Description
		and is capable of high-speed clock distribution. Refer to **PXIe DSTARA Network** for more information.
PXIe_DSTARB	Out (to chassis)	The PXIe_DSTARB lines connect the system timing module to each peripheral slot in a PXI Express chassis, allowing the system timing module to send out high-speed triggers to every slot. PXIe_DSTARB uses differential LVDS signaling and is capable of sending out higher-speed trigger signals.
PXIe_DSTARC	In (from chassis)	The PXIe_DSTARC lines connect each peripheral slot in a PXI Express chassis to the system timing module, allowing the system timing module to receive high-speed clock and trigger signals from every slot. PXIe_DSTARC uses differential LVDS signaling.

Generating and Routing Clocks

This section describes the two types of clock generation in the PXIe-6674T and explains the considerations for choosing either type.

Generating Clocks Using the Onboard Clock Generation Circuitry

The PXIe-6674T includes built-in advanced clock generation circuitry for generating clock signals from below 1 Hz to 1 GHz with very fine frequency resolution. The clock generation circuitry is based on direct digital synthesis (DDS) with an 800 MHz reference phase locked to PXIe_CLK100. This allows the DDS to generate a 150 MHz to 300 MHz signal with microhertz resolution. The output from the DDS can then be divided down to lower frequencies, used directly, or multiplied up using a phase locked voltage controlled oscillator.

The individual components which make up the clock generation circuitry are controlled by NI-Sync software, which allows the user to simply specify the frequency they wish the clock generation circuitry to produce. NI-Sync then configures the clock generation circuitry to give the closest possible frequency match to the requested frequency and do so with the configuration that gives the lower possible phase noise. The user may request a clock frequency of 1 GHz (frequencies beyond 1 GHz are possible, but performance is not specified). The precision of the frequency generated is that of the DDS scaled up or down for any division or multiplication done to generate the requested frequency, as shown in the following table.

Table 8. Clock Generation Frequency and Resolution

Clock Generation Frequency	Resolution
18.75 MHz to 37.5 MHz	0.355 µHz
37.5 MHz to 75 MHz	0.711 µHz
75 MHz to 150 MHz	1.42 µHz
150 MHz to 300 MHz	2.84 µHz
300 MHz to 600 MHz	5.68 µHz
600 MHz to 1 GHz	11.4 µHz

Generating Clocks Using the Precise 10 MHz OCXO

The 800 MHz reference of the DDS clock generation circuitry is phase locked to PXIe_CLK100; therefore, its frequency accuracy is inherited from PXIe_CLK100. To give the best frequency accuracy, the OCXO of the PXIe-6674T can be routed to PXI_CLK10_IN. The chassis can then use the PXI_CLK10_IN to lock PXIe_CLK100 and PXI_CLK10. In addition, using the OCXO also lowers the phase noise of the generated clock frequency.

PXI_CLK10 and PXIe_CLK100

The PXI Express architecture allows a module in the system timing slot to provide a 10 MHz reference clock to the backplane for use in creating PXI_CLK10 and PXIe_CLK100. This is done by using the PXI_CLK10_IN pin on the backplane connector of the system timing slot.

Most PXI Express backplane architectures employ a PLL to lock a 100 MHz reference oscillator to the signal coming from the PXI_CLK10_IN pin. This 100 MHz reference is then used to directly create PXIe_CLK100 and is divided down by ten to create PXI_CLK10. One advantage of the PXI Express architecture is that the PXI_CLK10 and PXIe_CLK100 are always sourced from the same reference oscillator, and therefore it is impossible to lose PXI_CLK10 or PXIe_CLK100 by disconnecting the reference provided on PXI_CLK10_IN. For the same reason, it is also impossible for a runt pulse or glitch to occur on these lines as references are switched in and out, protecting the integrity of digital circuitry operating on these clocks.

Another feature of the PXI Express architecture is that the phase noise performance of PXI_CLK10 and PXIe_CLK100 is fixed beyond the bandwidth of the PLL loop of the backplane, regardless of the quality of the reference used. This is advantageous if a reference with poor phase noise performance is used, but it also means that supplying a high-end, low phase noise reference does not greatly improve PXI_CLK10 or PXIe_CLK100.

Using PXI_CLK10_IN

The PXIe-6674T provides three options for driving a clock to the backplane using PXI_CLK10_IN: OCXO, CLKIN, and 10 MHz PLL.

OCXO

The PXIe-6674T features a precision 10 MHz oven controlled crystal oscillator (OCXO). The main source of frequency error in reference oscillators is temperature variation. An OCXO minimizes this error by housing the crystal oscillator circuit inside a sealed oven, which is maintained at a constant temperature higher than the ambient temperature external to the OCXO. This results in a reference oscillator that is several orders of magnitude more stable and accurate than regular crystal oscillators.

Because the OCXO must warm up to a higher temperature than the ambient temperature around it, there is a warm-up time required to achieve the specified frequency accuracy. For this reason, to achieve the most stable operation of the OCXO it is desirable to avoid powering off the OCXO.

The OCXO used by the PXIe-6674T features electronic frequency control. This allows the OCXO to be fine-tuned by varying the control voltage to the OCXO. The PXIe-6674T uses a 16-bit digital analog converter to give precise control of the tuning voltage. While the tuning voltage can be varied by the user, it is normally controlled automatically by software, which sets it to the calibration tuning voltage. The PXIe-6674T is calibrated during the manufacturing process and should be recalibrated annually to remove frequency error that accumulates over time (such as crystal aging). Refer to **PXIe-6674T Calibration Executive Procedure** for more details.

The OCXO can also be routed to the CLKOUT SMA and be used as a trigger synchronization clock inside the FPGA.

CLKIN

The PXIe-6674T allows the user to connect their own 10 MHz reference directly to PXI_CLK10_IN by using the CLKIN SMA on the front panel. CLKIN is an AC-coupled, 50 Ω terminated input to the PXIe-6674T. In order to increase the amplitude of signals the CLKIN receiver can use, the CLKIN circuitry features software enabled attenuation, which attenuates the input signal by a factor of five when enabled. By default, the NI-Sync software configures the attenuation to be enabled. If the input signal supplied to CLKIN is less than 1.2 V_{pp}, the attenuation should be turned off in order to extend down the range of amplitudes CLKIN can receive.

When using CLKIN for driving PXI_CLK10_IN, refer to the user manual for your PXI Express chassis for information on the frequency range your chassis is capable of receiving on PXI_CLK10_IN.

CLKIN can also be routed to the DSTARA network and be used as a trigger synchronization clock inside the FPGA.

10 MHz PLL

The PXIe-6674T features a phase locked loop (PLL) circuit for aligning the frequency of the OCXO with a reference clock supplied by the user from CLKIN. In this configuration, the OCXO is routed to the backplane on PXI_CLK10_IN. The PXI Express backplane will in turn phase lock the PXI_CLK10 and PXIe_CLK10 signal to the PXI_CLK10_IN signal. The PXIe-6674T uses the PXI_CLK10 signal it receives from the backplane as feedback to the 10 MHz PLL circuitry. The PLL circuitry controls the frequency of the OCXO by varying the tuning voltage used for electronic frequency control. By increasing or decreasing the frequency of the OCXO as needed, the 10 MHz PLL of the PXIe-6674T is able to match the OCXO frequency to the reference clock supplied by the user from CLKIN.

Use of the 10 MHz PLL of the PXIe-6674T has advantages over using just CLKIN to drive PXI_CLK10_IN:

- Reference frequencies other than 10 MHz can be used. The 10 MHz PLL includes internal dividers to divide both the reference from CLKIN and PXI_CLK10 down as needed in order to make both a common frequency. This frequency is called the phase detector frequency, as it is the frequency at which the PLL compares edge alignment to determine if it should speed up or slow down the OCXO. NI-Sync allows any reference frequency that is an integer multiple of 1 MHz to be used.
- The 10 MHz PLL acts as a zero-delay buffer between the CLKIN SMA and PXI_CLK10/PXIe_CLK100 at the backplane connector. Because the 10 MHz PLL uses PXI_CLK10 for feedback, it is able to create a known fixed phase relation between PXI_CLK10 and the reference supplied on CLKIN. During manufacturing, the phase relation the 10 MHz PLL maintains is adjusted so that a rising edge at the CLKIN SMA will align in time with a rising edge of PXI_CLK10 at the peripheral slot connector of the backplane. This phase

relation will remain in place regardless of the PXI Express chassis used, allowing for simpler multi-chassis system synchronization.

PXIe_DSTARA, PXIe_DSTARB, and PXIe_DSTARC

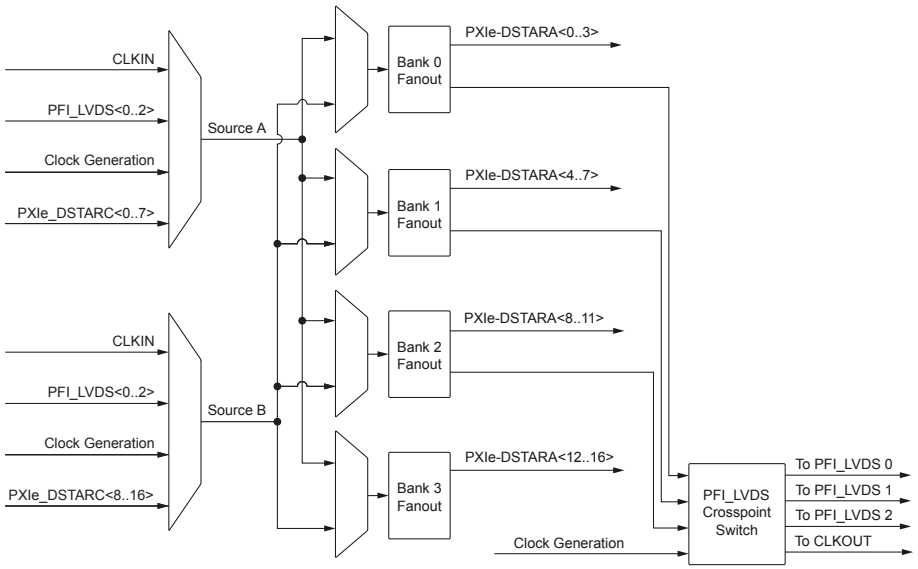
The PXI Express architecture includes a set of three high-speed differential signal paths to connect the system timing slot to each PXI Express peripheral slot (up to 17 peripheral slots). These signals are PXIe_DSTARA, PXIe_DSTARB, and PXIe_DSTARC.

- PXIe_DSTARA—PXIe_DSTARA is used to send clock signals from the system timing slot to each PXI Express peripheral slot in a star configuration. PXIe_DSTARA uses LVPECL signaling and closely matched trace lengths to achieve low skew, high-speed clock routing capabilities.
- PXIe_DSTARB—PXIe_DSTARB is used to send trigger signals from the system timing slot to each PXI Express peripheral slot in a star configuration. PXIe_DSTARB uses LVDS signaling and closely matched trace lengths to achieve faster, more precise triggering than is achievable with PXI_STAR or PXI_TRIG.
- PXIe_DSTARC—PXIe_DSTARC is used to send trigger signals from each PXI Express peripheral slot to the system timing slot in a star configuration. PXIe_DSTARC uses LVDS signaling and closely matched trace lengths and can be used to send a trigger signal or clock signal to the system timing slot module. The PXIe-6674T receives each PXIe_DSTARC signal and sends a copy to the PXIe_DSTARA network for clock sharing and to the FPGA for trigger routing.

PXIe_DSTARA Network

To achieve the high-speed, low skew routing performance required for PXIe_DSTARA, the PXIe-6674T uses circuitry specifically designed for routing clock signals to PXIe_DSTARA<0..16>. NI-Sync software automatically handles the routing through the PXIe_DSTARA network. However because the PXIe_DSTARA Network limits the number of connections that can be made, it is important to understand the underlying hardware architecture. The following figure provides an overview of the PXIe_DSTARA network:

Figure 6. PXIe_DSTARA Network



To drive signals out on the PXIe_DSTARA lines, the PXIe_DSTARA network divides the 17 PXIe_DSTARA lines into four banks, as shown in the following table:

Table 9. PXIe_DSTARA Divisions

Bank 0	Bank 1	Bank 2	Bank 3
PXIe_DSTARA<0..3>	PXIe_DSTARA<4..7>	PXIe_DSTARA<8.11>	PXIe_DSTARA<12..16>
PFI_LVDS cross point	PFI_LVDS cross point	PFI_LVDS cross point	—

All PXIe_DSTARA lines in a single bank share the same source. Each one of the banks can select from either Source A or Source B. Additionally, banks 0, 1, and 2 send a copy of their output to the PFI_LVDS cross point switch for routing out the front panel using PFI lines in LVDS mode. Refer to **PFI_LVDS<0..2>** for more information.

Note Only clock signals should be routed through the PXIe_DSTARA lines. PXIe_DSTARA lines may exhibit unexpected behavior when routing conventional triggers.

Note Because a single integrated circuit is used to make the five outputs in each bank, tighter skew is achieved within a single Bank than from Bank to Bank.

PFI_LVDS<0..2>

To allow for sending and receiving signals between system timing modules that are too fast for single-ended PFI signaling, two PFI SMA connectors can be combined to send or receive LVDS signals. The following table shows the relation between the front panel SMA connectors used for PFI and PFI_LVDS.

Table 10. Combinations of PFI Lines for PFI_LVDS

PFI Line	PFI_LVDS Line
PFI 0	PFI_LVDS 0 Negative
PFI 1	PFI_LVDS 0 Positive
PFI 2	PFI_LVDS 1 Negative
PFI 3	PFI_LVDS 1 Positive
PFI 4	PFI_LVDS 2 Negative
PFI 5	PFI_LVDS 2 Positive

Each of the three PFI_LVDS can be enabled for LVDS operation or used for two single-ended PFIs. When enabled for LVDS operation, the PFI_LVDS pair can be configured as either an input or an output. PFI_LVDS lines cannot be used as an input and output at the same time.

Because of the increased speed capabilities, the PFI_LVDS includes additional routing capabilities not offered with the single-ended PFI. When used as an input, the PFI_LVDS signal goes to both the FPGA for trigger routing and to the PXIe_DSTARA Network for use in routing high-speed clocks. When used as an output, the PFI_LVDS can be sourced from the FPGA for trigger usage, or from a 4x4 cross point switch which allows for any of the four inputs to be connected to any of the four outputs. The following table shows the inputs and outputs of the cross point switch.

Table 11. PFI_LVDS Inputs and Outputs

Inputs	Outputs
PXIe_DSTARA Network Bank 0	PFI_LVDS 0
PXIe_DSTARA Network Bank 1	PFI_LVDS 1
PXIe_DSTARA Network Bank 2	PFI_LVDS 2
Clock Generation	High-Speed CLKOUT

If the PFI_LVDS output is used for trigger routing, it is sourced from the FPGA and has all the same trigger routing characteristics as other trigger destinations. Refer to **Using Front Panel PFIs for LVDS Triggers** for details on using PFI_LVDS for sending and receiving trigger signals.

CLKOUT

The CLKOUT SMA connector on the front panel provides a means to export a clock signal from the PXIe-6674T to an external device or another system timing module. The CLKOUT driver uses two separate circuits for driving CLKOUT, one for low-speed frequencies (50 MHz and below) and one for high-speed frequencies (above 50 MHz). The low-speed driver uses 5 V CMOS logic with source impedance of 50 Ω and is AC-coupled. The high-speed driver produces an 800 mV_{pp} swing into a 50 Ω load and is also AC-coupled.

The sources available to be routed to CLKOUT differ depending on whether the low-speed or high-speed driver is used. The sources available to the low-speed driver are PXI_CLK10, OCXO, and Clock Generation for generated frequencies 100 MHz and below. Sources available to the high-speed CLKOUT are Clock Generation and outputs from the PXIe_DSTARA network through the PFI_LVDS cross point switch.

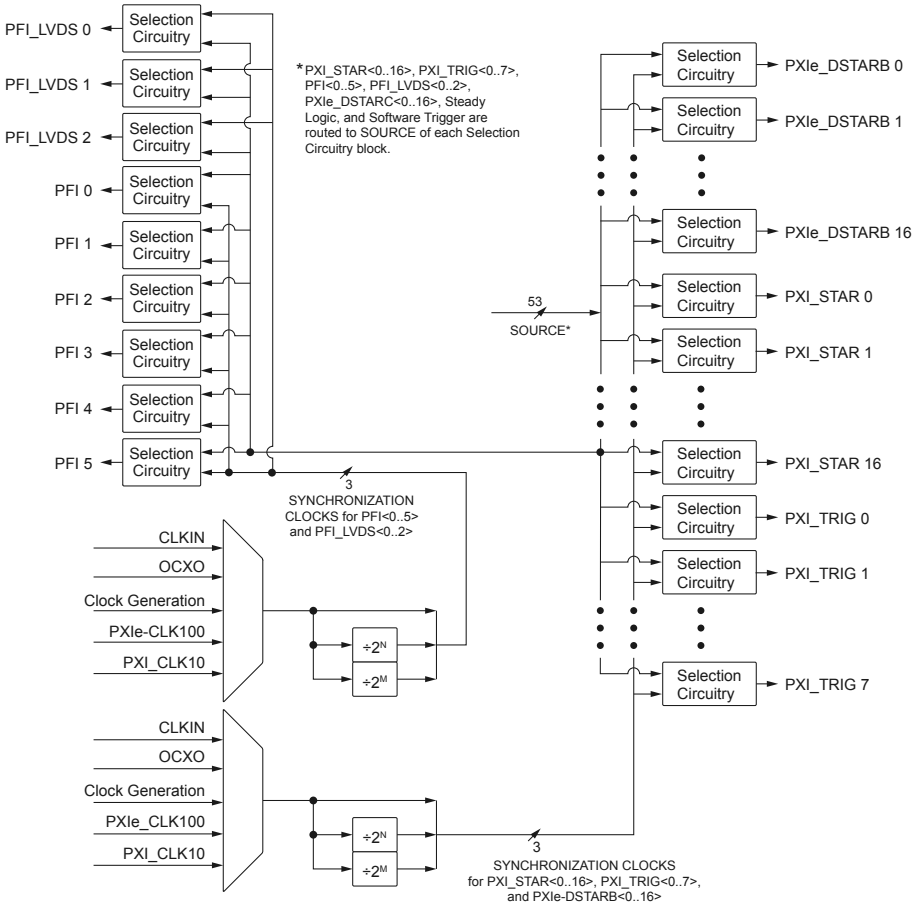
NI-Sync software selects the low-speed or high-speed driver automatically based on the source connected to CLKOUT.

Routing Signals

The PXIe-6674T has versatile trigger routing capabilities. It can route signals to and from the front panel, the PXI star triggers, PXIe_DSTARB, and PXIe_DSTARC.

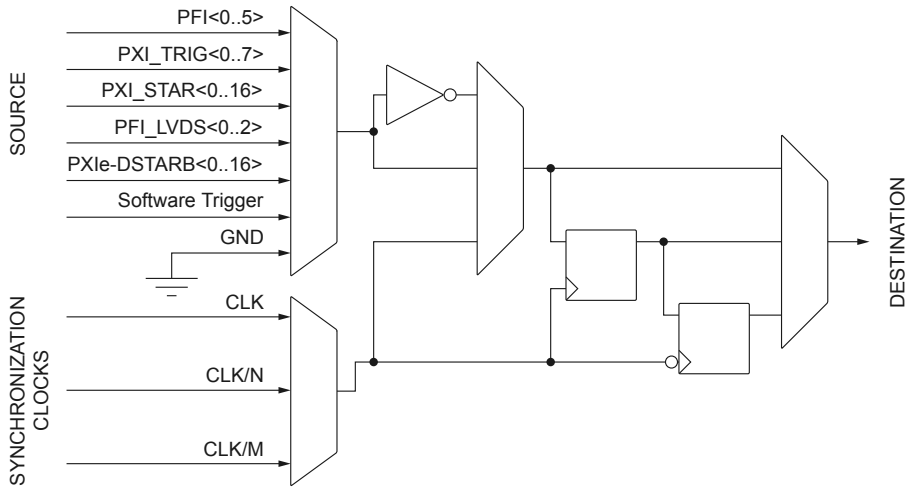
Refer to the following figure for the routing features of the PXIe-6674T.

Figure 7. High-Level Schematic of PXIe-6674T Signal Routing Architecture



The following figure provides a more detailed view of the Selection Circuitry.

Figure 8. PXIe-6674T Signal Selection Circuitry Diagram



Determining Sources and Destinations

All signal routing operations can be characterized by a source (input) and a destination. In addition, synchronous routing operations must also define a third signal known as the synchronization clock. Refer to **Choosing the Type of Routing** for more information on synchronous versus asynchronous routing.

The following figure summarizes the sources and destinations of the PXIe-6674T. The destinations are listed in the horizontal heading row, and the sources are listed in the column at the far left. A check in a cell indicates that the source and destination combination defined by that cell is a valid routing combination.

Figure 9. Sources and Destinations for PXIe-6674T Signal Routing Operations

Sources		Destinations: Front Panel: CLK OUT	PFI <0..5>	PFI LVDS <0..2>	Backplane: PXI CLK 10 IN	PXI Star Trigger <0..16>	PXI TRIG <0..7>	DSTARA <0..16>	DSTARB <0..16>	Onboard: OCXO Ref PLL
Front Panel	CLKIN	✓	✓†	✓†	✓	✓†	✓†	✓	✓†	✓
	PFI <0..5>		✓	✓		✓	✓		✓	
	PFI LVDS <0..2>		✓	✓		✓	✓	✓	✓	
Backplane	PXI CLK 10	✓	✓†	✓†		✓†	✓†		✓†	
	PXI CLK 100	✓	✓†	✓†		✓†	✓†		✓†	
	PXI STAR <0..16>		✓	✓		✓	✓		✓	
	PXI TRIG <0..7>		✓	✓		✓	✓		✓	
	DSTARC <0..16>		✓	✓		✓	✓	✓	✓	
Onboard	OCXO	✓	✓†	✓†	✓	✓†	✓†		✓†	
	Clock Gen	✓	✓†	✓		✓†	✓†	✓	✓†	
	Global Software Trigger		✓	✓		✓	✓		✓	

† Routing PXI_CLK10, PXIe_CLK100, OCXO or CLKGen is accomplished by setting the synchronization clock (using the NI-Sync Property Node) to the desired clock source and then routing the synchronization clock as the source.

Route through the FPGA.

Route to PFI LVDS can be made through the FPGA when used as a trigger, or through the PXIe-DSTARA network when used as a clock.

Related concepts:

- Choosing the Type of Routing

Using Front Panel PFIs as Single-Ended Inputs

The front-panel PFIs can receive external signals from 0 to +5 V. They can be terminated programmatically with 50 Ω resistances to match the cable impedance and minimize reflections.

Note Terminating the signals with a 50 Ω resistance is recommended when the source is another PXIe-6674T or any other source with a 50 Ω output.

The voltage thresholds for the front-panel PFI inputs are programmable. The input signal is generated by comparing the input voltage on the PFI connectors to the voltage output of software-programmable DACs. The thresholds for the PFI lines are individually programmable, which is useful if you are importing signals from multiple sources with different voltage swings.

Using Front Panel PFIs as Single-Ended Outputs

The front panel PFI outputs are +3.3 V drivers with 50 Ω output impedance. The outputs can drive 50 Ω loads, such as a 50 Ω coaxial cable with a 50 Ω receiver. This cable configuration is the recommended setup to minimize reflections. With this configuration, the receiver sees a single +1.6 V step—a +3.3 V step split across the 50 Ω resistors at the source and the destination.

You also can drive a 50 Ω cable with a high-impedance load. The destination sees a single step to +3.3 V, but the source sees a reflection. This cable configuration is acceptable for low-frequency signals or short cables.

You can independently select the output signal source for each PFI line from one of the following sources.

- Another PFI<0..5>
- Another PFI pair in LVDS mode.
- PXI triggers <0..7> (PXI_TRIG<0..7>
- PXI_STAR<0..16>
- Global software trigger
- PFI synchronization clock
- PXIe_DSTARC
- Steady logic high or low.

The PXI synchronization clock may be any of the following signals:

- Clock Generation
- PXI_CLK10
- PXIe_CLK100
- OCXO
- CLKIN
- Any of the previously listed signals divided by the first frequency divider (2^n, up to 512)
- Any of the previously listed signals divided by the second frequency divider(2^m, up to 512)

Refer to **Choosing the Type of Routing** section for more information on the synchronization clock.

Note The PFI synchronization clock is the same for all routing operations in which PFI<0..5> or PFI_LVDS<0..2> is defined as the output, although the divide-down ratio for this clock (full rate, first divider, second divider) may be chosen on a per-route basis.

Related concepts:

- Choosing the Type of Routing

Using Front Panel PFIs for LVDS Triggers

To allow for sending and receiving signals between system timing modules that are too fast for single-ended PFI signaling, two PFI SMA connectors can be combined to send or receive LVDS signals. Refer to the **Combinations of PFI Lines for PFI_LVDS** table in **PXIe_DSTARA, PXIe_DSTARB, and PXIe_DSTARC** for the relation between the front panel SMA connectors used for PFI and PFI_LVDS.
When used for trigger routing, the PFI_LVDS signals are routed to and from the FPGA. You can independently select the output signal source for each PFI_LVDS line from one of the following sources:

- Another PFI<0..5>
- Another PFI pair in LVDS mode.
- PXI triggers <0..7> (PXI_TRIG<0..7>)
- PXI_STAR<0..16>
- Global software trigger
- PFI synchronization clock
- PXIe_DSTARC
- Steady logic high or low.

The PFI synchronization clock is also used for the PFI_LVDS and as such may be one of the following signals:

- Clock Generation
- PXI_CLK10

- PXIe_CLK100
- OCXO
- CLKIN
- Any of the previously listed signals divided by the first frequency divider (2^n, up to 512)
- Any of the previously listed signals divided by the second frequency divider (2^m, up to 512)

Refer to the **Choosing the Type of Routing** section for more information on the synchronization clock.

Note The PFI synchronization clock is the same for all routing operations in which PFI<0..5> or PFI_LVDS<0..2> is defined as the output, although the divide-down ratio for this clock (full rate, first divider, second divider) may be chosen on a per route basis.

Related concepts:

- PXIe_DSTARA, PXIe_DSTARB, and PXIe_DSTARC

Using the PXI Triggers

The PXI triggers go to all the slots in the chassis. All modules receive the same PXI triggers, so PXI trigger 0 is the same for the system timing slot as it is for Slot 3, and so on. This feature makes the PXI triggers convenient in situations where you want, for instance, to start an acquisition on several devices at the same time because all modules receive the same trigger.

The frequency on the PXI triggers should not exceed 5 MHz to preserve signal integrity. The signals do not reach each slot at precisely the same time. A difference of several nanoseconds between slots can occur in an eight-slot chassis. However, this delay is not a problem for many applications.

You can independently select the output signal source for each PXI trigger line from one of the following sources.

- PFI<0..5>
- PFI_LVDS<0..2>
- Another PXI trigger <0..7> (PXI_TRIG<0..7>)

- PXI_STAR<0..16>
- Global software trigger
- Backplane synchronization clock
- PXIe_DSTARC
- Steady logic high or low

The backplane synchronization clock may be any of the following signals.

- Clock Generation
- PXI_CLK10
- PXIe_CLK100
- OCXO
- CLKIN
- Any of the previously listed signals divided by the first frequency divider (2^n, up to 512).
- Any of the previously listed signals divided by the second frequency divider (2^m, up to 512).

Refer to **Choosing the Type of Routing** for more information about the synchronization clock.

Note The backplane synchronization clock is the same for all routing operations in which PXI_TRIG<0..7>, PXIe_DSTARB<0..16>, or PXI_STAR<0..16> is defined as the output, although the divide-down ratio for this clock (full rate, first divider, second divider) may be chosen on a per route basis.

Related concepts:

- Choosing the Type of Routing

Using the PXI Star Triggers

There are up to 17 PXI star triggers per chassis. Each trigger line is a dedicated connection between the system timing slot and one other slot. The **PXI Specification, Revision 2.1** requires that the propagation delay along each star

trigger line be matched to within 1 ns. A typical upper limit for the skew in most NI PXI Express chassis is 500 ps. The low skew of the PXI star trigger bus is useful for applications that require triggers to arrive at several modules nearly simultaneously.
The star trigger lines are bidirectional, so signals can be sent to the system timing slot from a module in another slot or from the system timing slot to the other module.
You can independently select the output signal source for each PXI star trigger line from one of the following sources:

- PFI<0..5>
- PFI_LVDS<0..2>
- PXI triggers <0..7> (PXI_TRIG<0..7>)
- Another PXI star trigger line (PXI_STAR<0..16>)
- Global software trigger
- Backplane synchronization clock
- PXIe_DSTARC
- Steady logic high or low

Refer to **Using the PXI Triggers** for more information on the backplane synchronization clock.

Related concepts:

- Using the PXI Triggers

Related information:

- PXI Specification

Using the PXIe_DSTARB and PXIe_DSTARC Triggers

To improve beyond the performance the PXI Star triggers offer in low skew trigger routing, PXI Express implements PXIe_DSTARB and PXIe_DSTARC triggers. Each PXI Express peripheral slot in a PXI Express chassis has independent PXIe_DSTARB and PXIe_DSTARC connections with the system timing slot module. The PXIe_DSTARB and PXIe_DSTARC lines are unidirectional. DSTARB lines are used for the system timing slot module to send triggers to peripheral modules. DSTARC lines are used for peripheral modules to send triggers to the system timing module. The PXI

Express Specification requires PXI Express chassis to limit the skew between any two PXIe_DSTAR routes to 150 ps, thus triggers are sent and received with low skew.
The PXIe-6674T can route PXIe_DSTARC inputs to both the PXIe_DSTARA network for use as a clock source and to the FPGA for use as a trigger source.
For the PXIe_DSTARB outputs, the PXIe-6674T can independently select from the following sources to be routed to PXIe_DSTARB:

- PFI<0..5>
- PFI_LVDS<0..2>
- PXI Triggers<0..7> (PXI_TRIG<0..7>)
- PXI Star Triggers (PXI_STAR<0..16>)
- PXIe_DSTARC<0..16>
- Global Software Trigger
- Steady logic high or low
- Backplane synchronization clock

Refer to **Using the PXI Triggers** for more information on the backplane synchronization clock.

Related concepts:

- Using the PXI Triggers

Choosing the Type of Routing

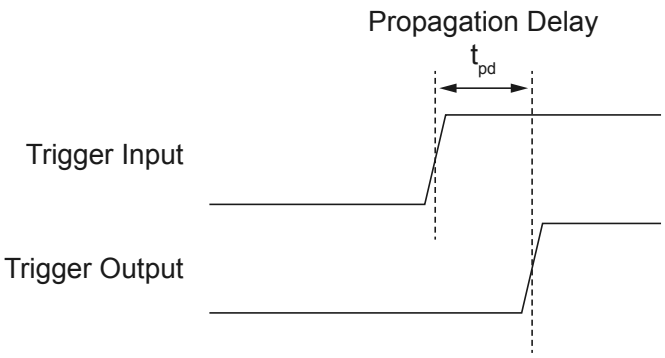
The PXIe-6674T routes signals in one of two ways: asynchronously or synchronously. The following sections describe the two routing types and the considerations for choosing each type.

Asynchronous Routing

Asynchronous routing is the most straightforward method of routing signals.

Any asynchronous route can be defined in terms of two signals: a source and a destination. A digital pulse or train comes in on the source and is propagated to the destination. When the source signal goes from low to high, this rising edge is transferred to the destination after a propagation delay through the module. The following figure illustrates an asynchronous routing operation.

Figure 10. Asynchronous Routing Operation



Some delay is always associated with an asynchronous route, and this delay varies among PXIe-6674T modules, depending on variations in temperature and chassis voltage. Typical delay times in the PXIe-6674T for asynchronous routes between various sources and destinations are given in the device's Specifications.

Asynchronous routing works well if the total system delays are not too long for the application. Propagation delay could be caused by the following reasons:

- Output delay on the source.
- Propagation delay of the signal across the backplane(s) and cable(s).
- Propagation delay of the signal through the PXIe-6674T.
- Time for the receiver to recognize the signal.

Both the source and the destination of an asynchronous routing operation on the PXIe-6674T can be any of the following lines:

- Any front panel PFI pin (PFI<0..5>) as single-ended.
- Any front panel PFI pin as LVDS (PFI_LVDS<0..2>)
- Any PXI star trigger line (PXI_STAR<0..16>)
- Any PXI trigger line (PXI_TRIG<0..7>)
- Any PXIe_DSTARB<0..16>

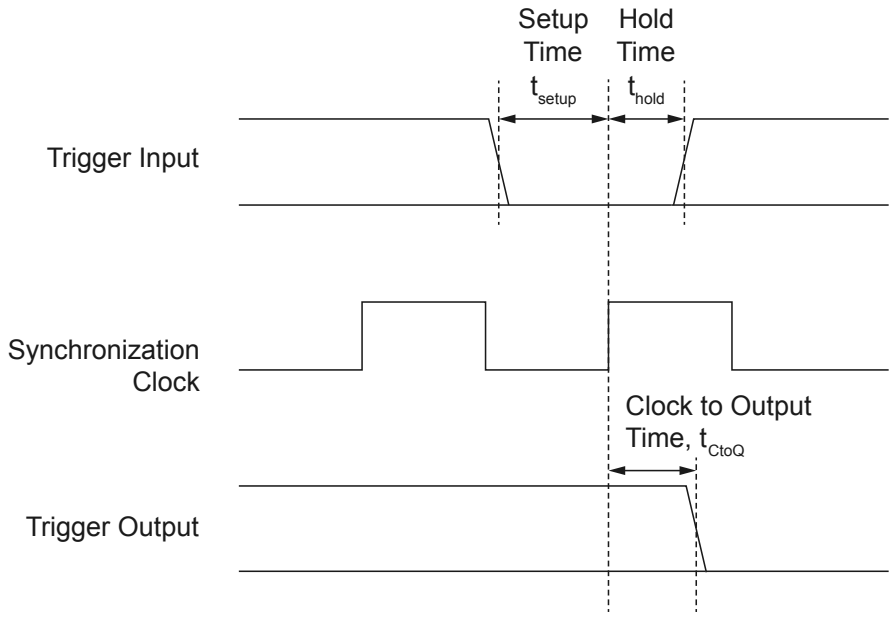
Synchronous Routing

A synchronous routing operation is defined in terms of three signals: a source, a destination, and a synchronization clock.

Unlike asynchronous routing, the output of a synchronous routing operation does not directly follow the input after a propagation delay. Instead, the logic state of the input is sampled on each active edge of the synchronization clock, and the output is set to that logic state after a small delay, as shown in the following figure. Thus, the output is said to be synchronous with this clock.

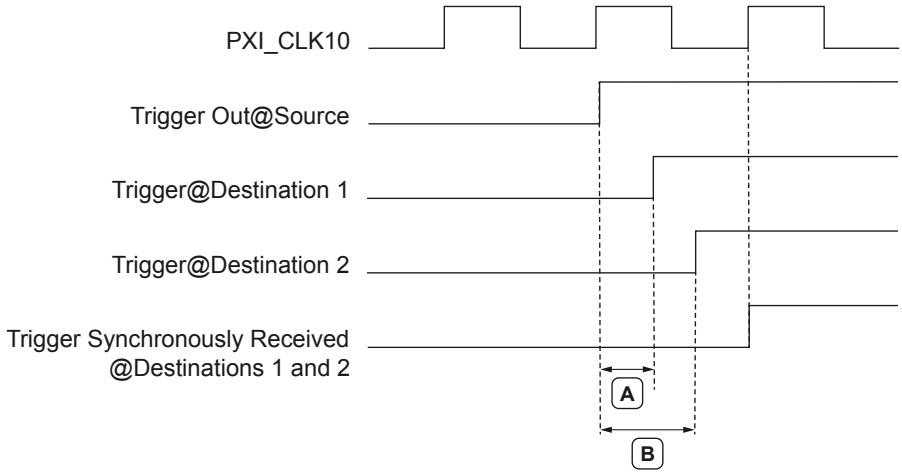
The following figure shows a timing diagram that illustrates synchronous routing.

Figure 13. Synchronous Routing Operation



The PXIe-6674T board supports synchronous routing to either the rising or falling edge of the synchronization clock. In addition, the polarity of the destination signal can be inverted, which is useful when handling active-low digital signals. Synchronous routing can be useful for eliminating skew when sending triggers to several destinations. For example, when sending triggers using the PXI Trigger lines, the trigger arrives at each slot at a slightly different time. However, if the trigger is sent and received synchronously using a low-skew synchronization clock (for example, PXI_CLK10), all receiving devices can act on the trigger at the same time, as shown in the following figure:

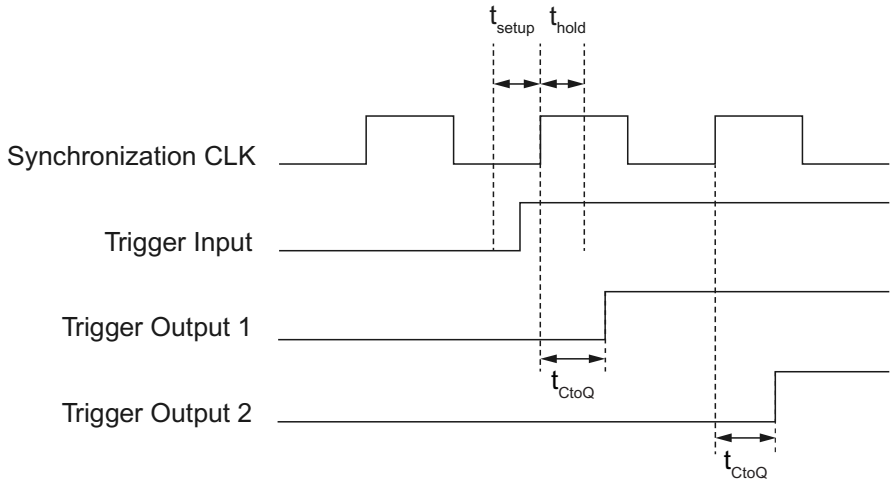
Figure 12. Synchronous Routing to Multiple Destinations



A: Propagation delay from source to destination 1.
B: Propagation delay from source to destination 2.

Synchronous routing requires the input to be stable at a logic low or logic high state within a window of time around the clock edge. This window of time around the clock edge is defined by the setup time (t_{setup}) and hold time (t_{hold}). If the input signal changes within this window of time, it is undetermined whether the output of the synchronous route will go to the old or new logic state. This is important, for example, if a source is being routed synchronously to several destinations. If the source signal changes within the setup-and-hold window around the synchronization clock edge, one of the destinations might go to the new logic level while the other destination might remain at the old logic level and change when the next synchronization clock edge occurs, as shown in the following figure:

Figure 13. Synchronous Routing Uncertainty with Setup-and-Hold Variation



Therefore, if your application requires that the trigger arrive at the multiple destinations simultaneously, you must ensure that the input is stable within the setup and hold window around the synchronization clock edge. For more information and possible methods to ensure this requirement is met, go to ni.com/info and enter the Info Code SyncTriggerRouting.

Possible sources for synchronous routing with the PXIe-6674T include the following sources:

- Any front panel PFI pin as single-ended.
- Any front panel PFI pin as LVDS.
- Any PXI star trigger line (PXI_STAR<0..16>)
- Any PXI trigger line (PXI_TRIG<0..7>)
- Any PXIe_DSTARC<0..16>
- Global software trigger
- The synchronization clock itself.

The synchronization clock for a synchronous route can be any of the following signals:

- 10 MHz PXI_CLK10
- 100 MHz PXIe_CLK100

- Clock Generation
- OCXO
- CLKIN
- One of two "divided copies" of any of the previously listed five signals.

The PXIe-6674T includes two clock-divider circuits that can divide the synchronization clock signals by any power of 2 up to 512.

Example Programs

NI-Sync includes several example applications that demonstrate the functionality of your device and can serve as interactive tools, programming models, and building blocks for your own applications.

NI Example Finder

The NI Example Finder is a utility that organizes examples into categories and allows you to browse and search installed examples. For example, search for "Sync" to locate all NI-Sync examples. You can see descriptions and compatible hardware models for each example or see all the examples compatible with one particular hardware model.

Select **Help** » **Find Examples** from LabVIEW to launch the NI Example Finder. You can modify an example VI to fit an application, or you can copy and paste from one or more examples into a VI that you create.

- For signal-based examples that use clocks and triggers directly, open the NI Example Finder and navigate to **Hardware Input and Output** » **Timing and Synchronization** » **Signal-Based**.
- For time-based examples that use time references such as IEEE 1588-2008 or GPS as a basis for synchronization, open the NI Example Finder and navigate to **Hardware Input and Output** » **Timing and Synchronization** » **Time-Based**.

Installed Example Locations

The installation location for NI-Sync example programs differs by programming language and development environment. Refer to the following table for information about example program installation locations.

Table 12. Installed NI-Sync Example Locations

Option	Installed Example Location
LabVIEW	<LabVIEW>\examples\instr\niSync, where <LabVIEW> is the directory for the specific LabVIEW version that is installed.
LabWindows/CVI	Users\Public\Documents\National Instruments\CVI\samples\niSync

Common Example Programs

The following example programs in NI Example Finder demonstrate common functions and operations of the PXIe-6674T.

- **Check Clk10 & Route Clock**—Uses the PLL circuit on the CLKIN input to check for the presence of an external clock.
- **Generate DDS Clock and Route**—Generates a clock signal using the onboard Direct Digital Synthesis (DDS) circuitry, and then routes the clock signal to the "Destination Terminal" specified.
- **Generate DDS Clock, Divide and Route**—Generates a clock signal using the onboard Direct Digital Synthesis (DDS) circuitry, and then routes the clock signal to the "Destination Terminal" specified. This example program also divides down the DDS clock with a given clock divisor (must be a power of 2) and routes that signal as well.
- **Measure Frequency on PFI0**—Measures the frequency of the TTL signal on PFI0.
- **PLL to External Clock and Drive PXI_CLK10_IN**—Uses the PLL circuit to lock to an external clock, and routes it to the PXI_CLK10 signal as well. It continues checking for PLL lock until the user stops the program.

- **Route Clock**—This example program can either replace the clock on the PXI backplane with a different clock, or it can route a clock from the chassis to the CLK OUT connector.
- **Route Ground to Trigger (Optional Invert)**—Routes a signal (Ground by default) to a specified destination. Specifically, this example program routes the signal from "Source Terminal" to "Destination Terminal".
- **Route Software Trigger**—Routes a software trigger to a hardware line. Specifically, this example program routes the software trigger to the line specified by "Destination Terminal".
- **Route to All PXI_STAR**—Routes triggers from a source trigger to the PXI_Star trigger. Specifically, this example program routes the triggers from the "Source Terminal" input to PXI_Star0 through PXI_Star16.
- **Route Trigger**—Routes triggers from an external line to the backplane, or from the backplane to an external line.
- **Share Clock Between Chassis**—Shares a common clock between two chassis.
- **Share PXI_CLK10 & Trigger Between Chassis**—Shares a common clock between two chassis, as well as a trigger.
- **Share PXI_CLK10 and Synchronous Trigger Between Chassis**—Shares a matched trace length clock and trigger between chassis, and synchronizes the triggers with the clock.
- **Share Trigger Between Chassis**—Shares a trigger signal between two chassis.

Calibration

Calibration of the PXIe-6674T consists of verifying the measurement accuracy of the device and correcting for any measurement error. The PXIe-6674T is factory calibrated before shipment at approximately 25 °C to the levels indicated in the **PXIe-6674T Specifications**. The associated calibration constants—the corrections that were needed to meet specifications—are stored in the onboard nonvolatile memory (EEPROM). The driver software uses these stored values.

Factory Calibration

The factory calibration of the PXIe-6674T involves calculating and storing four calibration constants. These values control the accuracy of two features of the device, which are discussed in the following sections.

OCXO Frequency

The OCXO frequency can be varied over a small range. The output frequency of the OCXO is adjusted using this constant to meet the specification listed in the PXIe-6674T Specifications.

PXI_CLK10 Phase

When using the PLL to lock PXI_CLK10 to an external reference clock, the phase between the clocks can be adjusted. The time between rising edges of PXI_CLK10 and the input clock is minimized using this constant.

Note The PXI_CLK10 phase is set during manufacturing and does not need to be recalibrated.

Cleaning the PXIe-6674T System

NI recommends the following to clean and maintain your instrument's system:

- Clean the fan filters on the chassis regularly to prevent fan blockage and to ensure efficient air circulation. Cleaning frequency depends on the amount of use and the operating environment. For specific information about cleaning procedures and other recommended maintenance, refer to the chassis user documentation.
- Clean the hardware with a soft, nonmetallic brush. Make sure that the hardware is completely dry and free from contaminants before returning it to service.