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LabVIEW PDM Acquisitions Toolkit Specifications

2022-09-29

Contents

PDM Acquisition Toolkit Specifications

The LabVIEW PDM Acquisition Toolkit supports the PXIe-7820R/7821R and USB-7845R/7846R. Refer to the product documentation for these hardware instruments on ni.com/manuals to view detailed specifications and getting started information.

PDM Acquisition Toolkit Specifications for PXIe-7820R/7821R

Refer to these specifications when using the LabVIEW PDM Acquisition Toolkit with the PXIe-7820R/7821R.

Input Characteristics

	Acquisition	Generation
Number of PDM data lines	32, consisting of four banks of 8 data lines and 2 clock lines	16
Number of PDM channels	64, consisting of four banks of 16 channels	32
Number of timing engines	2	1
Clock input/ output	Clock output—One master bit clock shared across 8 data lines (16 channels)	Clock input—One input shared across all output channels
Data, clock, and GPIO logical level	Single-ended logic 1.2 V, 1.8 V, and 3.3 V	Single-ended logic 1.2 V, 1.8 V, and 3.3 V
PDM clock rate	10 to 4800 kb/s, master mode only	10 to 4800 kb/s, slave mode only
Timebase reference source	PXI Express 100 MHz	N/A
Timebase accuracy error		
Divided clock	<2%, 250 ps peak-peak jitter	N/A
DDS clock	<100 ppm, 8.3 ns peak-peak jitter	N/A

	Acquisition	Generation
Phase/ Synchronization	All channels within a bank of 8 data lines are sampled synchronously from a common clock. Phase relationship between channels is fully maintained. Channels within a task are synchronized.	All channels are generated synchronously from the input clock. Phase relationship between channels is fully maintained.
Generation signal types	N/A	Sine, chirp (linear or logarithmic), white noise, and custom periodic signals
General purpose digital I/O (GPIO)	24 static GPIO lines can be configured independently as input or output lines	8 static GPIO lines can be configured independently as input or output lines

Refer to the **Bank to Channel Mapping for PXIe-7820R/7821R** section for the layout of banks, data lines, channels, and clock lines.

Decimation Filters

Decimation factor options	24, 32, 48, 64, 96, and 128. Select the option by task.

Decimation Filter Specifications

Decimation Factor	24 and 48	32 and 64	96 and 128
Normalized passband frequency	0.4275	0.438	0.45
Passband ripple (dB)	±0.0025	±0.001	±0.0004
Normalized stopband frequency	0.5725	0.562	0.55
Stopband attenuation (dB)	>110	>120	>123

Decimation Factor	24 and 48	32 and 64	96 and 128
Filter output delay (samples)	23	30	38

Acquisition and Generation Control

	Acquisition	Generation
Acquisition options	Raw PDM and/or PCM (decimated) data	N/A
Acquisition/Generation mode	Finite or Continuous	Continuous
Trigger options	Immediate or PXI-Trigger. Independent triggering on each task	Immediate or PXI-Trigger
Export signal options	N/A	Start trigger to a PXI trigger line
PXI trigger	PXI-Trig [0..7]. Rising or Falling edge	PXI-Trig [0..7]. Rising or Falling edge
Acquisition pre-delay	Common pre-delay for each task applied to both PDM and PCM data	N/A
Acquisition pre-delay resolution	1 PDM bitrate period	N/A
Acquisition pre-delay range	0 to 16383 bitrate periods	N/A
Acquisition post-delay	Common post-delay for each task and applied to decimated data	N/A
Acquisition post-delay resolution	1 decimated data period	N/A
Acquisition post-delay range	0 to 2^{27}-2 (134,217,726) decimated data periods	N/A

Simulation Mode

PDM simulation signal type	Sine tone with a PDM amplitude of ±0.7071 FS (0.500 RMS)

<table>
<tr><td>Tone frequency</td><td>Proportional to the selected PDM rate and repeats for every group of 16 PDM channel inputs.
For a PDM rate of 3.072 MHz, tone frequency is 1 kHz for the first PDM channel input, increments by 1 kHz for each PDM channel input, and repeats this sequence for every 16 PDM channel inputs. The following table illustrates the tone frequencies at 3.072 MHz for all 64 PDM channel inputs.
<table>
<tr><td>PDM Channel Input 0L</td><td>1 kHz</td></tr>
<tr><td>PDM Channel Input 0R</td><td>2 kHz</td></tr>
<tr><td>...</td><td></td></tr>
<tr><td>PDM Channel Input 7L</td><td>15 kHz</td></tr>
<tr><td>PDM Channel Input 7R</td><td>16 kHz</td></tr>
<tr><td>PDM Channel Input 8L</td><td>1 kHz</td></tr>
<tr><td>PDM Channel Input 8R</td><td>2 kHz</td></tr>
<tr><td>...</td><td></td></tr>
<tr><td>PDM Channel Input 31L</td><td>15 kHz</td></tr>
<tr><td>PDM Channel Input 31R</td><td>16 kHz</td></tr>
</table>
Refer to the Bank to Channel Mapping for PXIe-7820R/7821R section for the layout of banks, data lines, channels, and clock lines.</td></tr>
<tr><td>Tone start phase</td><td>0 degree for all tones when using the Configure PDM Trigger (None) VI</td></tr>
</table>

Related information

- Configure PDM Trigger VI

Bank to Channel Mapping for PXIe-7820R/7821R

The following table illustrates the bank to channel mapping for the PXIe-7820R/7821R.

Bank 0	PDM Data Input 0	PDM Channel Input 0L	Bank 2	PDM Data Input 16	PDM Channel Input 16L
		PDM Channel Input 0R			PDM Channel Input 16R
	...	.		...	.

		.			.
		.			.
	PDM Data Input 7	PDM Channel Input 7L		PDM Data Input 23	PDM Channel Input 23L
		PDM Channel Input 7R			PDM Channel Input 23R
	Clock 0,1			Clock 4,5	
Bank 1	PDM Data Input 8	PDM Channel Input 8L	Bank 3	PDM Data Input 24	PDM Channel Input 24L
		PDM Channel Input 8R			PDM Channel Input 24R
	...	.		...	.
		.			.
		.			.
	PDM Data Input 15	PDM Channel Input 15L		PDM Data Input 31	PDM Channel Input 31L
		PDM Channel Input 15R			PDM Channel Input 31R
	Clock 2,3			Clock 6,7	

Connector Pin Assignments for PXIe-7820R/7821R PDM Acquisition

Use the following connector pin assignments when you configure pin functions for PDM acquisition using the PXIe-7820R/7821R.

Connector 0

Terminal	Function	Assignment
1	DIO31	PDM Input 15
2	GND	
3	DIO29	GPIO 11
4	GND	
5	DIO27	GPIO 9

Terminal	Function	Assignment
6	GND	
7	DIO25	PDM Input 13
8	GND	
9	DIO23	PDM Input 11
10	GND	
11	DIO21	PDM Input 9
12	GND	
13	DIO19	PDM Clock Output 3
14	GND	
15	DIO17	GPIO 7
16	GND	
17	DIO15	GPIO 5
18	GND	
19	DIO13	PDM Clock Output 1
20	GND	
21	DIO11	PDM Input 7
22	GND	
23	DIO9	PDM Input 5
24	GND	
25	DIO7	PDM Input 3
26	GND	
27	DIO5	GPIO 3
28	GND	
29	DIO3	GPIO 1
30	GND	
31	DIO1	PDM Input 1
32	GND	
33	GND	
34	GND	
35	DIO30	PDM Clock Output 2
36	GND	

Terminal	Function	Assignment
37	DIO28	PDM Input 14
38	GND	
39	DIO26	PDM Input 12
40	GND	
41	DIO24	PDM Input 10
42	GND	
43	DIO22	GPIO 10
44	GND	
45	DIO20	GPIO 8
46	GND	
47	DIO18	GPIO 6
48	GND	
49	DIO16	PDM Input 8
50	GND	
51	DIO14	PDM Input 6
52	GND	
53	DIO12	GPIO 4
54	GND	
55	DIO10	GPIO 2
56	GND	
57	DIO8	GPIO 0
58	GND	
59	DIO6	PDM Input 4
60	GND	
61	DIO4	PDM Input 2
62	GND	
63	DIO2	PDM Input 0
64	GND	
65	DIO0	PDM Clock Output 0
66	GND	
67	External Clock **x***	

Terminal	Function	Assignment
68	GND	
* **x** is the connector number. External Clock **x** is an input only.		

Connector 1

Terminal	Function	Assignment
1	DIO31	PDM Input 31
2	GND	
3	DIO29	GPIO 23
4	GND	
5	DIO27	GPIO 21
6	GND	
7	DIO25	PDM Input 29
8	GND	
9	DIO23	PDM Input 27
10	GND	
11	DIO21	PDM Input 25
12	GND	
13	DIO19	PDM Clock Output 7
14	GND	
15	DIO17	GPIO 19
16	GND	
17	DIO15	GPIO 17
18	GND	
19	DIO13	PDM Clock Output 5
20	GND	
21	DIO11	PDM Input 23
22	GND	
23	DIO9	PDM Input 21
24	GND	
25	DIO7	PDM Input 19

Terminal	Function	Assignment
26	GND	
27	DIO5	GPIO 15
28	GND	
29	DIO3	GPIO 13
30	GND	
31	DIO1	PDM Input 17
32	GND	
33	GND	
34	GND	
35	DIO30	PDM Clock Output 6
36	GND	
37	DIO28	PDM Input 30
38	GND	
39	DIO26	PDM Input 28
40	GND	
41	DIO24	PDM Input 26
42	GND	
43	DIO22	GPIO 22
44	GND	
45	DIO20	GPIO 20
46	GND	
47	DIO18	GPIO 18
48	GND	
49	DIO16	PDM Input 24
50	GND	
51	DIO14	PDM Input 22
52	GND	
53	DIO12	GPIO 16
54	GND	
55	DIO10	GPIO 14
56	GND	

Terminal	Function	Assignment
57	DIO8	GPIO 12
58	GND	
59	DIO6	PDM Input 20
60	GND	
61	DIO4	PDM Input 18
62	GND	
63	DIO2	PDM Input 16
64	GND	
65	DIO0	PDM Clock Output 4
66	GND	
67	External Clock **x***	
68	GND	
* **x** is the connector number. External Clock **x** is an input only.		

Connector Pin Assignments for PXIe-7820R/7821R PDM Generation

Use the following connector pin assignments when you configure pin functions for PDM generation using the PXIe-7820R/7821R.

Connector 0

Terminal	Function	Assignment
1	DIO31	PDM Output 15
2	GND	
3	DIO29	
4	GND	
5	DIO27	
6	GND	
7	DIO25	PDM Output 13
8	GND	
9	DIO23	PDM Output 11

Terminal	Function	Assignment
10	GND	
11	DIO21	PDM Output 9
12	GND	
13	DIO19	
14	GND	
15	DIO17	GPIO 7
16	GND	
17	DIO15	GPIO 5
18	GND	
19	DIO13	
20	GND	
21	DIO11	PDM Output 7
22	GND	
23	DIO9	PDM Output 5
24	GND	
25	DIO7	PDM Output 3
26	GND	
27	DIO5	GPIO 3
28	GND	
29	DIO3	GPIO 1
30	GND	
31	DIO1	PDM Output 1
32	GND	
33	GND	
34	GND	
35	DIO30	
36	GND	
37	DIO28	PDM Output 14
38	GND	
39	DIO26	PDM Output 12
40	GND	

Terminal	Function	Assignment
41	DIO24	PDM Output 10
42	GND	
43	DIO22	
44	GND	
45	DIO20	
46	GND	
47	DIO18	GPIO 6
48	GND	
49	DIO16	PDM Output 8
50	GND	
51	DIO14	PDM Output 6
52	GND	
53	DIO12	GPIO 4
54	GND	
55	DIO10	GPIO 2
56	GND	
57	DIO8	GPIO 0
58	GND	
59	DIO6	PDM Output 4
60	GND	
61	DIO4	PDM Output 2
62	GND	
63	DIO2	PDM Output 0
64	GND	
65	DIO0	PDM Clock 0
66	GND	
67	External Clock **x***	
68	GND	
* **x** is the connector number. External Clock **x** is an input only.		

PDM Acquisition Toolkit Specifications for USB-7845R/7846R

Refer to these specifications when using the LabVIEW PDM Acquisition Toolkit with the USB-7845R/7846R.

Input Characteristics

	Acquisition	Generation
Number of PDM data lines	8, consisting of one bank of 8 data lines and 2 clock lines	8
Number of PDM channels	16	16
Number of timing engines	1	1
Clock input/ output	Clock output—One master bit clock shared across 8 data lines (16 channels)	Clock input—One input shared across all output channels
Data, clock, and GPIO logical level	Single-ended logic 1.2 V, 1.8 V, and 3.3 V	Single-ended logic 1.2 V, 1.8 V, and 3.3 V
PDM clock rate	10 to 4800 kb/s, master mode only	10 to 4800 kb/s, slave mode only
Timebase reference source	PXI Express 100 MHz	N/A
Timebase accuracy error		
Divided clock	<2%, 250 ps peak-peak jitter	N/A
DDS clock	<100 ppm, 8.3 ns peak-peak jitter	N/A
Phase/ Synchronization	All channels within a bank of 8 data lines are sampled synchronously from a common clock. Phase relationship between channels is fully maintained. Channels within a task are synchronized.	All channels are generated synchronously from the input clock. Phase relationship between channels is fully maintained.

	Acquisition	Generation
Generation signal types	N/A	Sine, chirp (linear or logarithmic), white noise, and custom periodic signals
General purpose digital I/O (GPIO)	8 static GPIO lines can be configured independently as input or output lines	8 static GPIO lines can be configured independently as input or output lines

Refer to the **Bank to Channel Mapping for USB-7845R/7846R** section for the layout of banks, data lines, channels, and clock lines.

Decimation Filters

Decimation factor options	24, 32, 48, 64, 96, and 128. Select the option by task.

Decimation Filter Specifications

Decimation Factor	24 and 48	32 and 64	96 and 128
Normalized passband frequency	0.4275	0.438	0.45
Passband ripple (dB)	±0.0025	±0.001	±0.0004
Normalized stopband frequency	0.5725	0.562	0.55
Stopband attenuation (dB)	>110	>120	>123
Filter output delay (samples)	23	30	38

Acquisition and Generation Control

	Acquisition	Generation
Acquisition options	Raw PDM and/or PCM (decimated) data	N/A
Acquisition/Generation mode	Finite or Continuous	Continuous

	Acquisition	Generation
Trigger options	Immediate only	Immediate only
Export signal options	N/A	None
Acquisition pre-delay	Common pre-delay for each task applied to both PDM and PCM data	N/A
Acquisition pre-delay resolution	1 PDM bitrate period	N/A
Acquisition pre-delay range	0 to 16383 bitrate periods	N/A
Acquisition post-delay	Common post-delay for each task and applied to decimated data	N/A
Acquisition post-delay resolution	1 decimated data period	N/A
Acquisition post-delay range	0 to 2^{27}-2 (134,217,726) decimated data periods	N/A

Simulation Mode

PDM simulation signal type	Sine tone with a PDM amplitude of ±0.7071 FS (0.500 RMS)
Tone frequency	Proportional to the selected PDM rate. For a PDM rate of 3.072 MHz, tone frequency is 1 kHz for the first PDM channel input and increments by 1 kHz for each PDM channel input. The following table illustrates the tone frequencies at 3.072 MHz for all 16 PDM channel inputs.

PDM Channel Input 0L	1 kHz
PDM Channel Input 0R	2 kHz
...	
PDM Channel Input 7L	15 kHz
PDM Channel Input 7R	16 kHz

Refer to the **Bank to Channel Mapping for USB-7845R/7846R** section for the layout of banks, data lines, channels, and clock lines.

Tone start phase	0 degree for all tones when using the Configure PDM Trigger (None) VI

Related information

- Configure PDM Trigger VI

Bank to Channel Mapping for USB-7845R/7846R

The following table illustrates the bank to channel mapping for the USB-7845R/7846R.

Bank 0	PDM Data Input 0	PDM Channel Input 0L
		PDM Channel Input 0R
	...	.
		.
		.
	PDM Data Input 7	PDM Channel Input 7L
		PDM Channel Input 7R
	Clock 0,1	

Connector Pin Assignments for USB-7845R/7846R PDM Acquisition

Use the following connector pin assignments when you configure pin functions for PDM acquisition using the USB-7845R/7846R.

Connector 0

Terminal	Function	Assignment
1	DIO31	
2	GND	
3	DIO29	
4	GND	
5	DIO27	
6	GND	
7	DIO25	
8	GND	

Terminal	Function	Assignment
9	DIO23	
10	GND	
11	DIO21	
12	GND	
13	DIO19	
14	GND	
15	DIO17	GPIO 7
16	GND	
17	DIO15	GPIO 5
18	GND	
19	DIO13	PDM Clock Output 1
20	GND	
21	DIO11	PDM Input 7
22	GND	
23	DIO9	PDM Input 5
24	GND	
25	DIO7	PDM Input 3
26	GND	
27	DIO5	GPIO 3
28	GND	
29	DIO3	GPIO 1
30	GND	
31	DIO1	PDM Input 1
32	GND	
33	GND	
34	GND	
35	DIO30	
36	GND	
37	DIO28	
38	GND	
39	DIO26	

Terminal	Function	Assignment
40	GND	
41	DIO24	
42	GND	
43	DIO22	
44	GND	
45	DIO20	
46	GND	
47	DIO18	GPIO 6
48	GND	
49	DIO16	
50	GND	
51	DIO14	PDM Input 6
52	GND	
53	DIO12	GPIO 4
54	GND	
55	DIO10	GPIO 2
56	GND	
57	DIO8	GPIO 0
58	GND	
59	DIO6	PDM Input 4
60	GND	
61	DIO4	PDM Input 2
62	GND	
63	DIO2	PDM Input 0
64	GND	
65	DIO0	PDM Clock Output 0
66	GND	
67	External Clock **x***	
68	GND	
* **x** is the connector number. External Clock **x** is an input only.		

Connector Pin Assignments for USB-7845R/7846R PDM Generation

Use the following connector pin assignments when you configure pin functions for PDM generation using the USB-7845R/7846R.

Connector 0

Terminal	Function	Assignment
1	DIO31	
2	GND	
3	DIO29	
4	GND	
5	DIO27	
6	GND	
7	DIO25	
8	GND	
9	DIO23	
10	GND	
11	DIO21	
12	GND	
13	DIO19	
14	GND	
15	DIO17	GPIO 7
16	GND	
17	DIO15	GPIO 5
18	GND	
19	DIO13	
20	GND	
21	DIO11	PDM Output 7
22	GND	
23	DIO9	PDM Output 5
24	GND	

Terminal	Function	Assignment
25	DIO7	PDM Output 3
26	GND	
27	DIO5	GPIO 3
28	GND	
29	DIO3	GPIO 1
30	GND	
31	DIO1	PDM Output 1
32	GND	
33	GND	
34	GND	
35	DIO30	
36	GND	
37	DIO28	
38	GND	
39	DIO26	
40	GND	
41	DIO24	
42	GND	
43	DIO22	
44	GND	
45	DIO20	
46	GND	
47	DIO18	GPIO 6
48	GND	
49	DIO16	
50	GND	
51	DIO14	PDM Output 6
52	GND	
53	DIO12	GPIO 4
54	GND	
55	DIO10	GPIO 2

Terminal	Function	Assignment
56	GND	
57	DIO8	GPIO 0
58	GND	
59	DIO6	PDM Output 4
60	GND	
61	DIO4	PDM Output 2
62	GND	
63	DIO2	PDM Output 0
64	GND	
65	DIO0	PDM Clock Output 0
66	GND	
67	External Clock **x***	
68	GND	
* **x** is the connector number. External Clock **x** is an input only.		

Function Generator Specifications

Refer to the following specifications and examples when generating signals using the LabVIEW PDM Acquisition Toolkit.

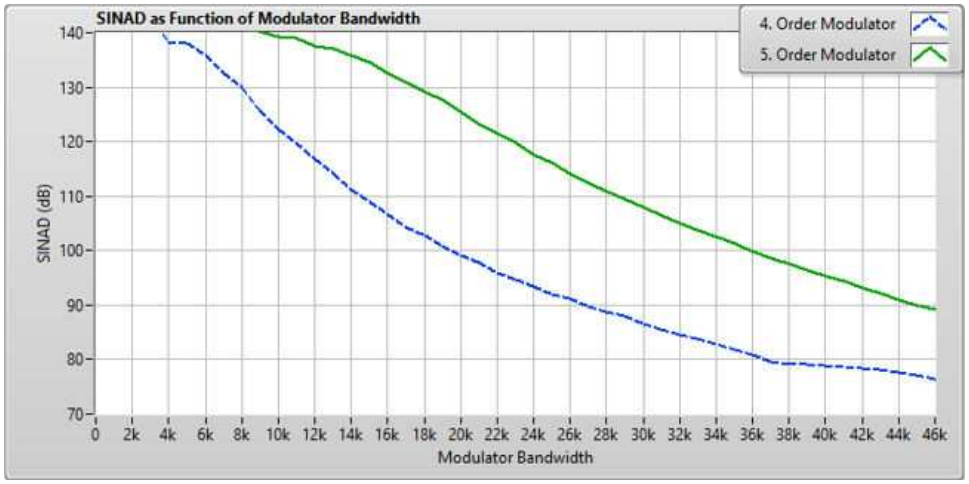
Dynamic Range and Distortion Specifications

SINAD, where test amplitude is 0.5 relative digital full scale	
Fourth order modulator	>98 dB
Fifth order modulator	>124 dB
Dynamic Range, where test amplitude is 0.0005 relative digital full scale	
Fourth order modulator	>100 dB
Fifth order modulator	>126 dB
* Measurement Conditions: PDM rate = 3.072 MHz; Modulator bandwidth = 20 kHz; Test signal = 1 kHz sine wave; Measurement bandwidth = Modulator bandwidth.	

Modulator Bandwidth

SINAD as a Function of Modulator Bandwidth

The following figure demonstrates the signal-to-noise and distortion ratio (SINAD) as a function of modulator bandwidth when the modulator order is 4 and 5.



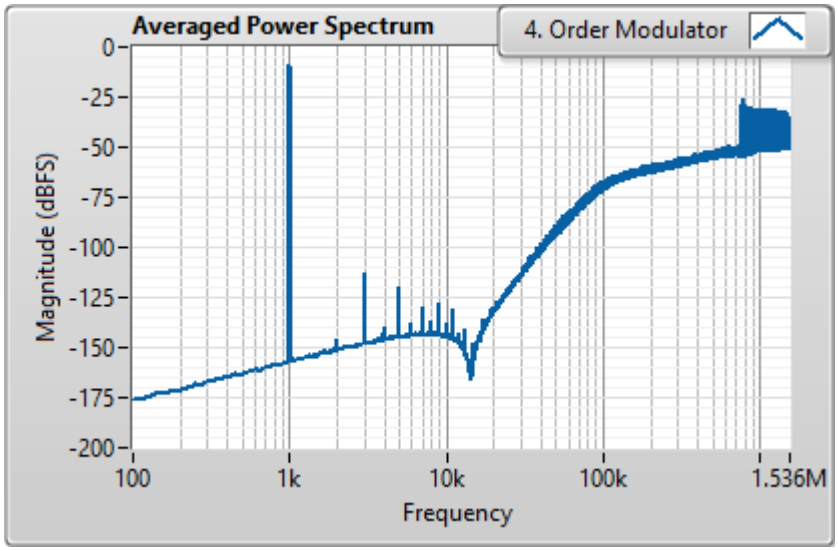
* Measurement Conditions: PDM rate = 3.072 MHz; Modulator bandwidth = 3 kHz to 46 kHz; Test frequency = 1 kHz; Test amplitude = 0.5 FS.

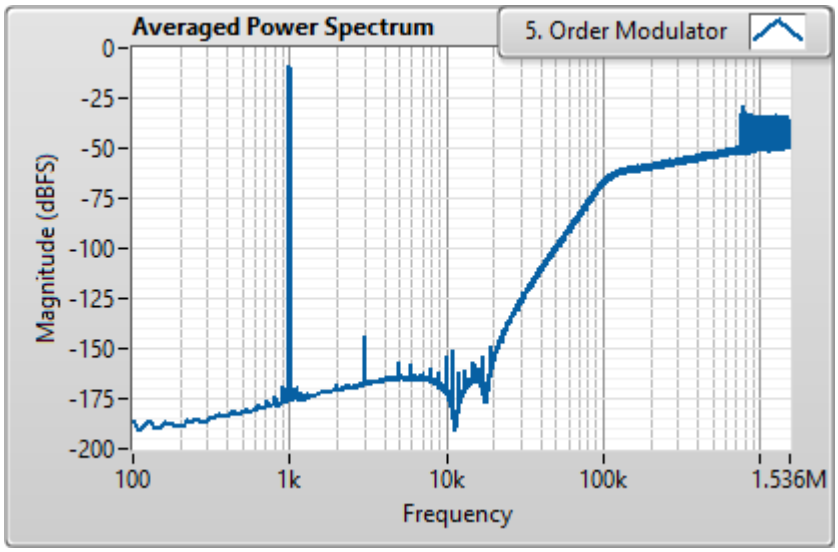
Modulator Flatness as a Function of Modulator Bandwidth

Fourth Order Modulator	
Modulator bandwidth ≤40 kHz	Ripple DC to modulation bandwidth < ±0.004 dB
Modulator bandwidth >40 kHz and ≤46 kHz	Ripple DC to modulation bandwidth < ±0.01 dB
Fifth Order Modulator	
Modulator bandwidth ≤40 kHz	Ripple DC to modulation bandwidth < ±0.001 dB
Modulator bandwidth >40 kHz and ≤46 kHz	Ripple DC to modulation bandwidth < ±0.002 dB
* Measurement Conditions: PDM rate = 3.072 MHz	

Spectral Characteristics

The following figures demonstrate the averaged power spectrum when the modulator order is 4 and 5, respectively.





* Measurement Conditions: PDM rate = 3.072 MHz; Modulator bandwidth = 20 kHz; Test frequency = 1 kHz; Test amplitude = 0.5 FS; Spectral resolution = 10 Hz; Window type = Hanning; Number of RMS averaging = 64.

Modulator Specifications

PDM modulator order	4 and 5. Use the Configure Modulator VI to select the modulator order.
PDM modulator bandwidth	DC to 0.015 * PCM rate. The bandwidth is DC to 46 kHz for PDM rate of 3.072 MHz. The default is
Recommended maximum output signal amplitude	The recommended maximum output signal amplitude depends on the modulator order. ▪ For the fourth order modulator, the recommended maximum output signal amplitude ▪ For the fifth order modulator, the recommended maximum output signal amplitude is

Related information

- Configure Modulator VI

Linear Chirp Specifications

The following specifications apply to the Configure Chirp (N Ch) VI when configuring a linear chirp signal.

Start frequency range	0 to PDM rate/2
Stop frequency range	0 to PDM rate/2
Pre-chirp duration range	0 to $2^{32} - 1$ PDM samples, or approximately 23 minutes at PDM rate of 3.072 MHz
Chirp duration range	0 to $2^{32} - 1$ – Pre-chirp duration samples

The linear chirp rate range, in seconds, is defined by the following equation:

$$\text{Linear chirp rate range} = \pm (\text{Stop freq} - \text{Start freq})/\text{Chirp duration}$$

Refer to the following table for maximum chirp rates at different PDM rates.

Maximum Linear Chirp Rate	PDM Rate = 600 kHz	PDM Rate = 800 kHz	PDM Rate = 2.4 MHz	PDM Rate = 3.072 MHz	PDM Rate = 4.8 MHz
Range	±1.37 MHz/s	±2.44 MHz/s	±21.9 MHz/s	±35.9 MHz/s	±87.8 MHz/s
Minimum Time DC to PDM rate/2	7 ms	5 ms	2 ms	2 ms	1 ms

Table 2. Maximum Linear Chirp Rate at Different PDM Rates

Related information

- Configure Chirp (N Ch) VI

Logarithmic Chirp Specifications

The following specifications apply to the Configure Chirp (N Ch) VI when configuring a logarithmic chirp signal.

Start frequency range	≤PDM rate/32, corresponding to 96 kHz at 3.072 MHz PDM rate
Stop frequency range	≤PDM rate/32
Pre-chirp duration range	0 to $2^{32} - 1$ PDM samples, or approximately 23 minutes at PDM rate of 3.072 MHz
Chirp duration range	0 to $2^{32} - 1$ − Pre-chirp duration samples

The logarithmic chirp rate range, in seconds, is defined by the following equation:

$$\text{Logarithmic chirp rate range} = \pm(\text{Stop freq} / \text{Start freq})/\text{Chirp duration}$$

Refer to the following table for maximum chirp rates at different PDM rates.

Maximum Logarithmic Chirp Rate	PDM Rate = 600 kHz	PDM Rate = 800 kHz	PDM Rate = 2.4 MHz	PDM Rate = 3.072 MHz	PDM Rate = 4.8 MHz
Range	±105 octave/s	±140 octave/s	±422 octave/s	±541 octave/s	±845 octave/s

Maximum Logarithmic Chirp Rate	PDM Rate = 600 kHz	PDM Rate = 800 kHz	PDM Rate = 2.4 MHz	PDM Rate = 3.072 MHz	PDM Rate = 4.8 MHz
Minimum chirp time for 10 octaves	95 ms	71 ms	24 ms	18.5 ms	12 ms

Table 2. Maximum Logarithmic Chirp Rate at Different PDM Rates

Related information

- Configure Chirp (N Ch) VI

Inter-IC Sound (I2S) Bus Specifications

Refer to these specifications when using the LabVIEW PDM Acquisition Toolkit with the PXIe-7820R/7821R and USB-7845R/7846R.

I2S Acquisition and Generation Specifications

Input Characteristics for PXIe-7820R/7821R

Characteristic	Acquisition	Generation
Number of I2S data lines	32, consisting of four banks of 8 data lines, 2 serial clock lines, and 2 word select lines (L/R clock)	16, consisting of two banks of 8 data lines, 2 serial clock lines, and 2 word select lines (L/R clock)
Number of I2S channels	64, consisting of four banks of 16 channels	32, consisting of two banks of 16 channels
Number of timing engines	2	2
Clock input/ output	Master and slave	Master and slave
I2S clock rate - SCK	160 kHz to 12.288 MHz	160 kHz to 12.288 MHz
Word select clock	10 kHz to 192 kHz	10 kHz to 192 kHz
Serial clock output (master mode)	One master bit clock shared across 8 data lines (16 channels)	N/A
Word select clock output (master mode)	One derived clock (from master serial clock) shared across the data lines configured in a timing engine	N/A
Serial clock input (slave mode)	The first clock line shared across 8 data lines (16 channels) in the bank	N/A
Word select clock input (slave mode)	The first clock line shared across 8 data lines (16 channels) in the bank	N/A

Characteristic	Acquisition	Generation
Data, clock, and GPIO logic level	Single-ended logic 1.2 V, 1.8 V, and 3.3 V	Single-ended logic 1.2 V, 1.8 V, and 3.3 V
Frame lengths	32 bits and 64 bits	32 bits and 64 bits
Data word length	For 32 bits frame, maximum of 16 bits/channel. For 64 bit frame, maximum 32 bits/channel.	N/A
Data word format	2's complement, MSB first delayed by one serial clock period	N/A
Timebase reference source	PXI Express 100 MHz	PXI Express 100 MHz
Phase/ Synchronization	All channels within a bank of 8 data lines are sampled synchronously from a common clock (internal clock or input clock). Phase relationship between channels is fully maintained. Channels within a task are synchronized.	All channels within a task are generated synchronously from the internal clock or input clock. Phase relationship between channels is fully maintained.
Divided clock	<2%, 250 ps peak-peak jitter	<2%, 250 ps peak-peak jitter
DDS clock	<100 ppm, 8.3 ns peak-peak jitter	<100 ppm, 8.3 ns peak-peak jitter
Generation signal types	N/A	Custom periodic signals
General purpose digital I/O (GPIO)	16 static GPIO lines can be configured independently as input or output lines	16 static GPIO lines can be configured independently as input or output lines
Data output format	N/A	24 bits/channel

Input Characteristics for USB-7845R/7846R

Characteristic	Value
Number of I2S data lines	8 data lines, 2 serial clock lines, and 2 word select lines (L/R clock)
Number of I2S channels	16 channels

Characteristic	Value
Number of timing engines	1
Serial clock output (master mode)	One master bit clock shared across 8 data lines (16 channels)
Word select clock output (master mode)	One derived clock (from master serial clock) shared across the data lines
Serial clock input (slave mode)	The first clock line shared across 8 data lines (16 channels) in the bank
Word select clock input (slave mode)	The first clock line shared across 8 data lines (16 channels) in the bank
Data, clock, and GPIO logic level	Single-ended logic 1.2 V, 1.8 V, and 3.3 V
Frame lengths	32-bit and 64-bit
Data word length	For 32-bit frame, maximum of 16 bits/channel. For 64-bit frame, maximum 32 bits/channel.
Data word format	2's complement, MSB first delayed by one serial clock period
Timebase reference source	PXI Express 100 MHz
Phase/ Synchronization	All channels within a bank of 8 data lines are sampled synchronously from a common clock (internal clock or input clock). Phase relationship between channels is fully maintained. Channels within a task are synchronized.
Divided clock	<2%, 250 ps peak-peak jitter
DDS clock	<100 ppm, 8.3 ns peak-peak jitter
General purpose digital I/O (GPIO)	8 static GPIO lines can be configured independently as input or output lines
Data output format	24 bits/channel

I2S Bit Specifications

Frame Length	Word Length
32	16 bits maximum
64	32 bits maximum

Acquisition and Generation Control

	Acquisition	Generation
Acquisition mode	Finite or Continuous	Continuous
Trigger options	Immediate or PXI-Trigger. Independent triggering on each task	Immediate or PXI-Trigger
Export signal options	N/A	None
PXI trigger	PXI-Trig [0..7]. Rising or Falling edge	PXI-Trig [0..7]. Rising or Falling edge
Trigger options for USB targets	Immediate	Immediate
Data latch at SCK cycle[1]	50% (rising edge of the serial clock) to 140%	N/A

Simulation Mode

I2S simulation signal type	Sine tone with the frame length of 64 and word length of 16 at sampling rate of 192 kHz
Tone frequency	The simulated signal frequency repeats for every group of 16 channels. For a serial clock rate of 12.88 MHz, tone frequency is 1 kHz for channel 0L with channel 0R at -90 phase shift.

I2S Channel Input 0L	1 kHz0 phase
I2S Channel Input 0R	1 kHz-90 phase
I2S Channel Input 1L	2 kHz0 phase
I2A Channel Input 1R	2 kHz-90 phase
...	
I2S Channel Input 7L	8 kHz0 phase
I2S Channel Input 7R	8 kHz-90 phase
I2S Channel Input 8L	1 kHz0 phase
I2S Channel Input 8R	1 kHz-90 phase
...	
I2S Channel Input 15L	8 kHz0 phase

	I2S Channel Input 15R	8 kHz-90 phase

Timing (Master Mode)

Master Mode	Minimum	Maximum	Conditions
Clock frequency	160 kHz	12.31 MHz	
Clock high	0.35 T		
Clock low	0.35 T		
Delay		0.80 T	
Hold time	0		
Clock rise-time			0.15 T

Timing (Slave Mode)

Slave Mode[2]	Minimum	Maximum	Conditions
Clock frequency	160 kHz	12.31 MHz	
Clock high	0.35 T		
Clock low	0.35 T		
Setup time	0.5 T	1.40 T	Depending on the input Data Latch at SCK cycle
Hold time			

Voltage Output Levels

Logic Level[3]	Output Low Voltage Maximum	Output High Voltage Minimum
1.2 V	0.20 V	1.00 V
1.8 V	0.20 V	1.54 V
3.3 V	0.20 V	2.40 V

Voltage Input Levels

Logic Level[3]	Input Low Voltage Maximum	Input High Voltage Minimum
1.2 V	0.42 V	0.84 V
1.8 V	0.61 V	1.21 V
3.3 V	0.80 V	2.00 V

1 Default latch point is at 50% of the serial clock period which is at the rising edge of the clock. To compensate for the cable delays, especially at the higher clock rates, you can increase this value up to 140%.
2 The receiver specifications must match the performance of the transmitter.
3 Logic levels are the same as the logic levels of the FPGA target.

I2S Bank to Channel Mapping for PXIe-7820R/7821R

The following table illustrates the I2S bank to channel mapping for the PXIe-7820R/7821R.

Bank 0	I2S Data Input 0	I2S Channel Input 0L	Bank 2	I2S Data Input 16	I2S Channel Input 16L
		I2S Channel Input 0R			I2S Channel Input 16R
	…	.		…	.
		.			.
		.			.
	I2S Data Input 7	I2S Channel Input 7L		I2S Data Input 23	I2S Channel Input 23L
		I2S Channel Input 7R			I2S Channel Input 23R
	Serial Clock 0,1 and Word Select Clock 0,1			Serial Clock 4,5 and Word Select Clock 4,5	
Bank 1	I2S Data Input 8	I2S Channel Input 8L	Bank 3	I2S Data Input 24	I2S Channel Input 24L
		I2S Channel Input 8R			I2S Channel Input 24R

	...	.		...	.
		.			.
		.			.
	I2S Data Input 15	I2S Channel Input 15L		I2S Data Input 31	I2S Channel Input 31L
		I2S Channel Input 15R			I2S Channel Input 31R
	Serial Clock 2,3 and Word Select Clock 2,3			Serial Clock 6,7 and Word Select Clock 6,7	

I2S Bank to Channel Mapping for USB-7845R/7846R

The following table illustrates the I2S bank to channel mapping for the USB-7845R/7846R.

Bank 0	I2S Data Input 0	I2S Channel Input 0L
		I2S Channel Input 0R
	...	.
		.
		.
	I2S Data Input 7	I2S Channel Input 7L
		I2S Channel Input 7R
	Serial Clock 0,1 and Word Select Clock 0,1	

Connector Pin Assignments for PXIe-7820R/7821R I2S Acquisition

Use the following connector pin assignments when you configure pin functions for I2S acquisition using the PXIe-7820R/7821R.
In the following tables, **WS** represents Word Select or L/R clock and **SCK** represents serial clock.

Connector 0

Terminal	Function	Assignment
1	DIO31	I2S Input 15
2	GND	
3	DIO29	WS 3
4	GND	
5	DIO27	GPIO 6
6	GND	
7	DIO25	I2S Input 13
8	GND	
9	DIO23	I2S Input 11
10	GND	
11	DIO21	I2S Input 9
12	GND	
13	DIO19	SCK 3
14	GND	
15	DIO17	GPIO 5
16	GND	
17	DIO15	GPIO 3
18	GND	
19	DIO13	SCK 1
20	GND	
21	DIO11	I2S Input 7
22	GND	
23	DIO9	I2S Input 5
24	GND	
25	DIO7	I2S Input 3
26	GND	
27	DIO5	WS 0
28	GND	
29	DIO3	GPIO 1

Terminal	Function	Assignment
30	GND	
31	DIO1	I2S Input 1
32	GND	
33	GND	
34	GND	
35	DIO30	SCK 2
36	GND	
37	DIO28	I2S Input 14
38	GND	
39	DIO26	I2S Input 12
40	GND	
41	DIO24	I2S Input 10
42	GND	
43	DIO22	GPIO 7
44	GND	
45	DIO20	WS 2
46	GND	
47	DIO18	GPIO 4
48	GND	
49	DIO16	I2S Input 8
50	GND	
51	DIO14	I2S Input 6
52	GND	
53	DIO12	GPIO 2
54	GND	
55	DIO10	WS 1
56	GND	
57	DIO8	GPIO 0
58	GND	
59	DIO6	I2S Input 4
60	GND	

Terminal	Function	Assignment
61	DIO4	I2S Input 2
62	GND	
63	DIO2	I2S Input 0
64	GND	
65	DIO0	SCK 0
66	GND	
67	External Clock **x***	
68	GND	
* **x** is the connector number. External Clock **x** is an input only.		

Connector 1

Terminal	Function	Assignment
1	DIO31	I2S Input 31
2	GND	
3	DIO29	WS 7
4	GND	
5	DIO27	GPIO 14
6	GND	
7	DIO25	I2S Input 29
8	GND	
9	DIO23	I2S Input 27
10	GND	
11	DIO21	I2S Input 25
12	GND	
13	DIO19	SCK 7
14	GND	
15	DIO17	GPIO 13
16	GND	
17	DIO15	GPIO 11
18	GND	

Terminal	Function	Assignment
19	DIO13	SCK 5
20	GND	
21	DIO11	I2S Input 23
22	GND	
23	DIO9	I2S Input 21
24	GND	
25	DIO7	I2S Input 19
26	GND	
27	DIO5	WS 4
28	GND	
29	DIO3	GPIO 9
30	GND	
31	DIO1	I2S Input 17
32	GND	
33	GND	
34	GND	
35	DIO30	SCK 6
36	GND	
37	DIO28	I2S Input 30
38	GND	
39	DIO26	I2S Input 28
40	GND	
41	DIO24	I2S Input 26
42	GND	
43	DIO22	GPIO 15
44	GND	
45	DIO20	WS 6
46	GND	
47	DIO18	GPIO 12
48	GND	
49	DIO16	I2S Input 24

Terminal	Function	Assignment
50	GND	
51	DIO14	I2S Input 22
52	GND	
53	DIO12	GPIO 10
54	GND	
55	DIO10	WS 5
56	GND	
57	DIO8	GPIO 8
58	GND	
59	DIO6	I2S Input 20
60	GND	
61	DIO4	I2S Input 18
62	GND	
63	DIO2	I2S Input 16
64	GND	
65	DIO0	SCK 4
66	GND	
67	External Clock **x***	
68	GND	
* **x** is the connector number. External Clock **x** is an input only.		

Connector Pin Assignments for PXIe-7820R/7821R I2S Generation

Use the following connector pin assignments when you configure pin functions for I2S generation using the PXIe-7820R/7821R.
In the following tables, **WS** represents Word Select or L/R clock and **SCK** represents serial clock.

Connector 0

Terminal	Function	Assignment
1	DIO31	I2S Output 15
2	GND	
3	DIO29	WS 3
4	GND	
5	DIO27	GPIO 6
6	GND	
7	DIO25	I2S Output 13
8	GND	
9	DIO23	I2S Output 11
10	GND	
11	DIO21	I2S Output 9
12	GND	
13	DIO19	SCK 3
14	GND	
15	DIO17	GPIO 5
16	GND	
17	DIO15	GPIO 3
18	GND	
19	DIO13	SCK 1
20	GND	
21	DIO11	I2S Output 7
22	GND	
23	DIO9	I2S Output 5
24	GND	
25	DIO7	I2S Output 3
26	GND	
27	DIO5	WS 0
28	GND	
29	DIO3	GPIO 1

Terminal	Function	Assignment
30	GND	
31	DIO1	I2S Output 1
32	GND	
33	GND	
34	GND	
35	DIO30	SCK 2
36	GND	
37	DIO28	I2S Output 14
38	GND	
39	DIO26	I2S Output 12
40	GND	
41	DIO24	I2S Output 10
42	GND	
43	DIO22	GPIO 7
44	GND	
45	DIO20	WS 2
46	GND	
47	DIO18	GPIO 4
48	GND	
49	DIO16	I2S Output 8
50	GND	
51	DIO14	I2S Output 6
52	GND	
53	DIO12	GPIO 2
54	GND	
55	DIO10	WS 1
56	GND	
57	DIO8	GPIO 0
58	GND	
59	DIO6	I2S Output 4
60	GND	

Terminal	Function	Assignment
61	DIO4	I2S Output 2
62	GND	
63	DIO2	I2S Output 0
64	GND	
65	DIO0	SCK 0
66	GND	
67	External Clock **x***	
68	GND	
* **x** is the connector number. External Clock **x** is an input only.		

Connector Pin Assignments for USB-7845R/7846R I2S Acquisition

Use the following connector pin assignments when you configure pin functions for I2S acquisition using the USB-7845R/7846R.
In the following tables, **WS** represents Word Select or L/R clock and **SCK** represents serial clock.

Connector 0

Terminal	Function	Assignment
1	DIO31	
2	GND	
3	DIO29	
4	GND	
5	DIO27	GPIO 6
6	GND	
7	DIO25	
8	GND	
9	DIO23	
10	GND	
11	DIO21	

Terminal	Function	Assignment
12	GND	
13	DIO19	
14	GND	
15	DIO17	GPIO 5
16	GND	
17	DIO15	GPIO 3
18	GND	
19	DIO13	SCK 1
20	GND	
21	DIO11	I2S Input 7
22	GND	
23	DIO9	I2S Input 5
24	GND	
25	DIO7	I2S Input 3
26	GND	
27	DIO5	WS 0
28	GND	
29	DIO3	GPIO 1
30	GND	
31	DIO1	I2S Input 1
32	GND	
33	GND	
34	GND	
35	DIO30	
36	GND	
37	DIO28	
38	GND	
39	DIO26	
40	GND	
41	DIO24	
42	GND	

Terminal	Function	Assignment
43	DIO22	GPIO 7
44	GND	
45	DIO20	
46	GND	
47	DIO18	GPIO 4
48	GND	
49	DIO16	
50	GND	
51	DIO14	I2S Input 6
52	GND	
53	DIO12	GPIO 2
54	GND	
55	DIO10	WS 1
56	GND	
57	DIO8	GPIO 0
58	GND	
59	DIO6	I2S Input 4
60	GND	
61	DIO4	I2S Input 2
62	GND	
63	DIO2	I2S Input 0
64	GND	
65	DIO0	SCK 0
66	GND	
67	External Clock **x***	
68	GND	
* **x** is the connector number. External Clock **x** is an input only.		

Connector Pin Assignments for USB-7845R/7846R I2S Generation

Use the following connector pin assignments when you configure pin functions for I2S generation using the USB-7845R/7846R.
In the following tables, **WS** represents Word Select or L/R clock and **SCK** represents serial clock.

Connector 0

Terminal	Function	Assignment
1	DIO31	
2	GND	
3	DIO29	
4	GND	
5	DIO27	GPIO 6
6	GND	
7	DIO25	
8	GND	
9	DIO23	
10	GND	
11	DIO21	
12	GND	
13	DIO19	
14	GND	
15	DIO17	GPIO 5
16	GND	
17	DIO15	GPIO 3
18	GND	
19	DIO13	SCK 1
20	GND	
21	DIO11	I2S Output 7
22	GND	
23	DIO9	I2S Output 5

Terminal	Function	Assignment
24	GND	
25	DIO7	I2S Output 3
26	GND	
27	DIO5	WS 0
28	GND	
29	DIO3	GPIO 1
30	GND	
31	DIO1	I2S Output 1
32	GND	
33	GND	
34	GND	
35	DIO30	
36	GND	
37	DIO28	
38	GND	
39	DIO26	
40	GND	
41	DIO24	
42	GND	
43	DIO22	GPIO 7
44	GND	
45	DIO20	
46	GND	
47	DIO18	GPIO 4
48	GND	
49	DIO16	
50	GND	
51	DIO14	I2S Output 6
52	GND	
53	DIO12	GPIO 2
54	GND	

Terminal	Function	Assignment
55	DIO10	WS 1
56	GND	
57	DIO8	GPIO 0
58	GND	
59	DIO6	I2S Output 4
60	GND	
61	DIO4	I2S Output 2
62	GND	
63	DIO2	I2S Output 0
64	GND	
65	DIO0	SCK 0
66	GND	
67	External Clock **x***	
68	GND	
* **x** is the connector number. External Clock **x** is an input only.		