PXIe-7891 Specifications

2023-11-21

Contents

PXIe-7891 Specifications

Definitions

Warranted specifications describe the performance of a model under stated operating conditions and are covered by the model warranty.

Characteristics describe values that are relevant to the use of the model under stated operating conditions but are not covered by the model warranty.

- **Typical** specifications describe the performance met by a majority of models.
- **Nominal** specifications describe an attribute that is based on design, conformance testing, or supplemental testing.
- **Measured** specifications describe the measured performance of a representative model.

Specifications are **Typical** unless otherwise noted.

Conditions

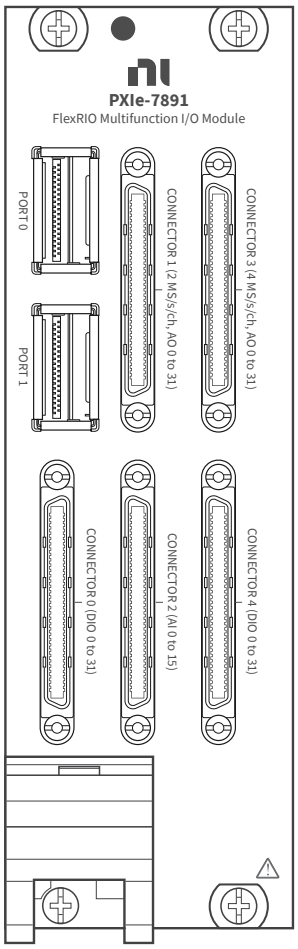
Specifications are valid under the following conditions unless otherwise noted.

- Ambient temperature of 0 °C to 55 °C .
- Installed in chassis with slot cooling capacity ≥58 W.

Front Panel

Figure 1 shows the front panel of the PXIe-7891 module. This document groups specifications per connector on the front panel.

Figure 1. PXIe-7891 Front Panel



Port 0 and Port 1

Connector	QSFP, SFF-8436 compliant
Data rate	500 Mbps to 5 Gb/s
Number of lanes	8 RX/TX (GTH)
Supported high-speed cable type	Electrical/ optical
Optical cable power	3.3 V ±5%, 1 A per port

Multi-Gigabit Transceiver (MGT)

MGT TX± Channels

Note For detailed FPGA and High-Speed Serial Link specifications, refer to Xilinx documentation.

Minimum differential output voltage[1]	170 mV pk-pk into 100 Ω, nominal
I/O coupling	AC-coupled, includes 100 nF capacitor

MGT RX± Channels

Differential input voltage range at ≤ 6.6 Gb/s	150 mV pk-pk to 2000 mV pk-pk , nominal

MGT Reference Clock Generator

Supported generated frequencies	60.000 MHz to 385.714 MHz 400.000 MHZ to 450.000 MHz 480.000 MHz to 675.000 MHz 685.714 MHz to 771.428 MHz 800 MHz
Clocking resources	PXIe_CLK100
Available MGT Reference Clocks	4

[1] 800 mV pk-pk when transmitter output swing is set to the maximum setting.

Connector 0 and Connector 4

The following section describes the digital input and output characteristics accessible through CONNECTOR 0 and CONNECTOR 4.

CONNECTOR 0 and CONNECTOR 4 are identical and share the same pinout, but are oriented in opposite directions on the module. For more information, including pinout descriptions, refer to the **PXIe-7890/7891 Getting Started** content in the NI Product Documentation Center.

Connectors 0 and 4	68-pin VHDCI receptacle

Note The number of channels listed in each of the following sections represents the total number of channels for both CONNECTOR 0 and CONNECTOR 4. To determine the number of channels for a single connector, divide the listed number of channels in half.

Related information:

- NI Product Documentation Center

Digital I/O

Number of channels	64
Signal type	Single-ended
Voltage level	
Digital input	3.3 V / 5 V (selectable by bank of 16 channels)
Digital output	3.3 V / 5 V (selectable by bank of 16 channels)
Direction control	Per channel

Latency	25 ns
Power-on-state	Digital input
Number of external clock input	2
Protection	±15 V per line, up to two lines simultaneously

Note Digital input and output voltage levels are guaranteed by design through the digital buffer specifications.

Table 1. Digital Input Logic Levels

Voltage Family	Input Low Voltage (V_{IL}) Maximum	Input High Voltage (V_{IH}) Minimum
3.3 V	0.80 V	2.00 V
5.0 V	1.50 V	3.50 V

Minimum input voltage	0 V
Maximum input voltage	5 V
Input impedance	100 kΩ, pull-down

Table 2. Digital Output Logic Levels

Voltage Family	Current	Output Low Voltage (V_{OL}) Maximum	Output High Voltage (V_{OH}) Minimum
3.3 V	100 µA	0.10 V	3.20 V
	4 mA	0.45 V	2.85 V
5 V	100 µA	0.10 V	4.90 V
	4 mA	0.45 V	4.55 V

Maximum DC output current per channel	4.0 mA (sink or source)

Output impedance	50 Ω ± 20%
Maximum output toggle rate	10 MHz

Connector 1

The following section describes the analog output characteristics accessible through CONNECTOR 1. For more information, including pinout descriptions, refer to **PXIe-7890/7891 Getting Started** content in the NI Product Documentation Center.

Connector type	68-pin VHDCI receptacle

Analog Output

Output type	Single-ended, voltage output
Number of channels	32
Resolution	16 bits
Update latency	
Uncalibrated	440 nsec
Calibrated	460 nsec
Analog latency	75 nsec
Maximum update rate	2 MS/s
INL	±0.5 LSB typical, ±2 LSB maximum

DNL	±0.5 LSB typical, ±1 LSB maximum
Output range	
Nominal	±10 V
Typical	±10.13 V
Minimum	±10.10 V
Output coupling	DC
Output impedance	0.3 Ω
Gain drift	5.5 ppm/°C
Offset drift	30 µV/°C
Slew rate	20 V/µs
Noise (DC to 612 kHz)	70 µVrms
Current drive	±15 mA
Protection	Short circuit to ground
Crosstalk @100 kHz	-85 dB
Overvoltage protection	
Powered on	±15 V
Powered off	±10 V
Power-on output state	0 V

Power-on glitch	640 mV, decays to 0 V in 860 µs
Power-off glitch	1.4 V, decays to 0 V in 200 µs
Glitch during module reset	1.4 V, decays to 0 V in 200 µs

Note Total hardware latency is Update latency + Analog latency.

Table 3. Settling Time

Step Size	Accuracy	
±10 V	±16 LSB	±2 LSB
	3.0 µs	7.4 µs

Table 4. Analog Output Calibrated Accuracy

Nominal Range	Condition	Gain Error (Percent of Reading)	Offset Error
±10 V	Typical (25°C to ±5°C)	±0.016%	±0.11 mV
	Maximum (0°C to 55°C)	±0.070%	1.79 mV

Table 5. Analog Output Uncalibrated Accuracy

Nominal Range	Condition	Gain Error (Percent of Reading)	Offset Error
±10 V	Typical (25°C to ±5°C)	±0.096%	±2.73 mV
	Maximum (0°C to 55°C)	±0.219%	±8.86 mV

Note Uncalibrated accuracy in Table 4 refers to the accuracy achieved when outputting in raw or unscaled modes where the calibration constants stored in the module are not applied to the data. The gain error is relative to the typical output range of ±10.13 V.

AO Absolute Accuracy Equation

$$AO\_AbsoluteAccuracy = (OutputValue) \cdot GainError + \text{OffsetError} + INLError \cdot OutputRange \cdot 2/2^{16\ bits}$$

The following example calculates the absolute full scale calibrated accuracy at 25 ±5 ˚C on the 10 V range.

$$AO\_AbsoluteAccuracy = (10\ V) \cdot 0.016\,\% + 0.11\ mV + \frac{0.5\ LSB \cdot (10.13\ V) \cdot 2}{2\text{^}16\ bits} = 1.865\ mV$$

Connector 2

The following section describes the analog input characteristics accessible through CONNECTOR 2. For more information, including pinout descriptions, refer to **PXIe-7890/7891 Getting Started** content in the NI Product Documentation Center.

Connector type	68-pin VHDCI receptacle

Analog Input

Number of channels	16
Input mode	Differential
Type of ADC	Successive approximation register (SAR)
Resolution	16 bits
Input ranges	±20 V, ±10 V, ±5 V, ±2 V, ±1 V
Conversion latency	

Uncalibrated	480 nsec
Calibrated	480 nsec
Analog latency	
Range ±20 V	415 nsec
Ranges ±10 V±5 V±2 V	170 nsec
Range ±1 V	200 nsec
Maximum rate (per channel)	2 MS/s
Input impedance	
Powered on	
Range ±20 V	1 MΩ
Range ±10 V, ±5 V, ±2 V, ±1 V	> 1 GΩ
Powered off/overload	3.8 kΩ
Input coupling sampling	DC
Input bias current	±5 nA
Input offset current	±5 nA
INL	±6 LSB typical, ±12.7 LSB maximum
DNL	±0.4 LSB typical, ±1 LSB maximum
CMRR, DC to 60 Hz	
Range ±20 V	-48 dB

Ranges ±10 V, ±5 V, ±2 V	-80 dB
Bandwidth	
Small signal	
Range ±20 V	900 kHz
Ranges ±10 V, ±5 V, ±2 V	1600 kHz
Range ±1 V	1400 kHz
Large signal	
Ranges ±20 V, ±10 V	740 kHz
Ranges ±5 V, ±2 V, ±1 V	970 kHz
Crosstalk (100 kHz) into 50 Ω	-70 dB
Overvoltage protection	
Powered on	±42 V [2]
Powered off	±30 V

Note Total hardware latency is Conversion latency + Analog latency.

Table 6. Analog Input Characteristics by Range

Specification	Nominal Range				
	±20 V	±10 V	±5 V	±2 V	±1 V
Input noise (µVrms)	1600	670	340	140	80

[2] Only valid for fault on +/- input for 8 AI channels maximum. Degrades to +/-30 V for all 16 channels fault.

Specification	Nominal Range				
	±20 V	±10 V	±5 V	±2 V	±1 V
Gain drift (ppm/˚C)	22.6	16.7			
Offset drift (µV/˚C)	64.0	29.2	14.9	6.5	3.8
Typical input range, AI+ to AI- (V)	±20.62	±10.22	±5.11	±2.04	±1.02
Minimum input range, AI+ to AI- (V)	±20.38	±10.16	±5.08	±2.03	±1.01
Maximum Working Voltage (V) (Signal + Common Mode to Ground)	±22	±13	±10.5	±9.0	±8.5

Table 7. Analog Input Calibrated Accuracy

Nominal Range	Condition	Gain Error (Percent of Reading)	Offset Error
±20 V	Typical (25°C ± 5°C)	±0.038%	±1.44 mV
	Maximum (0°C to 55°C)	±0.278%	±5.94 mV
±10 V	Typical (25°C ± 5°C)	±0.032%	±0.71 mV
	Maximum (0°C to 55°C)	±0.215%	±2.04 mV
±5 V	Typical (25°C ± 5°C)	±0.032%	±0.36 mV
	Maximum (0°C to 55°C)	±0.215%	±1.05 mV
±2 V	Typical (25°C ± 5°C)	±0.032%	±0.15 mV
	Maximum (0°C to 55°C)	±0.215%	±0.47 mV
±1 V	Typical (25°C ± 5°C)	±0.032%	±0.08 mV
	Maximum (0°C to 55°C)	±0.215%	±0.27 mV

Table 8. Analog Input Uncalibrated Accuracy

Nominal Range	Condition	Gain Error (Percent of Reading)	Offset Error
±20 V	Typical (25°C ± 5°C)	±0.143%	±3.10 mV
	Maximum (0°C to 55°C)	±0.808%	±22.80 mV
±10 V	Typical (25°C ± 5°C)	±0.139%	±0.98 mV
	Maximum (0°C to 55°C)	±0.536%	±6.89 mV
±5 V	Typical (25°C ± 5°C)	±0.142%	±0.54 mV
	Maximum (0°C to 55°C)	±0.546%	±3.67 mV
±2 V	Typical (25°C ± 5°C)	±0.142%	±0.28 mV
	Maximum (0°C to 55°C)	±0.546%	±1.74 mV
±1 V	Typical (25°C ± 5°C)	±0.142%	±0.19 mV
	Maximum (0°C to 55°C)	±0.546%	±1.09 mV

Note Uncalibrated accuracy in Table 8 refers to the accuracy achieved when acquiring in raw or unscaled modes where the calibration constants stored in the module are not applied to the data. The gain error is relative to the typical input range from Table 6. For example, on the ±10 V nominal range, the gain error is relative to a full-scale value of ±10.22 V.

AI Absolute Accuracy Equation

$$AI\_AbsoluteAccuracy = (Reading) \cdot GainError + \text{OffsetError} + INLError \cdot InputRange \cdot 2/2^{16\ bits} + Noise \cdot CoverageFacrtor/\sqrt{Number\_of\_reading}$$

The following example calculates the absolute full scale calibrated accuracy at 25 ±5 ˚C on the 20 V range with 10,000 readings and 3δ coverage factor.

$$AI\_AbsoluteAccuracy = (20\ V) \cdot 0.038\,\% + 1.44\ mV + \frac{6\ LSB \cdot (20.62\ V) \cdot 2}{2\text{^}16\ bits} + \frac{(1600\ \mu V) \cdot 3}{\sqrt{10,000}} = 12.864\ mV$$

Connector 3

The following sections describe the low-latency analog output characteristics accessible through CONNECTOR 3. For more information, including pinout descriptions, refer to **PXIe-7890/7891 Getting Started** content in the NI Product Documentation Center.

Connector type	68-pin VHDCI receptacle

Low-Latency Analog Output

Output type	Single-ended, voltage output
Number of channels	32
Resolution	16 bits
Output range	±10 V, ±0.5 V[3]
Update latency	
Uncalibrated	148 nsec
Calibrated	168 nsec
Analog latency	50 nsec
Maximum update rate	4 MS/s
INL	±4 LSB maximum
DNL	±1 LSB maximum

[3] The PXIe-7891 supports 0.5 V range only on Ch<0..7> and Ch<16..23>.

Output coupling	DC
Output impedence	50 Ω
Slew rate	320 V/µs
Current drive	±100 mA
Crosstalk @100 kHz	-78 dB
Protection	Short circuit to ground
Overvoltage protection	
Powered on	±32 V[4]
Powered off	±20 V
Power on state	0 V
Power on glitch	
Dual range channel	1.3 V, decays to 0 V in 400 µs
Single range channel	0.4 V, decays to 0 V in 80 ms
Power off glitch	
10 V range channels	4.6 V, decays to 0 V in 4 µs
0.5 V range channels	0.25 V, decays to 0 V in 4 µs
Settling time at Full Scale to 16 LSB	1.2 µs

[4] AO channel will shut down at fault voltage more than ±5 V from configured AO output.

Note Total hardware latency is Update latency + Analog latency.

Table 9. Low-Latency Analog Output Characteristics by Range

Specification	Nominal Range	
	±10 V	±0.5 V
Output Noise (µVrms) – DC to 612 kHz	78	16
Gain Drift (ppm/˚C)	13	78
Offset Drift (µV/˚C)	260	13
Typical Output Range (V)	±10.32	±0.51
Minimum Output Range (V)	±10.15	±0.50

Information in Table 10 and Table 11 is applicable only for high impedance loads (> 1 Mohm), in which the load current is negligible due to the 50 ohm source resistance.

Table 10. Low-Latency Analog Output Calibrated Accuracy

Nominal Range	Condition	Gain Error (Percent of Reading)	Offset Error
±10 V	Typical (25°C to ±5°C)	±0.028%	±2.67 mV
	Maximum (0°C to 55°C)	±0.162%	±19.94 mV
±0.5 V	Typical (25°C to ±5°C)	±0.099%	±0.13 mV
	Maximum (0°C to 55°C)	±0.852%	±1.03 mV

Table 11. Low-Latency Analog Output Uncalibrated Accuracy

Nominal Range	Condition	Gain Error (Percent of Reading)	Offset Error
±10 V	Typical (25°C to ±5°C)	±0.256%	±24.42 mV
	Maximum (0°C to 55°C)	±0.828%	±81.65 mV
±0.5 V	Typical (25°C to ±5°C)	±1.164%	±1.22 mV
	Maximum (0°C to 55°C)	±4.319%	±4.21 mV

Note Uncalibrated accuracy refers to the accuracy achieved when outputting in raw or unscaled modes where the calibration constants stored in the module are not applied to the data. The gain error is relative to the typical output from Table 9. For example, on the ±10 V nominal range, the gain error is relative to a full-scale value of ±10.32 V.

Low Latency AO Absolute Accuracy Equation

$$LLAO\_AbsoluteAccuracy = (OutputValue) \cdot GainError + \text{OffsetError} + INLError \cdot OutputRange \cdot 2/2^{16\ bits}$$

The following example calculates the absolute full scale calibrated accuracy at 25 ±5 °C on the 10 V range.

$$LLAO\_AbsoluteAccuracy = (10\ V) \cdot 0.028\,\% + 2.67\ mV + \frac{4\ LSB \cdot (10.32\ V) \cdot 2}{2\text{^}16\ bits} = 6.730\ mV$$

Calibration

Interval	2 years

Reconfigurable FPGA

The PXIe-7891 provides a KU060 FPGA with characteristics shown in the following table.

Table 12. KU060 FPGA Characteristics

Characteristics	KU060
LUTs	331,680
DSP48 slices (25 × 18 multiplier)	2,760
Embedded Block RAM	38.0 Mb
Timebase reference sources	PXI Express 100 MHz (PXIe_CLK100)

Characteristics	KU060
Data transfers	DMA, interrupts, programmed I/O, multi-gigabit transceivers
Number of DMA channels	60

Note The list above depicts the total number of FPGA resources available on the part. The number of resources available to the user is slightly lower, as some FPGA resources are consumed by board-interfacing IP for PCI Express, device configuration, and various board I/O. For more information, contact NI Support.

Onboard DRAM

Memory size	4 GB (2 banks of 2 GB)
DRAM clock rate	1064 MHz
Physical bus width	32 bit
LabVIEW FPGA DRAM clock rate	267 MHz
LabVIEW FPGA DRAM bus width	256 bit per bank
Maximum theoretical data rate	17 GB/s (8.5 GB/s per bank)

Bus Interface

Form factor	PCI Express Gen-3 x8

Maximum Power Requirements

Note Power requirements are dependent on the contents of the LabVIEW FPGA VI used in your application.

Maximum Current	
+3.3 Vdc	2.6 A
+12.0 Vdc	7.3 A
Maximum total power	96.2 W

Power consumption is from both PXI Express backplane power connectors.

Physical Characteristics

Dimensions (not including connectors)	4.0 cm × 13.0 cm × 21.6 cm (0.8 in. × 5.1 in. × 8.5 in.)
Weight	778 g (27.4 oz)

Environmental Characteristics

Temperature	
Operating	0 °C to 55 °C
Storage	-40 °C to 71 °C
Humidity	
Operating	10% to 90%, noncondensing

Storage	5% to 95%, noncondensing
Pollution Degree	2
Maximum altitude	2,000 m (800 mbar) (at 25 °C ambient temperature)
Shock and Vibration	
Operating vibration	5 Hz to 500 Hz, 0.3 g RMS
Non-operating vibration	5 Hz to 500 Hz, 2.4 g RMS
Operating shock	30 g, half-sine, 11 ms pulse