PXIe-7903 Getting Started

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Contents

PXIe-7903 Getting Started

Note Before you begin, install and configure your chassis and controller.

This document explains how to install, configure, and troubleshoot the PXIe-7903 high-speed serial module. You can program the PXIe-7903 using NI-FlexRIO driver software

For device specifications, refer to the **PXIe-7903 Specifications**.

Caution Observe all instructions and cautions in the user documentation. Using the product in a manner not specified can damage the product and compromise the built-in safety protection.

Attention Suivez toutes les instructions et respectez toutes les mises en garde de la documentation d'utilisation. L'utilisation du produit de toute autre façon que celle spécifiée risque de l'endommager et de compromettre la protection de sécurité intégrée.

FlexRIO Documentation and Resources

Use the following resources to find more information about the PXIe-7903.

All documentation can be found at ni.com/manuals or in LabVIEW by clicking **Help**.

Table 1. FlexRIO Documentation and Resources

Document	Contents
PXIe-7903 Getting Started Guide (this document)	▪ Installation instructions ▪ Basic programming information
PXIe-7903 Specifications	▪ Operating environment requirements ▪ DIO specifications ▪ Clocking specifications ▪ Physical and mechanical specifications
PXIe-7903 Safety, Environmental, and Regulatory Information	▪ Safety and compliance information ▪ Environmental information
LabVIEW FPGA Module Help	▪ Basic functionality of the FPGA module ▪ Instructions for developing and debugging custom hardware logic
FlexRIO Readme	▪ Minimum system requirements ▪ Supported Application Development Environments (ADEs) ▪ Known issues and bug fixes ▪ Recent updates
FlexRIO Help	▪ FlexRIO driver API and programming information ▪ I/O Component Level IP (CLIP) development information

Document	Contents
LabVIEW Examples	▪ Examples showing how to run FPGA VIs on your device ▪ Examples showing how to run host VIs on your device

Unpacking the Kit

Notice To prevent electrostatic discharge (ESD) from damaging the device, ground yourself using a grounding strap or by holding a grounded object, such as your computer chassis.

1. Touch the antistatic package to a metal part of the computer chassis.
2. Remove the device from the package and inspect the device for loose components or any other sign of damage.

   Notice Never touch the exposed pins of connectors.

   Note Do not install a device if it appears damaged in any way.
3. Unpack any other items and documentation from the kit.

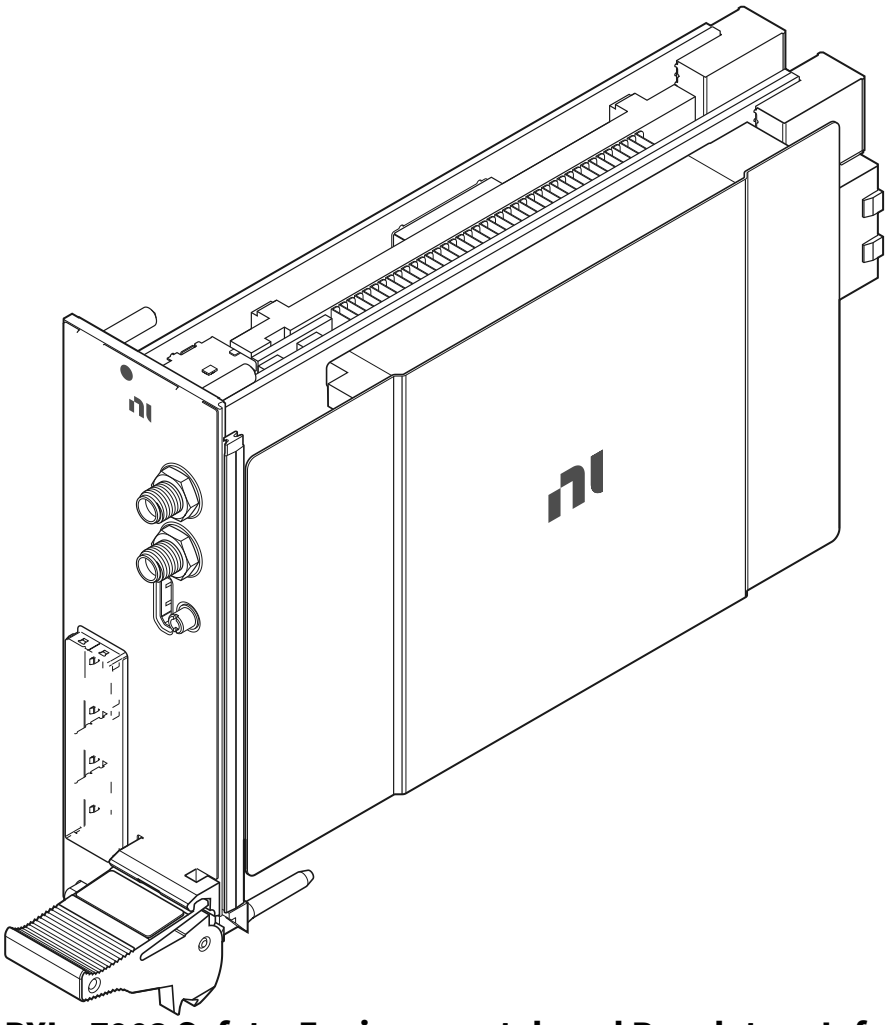
Store the device in the antistatic package when the device is not in use.

What You Need to Get Started

Kit Contents

Verify that the following items are included in the PXIe-7903 kit.

Figure 1. PXIe-7903



PXIe-7903 Safety, Environmental, and Regulatory Information

Recommended Cables

NI recommends the following cables for use with the PXIe-7903.

Model	Description	NI Part Number
Mini-SAS zHD-Mini-SAS zHD HSS Passive Cable	0.5 m zHD to zHD cable	788927-0R5
Mini-SAS zHD-Mini-SAS zHD HSS Passive Cable	1 m zHD to zHD cable	788927-01

Model	Description	NI Part Number
Mini-SAS zHD-Mini-SAS zHD HSS Passive Cable	2 m zHD to zHD cable	788927-02
Mini-SAS zHD-QSFP28 HSS Passive Cable	2 m zHD to QSFP28 Cable	788928-02
Cable Assembly, Mini-HDMI to Mini-HDMI, 1 Meter[1]	Cable Assembly, Mini-HDMI to Mini-HDMI, 1 Meter	143045-01

Notice Use care when handling zHD cables. If you meet resistance when connecting the cable, stop and inspect the cable; replace the cable if the EMI gasket is damaged.

[1] NI Mini-HDMI (Type C) cable used to connect the module to DIO ports on other devices.

Preparing the Environment

Ensure that the environment you are using the PXIe-7903 in meets the following specifications.

Caution Do not use the PXIe-7903 in a manner not specified in this document. Product misuse can result in a hazard. You can compromise the safety protection built into the product if the product is damaged in any way. If the product is damaged, return it to NI for repair.

Attention Le PXIe-7903 ne doit en aucun cas être utilisé d'une autre façon que celle spécifiée dans ce document. Une mauvaise utilisation du produit peut s'avérer dangereuse. Si le produit est endommagé de quelque manière que ce soit, la sécurité intégrée dans le produit risque d'en être compromise. Si le produit est endommagé, le renvoyer à NI pour réparation.

Operating ambient temperature (IEC-60068-2-1, IEC-60068-2-2)	0 °C to 40 °C
Operating relative humidity (IEC-60068-2-56)	10% to 90%, noncondensing
Maximum altitude	2,000 m (800 mbar) (at 25 °C ambient temperature)
Pollution degree	2

Indoor use only.

Note Refer to the **PXIe-7903 Specifications** at ni.com/manuals for complete specifications.

Installing the Software

You must install the FlexRIO driver software before installing the PXIe-7903.

1. Install LabVIEW. Refer to the **LabVIEW Installation Guide** for installation instructions and system requirements. Refer to the **LabVIEW Upgrade Notes** for additional information about upgrading to the most recent version of LabVIEW.
   Documentation for LabVIEW is available at ni.com/manuals and by selecting **Start** » **All Programs** » **National Instruments** » **LabVIEW** » **LabVIEW Manuals**.
2. Install the LabVIEW FPGA Module. Refer to the **LabVIEW FPGA Module Release and Upgrade Notes** for installation instructions and information about getting started with the LabVIEW FPGA Module.
   Documentation for the LabVIEW FPGA Module is available is available at ni.com/manuals and by selecting **Start** » **All Programs** » **National Instruments** » **LabVIEW** » **LabVIEW Manuals**.
3. Install the FlexRIO driver. Refer to the **FlexRIO Readme** on the FlexRIO installation media for system requirements and installation instructions.
   For the latest version of the FlexRIO driver, visit ni.com/downloads
   Documentation for the FlexRIO driver is available at ni.com/manuals and by selecting **Start** » **All Programs** » **National Instruments** » **FlexRIO**.

Installing the PXIe-7903

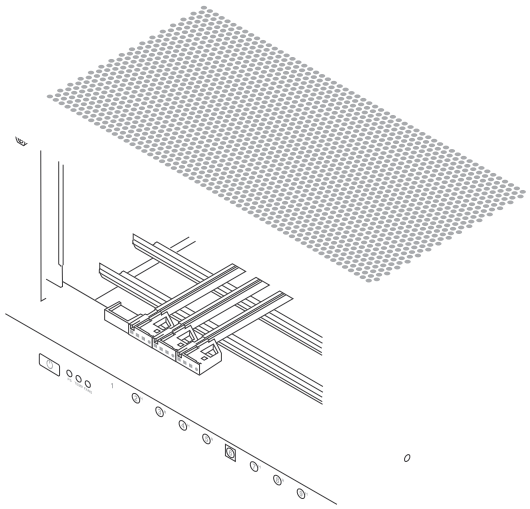
This section contains general installation instructions for installing the PXIe-7903 in a PXI Express chassis.

Note The PXIe-7903 requires a chassis with a slot cooling capacity of 82 W. Refer to chassis specifications to determine the ambient temperature ranges your chassis can achieve.

Refer to your chassis user manual for specific instructions and warnings. To install the module, complete the following steps:

1. Connect the AC power source to the PXI Express chassis before installing the module. The AC power cord grounds the chassis and protects it from electrical damage while you install the module.
2. Ensure that the chassis is powered off.
3. Install the PXIe-7903 into a chassis slot by first placing the module card PCB into the front of the card guides (top and bottom), as shown in the following figure. Slide the module to the rear of the chassis, making sure that the injector/ejector handle is pushed down, as shown in the following figure.
4. When you begin to feel resistance, push up on the injector/ejector handle to fully seat the module into the chassis frame. Secure the module front panel to the chassis using the module front-panel mounting screws.

Figure 2. Installing the PXI-7903 Module



a. Injector/Ejector Handle
b. FlexRIO Module
c. Front Panel Mounting Screws (4x)
d. PXI Express Chassis
e. Injector/Ejector Rail

PXIe-7903 Front Panel

The following table and figures show the available connections on the PXIe-7903.

Table 2. Connector Types

Signal	Connector Type	Description
0–7	MiniSAS zHD	Use passive, copper cables only
8–11	MiniSAS zHD	Use passive or powered optical cables
CLK IN	SMA	Sample Clock or Reference Clock input
CLK Out	SMA	Reference Clock output
DIO	mini-HDMI	Programmable function digital I/O (DIO) connector for use with triggers or events

Figure 3. Ports 0–7 and 8–11

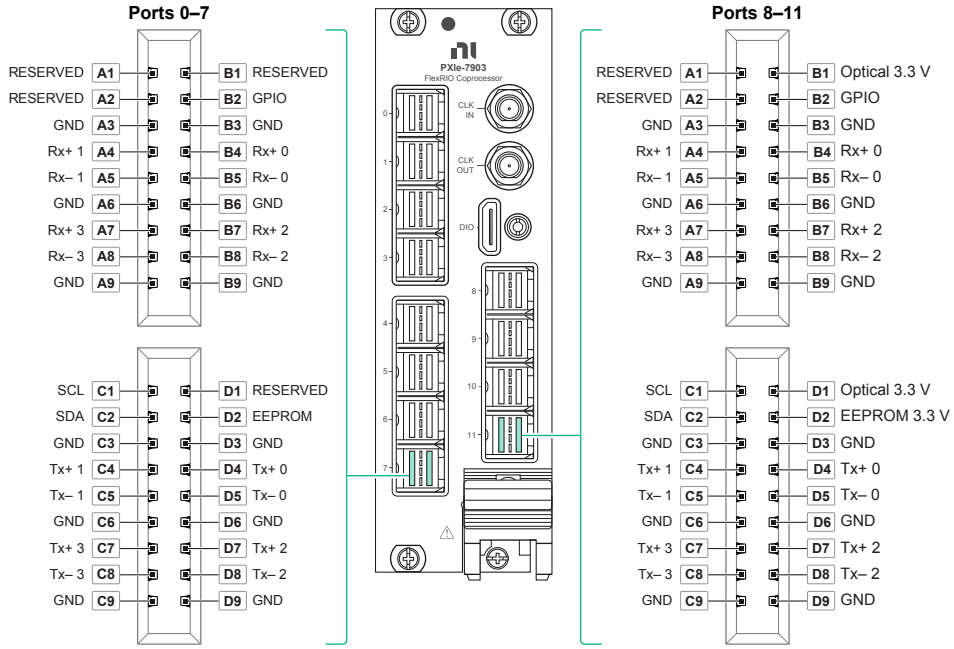


Figure 4. DIO Port

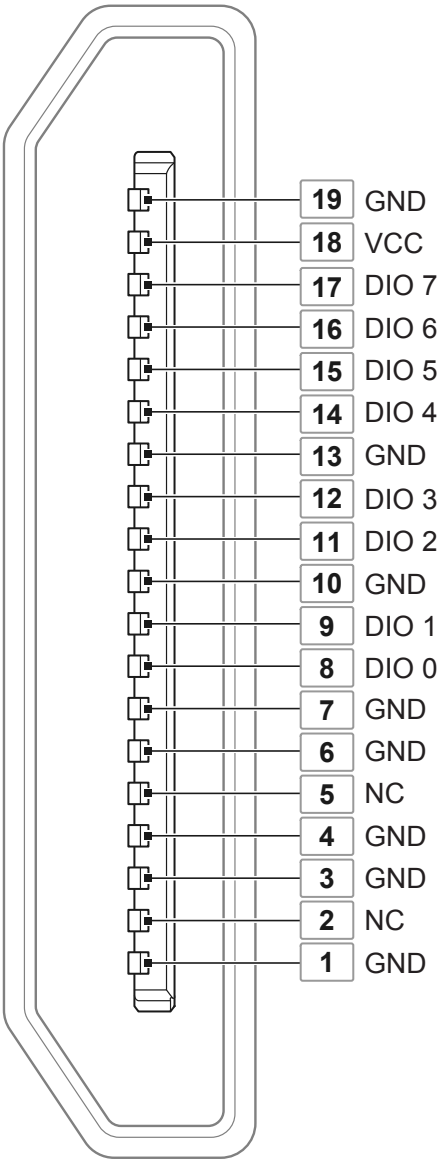


Table 3. NI Mini-HDMI (Type C) Pinout

Pin Number	Signal Type	Signal Description
1	Ground	Ground reference for signals
2	NC	No connection
3	Ground	Ground reference for signals
4	Ground	Ground reference for signals
5	NC	No connection

Pin Number	Signal Type	Signal Description
6	Ground	Ground reference for signals
7	Ground	Ground reference for signals
8	Digital	Digital signal
9	Digital	Digital signal
10	Ground	Ground reference for signals
11	Digital	Digital signal
12	Digital	Digital signal
13	Ground	Ground reference for signals
14	Digital	Digital signal
15	Digital	Digital signal
16	Digital	Digital signal
17	Digital	Digital signal
18	Power	Power provided by PXI module
19	Ground	Ground reference for signals

Notice The DIO port is not an HDMI interface. Do not connect the DIO port on the PXIe-7903 to the HDMI interface of another device. NI is not liable for any damage resulting from such signal connections.

Notice Do not connect a commercial HDMI cable to the PXIe-7903. Instead, use the cable suggested in Recommended Cables.

Verifying the Installation in MAX

Use Measurement & Automation Explorer (MAX) to configure your NI hardware. MAX informs other programs about which NI hardware products are in the system and how they are configured. MAX is automatically installed with FlexRIO.

1. Launch MAX.
2. In the configuration tree, expand **Devices and Interfaces** to see the list of installed NI hardware.
   Installed modules appear under the name of their associated chassis.
3. Expand your **Chassis** tree item.
   MAX lists all modules installed in the chassis. Your default names may vary.

   Note If you do not see your module listed, press <F5> to refresh the list of installed modules. If the module is still not listed, power off the system, ensure the module is correctly installed, and restart.
4. Record the identifier MAX assigns to the hardware. Use this identifier when programming the PXIe-7903.
5. Self-test the hardware by selecting the item in the configuration tree and clicking **Self-Test** in the MAX toolbar.
   MAX self-test performs a basic verification of hardware resources.

Accessing FlexRIO with Integrated I/O Examples

The FlexRIO driver includes several example applications for LabVIEW. These examples serve as interactive tools, programming models, and as building blocks in your own applications. To access all FlexRIO with Integrated I/O getting started examples, complete the following steps.

1. In LabVIEW, click **Help** » **Find Examples**.
2. In the NI Example Finder window that opens, click **Hardware Input and Output** » **FlexRIO** » **Integrated IO** » **Getting Started**.
3. Double click Getting Started with FlexRIO Integrated IO.vi.
   The FlexRIO with Integrated IO Project Creator window opens.
4. Select the example that corresponds to the name of your FlexRIO module. The Description window includes a short description of the getting started example for your device. Rename the project, select a location for the project, and click **OK**.
   The Project Explorer window for your new project opens.

Online examples are also available to demonstrate FlexRIO basics, such as using DRAM, acquiring data, and performing high throughput streaming. To access these examples, search FlexRIO examples in the **Search the community** field at ni.com/examples.

Block Diagram

Figure 5. PXIe-7903 Block Diagram

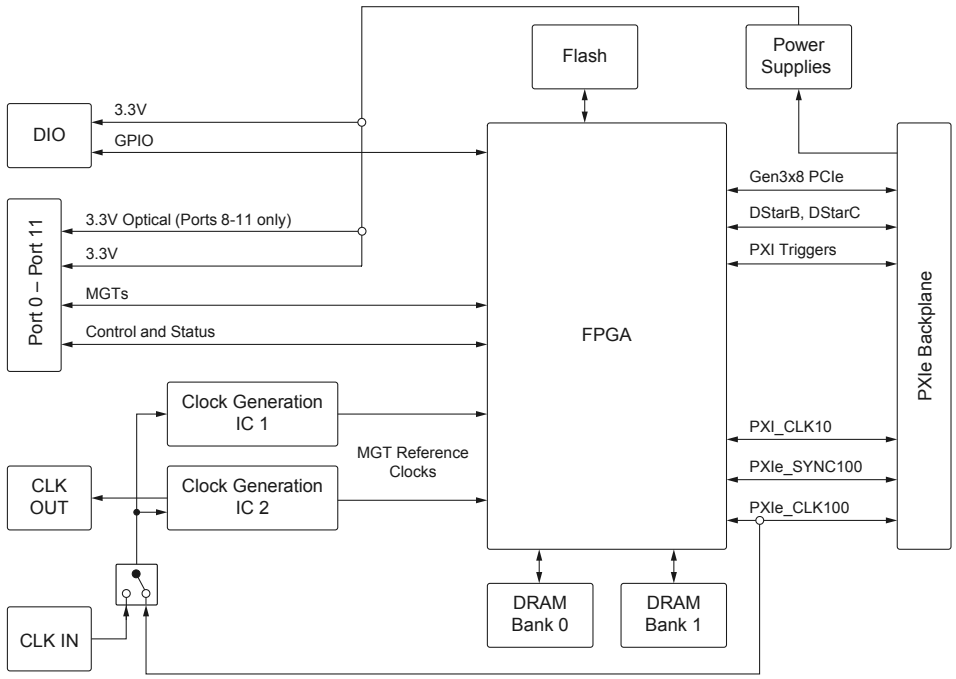


Table 4. MGT Resources

Connector	Mini-SAS zHD Connector Lane	CLIP Signal Name	Common Physical Resource	Channel Physical Resource
Port 0	0	MgtPortRx_p/n(0), MgtPortTx_p/n(0)	GTYE4_COMMON_X0Y0	GTYE4_CHANNEL_X0Y1
	1	MgtPortRx_p/n(1), MgtPortTx_p/n(1)		GTYE4_CHANNEL_X0Y0
	2	MgtPortRx_p/n(2), MgtPortTx_p/n(2)		GTYE4_CHANNEL_X0Y2
	3	MgtPortRx_p/n(3), MgtPortTx_p/n(3)		GTYE4_CHANNEL_X0Y3
Port 1	0	MgtPortRx_p/n(4), MgtPortTx_p/n(4)	GTYE4_COMMON_X0Y1	GTYE4_CHANNEL_X0Y5
	1	MgtPortRx_p/n(5), MgtPortTx_p/n(5)		GTYE4_CHANNEL_X0Y4

Connector	Mini-SAS zHD Connector Lane	CLIP Signal Name	Common Physical Resource	Channel Physical Resource
	2	MgtPortRx_p/n(6), MgtPortTx_p/n(6)		GTYE4_CHANNEL_X0Y6
	3	MgtPortRx_p/n(7), MgtPortTx_p/n(7)		GTYE4_CHANNEL_X0Y7
Port 2	0	MgtPortRx_p/n(8), MgtPortTx_p/n(8)	GTYE4_COMMON_X0Y2	GTYE4_CHANNEL_X0Y9
	1	MgtPortRx_p/n(9), MgtPortTx_p/n(9)		GTYE4_CHANNEL_X0Y8
	2	MgtPortRx_p/n(10), MgtPortTx_p/n(10)		GTYE4_CHANNEL_X0Y10
	3	MgtPortRx_p/n(11), MgtPortTx_p/n(11)		GTYE4_CHANNEL_X0Y11
Port 3	0	MgtPortRx_p/n(12), MgtPortTx_p/n(12)	GTYE4_COMMON_X0Y3	GTYE4_CHANNEL_X0Y13
	1	MgtPortRx_p/n(13), MgtPortTx_p/n(13)		GTYE4_CHANNEL_X0Y12
	2	MgtPortRx_p/n(14), MgtPortTx_p/n(14)		GTYE4_CHANNEL_X0Y14
	3	MgtPortRx_p/n(15), MgtPortTx_p/n(15)		GTYE4_CHANNEL_X0Y15
Port 4	0	MgtPortRx_p/n(16), MgtPortTx_p/n(16)	GTYE4_COMMON_X1Y4	GTYE4_CHANNEL_X1Y17

Connector	Mini-SAS zHD Connector Lane	CLIP Signal Name	Common Physical Resource	Channel Physical Resource
	1	MgtPortRx_p/n(17), MgtPortTx_p/n(17)		GTYE4_CHANNEL_X1Y16
	2	MgtPortRx_p/n(18), MgtPortTx_p/n(18)		GTYE4_CHANNEL_X1Y18
	3	MgtPortRx_p/n(19), MgtPortTx_p/n(19)		GTYE4_CHANNEL_X1Y19
Port 5	0	MgtPortRx_p/n(20), MgtPortTx_p/n(20)	GTYE4_COMMON_X1Y5	GTYE4_CHANNEL_X1Y21
	1	MgtPortRx_p/n(21), MgtPortTx_p/n(21)		GTYE4_CHANNEL_X1Y20
	2	MgtPortRx_p/n(22), MgtPortTx_p/n(22)		GTYE4_CHANNEL_X1Y22
	3	MgtPortRx_p/n(23), MgtPortTx_p/n(23)		GTYE4_CHANNEL_X1Y23
Port 6	0	MgtPortRx_p/n(24), MgtPortTx_p/n(24)	GTYE4_COMMON_X1Y6	GTYE4_CHANNEL_X1Y25
	1	MgtPortRx_p/n(25), MgtPortTx_p/n(25)		GTYE4_CHANNEL_X1Y24

Connector	Mini-SAS zHD Connector Lane	CLIP Signal Name	Common Physical Resource	Channel Physical Resource
	2	MgtPortRx_p/n(26), MgtPortTx_p/n(26)		GTYE4_CHANNEL_X1Y26
	3	MgtPortRx_p/n(27), MgtPortTx_p/n(27)		GTYE4_CHANNEL_X1Y27
Port 7	0	MgtPortRx_p/n(28), MgtPortTx_p/n(28)	GTYE4_COMMON_X1Y7	GTYE4_CHANNEL_X1Y29
	1	MgtPortRx_p/n(29), MgtPortTx_p/n(29)		GTYE4_CHANNEL_X1Y28
	2	MgtPortRx_p/n(30), MgtPortTx_p/n(30)		GTYE4_CHANNEL_X1Y30
	3	MgtPortRx_p/n(31), MgtPortTx_p/n(31)		GTYE4_CHANNEL_X1Y31
Port 8	0	MgtPortRx_p/n(32), MgtPortTx_p/n(32)	GTYE4_COMMON_X0Y4	GTYE4_CHANNEL_X0Y17
	1	MgtPortRx_p/n(33), MgtPortTx_p/n(33)		GTYE4_CHANNEL_X0Y16
	2	MgtPortRx_p/n(34), MgtPortTx_p/n(34)		GTYE4_CHANNEL_X0Y18

Connector	Mini-SAS zHD Connector Lane	CLIP Signal Name	Common Physical Resource	Channel Physical Resource
	3	MgtPortRx_p/n(35), MgtPortTx_p/n(35)		GTYE4_CHANNEL_X0Y19
Port 9	0	MgtPortRx_p/n(36), MgtPortTx_p/n(36)	GTYE4_COMMON_X0Y5	GTYE4_CHANNEL_X0Y21
	1	MgtPortRx_p/n(37), MgtPortTx_p/n(37)		GTYE4_CHANNEL_X0Y20
	2	MgtPortRx_p/n(38), MgtPortTx_p/n(38)		GTYE4_CHANNEL_X0Y22
	3	MgtPortRx_p/n(39), MgtPortTx_p/n(39)		GTYE4_CHANNEL_X0Y23
Port 10	0	MgtPortRx_p/n(40), MgtPortTx_p/n(40)	GTYE4_COMMON_X0Y6	GTYE4_CHANNEL_X0Y25
	1	MgtPortRx_p/n(41), MgtPortTx_p/n(41)		GTYE4_CHANNEL_X0Y24
	2	MgtPortRx_p/n(42), MgtPortTx_p/n(42)		GTYE4_CHANNEL_X0Y26
	3	MgtPortRx_p/n(43), MgtPortTx_p/n(43)		GTYE4_CHANNEL_X0Y27

Connector	Mini-SAS zHD Connector Lane	CLIP Signal Name	Common Physical Resource	Channel Physical Resource
Port 11	0	MgtPortRx_p/n(44), MgtPortTx_p/n(44)	GTYE4_COMMON_X0Y7	GTYE4_CHANNEL_X0Y29
	1	MgtPortRx_p/n(45), MgtPortTx_p/n(45)		GTYE4_CHANNEL_X0Y28
	2	MgtPortRx_p/n(46), MgtPortTx_p/n(46)		GTYE4_CHANNEL_X0Y30
	3	MgtPortRx_p/n(47), MgtPortTx_p/n(47)		GTYE4_CHANNEL_X0Y31

Each reference clock is driven by one of the two clocking integrated circuits (ICs), listed in the following table. Each clocking IC can generate two independent frequencies, for a total of four possible frequencies across all ports.

Note MgtRefClk_p/n are connected to REFCLK0 of each respective quad.

Table 5. MGT Clocking

Connector	CLIP Signal Name	Common Physical Resource	User Clock Index	Clocking IC
CLK OUT	N/A	N/A	0	2
Port 0	MgtRefClk_p/n(0)	GTYE4_COMMON_X0Y0	1[2]	1
Port 1	MgtRefClk_p/n(1)	GTYE4_COMMON_X0Y1		
Port 2	MgtRefClk_p/n(2)	GTYE4_COMMON_X0Y2	2[3]	

[2] User Clock 1 controls both MgtRefClk_p/n(0) and MgtRefClk_p/n(1). These clocks cannot be independently configured.

Connector	CLIP Signal Name	Common Physical Resource	User Clock Index	Clocking IC
Port 3	MgtRefClk_p/n(3)	GTYE4_COMMON_X0Y3		
Port 4	MgtRefClk_p/n(4)	GTYE4_COMMON_X1Y4	3	2
Port 5	MgtRefClk_p/n(5)	GTYE4_COMMON_X1Y5	4	
Port 6	MgtRefClk_p/n(6)	GTYE4_COMMON_X16	5	
Port 7	MgtRefClk_p/n(7)	GTYE4_COMMON_X1Y7	6	
Port 8	MgtRefClk_p/n(8)	GTYE4_COMMON_X0Y4	7	1
Port 9	MgtRefClk_p/n(9)	GTYE4_COMMON_X0Y5	8	
Port 10	MgtRefClk_p/n(10)	GTYE4_COMMON_X0Y6	9	
Port 11	MgtRefClk_p/n(11)	GTYE4_COMMON_X0Y7	10	

[3] User Clock 2 controls both MgtRefClk_p/n(2) and MgtRefClk_p/n(3). These clocks cannot be independently configured.

Component-Level Intellectual Property (CLIP)

The LabVIEW FPGA Module includes component-level intellectual property (CLIP) for HDL IP integration. FlexRIO devices support two types of CLIP: user-defined and socketed.

- **User-defined CLIP** allows you to insert HDL IP into an FPGA target, enabling VHDL code to communicate directly with an FPGA VI.
- **Socketed CLIP** provides the same IP integration of the user-defined CLIP, but it also allows the CLIP to communicate directly with circuitry external to the FPGA. Adapter module socketed CLIP allows your IP to communicate directly with both the FPGA VI and the external adapter module connector interface.

The PXIe-7903 ships with socketed CLIP items that add module I/O to the LabVIEW project.

Refer to **Configuring Your Adapter Module Using LabVIEW FPGA** in FlexRIO documentation for more information about CLIP.

Adding the Socketed CLIP to a LabVIEW Project (FPGA Module)

Before you begin, ensure that you have installed your hardware into the chassis and completed the steps in Installing the Software.

Add a component-level IP (CLIP) item to the LabVIEW project to instantiate the CLIP inside the FPGA.

Complete the following steps to add a CLIP item in a project:

1. Create and save a new LabVIEW project (for example, My7903Clip.lvproj).
2. Add an FPGA target that supports CLIP to the project.
3. Right-click the FPGA target and select **Properties** from the shortcut menu to display the FPGA Target Properties dialog box.
4. Select **Component-Level IP** from the **Category** list to display the Component-Level IP Properties page.
5. Click **Add**, select the declaration XML file for the socketed clip, and then click **OK**.

   Note The CLIP wizard automatically adds the declaration XML file to the project.

6. Click **OK** to close the FPGA Target Properties dialog box.
7. In the Project Explorer window, right-click the IO Socket under the FPGA target, and select **Properties** from the shortcut menu.
8. On the **General** page of the IO Socket Properties dialog box, select the socketed CLIP to instantiate.
9. On the **Clock Selections** page, select the appropriate clocks for the CLIP. Clock selections will vary depending on CLIP requirements.
10. Click **OK**. Notice that the Project Explorer window now includes socketed CLIP under the IO Socket, as well as the I/O defined in the declaration XML file.

Troubleshooting

If an issue persists after you complete a troubleshooting procedure, search our KnowledgeBase for additional information our technical support engineers create as they answer common user questions and resolve unexpected issues.

What Should I Do if the PXIe-7903 Does Not Appear in MAX?

1. In the MAX configuration tree, expand **Devices and Interfaces**.
2. Expand the **Chassis** tree to see the list of installed hardware, and press <F5> to refresh the list.
3. If the module is still not listed, power off the system, ensure that all hardware is correctly installed, and restart the system.
4. Navigate to the Device Manager by right-clicking the Start button, and selecting **Device Manager**.
5. Verify the PXIe-7903 appears in the Device Manager.
    a. Under an NI entry, confirm that a PXIe-7903 entry appears.

    > **Note** If you are using a PC with a device for PXI remote control system, under **System Devices**, also confirm that no error conditions appear for the **PCI-to-PCI Bridge**.

    b. If error conditions appear, reinstall the FlexRIO driver.

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