PXIe-7903 Specifications

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PXIe-7903 Specifications

Definitions

Warranted specifications describe the performance of a model under stated operating conditions and are covered by the model warranty.

Characteristics describe values that are relevant to the use of the model under stated operating conditions but are not covered by the model warranty.

- **Typical** specifications describe the performance met by a majority of models.
- **Nominal** specifications describe an attribute that is based on design, conformance testing, or supplemental testing.
- **Measured** specifications describe the measured performance of a representative model.

Specifications are **Typical** unless otherwise noted.

Conditions

Specifications are valid under the following conditions unless otherwise noted.

- Ambient temperature of 0 °C to 40 °C .
- Installed in chassis with slot cooling capacity ≥82 W.

Front Panel

Figure 1 shows the front panel of the PXIe-7903 module.

Figure 1. PXIe-7903 Front Panel

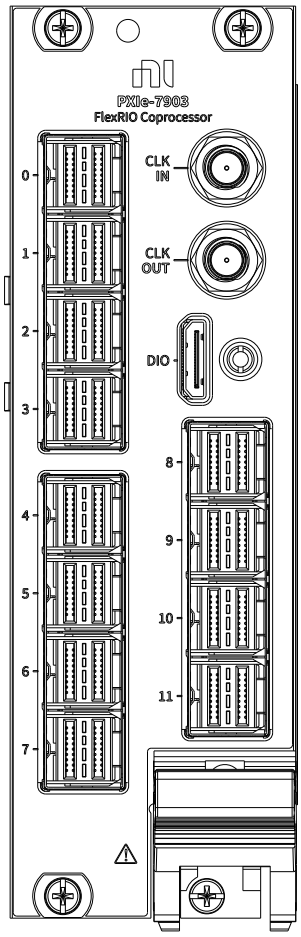

Table 1 describes the PXIe-7903 front panel connectors.

Table 1. Front Panel Connectors

Connector	Description
Ports 0–11	Mini-SAS HD connectors that provide a high speed serial interface.
CLK IN	SMA (f) input for reference clock.
CLK OUT	SMA (f) output terminal for reference clock.
DIO	Programmable function digital I/O (DIO) connector for use with triggers or events.

Front Panel Ports

Ports 0 – 11

Connector	Mini-SAS HD
Data rate	500 Mb/s to 28.2 Gb/s
Supported high-speed cable type	Ports 0–7: Passive, copper cables only. Ports 8–11: Passive cables and powered optical cables.[1]
Multi-gigabit transceivers (MGTs)	
Total number of MGTs	48 (4 per connector)
I/O AC coupling capacitor	100 nF

CLK OUT

Connector	SMA
Coupling	AC
Output impedance	50 Ω, nominal
Frequency range	2.344 MHz to 385.714 MHz 400.000 MHz to 450.000 MHz 480.000 MHz to 675.000 MHz

[1] Ports 8–11 can provide power at 3.3 V ±5%, 1 A for active optical cables but NI has not validated these cables across the range of data rates and protocols. NI strongly recommends that the system designer specifies and validates appropriate active optical cables for the intended application.

	685.714 MHz to 771.428 MHz 800.000 MHz to 900.000 MHz 960.000 MHz to 1000.000 MHz
Output voltage range	0.61 V peak-to-peak to 1.04 V peak-to-peak

CLK IN

Connector	SMA
Input coupling	AC
Input impedance	50 Ω
Frequency range	10 MHz to 300 MHz
Input voltage range	0.3 V peak-to-peak to 4 V peak-to-peak
Absolute maximum voltage	5 V peak-to-peak AC
Duty cycle	45% to 55%

Digital I/O (DIO)

Connector	Mini-HDMI

Notice The DIO port is not an HDMI interface. Do not connect the DIO port on the PXIe-7903 to the HDMI interface of another device. NI is not liable for any damage resulting from such signal connections.

Number of channels	8
Signal type	Single-ended
Voltage families	3.3 V, 2.5 V, 1.8 V
Input impedence	100 kΩ, nominal
Output impedence	50 kΩ, nominal
Signal direction control	Per channel
Minimum latency required for direction change	200 ns
Maximum frequency	60 MHz
5.0 V Power	±5%, 50 mA maximum, nominal

Reconfigurable FPGA

The PXIe-7903 provides a XCVU11P FPGA with characteristics shown in the following table.

Table 2. XCVU11P FPGA Characteristics

Characteristics	XCVU11P
System Logic Cells	2,835 K
DSP slices (27 × 18 multiplier)	9,216
Embedded Block RAM	341.0 Mb
Timebase reference sources	PXI Express 100 MHz (PXIe_CLK100)
Data transfers	DMA, interrupts, programmed I/O, multi-gigabit transceivers
Number of DMA channels	60

Note The list above depicts the total number of FPGA resources available on the part. The number of resources available to the user is slightly lower, as some FPGA resources are consumed by board-interfacing IP for PCI Express, device configuration, and various board I/O. For more information, contact NI Support.

Onboard DRAM

Memory size	20 GB (2 banks of 10 GB)
DRAM clock rate	1333 MHz
Physical bus width	80 bit
LabVIEW FPGA DRAM clock rate	333 MHz
LabVIEW FPGA DRAM bus width	640 bits per bank
Maximum theoretical data rate	53.2 GB/s (26.6 GB/s per bank)

Bus Interface

Form factor	PCI Express Gen-3 x8

Maximum Power Requirements

Note Power requirements are dependent on the contents of the LabVIEW FPGA VI used in your application.

Maximum Current

+3.3 V	6 A
+12 V	12 A
Maximum total power	164 W

Power consumption is from both PXI Express backplane power connectors.

Physical Characteristics

Dimensions (not including connectors)	3U, two-slot PXI Express module, 21.6 cm × 4.1 cm × 13.0 cm (8.5 in. × 1.6 in. × 5.1 in.)
Weight	1134 g (40.0 oz)

Environmental Characteristics

Temperature	
Operating[2]	0 °C to 40°C
Storage	-40 °C to 71°C
Humidity	
Operating	10% to 90%, noncondensing
Storage	5% to 95%, noncondensing

Pollution Degree	2

[2] The PXIe-7903 requires a chassis with 82 W slot cooling capacity. Refer to chassis specifications to determine the ambient temperature ranges your chassis can achieve.

Maximum altitude	2,000 m (800 mbar) (at 25 °C ambient temperature)

Shock and Vibration	
Operating vibration	5 Hz to 500 Hz, 0.3 g RMS
Non-operating vibration	5 Hz to 500 Hz, 2.4 g RMS
Operating shock	30 g, half-sine, 11 ms pulse

Note In operational environments that could subject the device to shock impulses, use ample strain relief on all cable assemblies near the front panel connection points, and also support the mass of cables further away from the device.