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GETTING STARTED GUIDE

MIMO Prototyping System

This document explains how to use the MIMO Application Framework with a modular hardware system consisting of multiple universal software radio peripheral (USRP) devices in a multiple input, multiple output (MIMO) configuration.

Contents

NATIONAL INSTRUMENTS™

System Requirements

Software Requirements

- Microsoft Windows 8/7 (64-bit) preinstalled on the PXI controller
- NI-USRP 15.5
- LabVIEW Communication System Design Suite 2.0
- MIMO Application Framework 1.0

The installation of NI software is started by running `setup.exe` from the provided installation media. Follow the installer prompts to complete the installation process.

Hardware Requirements

Depending on the configuration, the main system hardware components are listed in the following table.

Table 1. MIMO Base Station (BS) Parts List[1]

Description	Quantity needed for each configuration			
	128 antennas (8 subsystems)	**64 antennas (4 subsystems)**	**32 antennas (2 subsystems)**	**16 antennas (1 subsystem)**
USRP RIO Software Defined Radio (SDR)[2]	64	32	16	8
x4 MXI-Express Cable	64	32	16	8
PXIe-1085 Chassis (18-Slot, 24 GB/s Sys Bandwidth (BW))	1	1	1	1
PXIe-8135 Controller	1	1	1	1
PXIe-7976R FPGA Module for FlexRIO	5	3	2	2
PXIe-6674T Synchronization Module	1	1	1	1
2.4 GHz and 5 GHz Dual Band Vertical Antenna	128	64	32	16
CDA-2990 Clock Distribution Device[3]	9	5	3	1
8 GB RAM Upgrade for PXIe-8135	1	1	1	1
PXIe-8384 Remote Control Module (x8 Gen2 MXI-Express)	8	4	2	1
x8 MXI-Express Cable	8	4	2	1
SMA to SMA Cable	19	11	7	3
CPS-8910 Switch Device for PCI Express[4]	8	4	2	1

[1] This is not a complete list of required hardware. For a complete list please contact your local sales representative.

[2] USRP-2940R/2942R/2943R/2944R/2950R/2952R/2953R/2954R.

[3] Also referred to as a Clock Distribution Accessory (CDA).

[4] Also referred to as a Cabled PXI Express Switch Box (CPS).

Hardware Setup

Electromagnetic Compatibility Guidelines

The individual components of this product were tested and comply with the regulatory requirements and limits for electromagnetic compatibility (EMC) stated in their respective specifications. These requirements and limits provide reasonable protection against harmful interference when the product is operated in the intended operational electromagnetic environment. However, the system as a whole has not been through EMC testing as a unit and the users are expected to use it in a way that complies to all regulations in their region.

To minimize interference with radio and television reception and prevent unacceptable performance degradation, install and use this product in strict accordance with the instructions in the product documentation.

Furthermore, any changes or modifications to the product not expressly approved by National Instruments could void your authority to operate it under your local regulatory rules.

Note In the United States (per FCC 47 CFR), Class A equipment is intended for use in commercial, light-industrial, and heavy-industrial locations. In Europe, Canada, Australia, and New Zealand (per CISPR 11), Class A equipment is intended for use only in heavy-industrial locations.

Caution The MIMO System is intended for use only indoors test environment as test and measurement equipment. This product is intended for professional use only.

Caution To ensure the specified EMC performance, operate this product only with shielded cables and accessories.

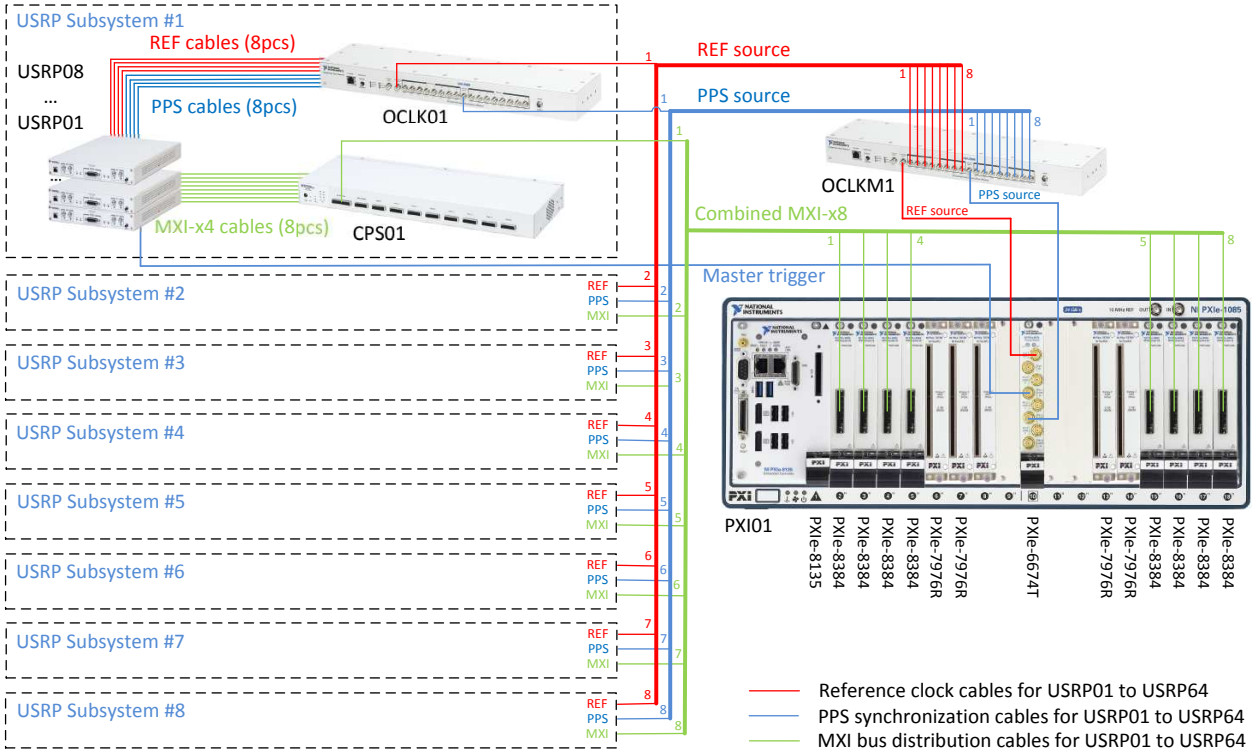
Caution To ensure the specified EMC performance, operate this product only with cables less than 3 meters in length.

About the Hardware

The system consists of the BS and Mobile Station (MS).

Base Station

Figure 1. Base Station



The BS consists of the PXIe-8135 controller, one to eight PXIe-8384 MXI-Express modules for communication with the USRP RIO devices (through the CPS-8910), up to five PXIe-7976R modules (depending on the number of USRP subsystems), and a PXIe-6674T module, installed on the PXIe-1085 chassis.

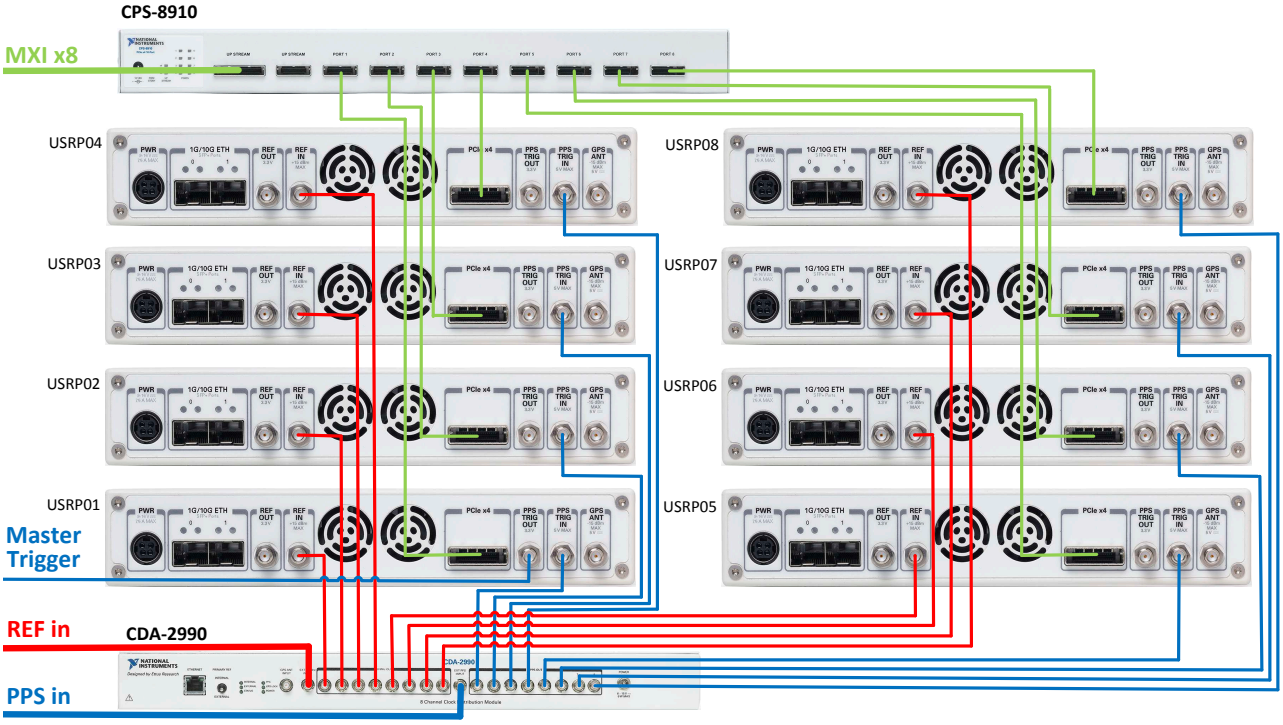
Clock and synchronization signals are distributed to up to eight USRP subsystems through the CDA-2990 (OCLKM1)[5]. It provides both clock and time synchronization by amplifying and splitting a 10 MHz reference signal, generated by the PXIe-6674T and the pulse per second (PPS) signal from master USRP, eight ways through matched-length traces.

The system can control up to eight USRP subsystems. Each subsystem consists of eight USRP RIO devices, connected to the CPS-8910 device (CPS01 to CPS08). The clock and synchronization signals received by the USRP subsystem are distributed among the eight USRP RIO devices in the subsystem through the CDA-2990 (OCLK01 to OCLK08). A detailed connections diagram for each USRP subsystem is given in **Figure 2**.

Note The lengths of used cables are critical for timing. The signal path (the sum of the lengths of all cables from the PXIe-6674T module to each USRP RIO) must be equal for each channel.

[5] Not required for the single subsystem configuration (up to 16 antennas), in which both clock and PPS are provided directly from the PXIe-6674T module.

Figure 2. Connections in Each USRP Subsystem



Mobile Station

The MIMO Application Framework supports up to 12 simultaneous MSs. An MS represents a handset or other wireless device with single input, single output (SISO) wireless capabilities. The MS prototype uses a USRP RIO with an integrated GPS disciplined oscillator[6] (GPSDO)[7], connected to a PC (typically a laptop) or PXI chassis using a cabled PCI Express to an ExpressCard. A typical testbed implementation includes multiple MSs where each USRP RIO might represent one or two MS devices. Software on the MS is implemented as a single antenna system, placing the physical layer (PHY) in the FPGA of the USRP RIO while the basic media access control (MAC) layer functionality (data piping) is split between the FPGA and host.

[6] The GPSDO is important because it provides improved clock accuracy and enables synchronization and geo-location capability if needed in future system expansion.

[7] USRP-2950R/2952R/2953R/2954R (USRP-295x)

Figure 3. Typical MS Setup with Laptop and USRP RIO

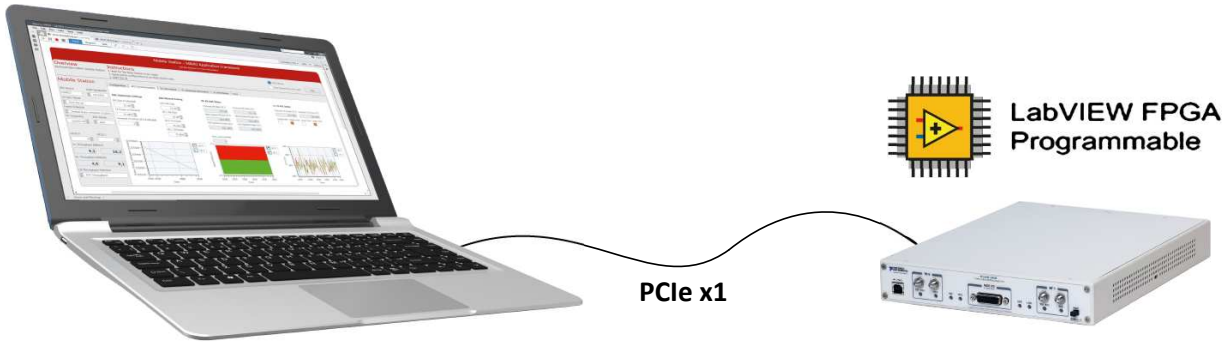


Table 2 provides a quick reference of parts used in a single MS system. It includes hardware devices and cables used to connect the devices as shown in Figure 3. Alternatively, a PCI Express connection can be used if a desktop or PXI chassis is chosen for the MS controller.

Table 2. Mobile Station Equipment

Description	Per MS
USRP-295x device	1
USRP RIO Laptop Connectivity Kit (ExpressCard and Cable)	1
Laptop with ExpressCard Slot	1

System Configurations

The software can be configured to use four to 128 antennas, and the BS is typically used in one of the following configurations:

- 16 antenna MIMO (1 USRP subsystem)
- 32 antenna MIMO (2 USRP subsystems)
- 64 antenna MIMO (4 USRP subsystems)
- 128 antenna MIMO (8 USRP subsystems)

Refer to the Connection Diagrams section for detailed connection diagrams for BS systems based on each configuration.

Hardware Setup

Rack Assembly Diagrams

Figure 4. 16-Antenna System

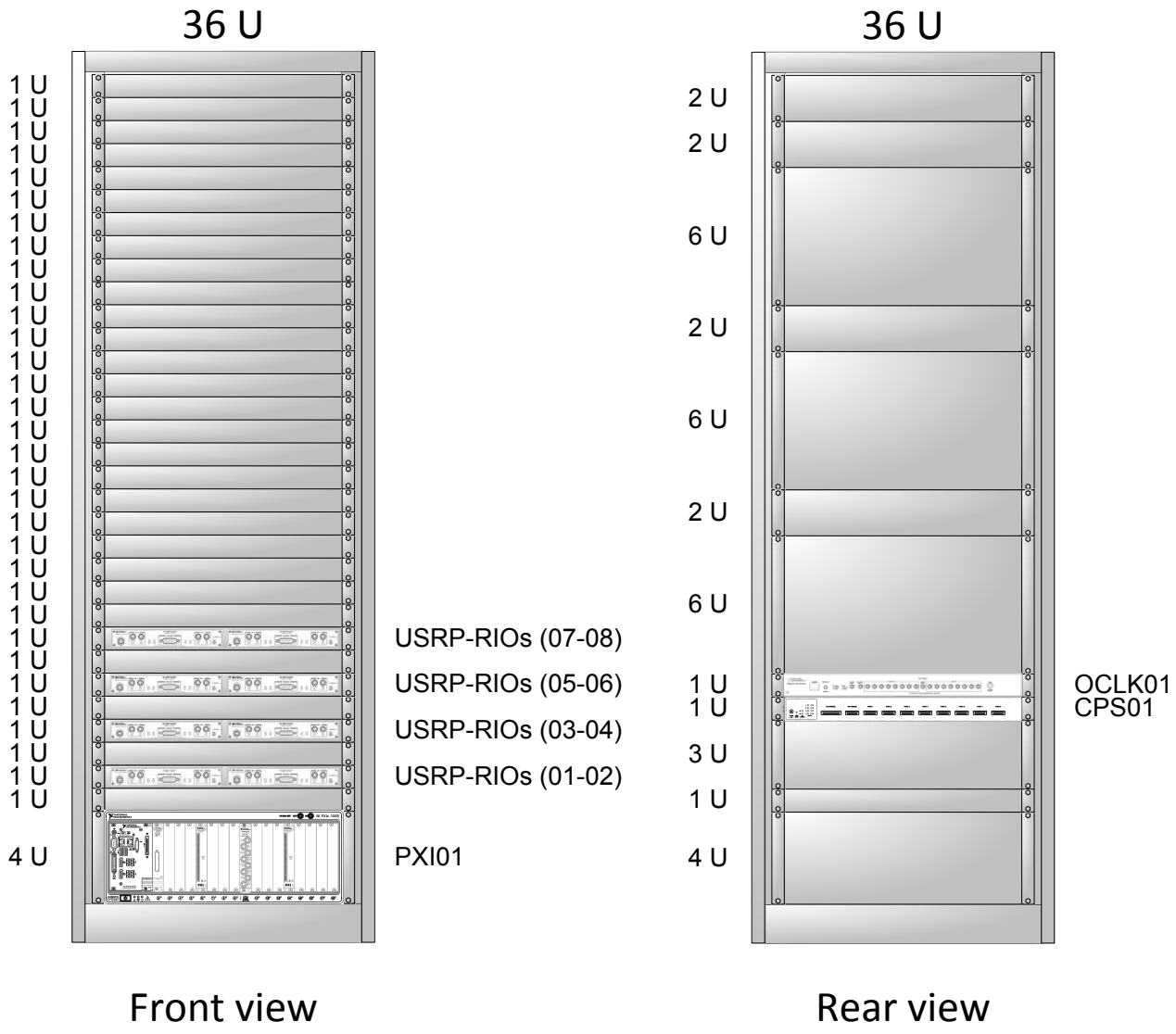


Figure 5. 32-Antenna System

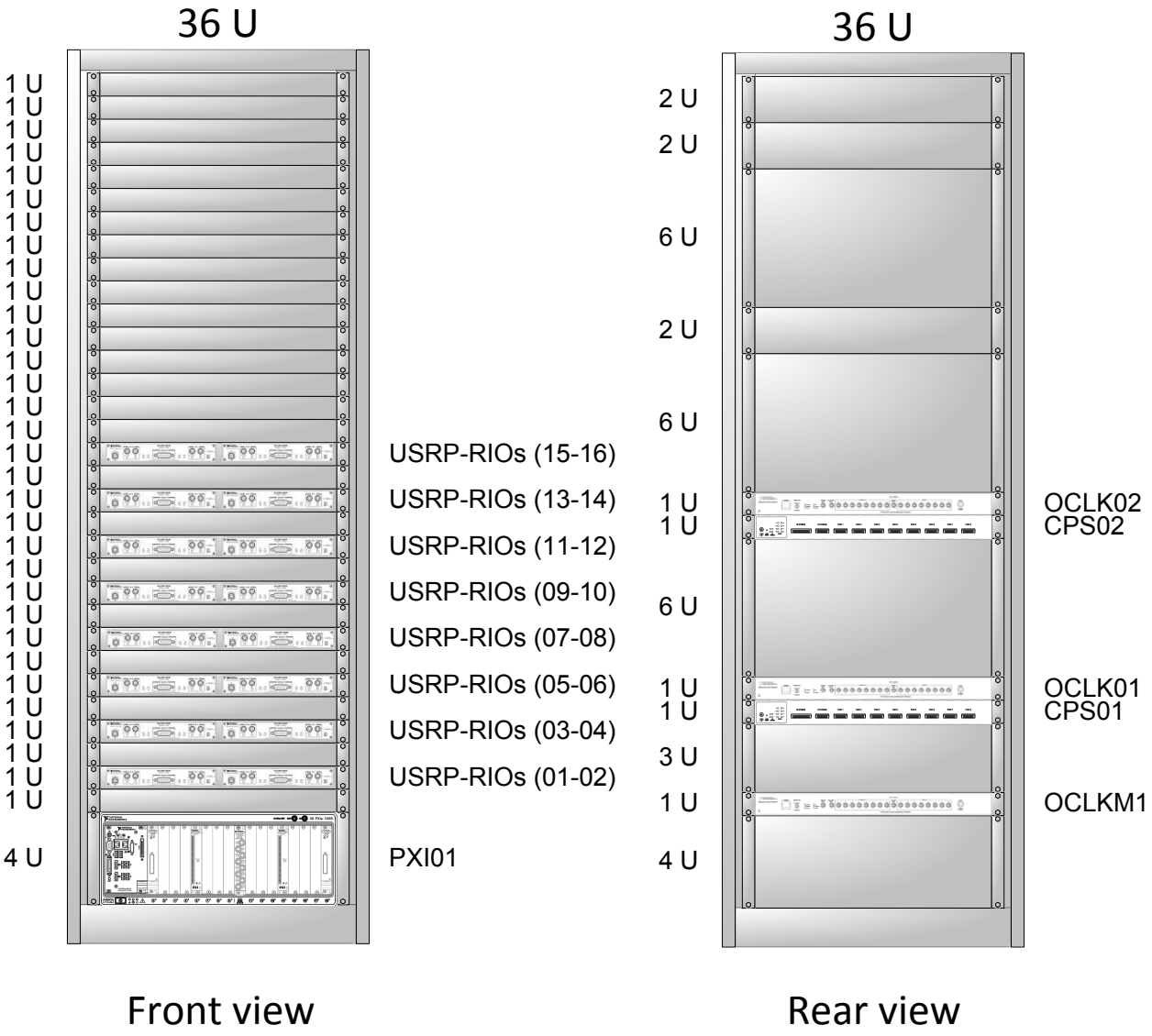


Figure 6. 64-Antenna System

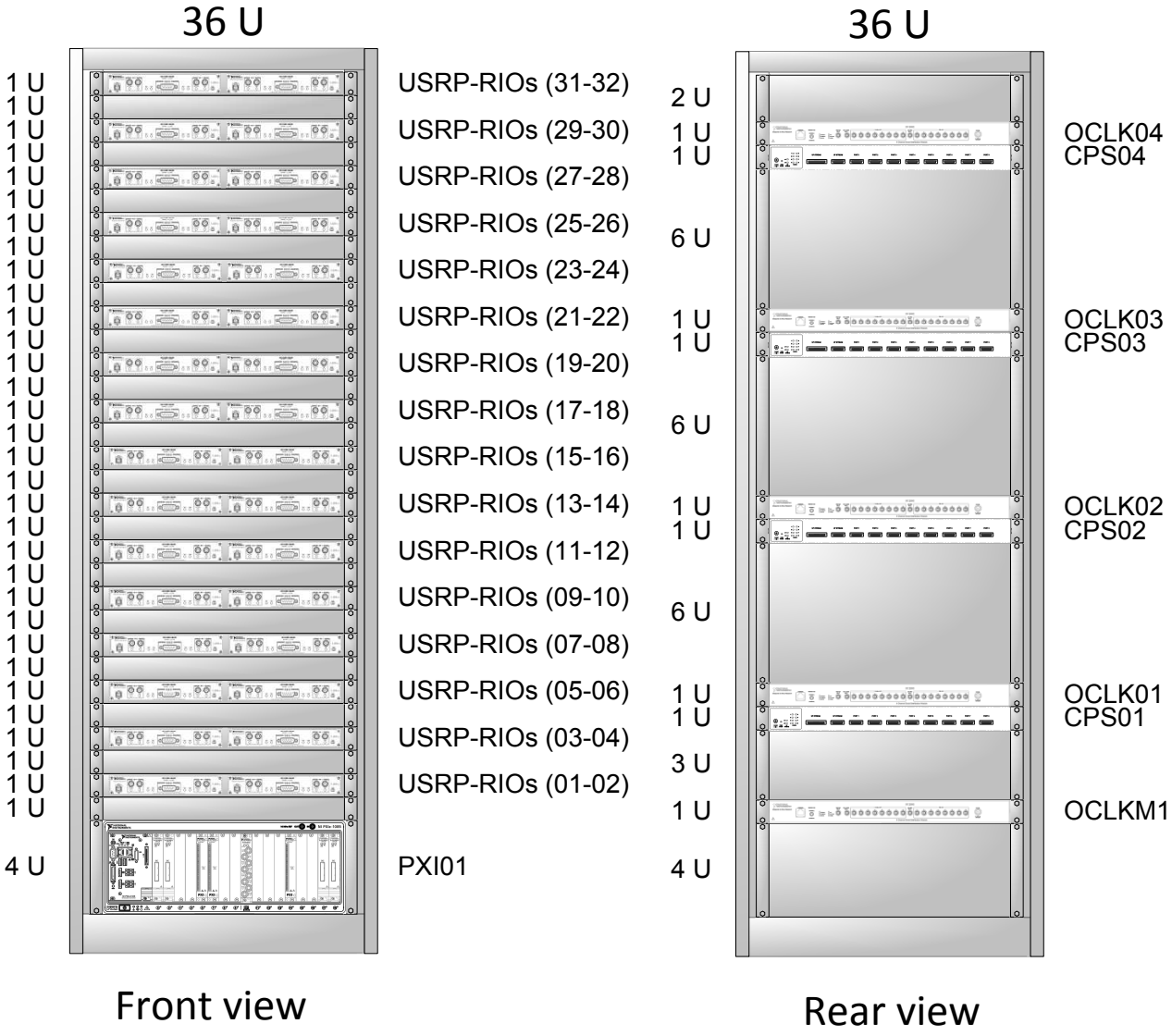


Figure 7. 128-Antenna System: Subrack 1 of 2

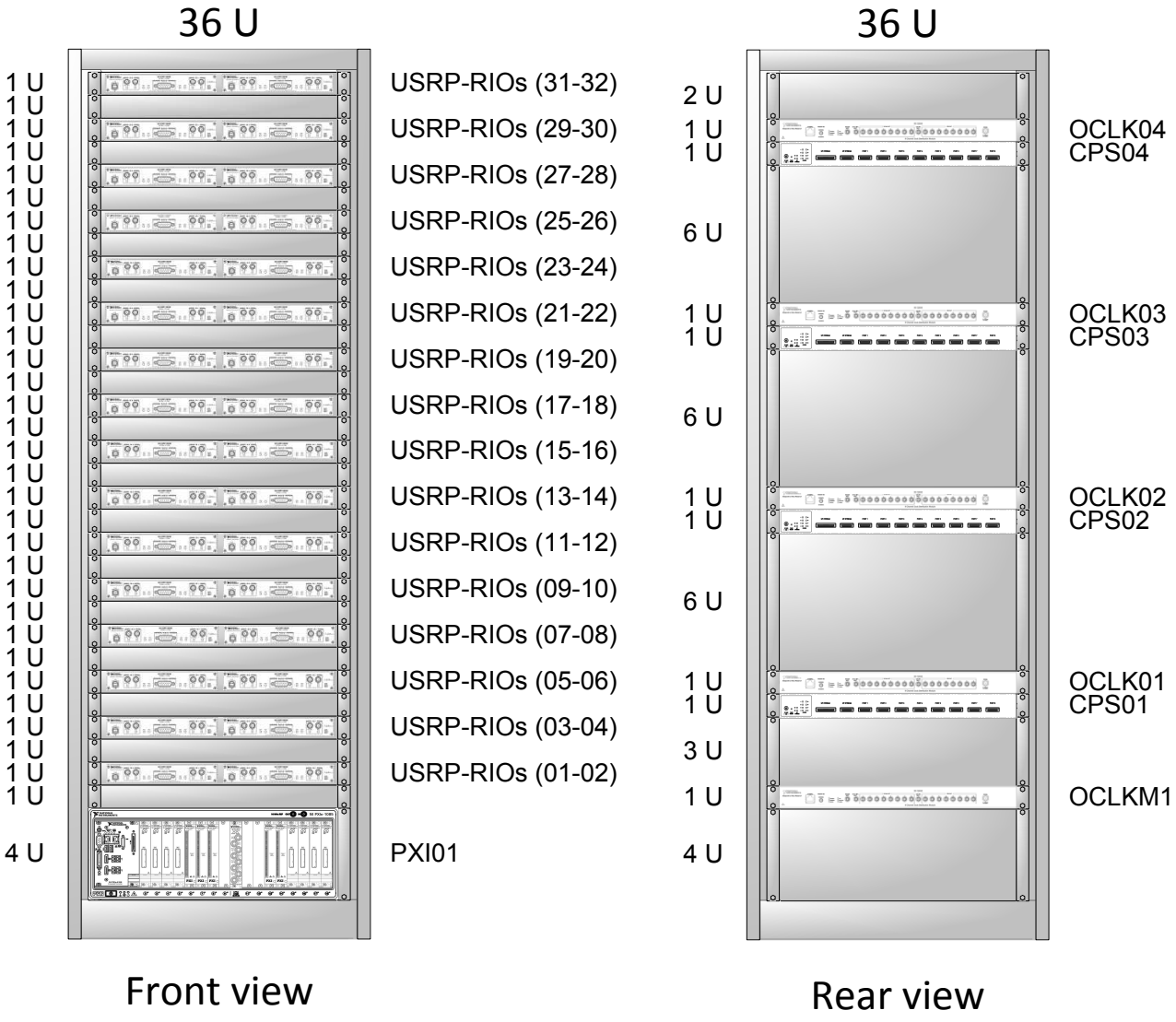
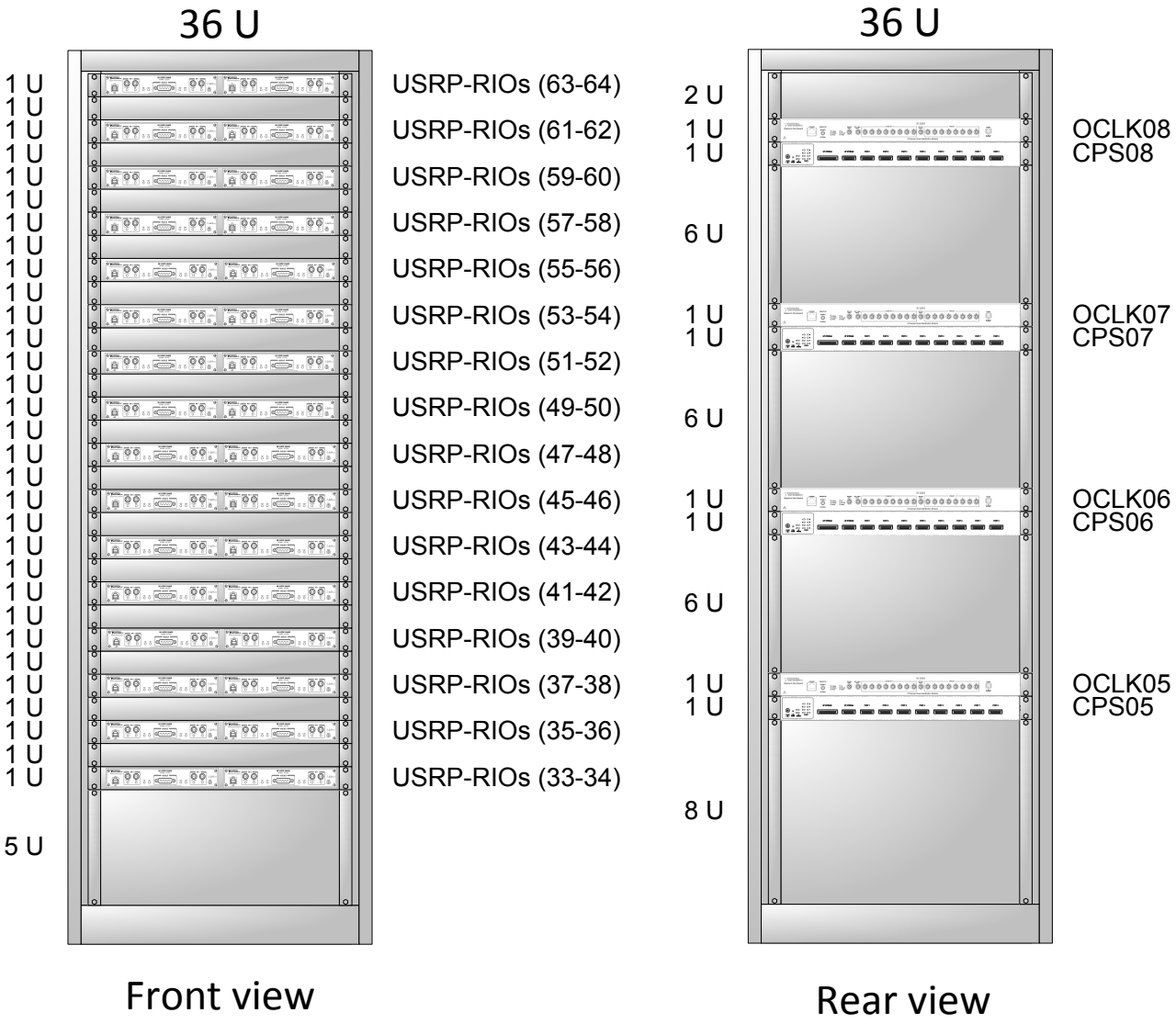


Figure 8. 128-Antenna System: Subrack 2 of 2



Installing PXIe Modules

Install the PXIe modules on the chassis in accordance with the hardware configuration as shown in the following table.

Table 3. MIMO BS Parts

PXIe-1085 slot #	Number of Antennas (USRP subsystems)			
	128 (8)	64 (4)	32 (2)	16 (1)
1	PXIe-8135	PXIe-8135	PXIe-8135	PXIe-8135
2	PXIe-8384	PXIe-8384	PXIe-8384	PXIe-8384
3	PXIe-8384	PXIe-8384	–	–
4	PXIe-8384	–	–	–
5	PXIe-8384	–	–	–
6	PXIe-7976R	PXIe-7976R	PXIe-7976R	PXIe-7976R
7	PXIe-7976R	PXIe-7976R	–	–
8	PXIe-7976R	–	–	–
9	–	–	–	–
10	PXIe-6674T	PXIe-6674T	PXIe-6674T	PXIe-6674T
11	–	–	–	–
12	–	–	–	–
13	PXIe-7976R	–	–	–
14	PXIe-7976R	PXIe-7976R	PXIe-7976R	PXIe-7976R
15	PXIe-8384	–	–	–
16	PXIe-8384	–	–	–
17	PXIe-8384	PXIe-8384	–	–
18	PXIe-8384	PXIe-8384	PXIe-8384	–

Refer to the Connection Diagrams section for detailed connection diagrams and interconnections tables.

Cable Connections

Cabled connections between various hardware components of the system are listed in Tables 4 through 9 below.

Table 4. Cable Connections within USRP Subsystems

Device #1	Port	Device #2	Port	Cable type and quantity	Description
USRP01 to USRP08	REF IN	CDA	10 MHz OUT 1 to 8	RF_coax (x8)	Reference clock for USRP
USRP01 to USRP08	PPS TRIG IN	CDA	PPS OUT 1 to 8	RF_coax (x8)	PPS trigger for USRP
USRP01 to USRP08	PCIe x4	CPS	PORT 1 to PORT 8	MXI (x8)	MXI for USRP

Table 5. Cable Connections between the Master CDA and the CDAs in USRP Subsystems

USRP subsystem #	Port in Master CDA	Port in MIMO subsystem CDA	Cable type	Description	Number of antennas (USRP subsystems)			
					128 (8)	64 (4)	32 (2)	16 (1)
01	10 MHz OUT 1	EXT 10 MHz INPUT	RF_coax	Reference clock for subsystem #1	X	X	X	X
02	10 MHz OUT 2	EXT 10 MHz INPUT	RF_coax	Reference clock for subsystem #2	X	X	X	
03	10 MHz OUT 3	EXT 10 MHz INPUT	RF_coax	Reference clock for subsystem #3	X	X		
04	10 MHz OUT 4	EXT 10 MHz INPUT	RF_coax	Reference clock for subsystem #4	X	X		
05	10 MHz OUT 5	EXT 10 MHz INPUT	RF_coax	Reference clock for subsystem #5	X			
06	10 MHz OUT 6	EXT 10 MHz INPUT	RF_coax	Reference clock for subsystem #6	X			
07	10 MHz OUT 7	EXT 10 MHz INPUT	RF_coax	Reference clock for subsystem #7	X			
08	10 MHz OUT 8	EXT 10 MHz INPUT	RF_coax	Reference clock for subsystem #8	X			
01	PPS OUT 1	EXT PPS INPUT	RF_coax	PPS trigger for subsystem #1	X	X	X	X
02	PPS OUT 2	EXT PPS INPUT	RF_coax	PPS TRIGGER for subsystem #2	X	X	X	
03	PPS OUT 3	EXT PPS INPUT	RF_coax	PPS TRIGGER for subsystem #3	X	X		
04	PPS OUT 4	EXT PPS INPUT	RF_coax	PPS TRIGGER for subsystem #4	X	X		
05	PPS OUT 5	EXT PPS INPUT	RF_coax	PPS TRIGGER for subsystem #5	X			
06	PPS OUT 6	EXT PPS INPUT	RF_coax	PPS TRIGGER for subsystem #6	X			
07	PPS OUT 7	EXT PPS INPUT	RF_coax	PPS TRIGGER for subsystem #7	X			
08	PPS OUT 8	EXT PPS INPUT	RF_coax	PPS TRIGGER for subsystem #8	X			

Table 6. Cable Connections between the PXI and the CPS in USRP subsystems

PXIe-8384 in slot #	128 (8)	64 (4)	32 (2)	16 (1)	CPS port	Cable type	Description
	USRP subsystem #						
02	1	1	1	1	UP STREAM	MXI	MXI for subsystem #1
03	2	2			UP STREAM	MXI	MXI for subsystem #2
04	3				UP STREAM	MXI	MXI for subsystem #3
05	4				UP STREAM	MXI	MXI for subsystem #4
15	5				UP STREAM	MXI	MXI for subsystem #5
16	6				UP STREAM	MXI	MXI for subsystem #6
17	7	3			UP STREAM	MXI	MXI for subsystem #7
18	8	4	2		UP STREAM	MXI	MXI for subsystem #8

Table 7. Cable Connections between PXIe-6674T and Master CDA

Output Port on PXIe-6674T	Input Port on CDA	Cable type	Description
CLK OUT	EXT 10 MHz INPUT	RF_coax	Reference clock from PXI
PFI3	EXT PPS INPUT	RF_coax	PPS trigger from PXI

Table 8. Cable Connection between USRP Subsystem #1 and the PXIe-6674T (Master Trigger)

Port on USRP01 in subsystem #1	Port on PXIe-6674T	Cable type	Description
PPS TRIG OUT	PFI1	RF_coax	Master PPS trigger

Installing the Software

You must be an Administrator to install NI software on your computer.

1. Install LabVIEW Communication System Design Suite 2.0.
2. Install NI-USRP 15.5.
3. Install MIMO Application Framework.
4. When the installers complete the installation, select **Restart** in the dialog box.

Powering on the Hardware

Caution Ensure that all SMA connectors are properly tightened. Poor connections may result in a delay in signal propagation, resulting in poor system operation.
Caution Ensure that the **PRIMARY REF** flip switches on all CDA-2990 devices are in the EXTERNAL position.

Base Station

1. Power on all the USRP subsystems.
2. Power on the PXI controller.

Mobile Station

1. Power on the USRP RIO.
2. Power on the computer (laptop, PC, or PXI chassis) to which the USRP RIO is connected.

Connection Diagrams

Figure 9. 16-Antenna MIMO System Connection Diagram

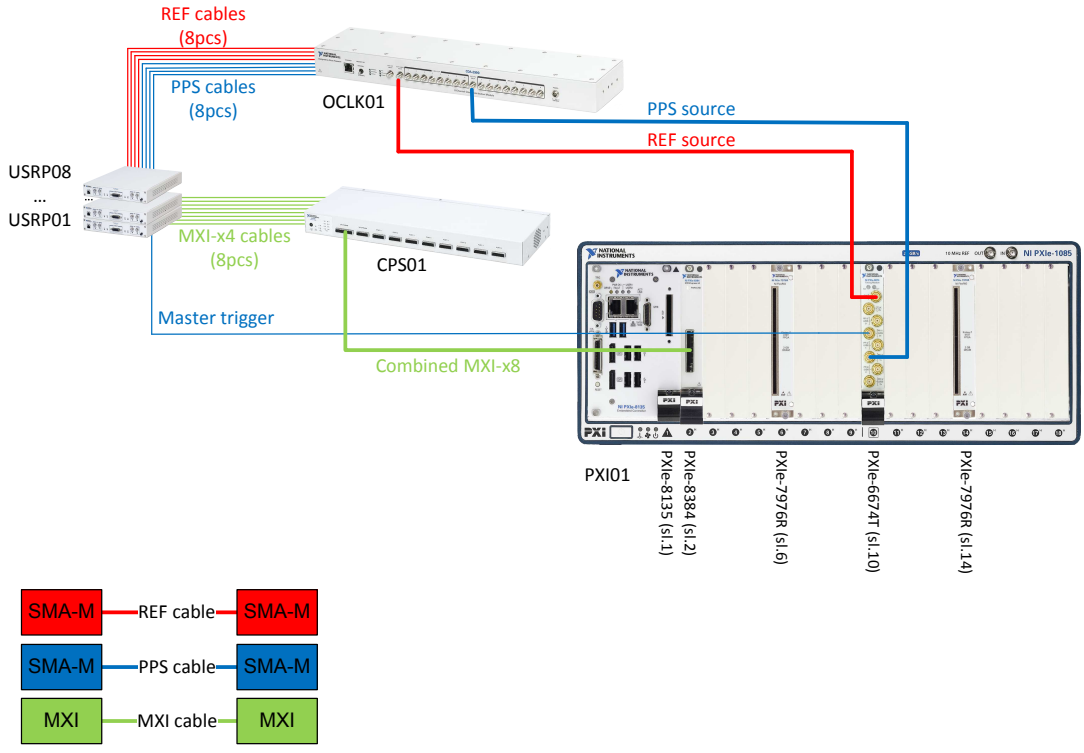


Figure 10. 32-Antenna MIMO System Connection Diagram

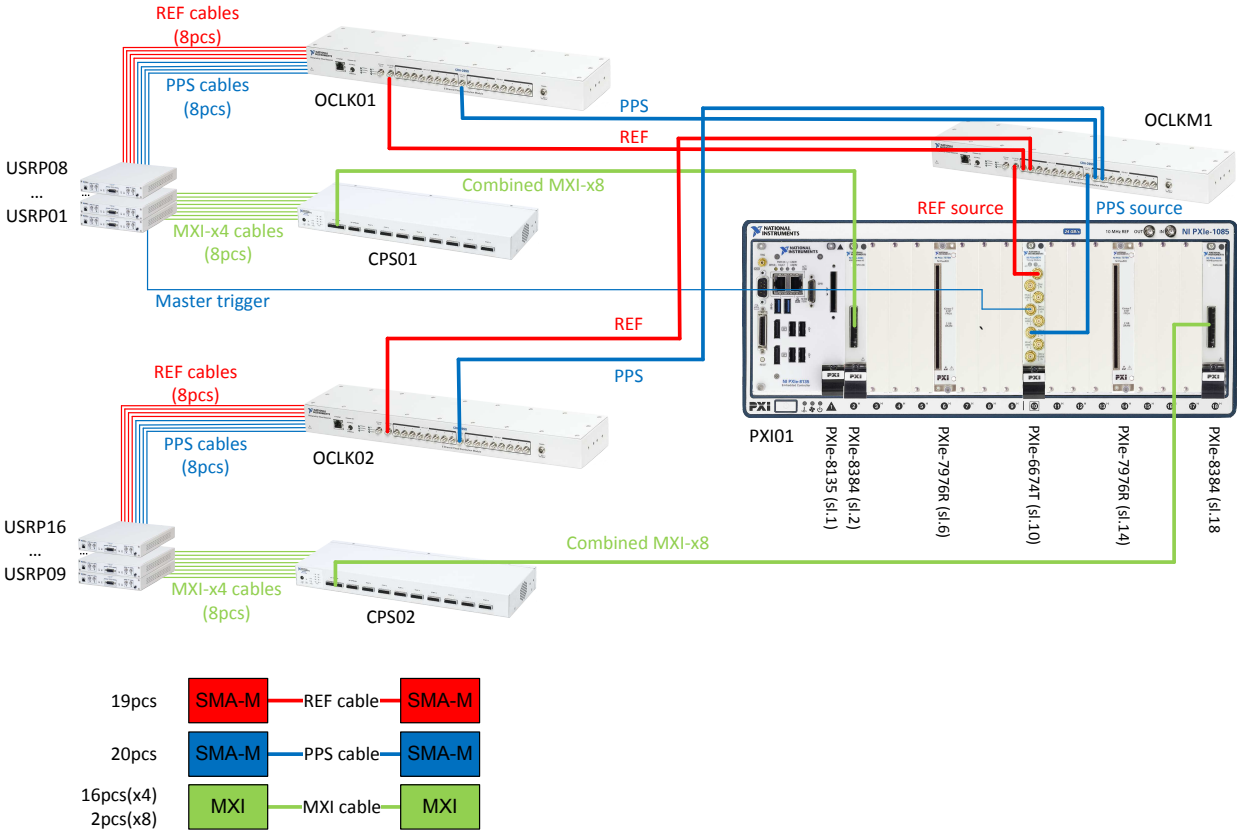


Figure 11. 64-Antenna MIMO System Connection Diagram

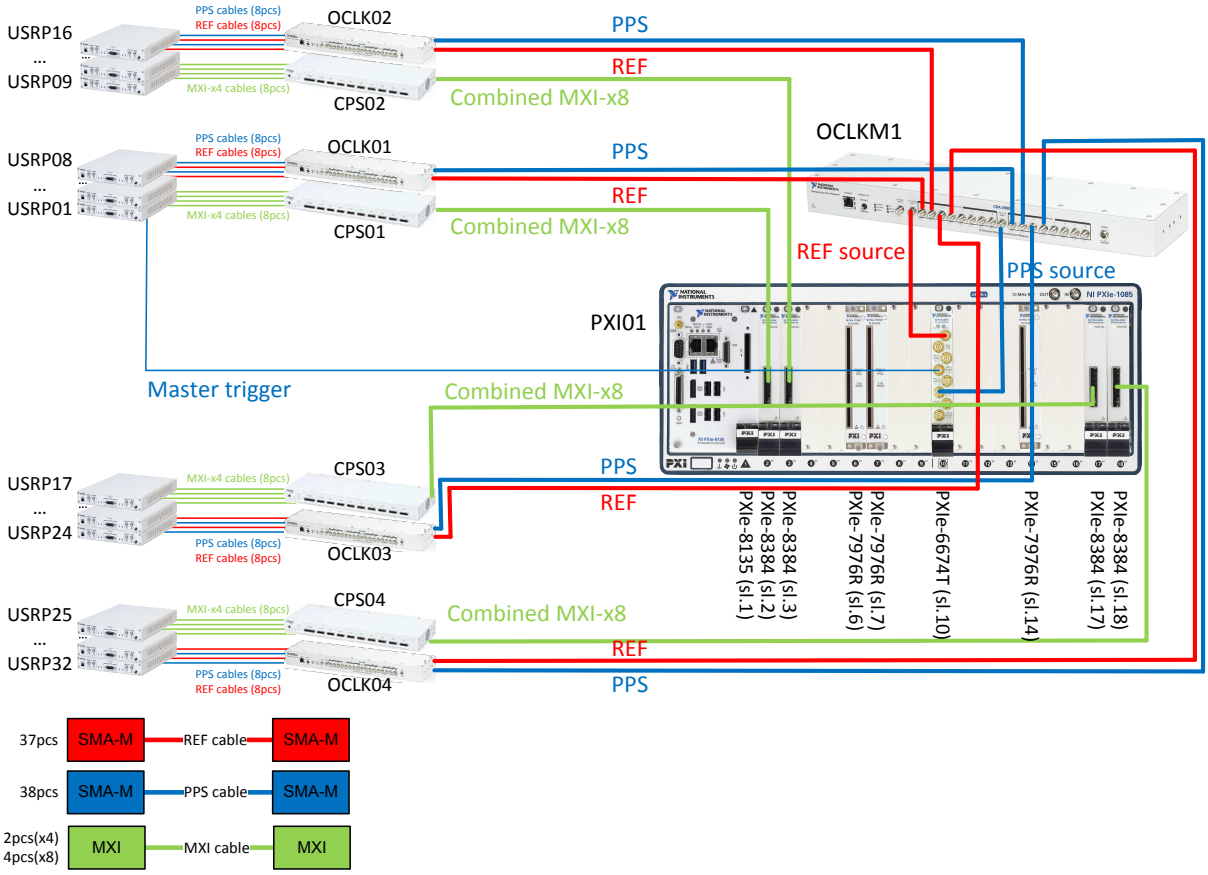
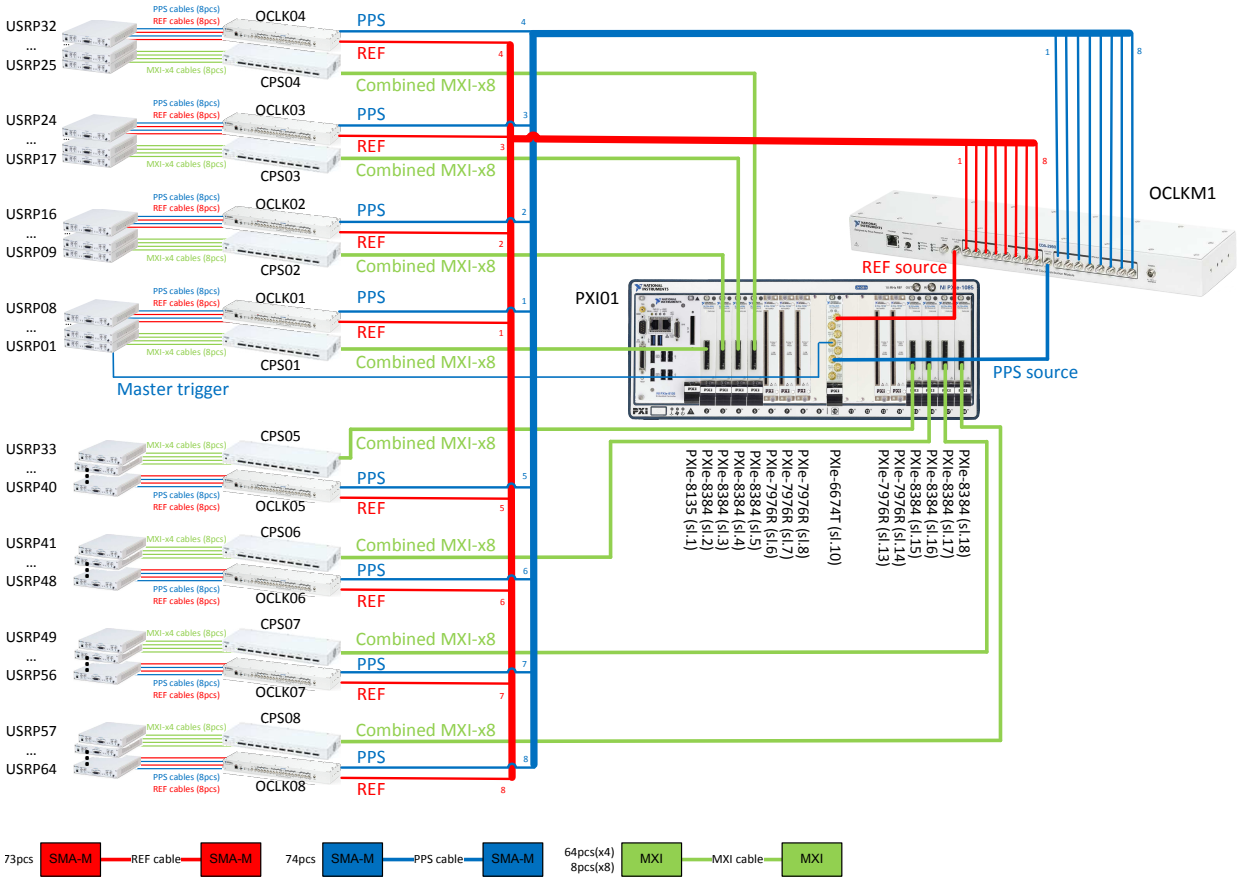


Figure 12. 128-Antenna MIMO System Connection Diagram



Software

Hardware Naming

Use MAX, or **System Diagram** in LabVIEW Communications, to change the hardware aliases. The MIMO Application Framework is designed to work with the hardware aliases in the following table.

Table 9. Hardware Aliases

Device	Configuration	Alias
PXIe-6674T	All	TIME
PXIe-7976	All	FLEX0, FLEX1,…,FLEX4
USRP RIO	CPS switch box	CPS1Port1Dev1, CPS1Port2Dev1,…,CPS1Port8Dev1, CPS2Port1Dev1, CPS2Port2Dev1,…,CPS2Port8Dev1, and so on. You can keep the default names if you set **USRP Naming Scheme** to CPS(1-8)Port(1-8)Dev1.
	PXI chassis	PXI2Slot2Port1Dev1, PXI2Slot3Port1Dev1,…, PXI2Slot18Port1Dev1, PXI3Slot2Port1Dev1,

		PXI3Slot2Port1Dev1,...,PXI3Slot18Port1Dev1. You can keep the default names if you set **USRP Naming Scheme** to PXI(2-5)Slot(2-18)Port1Dev1.
	All	Rename the USRP RIO devices to USRP01, USRP02, USRP03, and so on, and set **USRP Naming Scheme** to USRP (01-64).

Understanding the Components of this Sample Project

The development project is comprised of LabVIEW host code and LabVIEW FPGA code. The related folder structure and components of the project are described in the following subsections. The description covers the Development project, which comprises all FPGA and Host software parts. There is a Deployment project limited to the Mobile Station Host code only and does not include all contents listed below.

Create a New Project Instance

To create a new instance of the MIMO Application Framework, launch LabVIEW Communications System Design Suite 2.0 by selecting **LabVIEW Communications 2.0** from the **Start** menu. From the Project Templates on the launched **Project** tab, select **Application Frameworks » MIMO Application Framework Development v1.0** to launch the project.

Folder Structure

The following files and folders are created inside the specified folder:

MIMO Development v1.0.lvproject

This project file contains reference to all VIs and targets.

Base Station Host.gvi

This is the top-level host VI of the BS, also called the Evolved Node B (eNodeB). It implements a downlink (DL) transmitter (TX) and an uplink (UL) receiver (RX) and can communicate with up to twelve MSs.

The host interfaces with multiple FlexRIO FPGA modules which serve as processors and multiple USRP RIOs which serve as remote radio heads (RRHs). The bitfiles are built from the following corresponding FPGA top-levels:

- **Base Station MIMO Processor FPGA.gvi:** This is the MIMO Processor top-level where the largest part of the in-phase/quadrature (I/Q) baseband signal processing is executed. A MIMO Processor bitfile can be configured to work for up to 32, 64 or 128 antennas. Each bitfile handles either all, the half or a fourth of all subcarriers per OFDM symbol. Refer to the “System Overview” section for more details.
- **Base Station Bit Processor FPGA.gvi:** This is the Bit Processor top-level where the TX and RX bit processing are executed. The TX packet generator as well as the RX packet validator are executed in the bit processor.

- **Base Station RRH FPGA.gvi:** This is the RRH top-level where the OFDM modulation and demodulation as well the interfacing with the RF is performed. Refer to the “System Overview” section for more details.

Mobile Station Host.gvi

This is the top-level host VI of the MS, also called User Equipment (UE). Each host configures two MSs. The host interfaces with the bitfile built from the following corresponding FPGA top-level:

- **Mobile Station FPGA.gvi:** This is the MS top-level. It implements two MSs (“UE 0” and “UE 1”), each with a DL RX and UL TX.

Builds

This folder contains the precompiled bitfiles. The FlexRIO modules are loaded with MIMO Processor bitfiles. Which bitfile is used specifically depends on which of the following system configurations is used:

- **MIMO Processor 32 Antennas.lvbitx:** Used for BSs that are configured for up to 32 antennas.
- **MIMO Processor 64 Antennas.lvbitx:** Used for BSs that are configured for up to 64 antennas.
- **MIMO Processor 128 Antennas.lvbitx:** Used for BSs that are configured for up to 128 antennas.

For bit processing, a single FlexRIO module is loaded with Bit Processor bitfile:

- **Bit Processor.lvbitx:** Used for BS bit processing. It works with all BS configurations.

The USRP RIOs that serve as RRHs are loaded with the following bitfiles:

- **RRH Combiner.lvbitx:** Used for all RRHs in a subsystem except the last one. Applicable for USRP RIO devices with 120 or 160 MHz bandwidth.
- **RRH Splitter.lvbitx:** Used for the last RRH in a subsystem. Applicable for USRP RIO devices with 120 or 160 MHz bandwidth.
- **RRH Combiner 40 MHz.lvbitx:** Used for all RRHs in a subsystem except the last one. Applicable for USRP RIO devices with 40 MHz bandwidth.
- **RRH Splitter 40 MHz.lvbitx:** Used for the last RRH in a subsystem. Applicable for USRP RIO devices with 40 MHz bandwidth.

The USRP RIO devices that serve as MSs are loaded with the following bitfiles:

- **Mobile Station.lvbitx:** Used for USRO RIO devices with 120 MHz or 160 MHz bandwidth.
- **Mobile Station 40 MHz.lvbitx:** Used for USRO RIO devices with 40 MHz bandwidth.

Common

The common folder contains generic nodes for host and FPGA that are shared between different Application Frameworks, such as mathematical functions, type conversions, and so on.

Link Simulator

This folder contains the Link Simulator which simulates the UL and DL transmission chain on the host.

MIMO v1.0

This folder contains host and FPGA nodes, which were specifically designed for the MIMO Application Framework. It has three subfolders: **FPGA**, **Host**, and **Types**. The **Types** subfolder contains type definitions that are required in the system.

Resources

This folder contains the FPGA resources which are needed for the bitfiles to compile.

USRP RIO 120 MHz BW

This directory was taken from the NI USRP RIO Multi-Device Streaming project.

Testbenches

Host simulation test benches for all parts of the design.

System Overview

The MIMO Application framework provides the functional elements of the PHY as well as the basic MAC of both BS and MSs. It includes the following elements:

- MIMO DL data transmission and reception
- MIMO UL data transmission and reception
- Synchronization of BSs and MSs, either over a common trigger signal, or over-the-air using the primary synchronization sequence (PSS)
- Basic MAC functionality provided for packet-based user data transmission in DL and UL to enable user data streaming applications

System Features

The MIMO Application Framework is presented on a flexible platform. It supports the following features:

- Scalable number of antennas from four to 128 at the BSs. Data rates and interfaces scale automatically.
- One to 12 MSs.
- 20 MHz bandwidth with a frame structure based on long-term evolution (LTE).
- Fully reconfigurable frame schedule.
- Multi-user MIMO precoding and equalization on FPGA including 128×12 minimum mean squared error (MMSE), zero-forcing (ZF), and maximum-ratio combining (MRC).
- Bidirectional Time Division Duplex (TDD) with fully reconfigurable UL and DL.
- Channel reciprocity calibration per RF channel.
- Aggregates all data to the processing units.
- Time and frequency synchronization over-the-air, all using commercial off-the-shelf components.
- Support for different modulation schemes for modulating the data subcarriers: quadrature phase shift keying (QPSK), 16-quadrature amplitude modulation (QAM), 64-QAM, and 256-QAM.

Visit ni.com/info and enter the Info Code exrukz to access the *MIMO Application Framework White Paper* for more information about the MIMO Application Framework design.

System Components

Base Station

The following figure shows the block diagram of the BS in the UL and DL. The components perform the following tasks:

Host: Configures the system and displays the system status. Interfaces with multiple processor bitfiles loaded to the FlexRIO modules and multiple RRH bitfiles loaded to the USRP RIO devices. It also receives and transmits payload data using the user datagram protocol (UDP).

- **Data Source:** Data source for the DL payload data. If configured as "UDP," data is read from the configured UDP ports.
- **Data Sink:** Data sink for the received UL payload data. If configured as "Off," the received data is discarded. If configured as "UDP," the received data is sent as UDP packets to the configured remote address and ports.

Bit Processor: The central processing unit for TX and RX bit Processing. The main components of this module are:

- **TX Packet Generator:** Generates the packets based on the MAC packet structure.
- **RX Packet Validator:** Performs frame validation by means of frame check sequence (FCS), which contains an IEEE 32-bit cyclic redundancy code (CRC).
- **TX Bit Processing:** It is responsible for TX bit processing including data scrambling, TX bit grouping, modulation and data reordering.
- **RX Bit Processing:** It is responsible for RX bit processing including data reordering, demapping, packing, and descrambling.
- **Router 0 & 1:** Used for dynamically routing data. Every router has its own routing program which is written from the host depending on the given system configuration. **Router 0** is used to route the receive data from MIMO processors to the RX bit processing chain. **Router 1** is used to route the transmit data from the TX bit processing chain to the MIMO processors.

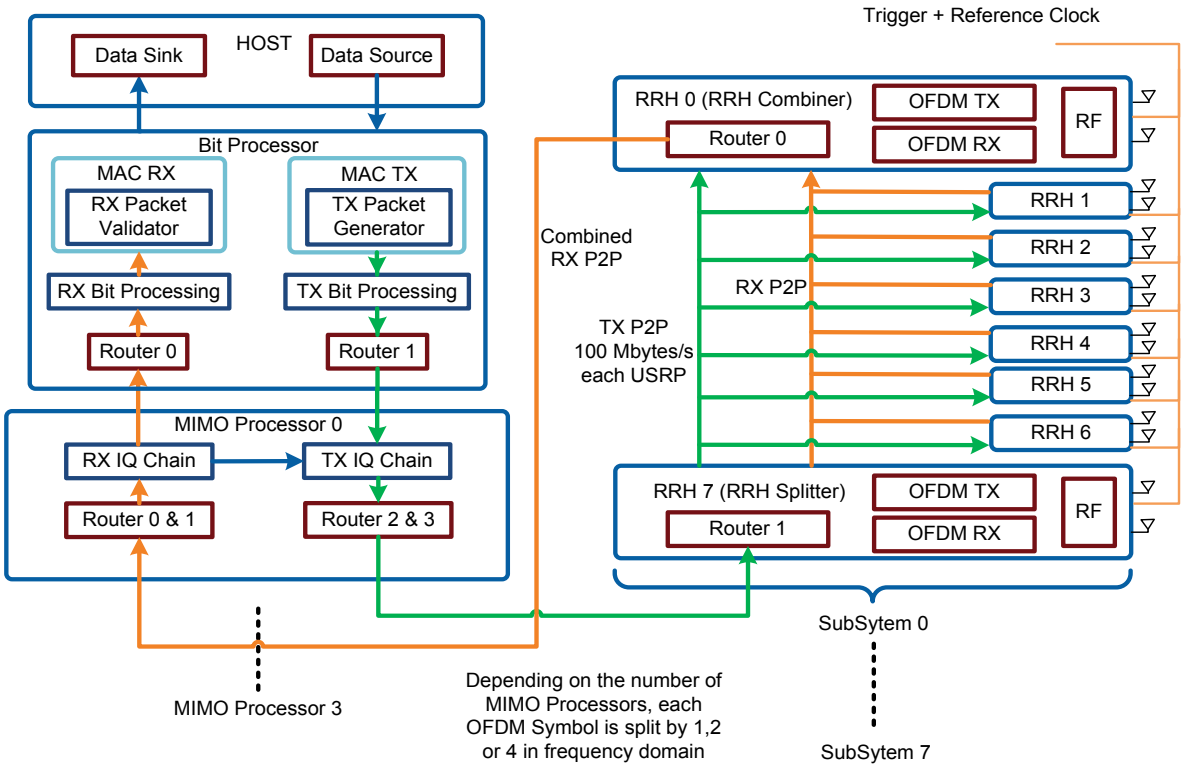
MIMO Processors: The central processing units for TX and RX I/Q Processing. Depending on the system configuration, a MIMO processor process all, one half or one fourth of the subcarriers per orthogonal frequency division multiplexing (OFDM) symbol.

- **TX I/Q Chain:** Includes modules such as Precoding, Stream Combiner, and so on.
- **Routers:** Used for dynamically routing data. Every router has its own routing program which is written from the host depending on the given system configuration.
    - **Router 0 & 1:** Used to route receive data from RRH subsystems to the MIMO processor.
    - **Router 2 & 3:** Used to route transmit data from the MIMO processor to the RRH subsystems.
- **RX I/Q Chain**: Estimates the channel towards the MS from the received data and equalizes the received signals.

RRH Subsystem: The RRHs contain the analog-to-digital converters (ADC) and digital-to-analog converters (DAC). They handle the transformation from time domain to frequency domain and vice versa. Multiple RRHs (two to eight) build a subsystem. A base station can consist of one to eight subsystems.

- **RRH Splitter (last RRH in subsystem):** Receives the transmit data from the MIMO processors, distributes it to the TX chains of all other RRHs in the subsystem, one after the other, and finally to its own TX chain.
- **RRH Combiner (remaining RRHs):** Accumulates the received data from its own RX chain, followed by the RX chains of all other RRHs in a subsystem, one after the other, and sends it to the MIMO processors.
- **OFDM TX** and **OFDM RX:** Each RRH contains OFDM modulation and OFDM demodulation.
- **RF:** In the transmit path, it performs DUC, RF impairments correction, and writes the transmit data to the RF. In the receive path, it reads the receive data from the RF, performs DDC and performs RF impairments correction.

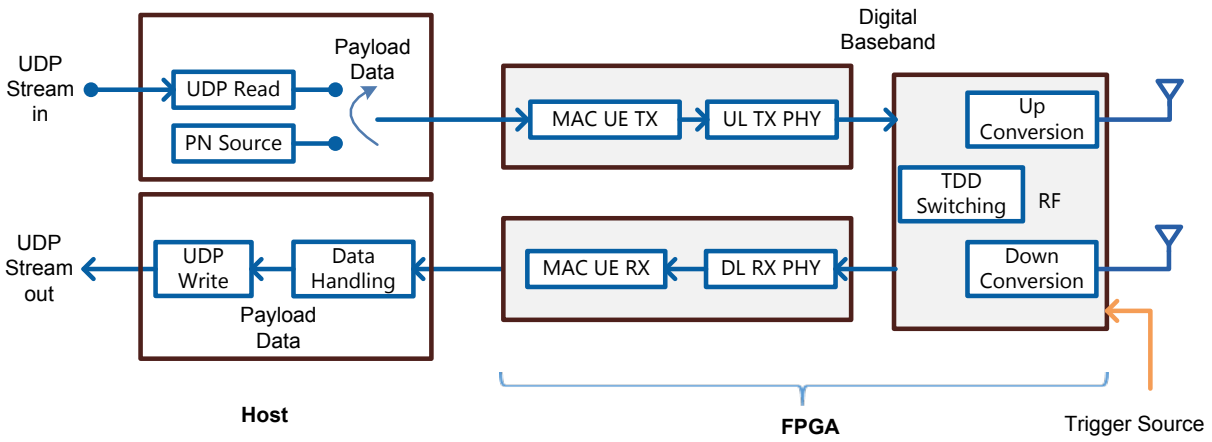
Figure 13. Block Diagram of the BS (TX and RX Chain)



Mobile Station

The following figure shows the block diagram of the MS system in the UL and DL.

Figure 14. Block Diagram of the MS (TX and RX Chains)



The components shown in Figure 14 perform the following tasks:

- **Host:** Configures the FPGA and displays the system status. Interfaces with the MS bitfile.
  - **UDP read:** Reads data, provided by an external application, from a UDP socket. The data is used as a payload data in the UL Data field of each slot, which is then encoded and modulated as an UL signal by the UL TX (UL TX PHY).
  - **PN Source:** Generates a pseudo noise (PN) sequence, a sequence of pseudorandom numbers.
  - **UDP write:** Writes the payload data that was received and decoded from the DL signal by the DL RX (DL RX PHY) to an UDP socket. The data can then be read by an external application.
  - **Data Handling:** Reads received data from FPGA, checks packets validation, and stores received payload to queues.
- **FPGA:** Contains the MAC and PHY modules for the UL and the DL.
  - **MAC TX:** A simple MAC implementation which adds a header containing the number of payload bytes. The header is followed by the payload in bytes and the remaining bytes are filled with padding bytes. The 32-bit CRC is then added.
  - **MAC RX:** Packets validator and payload extraction.
  - **UL TX PHY:** The physical layer of the UL TX creates the UL signal based on the configured frame structure as digital baseband I/Q data. This includes resource mapping, pilot generation, and OFDM modulation.
  - **DL RX PHY:** The physical layer of the DL RX demodulates the downlink signal. This includes PSS-based synchronization, OFDM demodulation, channel estimation and equalization.
  - **Up Conversion:** Performs digital up conversion (from the LTE sampling rate of 30.72 MS/s to 120 MS/s or 200 MS/s, depending on the USRP RIO model), performs RF impairments correction, and writes the resulting TX samples to the RF interface.
  - **Down Conversion:** Reads RX samples from the RF interface, performs digital down conversion (from 120 MS/s or 200 MS/s, depending on the USRP RIO model, to the LTE sampling rate of 30.72 MS/s), and performs RF impairments correction.

- **Trigger Source:** The MS can be synchronized to the BS using the PSS over-the-air or by using an external trigger signal which is provided from the BS.
- **TDD Switching:** The TDD Switching module is responsible for TX and RX activation based on the frame schedule.

Running the LabVIEW Host Code

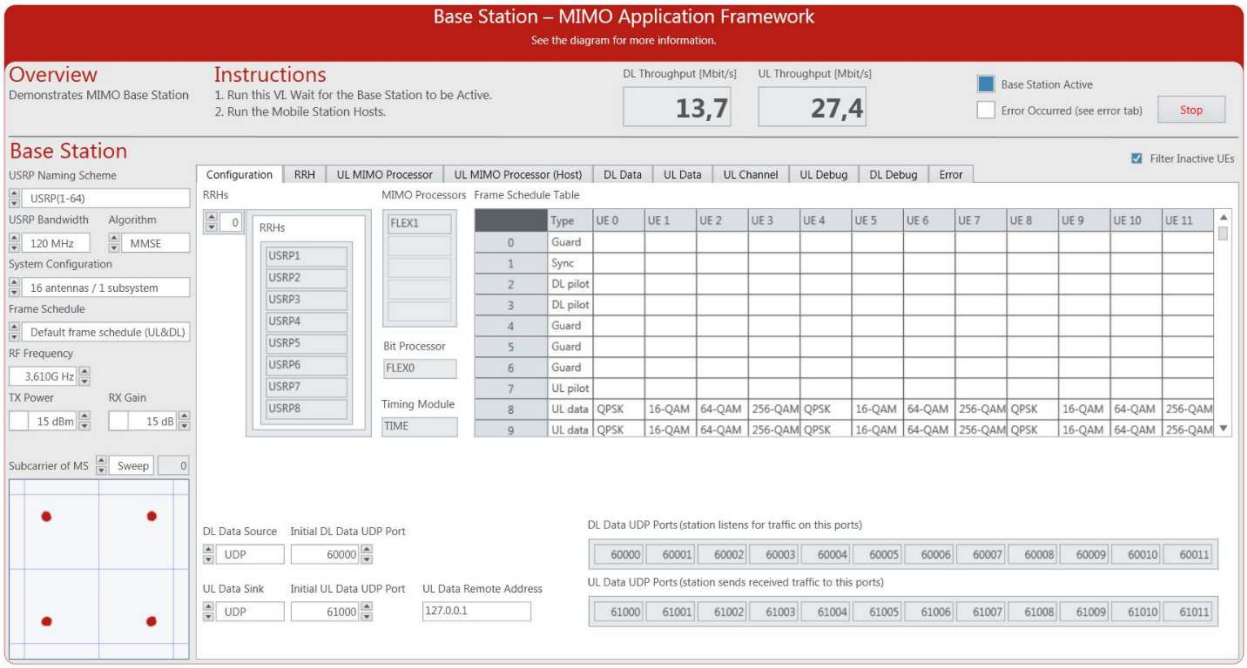
Caution Ensure you meet the hardware and software requirements before trying to run the host code.

On the BS Host Computer

1. Launch LabVIEW Communications System Design Suite 2.0 by selecting **LabVIEW Communications 2.0** from the Start menu.
2. From the Project Templates on the launched **Project** tab, select **Application Frameworks,** then select **MIMO Development** to launch the project.
3. Within that project, open **Base Station Host.gvi.** The front panel of this VI is shown in Figure 15.
4. Set the following configurations in **Base Station Host.gvi**:
   a. Set the **USRP Naming Scheme** depending on the hardware aliases that you configured using MAX (see Table 9 for details)
   b. Set the **USRP Bandwidth Model** depending on the hardware model of your USRP RIO devices.
   c. Set the **System Configuration** control to the required configuration
   d. Set the **RF Frequency** to a frequency supported by your USRP RIO devices.[8]
   e. Set the **TX power** in dBm and **RX gain** in dB or keep the default values.
5. Run the **Base Station Host.gvi** by clicking the run button ( ).
   - If successful, the **Base Station Active** indicator lights.
   - If an **error** is indicated, go to the **Error** tab to check the error message. Here you will also see if an error occurred during the initialization of the timing module, the MIMO Processors, the Bit processor or the RRHs. The **first failing element** tells which module could not be initialized correctly. Use MAX to check if the failing module is configured with the correct hardware alias.

[8] Consider local laws if you are transmitting over-the-air. The USRP-29xx is not approved or licensed for transmission over-the-air using an antenna.

Figure 15. Front panel of BS (Configuration Tab)



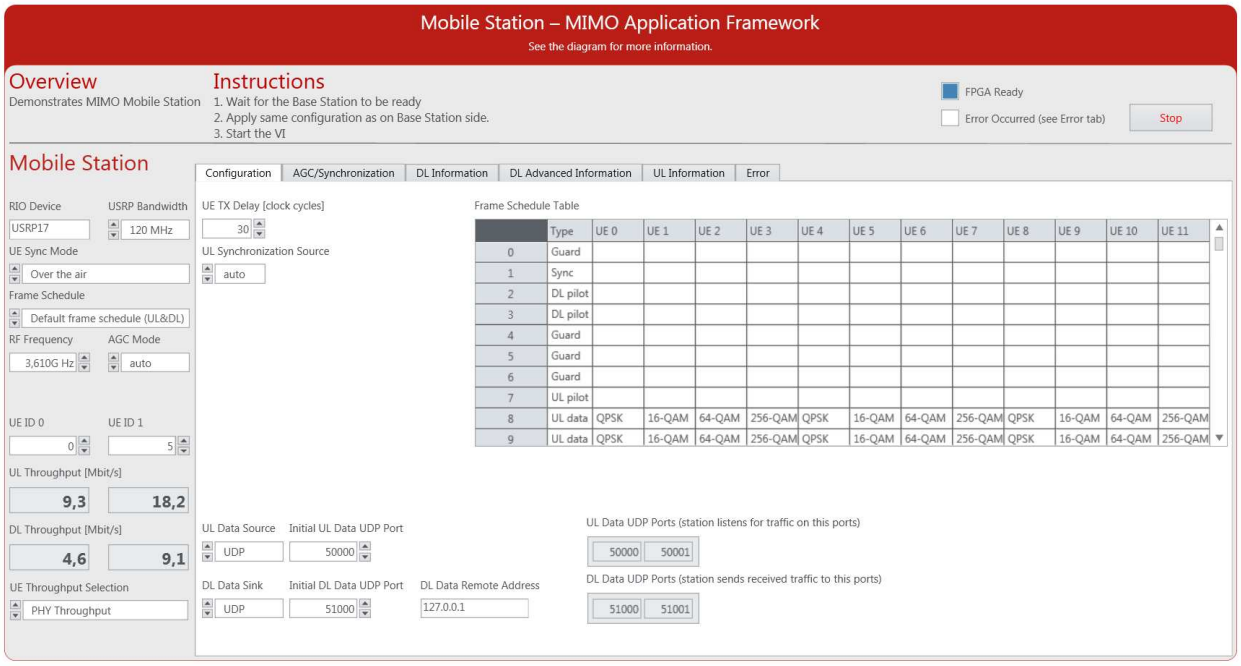
On the MS Host Computer

1. Launch LabVIEW Communications System Design Suite 2.0 by selecting **LabVIEW Communications 2.0** from the Start menu.
2. From the Project Templates on the launched **Project** tab, select **Application Frameworks,** then select **MIMO Development** to launch the project.
3. Within that project, open **Mobile Station Host.gvi.** The front panel of this VI is shown in **Figure 16**.
4. Set the following configurations in **Mobile Station Host.gvi**:
   a. Configure the RIO identifier in the **RIO Device** control. Use MAX to configure the hardware alias of the USRP RIO that you want to use as MS.
   b. Set the **USRP Bandwidth Model** depending on the hardware model of your USRP RIO devices.
   c. Select the **UE Synchronization Mode** using the **UE Sync Mode** control (over-the-air or using external trigger).
   d. Set the **RF Frequency** according to the base station.[9]
   e. Set the automatic gain control (AGC) mode to auto or manual. If the AGC is configured to manual, set the **TX power** in dBm and **RX gain** in dB that are available in the **AGC Settings and Status** tab.
   f. Set the MS ID of both MSs (**UE ID 0** and **UE ID 1**). Each MS ID has its modulation scheme as shown in Figure 15.
5. Run **Mobile Station Host.gvi** by clicking the run button ( ).
   - If successful, the **FPGA Ready** indicator lights.

[9] Consider local laws if you are transmitting over-the-air. The USRP-29xx is not approved or licensed for transmission over-the-air using an antenna.

- If an error is indicated, go to the **Error** tab to check the error message. Use MAX to check if the USRP RIO is configured with the correct hardware alias.

Figure 16. Front Panel of MS (Configuration Tab)



For initial verification that the system is running:

1. Select the **Frame Schedule Table** in the **Configuration** tab on the **Base Station Host.gvi** to find the modulation scheme of the selected MSs.
2. For UL investigation, select the **UL MIMO Processor** tab on the **Base Station Host.gvi,** and verify that the presented RX constellations match the corresponding modulation schemes according to the **Frame Schedule Table**. When using the default frame schedule UE 0 should have QPSK modulation and UE 1 should have 16 QAM modulation. Furthermore, select the **UL Data** tab and verify the UL throughput.
3. For DL investigation, select the **DL Advanced Information** tab on the **Mobile Station Host.gvi,** and verify that the presented RX constellations match the corresponding modulation schemes according to the **Frame Schedule Table**. Furthermore, select the **DL Information** tab and verify the DL throughput.

If you want to transmit and receive with more than two MSs (one MS host), you have two options:

1. Use different host computers. For example, use one laptop with one USRP RIO connected to it per MS Host.
2. Use the same host computer (for example, a PXI chassis) with multiple USRP RIOs connected to it. For running multiple MS Hosts, you have to duplicate **Mobile Station Host.gvi**.

When using multiple MS hosts, the above configurations should be repeated for each MS host. Please make sure to select the correct **RIO Device** each time and to choose unique **UE IDs**. When using the same UE ID twice the BS will not be able to decode the UL because it receives a mixed signal with the same UL pilots and the same UL data scrambling sequence.

Running Video Streaming

The MIMO Application Framework implements a basic MAC functionality which allows for packet-based data exchange of user-defined payload data. Figure 17 shows an example where user-defined data is transferred in the uplink. The user-data is received at the MS from a data source in form of UDP packets and send out at the BS to a data sink also in form of UDP packets. Any program capable of transmitting UDP data can serve as a data source. Similarly, any program capable of receiving UDP data can serve as a data sink.

If you use a video streaming application as a data source and a video player as a data sink, the MIMO Application Framework can be used for video streaming. The following section describes video streaming using the VLC media player that is available at www.videolan.org.

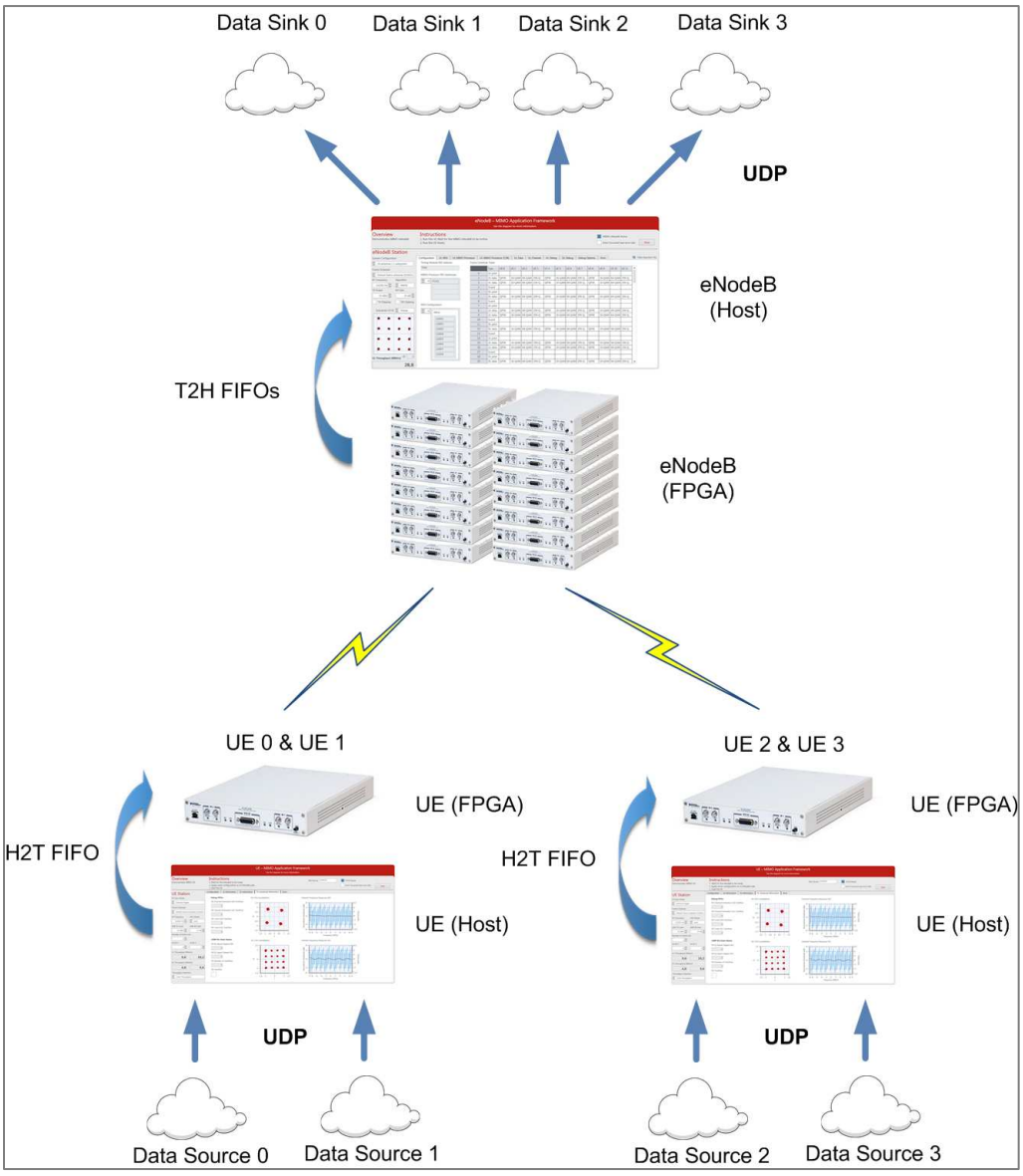
Start Video Stream at the Transmitter (MS)

The MS host acting as an UL transmitter receives UDP packets from the video streaming application and utilizes the MIMO Application Framework to transmit the data frames.

1. Create a new project as described in **Running the LabVIEW Host Code**.
2. Open the top-level host VI of the MS, **Mobile Station Host.gvi**, set the correct RIO identifier in the **RIO device** parameter, and then set **UL Data Source** on the **Configuration** tab to **UDP**
3. Run the LabVIEW host VI by clicking the run button ( ).
4. Start `cmd.exe` and change the directory to the VLC installation directory.
5. Start the VLC application as a streaming client with the following command:
   `vlc.exe --repeat "`*`PATH_TO_VIDEO_FILE`*`"`
   `:sout=#std{access=udp{ttl=1},mux=ts,dst=@:`*`UDP_PORT_TX`*`}`
   where *`PATH_TO_VIDEO_FILE`* should be replaced with the location of the video that should be used. The value of *`UDP_PORT_TX`* is 50.000, which is the default UDP Receive Port for MS ID 0. The default UDP receive port can be changed using the **Initial UL Data UDP Port** control on the **Configuration** tab.

   When using multiple MSs, the value of *`UDP_PORT_TX`* has to be adapted. Each MS Host opens two UDP ports for the two RF chains. See **UL UDP Data Ports** indicator for the used ports.

Figure 17. Data Streaming from MSs to the BS Using UDP



Start Video Stream of the Receiver (BS)

The BS host acting as a receiver utilizes the MIMO Application Framework to validate the received data frames and pass them via UDP to the video player.

1. Create a new project as described in **Running the LabVIEW Host Code section**.
2. Open the top-level host VI of the BS, **Base Station Host.gvi**, and then switch to **Configuration** tab and set **UL Data Sink** to **UDP.**
3. Run the LabVIEW host VI by clicking the run button ( ).

4. Start cmd.exe and change the directory to the VLC installation directory.
5. Start the VLC application as a streaming client with the following command: `vlc.exe udp://@:`*`UDP_PORT_RX`*

The value of *UDP_PORT_RX* is 61.000, which is the default UDP Transmit Port. The default value of *UDP_PORT_RX* can be changed using the **Initial UL Data UDP Port** control on **Configuration** tab. The UDP_PORT_RX values must be derived as **Initial UL Data UDP Port + UE-ID.**

Description of Controls and Indicators

Description of Controls and Indicators on the BS Host Front Panel

This section describes all controls, graphs and indicators which are placed on the BS Host front panel.

BS Basic Controls and Indicators

Several controls and indicators are placed outside the main tab control of **Base Station Host.gvi** as shown in Figure 15. The following table lists the corresponding controls. Table 11 lists the corresponding indicators.

Table 10. BS Basic Configuration - Controls

Control	Description
USRP Naming Scheme	Determines the naming scheme of the USRP RIO devices which are loaded with the RRH bitfiles. The enumeration contains the following values: • CPS(1-8)Port(1-8)Dev1 • PXI(2-5)Slot(2-18)Port1Dev1 • USRP(01-64)
USRP Bandwidth	Determines the bandwidth of the used USRP RIO devices. The enumeration contains the following values: • 120 or 160 MHz • 40 MHz
Algorithm	Configures the algorithm that is used for precoding. The enumeration contains the following values: • MMSE • MRC • ZF
System Configuration	Determines the system configuration. The number of antennas and subsystems is based on this configuration.
Frame Schedule	Determines the frame schedule to use.

RF Frequency	The center frequency for radio transmission and reception.[10]
TX Power	Sets the BS RF transmit power in dBm.
RX Gain	Sets the BS RF receive gain in dB.
Subcarrier of MS	Selects the MS ID for the constellation plot below. Set to "sweep" to sweep through the MSs over time. If the **Filter Inactive UEs** control is active, the sweeping will include only the active MSs.
Filter Inactive UEs	Filters inactive MSs in several graphs, for example in the constellation plots.

Table 11. BS Basic Configurations - Indicators and Graphs

Indicator	Description
TX Clipping	Indicates a numeric overflow at the output of DAC. It is located beside **TX Power** control
RX Clipping	Indicates a numeric overflow at the output of ADC. It is located beside **RX Gain** control.
Equalized Subcarriers	Shows the constellations of the selected MS using **Subcarrier of MS** control or of all MSs in sweep.
UL Throughput [MBit/s]	Numerical display showing the total UL throughput in Mbit/s
DL Throughput [MBit/s]	Numerical display showing the total DL throughput in Mbit/s
Base Station Active	A Boolean indicator that indicates the BS is ready.
Error Occurred (see error tab)	A Boolean indicator that lights up if an error occurred.

BS Indicators on Configuration Tab

The following two tables list the controls and indicators, respectively, which are placed on the Configuration tab of **Base Station Host.gvi** as shown in Figure 16.

Table 12. BS Host - Controls on Configuration Tab

Control	Description
DL Data Source	It has three options: • **Off:** Data source is inactive. • **UDP:** To read data from an UDP socket • **PN Data:** Generate data from a PN Source.
UL Data Sink	If it is set to UDP, received frames are forwarded to the configured UDP address and port.

[10] Consider local laws if you are transmitting over-the-air. The USRP-29xx is not approved or licensed for transmission over-the-air using an antenna.

Initial DL Data UDP Port	An offset to start opening UDP ports for UDP packet reception. The default UDP Transmit Port is 60.000. For each extra MS, the corresponding UDP port value is 60.000 plus the MS identity.
Initial UL Data UDP Port	An offset to start opening UDP ports for UDP packet transmission. The default UDP Receiver Port is 61.000. For each extra MS, the corresponding UDP port value is 61.000 plus the MS identity.
UL Data Remote Address	The IP address that the UDP packets received from MS are sent to.

Table 13. BS Host - Indicators on Configuration Tab

Indicator	Description
RRHs	Shows the RIO aliases of active USRP RIO devices per subsystem.
MIMO Processors	Shows the addresses of active FlexRIO modules for I/Q Processing.
Bit Processor	Shows the address of active FlexRIO module for bit processing.
Timing Module	Shows the address of Timing Module RIO card.
Frame Schedule Table	Shows the OFDM Frame Schedule of all 12 MSs. The OFDM symbol types of each MS frame (140 OFDM Symbols) are presented. The OFDM symbol type could be Guard, Sync, DL pilot, DL data, UL pilot, and UL data. In addition, the modulation schemes of all MSs are presented, which could be QPSK, 16-QAM, 64-QAM, and 256-QAM. The **Frame Schedule Table** indicator is controlled by **Frame Schedule** control.
DL Data UDP Ports	Shows the UDP ports to forward traffic to the MSs.
UL Data UDP Ports	Shows the UDP ports to forward traffic from the MSs.

BS Control and Indicators on RRH Tab

The following table lists the control which is placed on the **RRH** tab of **Base Station Host.gvi** as shown in Figure 19. Table 15 lists the corresponding indicators.

Table 14. BS Host - Control on RRH Tab

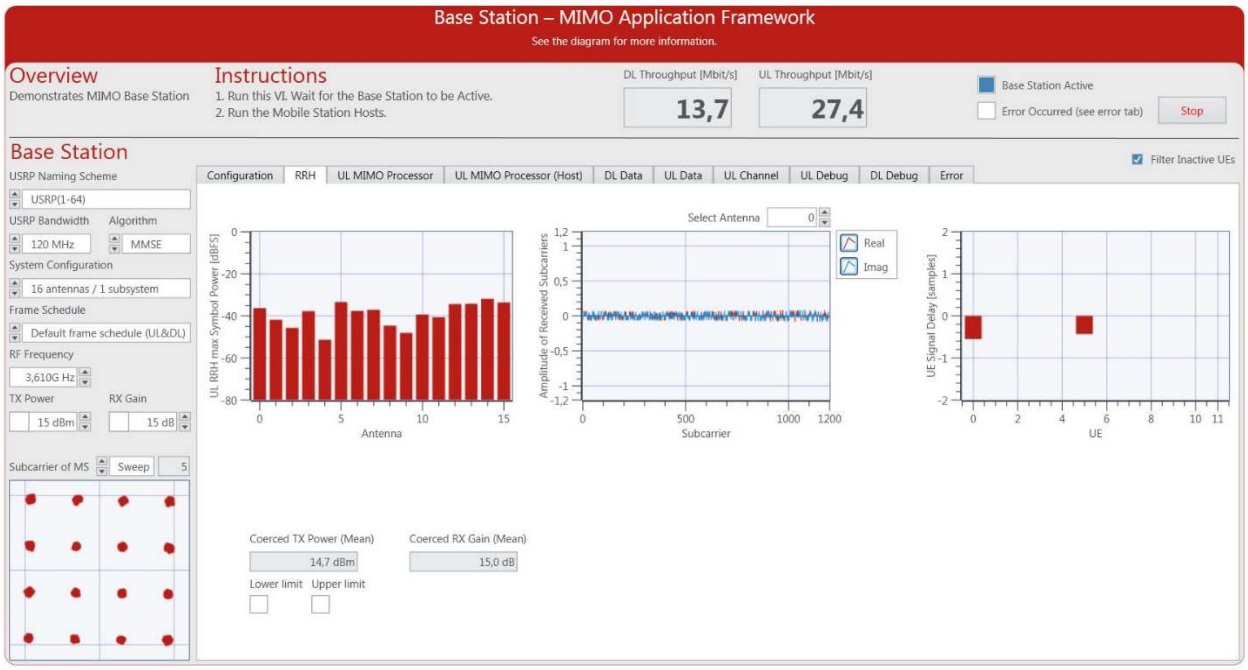
Control	Description
Select Antenna	Determines the antenna for which the received subcarriers are shown on this tab.

Table 15. BS Host – Graphs and Indicators on RRH Tab

Indicator	Description
Coerced TX Power (Mean)	Numerical indication shows the actual used analog TX RF power of all antennas as the mean value, which is set by **TX Power** control in [dBm]**.**
Lower limit	Boolean indicator shows if the configured **TX Power** value is coerced to the allowed range.

Upper limit	Boolean indicator shows if the configured **TX Power** value is coerced to the allowed range.
Coerced RX Gain (Mean)	Numerical indication shows the actual used analog RX RF gain of all antennas as the mean value, which is set by **RX Gain** control in [dB]**.** The gain value is coerced by the capabilities of the device.
UL RRH max Symbol Power [dBFS]	Graphical indication shows the maximum signal strength of a radio frame (calculated on OFDM symbol basis) over all antennas.
Amplitude of Received Subcarriers	Graphical indication shows the received subcarriers of the selected antenna. The antenna can be selected using **Select Antenna** control that is located on the above side of the figure.
UE Signal Delay [Samples]	Graphical indication shows the estimated time delay of all MSs in LTE samples. This graphical representation can be used to calibrate the time delay of each MS manually by using the **UE TX Delay** control on the **Configuration** tab of MS host top-level.

Figure 18. Front Panel of BS (RRH Tab)



BS Controls and Indicators on UL MIMO Processor Tab

The following table lists the controls that are placed on the **UL MIMO Processor** tab of **Base Station Host.gvi** as shown in Figure 20. Table 17 lists the corresponding indicators.

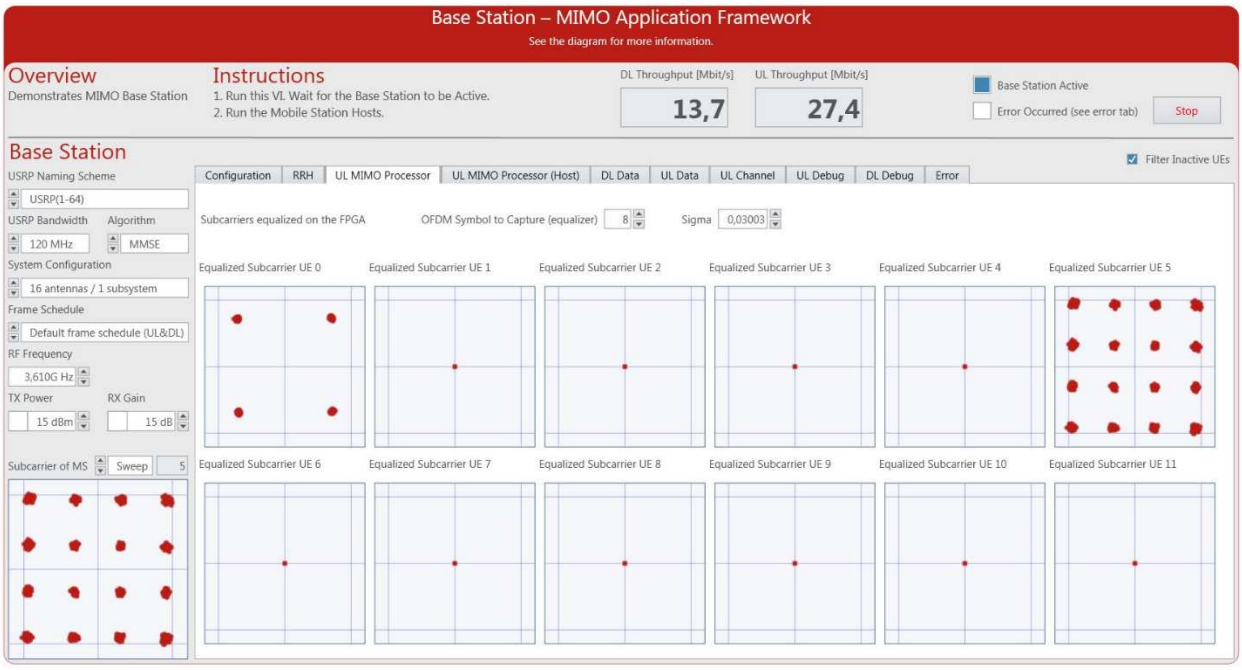
Table 16. BS Host - Controls on UL MIMO Processor Tab

Control	Description
OFDM Symbol to Capture (equalizer)	This control is used to show the constellation of RX I/Q samples of the selected OFDM symbol number after equalization. The same OFDM symbol number is selected for all MSs.
Sigma	Selects the scaling factor that is used in the modified Gram-Schmidt QR decomposition (MGS-QRD) algorithm of the MMSE channel estimator.

Table 17. BS Host - Indicators on UL MIMO Processor Tab

Indicator	Description
Equalized Subcarrier UE 0 to **Equalized Subcarrier UE 11**	Those 12 graphical representations show the constellation of RX I/Q samples of all MSs. If the number of active MSs is less than 12, it is recommended to filter the inactive MSs using the **Filter Inactive UEs** control located on the right side under the **Stop** button.

Figure 19. Front Panel of BS (UL MIMO Processor Tab)



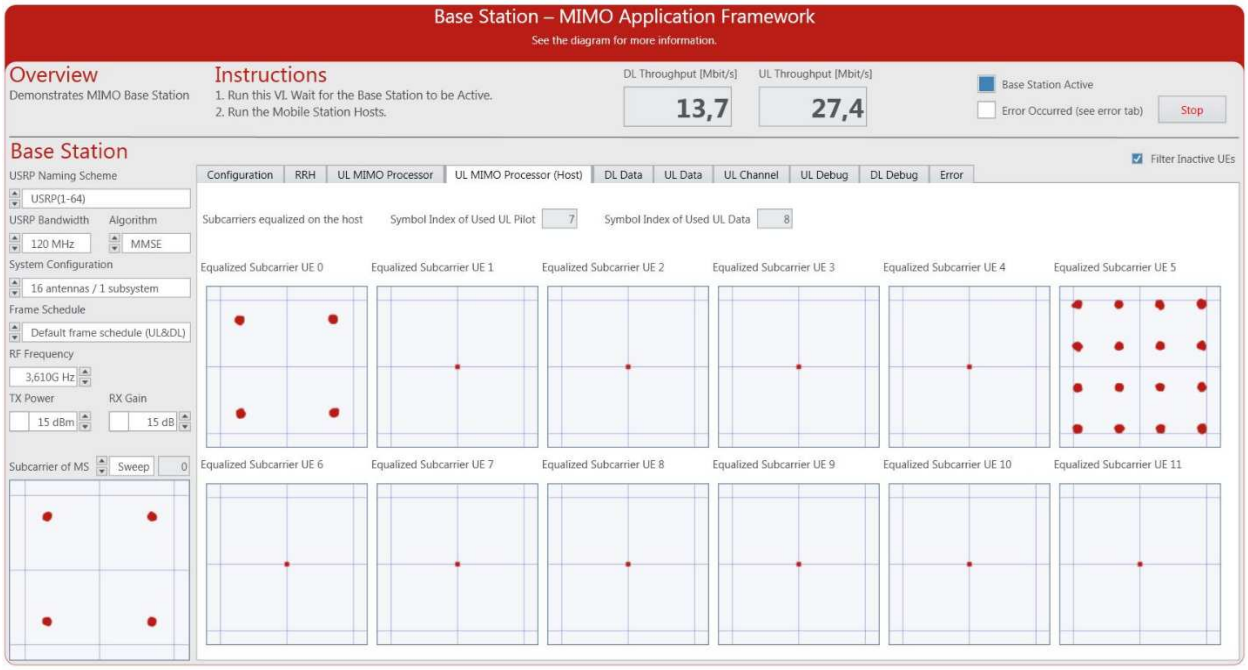
BS Indicators on UL MIMO Processor (Host) Tab

This tab contains the same graphical indicators as on the previous tab as shown on **Figure** 20. However, the channel estimation and equalization is performed on the host and not on the FPGA. The following table shows the corresponding numerical indicators.

Table 18. BS Host - Indicators on UL MIMO Processor (Host) Tab

Indicator	Description
Symbol index of Used UL Pilot	OFDM symbol index of the UL pilot to derive the channel estimation from.
Symbol index of Used UL Data	OFDM symbol index of the UL data to apply the channel equalization and display the constellations.

Figure 20. Front Panel of BS (UL MIMO Processor Tab (Host))



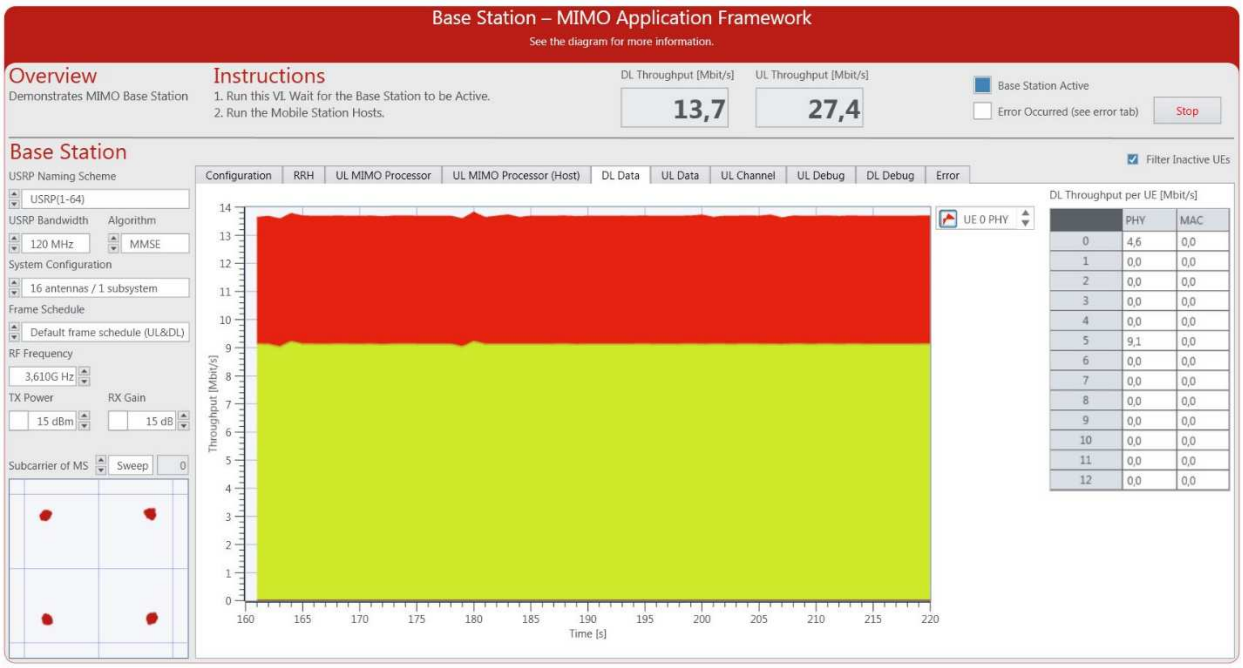
BS Indicators on DL Data Tab

The following table lists the indicators which are placed on the **DL Data** tab of **Base Station Host.gvi** as shown in Figure 21.

Table 19. BS Host - Indicators on DL Data Tab

Indicator	Description
Throughput Graph	Graphical indication showing the DL throughput of all MSs in Mbit per second with respect to time.
Throughput Table	Numerical indication of the DL throughput of all MSs in Mbit per second.

Figure 21. Front Panel of BS (DL Data Tab)



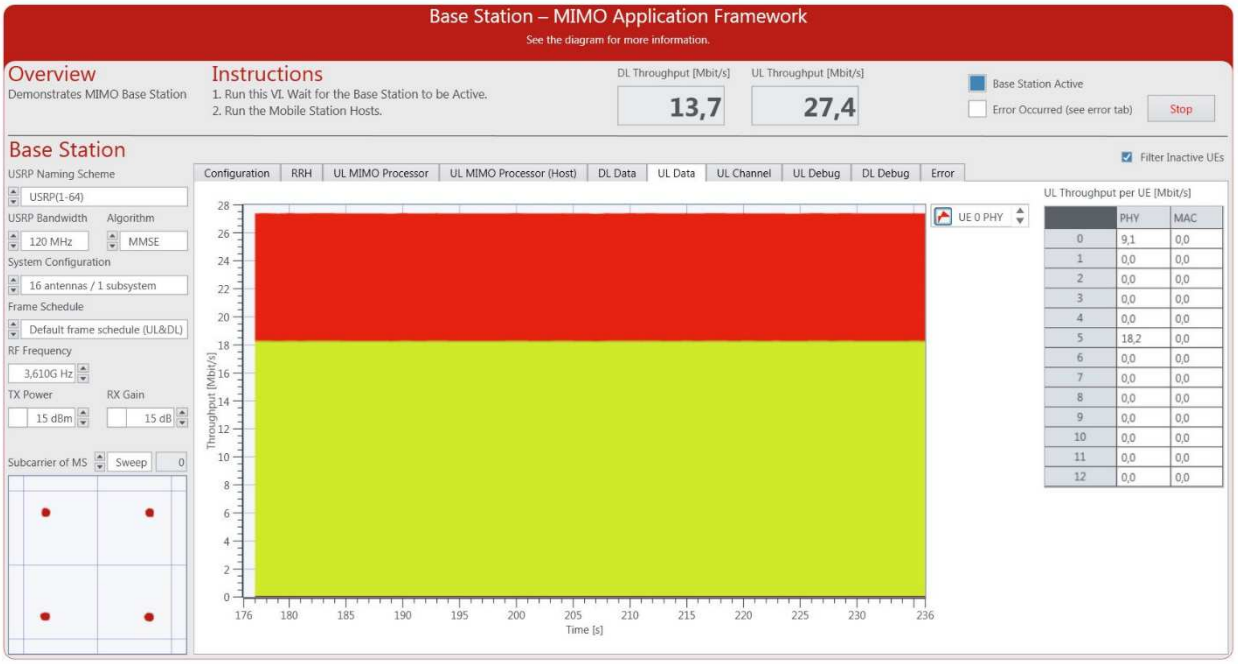
BS Indicators on UL Data Tab

The following table lists the indicators which are placed on the **UL Data** tab of **Base Station Host.gvi** as shown in Figure 22.

Table 20. BS Host - Indicators on UL Data Tab

Indicator	Description
Throughput Graph	Graphical indication showing the actual throughput of all MSs in Mbit per second.
Throughput Table	Numerical indication of the throughput of all MSs in Mbit per second.

Figure 22. Front Panel of BS (UL Data Tab)



BS Indicators and Controls on UL Channel Tab

Table 21 lists the control which is placed on the **UL Channel** tab of **Base Station Host.gvi** as shown in Figure 23. Table 22 lists the corresponding indicators.

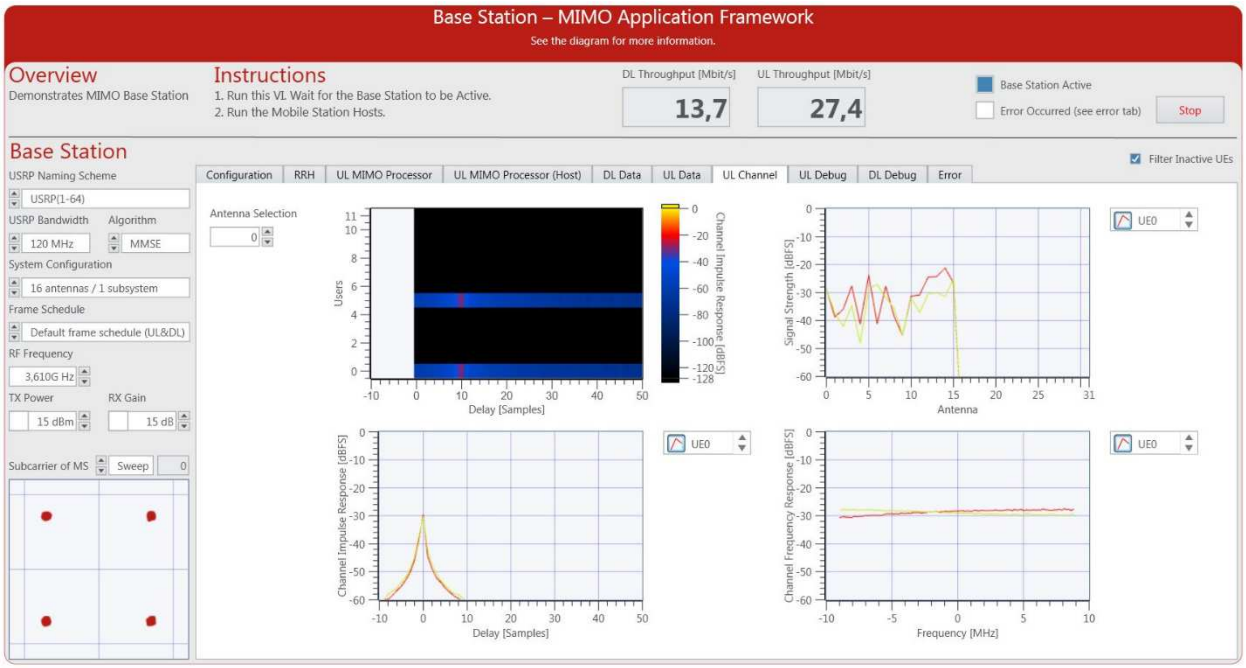
Table 21. BS Host - Control on UL Channel Tab

Control	Description
Antenna Selection	Numerical control selects the BS antenna to calculate the Channel Frequency Responses, Channel Impulse Responses, and the Users intensity.

Table 22. BS Host - Indicators on UL Channel Tab

Indicator	Description
Signal Strength	Graphical indication located on top-right side showing the received signal strength for all MSs versus all antennas of BS.
Channel Frequency Response	Graphical indication located on bottom-right showing the channel frequency responses of all MSs in dBFS.
Channel Impulse Response	Graphical indication located on bottom-left showing the channel impulse responses of all MSs. The amplitude of the channel impulse responses is in dBFS while the time delay is in terms of LTE samples.
Intensity Graph	Graphical indication located on top-left side showing the **Channel Impulse Response** of MSs as an intensity figure.

Figure 23. Front Panel of BS (UL Channel Tab)



BS Control and Indicators on UL Debug Tab

Figure 24 shows the screenshot of the UL Debug tab of **Base Station Host.gvi**. This tab contains a block diagram of the uplink part of the system overlaid with numeric and Boolean indicators which indicate the number of samples processed per second and fixed-point overflows. The control and indicators are listed in Table 23 and Table 24.

Table 23. BS Host - Control on UL Debug Tab

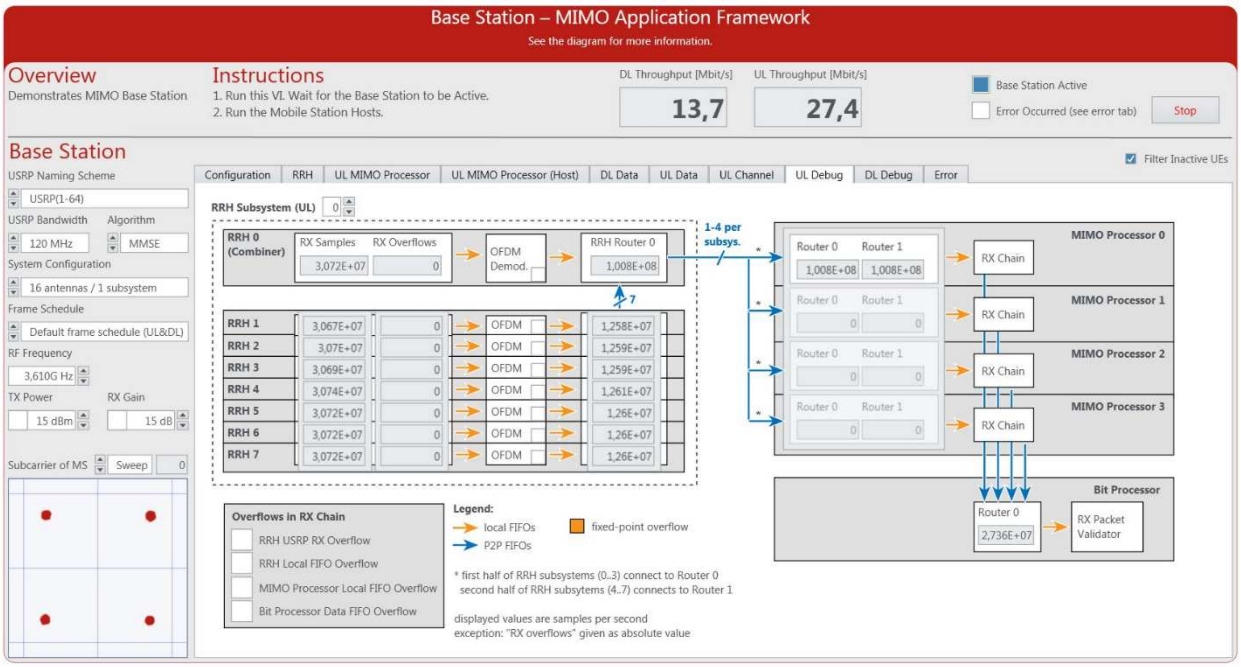
Control	Description
RRH Subsystem (UL)	Numerical control selects the subsystem number based on the MIMO system configuration. The maximum number of subsystems is 8, hence the control ranges from 0 to 7.

Table 24. BS Host - Indicators on UL Debug Tab

Indicator	Description
For **RRH 0** to **RRH 7**	
RX Samples	Numerical indicator displaying the number of RX samples in the time domain processed per second. Because the LTE sampling frequency is 30.72 MHz, the values should equal 3.072×10^7.

RX Overflows	Numerical indicator that indicates overflows in the FIFO which connects the USRP RX loop (which reads from the ADC and performs digital down-conversion) and the RX I/Q processing loop (which performs OFDM demodulation). Overflows can occur when the samples are not processed fast enough either in the RX I/Q processing chain or on the MIMO Processors. Another possibility is too high traffic on the PCI-Express bus which stalls the P2P streams. The values should be zero if the system is in normal operation.
Fixed-point overflow	Boolean indicator that indicates fixed-point overflows in the I/Q processing chain. The TX power levels and RX gains should be configured so that no fixed-point overflows occur.
RRH Router 0	Number of samples processed per second by RRH Router 0. The number should be 1.26×10^7 multiplied by the number of RRHs in the subsystem for the first RRH in a subsystem (RRH Combiner).
For **MIMO Processor 0** to **MIMO Processor 3**	
Router 0 and **Router 1**	Numeric indicators displaying the number of samples processed by router 0 and router 1 per second. The value should be 1.008×10^8.
Bit Processor	
Router 0	Numeric indicator displaying the number of samples processed by router 0 per second. The value depends on the selected frame schedule.
Overflows in RX Chain	
RRH USRP RX Overflow	Indicates that an overflow occurred on the RRH between RF and baseband clock domain.
RRH Local FIFO Overflow	Indicates that an overflow occurred on the RRH when forwarding RX data to Router 0.
MIMO Processor Local FIFO Overflow	Indicates that an overflow occurred on the MIMO processor when forwarding RX data to the bit processor.
Bit Processor Data FIFO Overflow	Indicates that an overflow occurred on the Bit processor when writing RX data to host.

Figure 24. Front Panel of BS (UL Debug Tab)



BS Control and Indicators on DL Debug Tab

Figure 25 shows the screenshot of the DL Debug tab of **Base Station Host.gvi**. This tab contains a block diagram of the downlink part of the system overlaid with numeric and Boolean indicators which indicate the number of samples processed per second and fixed-point overflows. The control and indicators are listed Table 25 and Table 26.

Table 25. BS Host - Control on DL Debug Tab

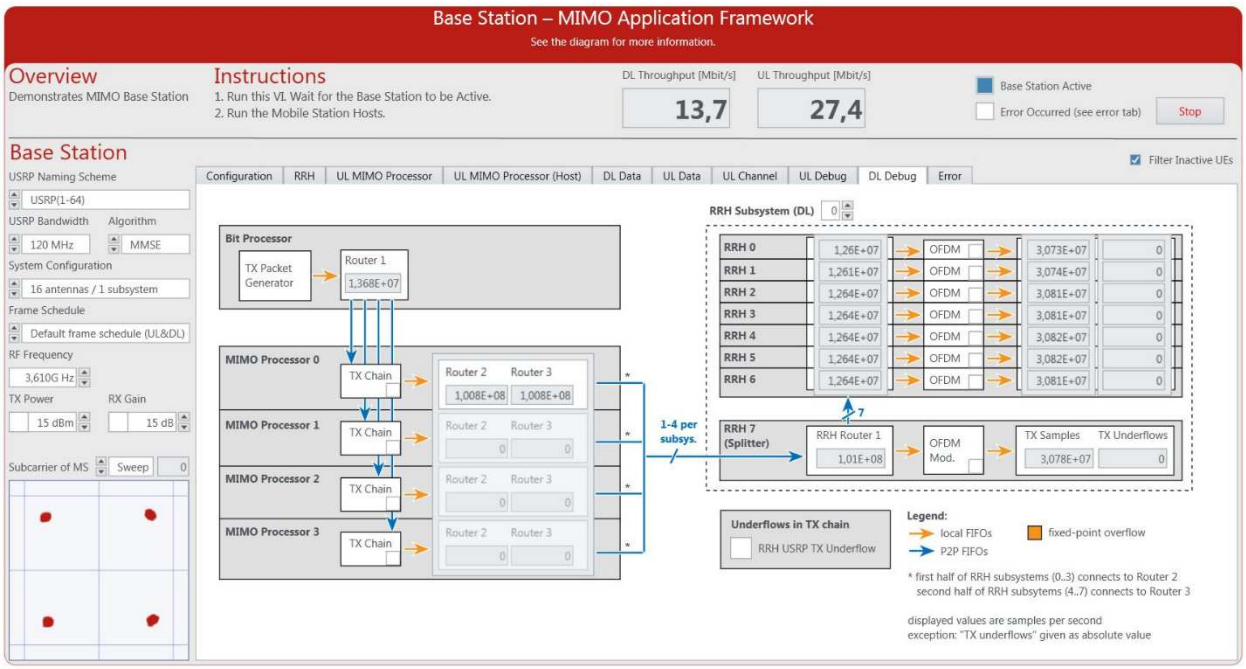
Control	Description
RRH Subsystem (DL)	Numerical control selects the subsystem number based on the MIMO system configuration. The maximum number of subsystems per MIMO system is 8, hence the control ranges from 0 to 7.

Table 26. BS Host - Indicators on DL Debug Tab

Indicator	Description
Bit processor	
Router 1	Numeric indicator displaying the number of samples processed by router 1 per second. The value depends on the selected frame schedule.
For **MIMO Processor 0** to **MIMO Processor 3**	
Fixed-point overflow	Boolean indicator that indicates fixed-point overflows in the TX chain.

Router 2 and **Router 3**	Numeric indicators displaying the number of samples processed by router 2 and router 3 per second. The value should be 1.008×10^8.
For **RRH 0** to **RRH 7**	
RRH Router 1	Number of samples processed per second by RRH Router 1. The number should be 1.26×10^7 multiplied by the number of RRHs in the subsystem for the last RRH in a subsystem (RRH Splitter).
Fixed-point overflow	Boolean indicator that indicates fixed-point overflows in the OFDM modulation.
TX Samples	Numerical indicator displaying the number of TX samples in the time domain processed per second. Because the LTE sampling frequency is 30.72 MHz, the values should equal 3.072×10^7.
TX Underflows	Numerical indicator that indicates underflows in the FIFO between baseband and RF processing on each RRH. Underflows can occur when the samples are not processed fast enough either on the MIMO Processors or in the TX I/Q processing chain. Another possibility is too high traffic on the PCI-Express bus which stalls the P2P streams. The values should be zero if the system is in normal operation.

Figure 25. Front Panel of BS (DL Debug Tab)



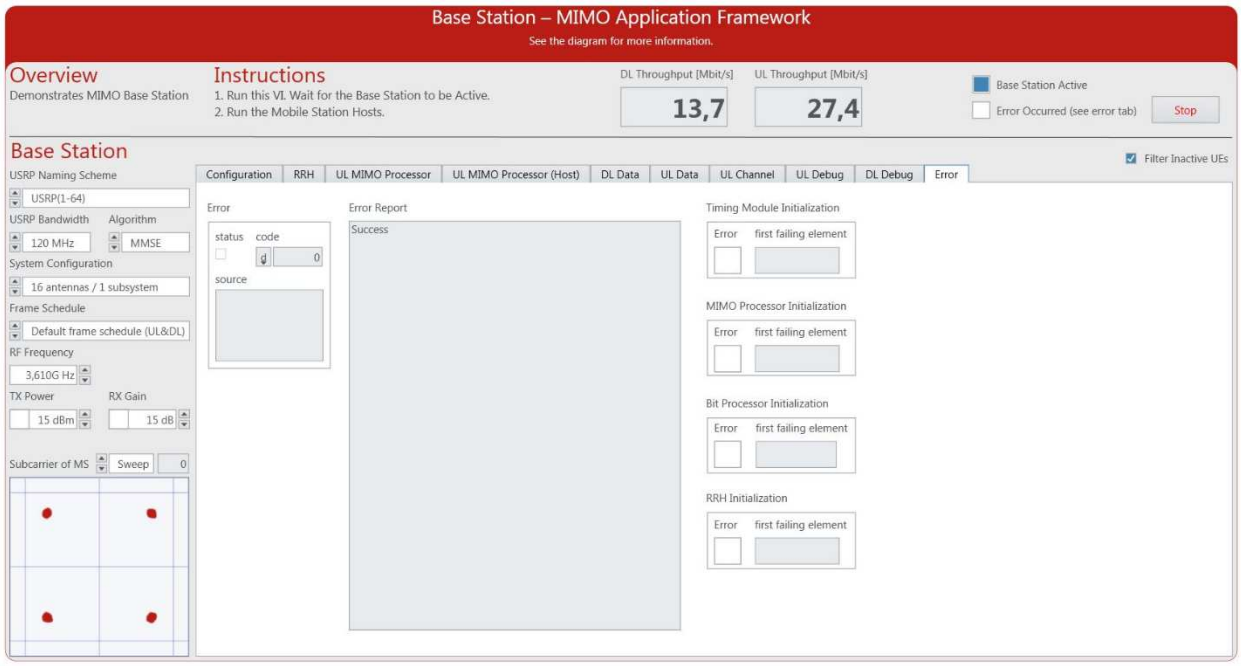
BS Indicators on Error Tab

Figure 26 shows the screenshot of the Error tab of **Base Station Host.gvi**. The indicators on this tab are listed in Table 27. The values are updated when the system stops, for example, upon receiving an error during initialization.

Table 27. BS Host – Indicators on Error Tab

Indicator	Description
Error	Displays the resulting error cluster.
Error Report	Displays resulting error as error report.
Timing Module Initialization	Indicates if an error occurred during initialization of the timing module and, if yes, displays the hardware alias that was used.
MIMO Processor Initialization	Indicates if an error occurred during initialization of the MIMO processors and, if yes, displays the hardware alias of the first failing element.
Bit Processor Initialization	Indicates if an error occurred during initialization of the bit processor.
RRH Initialization	Indicates if an error occurred during initialization of the RRHs and, if yes, displays the hardware alias of the first failing element.

Figure 26. Front Panel of BS (Error Tab)



Description of Controls and Indicators on the MS Host Front Panel

This section describes all controls and indicators that are placed on the front panel of **Mobile Station Host.gvi**.

MS Basic Configurations

Several controls and indicators are placed outside the main tab control of **Mobile Station Host.gvi** as shown in Figure 17. The following table lists the corresponding controls. Table 29 lists the corresponding indicators.

Table 28. MS – Controls on Basic Configurations

Control	Description
RIO Device	Configures the RIO identifier of the **RIO device.** Use MAX to get or modify the RIO identifiers of your devices. You can also launch **Hardware** tab, where LabVIEW Communications System Design Suite has an integrated hardware manager. This control should be configured before running MS.
USRP Bandwidth	Determines the bandwidth of the used USRP RIO devices. The enumeration contains the following values: • 120 or 160 MHz • 40 MHz
UE Sync Mode	Selects the MS Synchronization Mode: • Over-the-air by using synchronization signal. • Using external trigger provided by the BS via PPS trigger port.
Frame Schedule	Determines the frame schedule to use.
RF Frequency	Selects the **RF Frequency** to a frequency supported by your USRP RIO.[11]
AGC Mode	Selects the AGC mode: **manual** or **auto**.
UE ID 0	Selects the MS identity, which should be from the set {0, …, 11}.[12]
UE ID 1	Selects the MS identity, which should be from the set {0, …, 11}.[12]
UE Throughput Selection	Selects the MS throughput type of **UL Throughput [Mbit/s]** and **DL Throughput [Mbit/s]** indicators: • **PHY Throughput**: Shows the packet throughput. • **MAC Throughput**: Shows the payload throughput.

[11] Consider local laws if you are transmitting over-the-air. The USRP-29xx is not approved or licensed for transmission over-the-air using an antenna.

[12] Each MS should be given a different identity otherwise both MSs that have the same identity look like one MS with respect to the BS, and they will receive the same data.

Table 29. MS – Indicators on Basic Configurations

Indicator	Description
FPGA Ready	If the VI started up successfully, it lights.
Error Occurred (see Error tab)	A Boolean indicator that indicates if an error occurred during initialization.
UL Throughput [Mbit/s]	Numerical display showing the UL throughput in Mbit/s for UE 0 and UE 1.
DL Throughput [Mbit/s]	Numerical display showing the DL throughput in Mbit/s for UE 0 and UE 1.

MS Configuration Tab

The following two tables list the controls and indicators, respectively, which are placed on the Configuration tab of **Mobile Station Host.gvi** as shown in Figure 17.

Table 30. MS – Controls on Configuration Tab

Control	Description
UE TX Delay [clock cycles]	Used to adjust the time delay manually in RF clock cycles of the USRP. It should be used with the **UE Signal Delay** figure placed on **RRH** tab of the BS front panel.
UL Synchronization Source	Used to select the UL transmission synchronization source if the **UE Sync Mode** control is over-the-air. It can be automatic or UE 0 or UE 1.
UL Data Source	It has three options: • **Off:** Data source is inactive. • **UDP:** To read data from an UDP socket • **PN Data:** Generate data from a PN Source.
DL Data Sink	If it is set to UDP, received frames are forwarded to the configured UDP address and port.
Initial UL Data UDP Port	This UDP port address and the subsequent one is opened for UDP packet reception for both MSs. The default UDP UL Data Port is 50.000.
Initial DL Data UDP Port	This UDP port address and the subsequent one is opened for UDP packet transmission of both MSs. The default UDP DL Data Port is 51.000.
DL Data Remote Address	The IP address that the UDP packets received from BS are sent to.

Table 31: MS – Indicators on Configuration Tab

Indicator	Description
Frame Schedule Table	Shows the OFDM Frame Schedule of all 12 MSs. The OFDM symbol types of each MS frame (140 OFDM Symbols) are presented. The OFDM symbol type could be Guard, Sync, DL pilot, DL data, UL pilot, and UL data. In addition, the modulation schemes of all MSs are presented, which could be QPSK, 16-QAM, 64-QAM, and 256-QAM. The **Frame Schedule Table** indicator is controlled by **Frame Schedule** control.
UL Data UDP Ports	Shows the value of UDP ports to forward traffic to the BS.
DL Data UDP Ports	Shows the value of UDP ports to forward traffic from the BS.

MS Controls and Indicators on AGC/Synchronization Tab

The following table shows the MS controls that occur on **AGC/Synchronization** tab as shown in Figure 28. Table 33 shows the indicators of the MS on this tab.

Table 32. MS Controls on AGC/Synchronization Tab

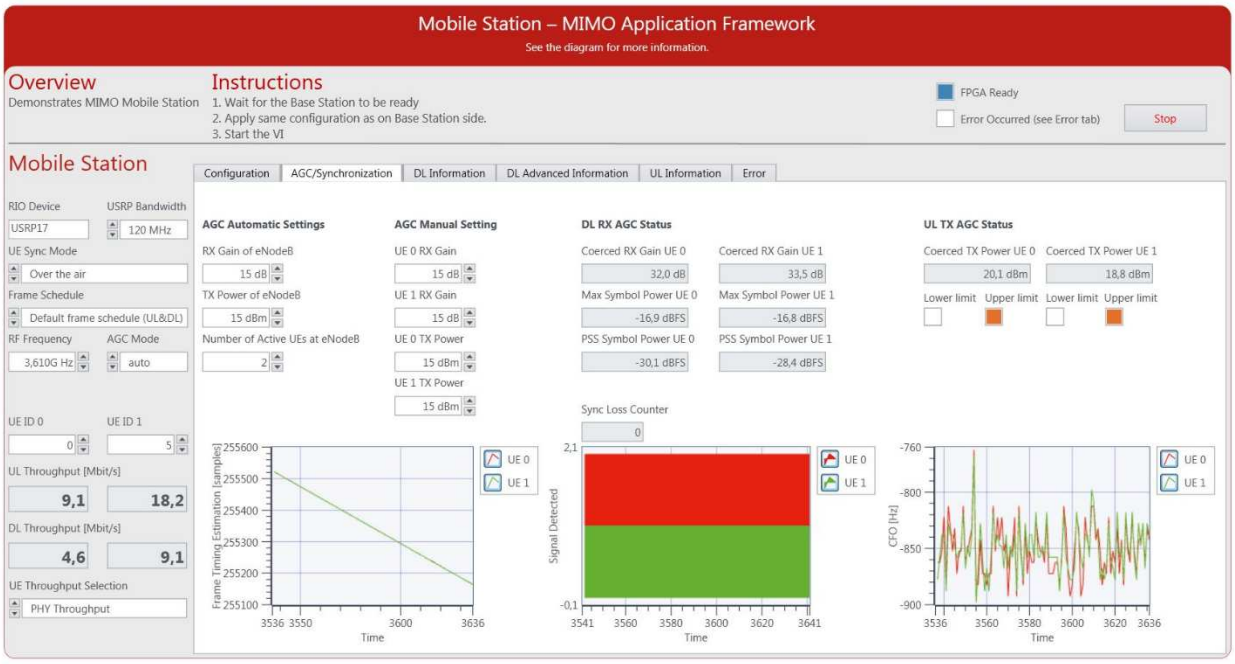
Control	Description
AGC Automatic Settings	Sets the required controls in the calculation of the AGC TX module if the **AGC Mode** control is set to automatic: • **RX Gain of Base Station:** Sets the value similar to that of BS RF receive gain in dB. • **TX Power of Base Station:** Sets the value similar to that of BS RF transmit power in dBm. • **Number of Active UEs at Base Station:** Selects the number of active MSs in the system.
AGC Manual Settings	Sets the required controls if the **AGC Mode** control is set to Manual: • **UE 0 RX Gain**: Sets the RF receive gain in dB of MS 0. • **UE 1 RX Gain**: Sets the RF receive gain in dB of MS 1. • **UE 0 TX Power**: Sets the RF transmit power in dBm of MS 0. • **UE 1 TX Power**: Sets the RF transmit power in dBm of MS 1.

Table 33. MS Indicators on AGC/Synchronization Tab

Indicator	Description
DL RX AGC Status	Shows the status of the DL RX AGC using the following numerical indicators:

	• **Coerced RX Gain UE0:** The actual used analog RX RF gain either set by automatic or manual **AGC Mode.** • **Coerced RX Gain UE1:** The actual used analog RX RF gain either set by automatic or manual **AGC Mode.** • **Max Symbol Power UE0:** Shows the maximum power from the received OFDM symbols of UE0. • **Max Symbol Power UE1:** Shows the maximum power from the received OFDM symbols of UE1. • **PSS Symbol Power UE0:** Shows the power of the received PSS synchronization signal of UE0. • **PSS Symbol Power UE1:** Shows the power of the received PSS synchronization signal of UE1.
UL TX AGC Status	Shows the status of the UL TX AGC using the following numerical and Boolean indicators: • **Coerced TX Power UE 0:** Indicates the coerced value that is actually used as maximum RF transmit output power for UE 0 after applying the device capabilities (range and resolution limitations) to the configured **UE TX Power control.** • **Lower Limit** and **Upper Limit** Boolean indicators corresponding to the **Coerced TX Power UE0** indicator: Show if the configured **UE TX Power** value is coerced to the allowed range. • **Coerced TX Power UE 1:** Similar to that **Coerced TX Power UE 0** of UE0. • **Lower Limit** and **Upper Limit** Boolean indicators corresponding to the **Coerced TX Power UE 1** indicator: Similar to that of UE 0.
Frame Timing Estimation [Samples]	Graphical indication showing the timing estimation of the radio frame.
Signal Detected	Graphical indication showing whether each of the UEs is able to detect the synchronization signal.
Sync Loss Counter	Counts how often the sync was lost since starting the VI.
CFO [Hz]	Graphical indication showing the carrier frequency offset (CFO) in Hz of both MSs.

Figure 27. Front Panel of MS (AGC/Synchronization)



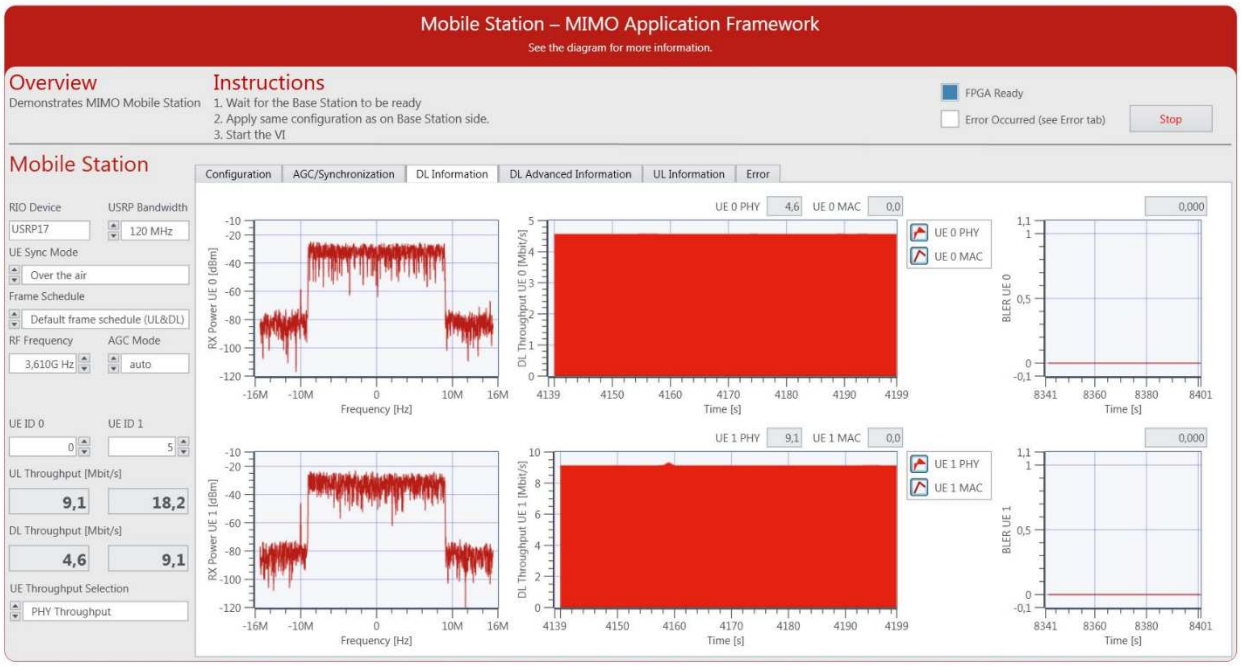
MS Control and Indicators on DL Information Tab

From Figure 28, the control and indicators on the DL Information tab of MS are presented in the following table.

Table 34. MS Control and Indicators on DL Information Tab

Parameter	Description
UE 0 RX Power Spectrum	Indicates the power spectrum of the DL RX baseband signal received from the RF of UE 0.
UE 1 RX Power Spectrum	Indicates the power spectrum of the DL RX baseband signal received from the RF of UE 1.
DL Throughput UE 0	Graphical indication showing the DL throughput of UE 0 in Mbit/s.
UE 0 PHY	Numerical display showing the PHY throughput of UE 0 in Mbit/s.
UE 0 MAC	Numerical display showing the MAC throughput of UE 0 in Mbit/s.
DL Throughput UE 1	Graphical indication showing the DL throughput of UE 1 in Mbit/s.
UE 1 PHY	Numerical display showing the PHY throughput of UE 1 in Mbit/s.
UE 1 MAC	Numerical display showing the MAC throughput of UE 1 in Mbit/s.
BLER UE 0	Graphical and numerical indicator showing the block error rate of UE 0.
BLER UE 1	Graphical and numerical indicator showing the block error rate of UE 1.

Figure 28. Front Panel of MS (DL Information Tab)



MS Indicators on DL Advanced Information Tab

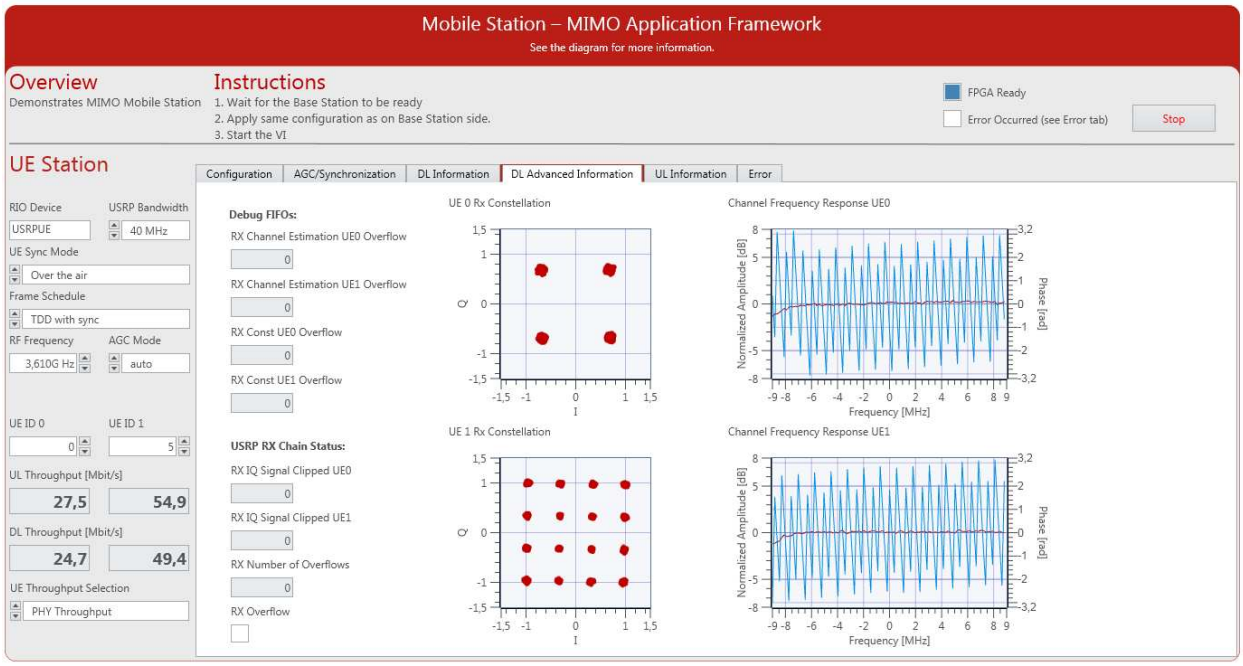
From Figure 29, the indicators on the DL Advanced Information tab of MS are presented in the following table.

Table 35. MS Indicators on DL Advanced Information Tab

Indicator	Description
Debug FIFOs	The following numerical indicators are used to show how many overflows occurred for the following target to host FIFOs: • **RX Channel Estimation UE0 Overflow** • **RX Channel Estimation UE1 Overflow** • **RX Const UE0 Overflow** • **RX Const UE1 Overflow**
USRP RX Chain Status	The following numerical and Boolean indicators are used to count occurrences within RX chain status: • **RX IQ Signal Clipped UE0** • **RX IQ Signal Clipped UE1** • **RX Number of Overflows** • **RX Overflow**

Rx Constellation UE 0	Constellation of RX I/Q samples of UE 0 after equalization. The OFDM symbol to display is changed after each update in a round robin fashion.
Rx Constellation UE 1	Constellation of RX I/Q samples of UE 1 after equalization. The OFDM symbol to display is changed after each update in a round robin fashion.
Channel Frequency Response UE 0	Graphical representation of the channel amplitude and phase estimated using the pilots.
Channel Frequency Response UE 1	Graphical representation of the channel amplitude and phase estimated using the pilots.

Figure 29. Front Panel of MS (DL Advanced Information Tab)



MS Indicators on UL Information Tab

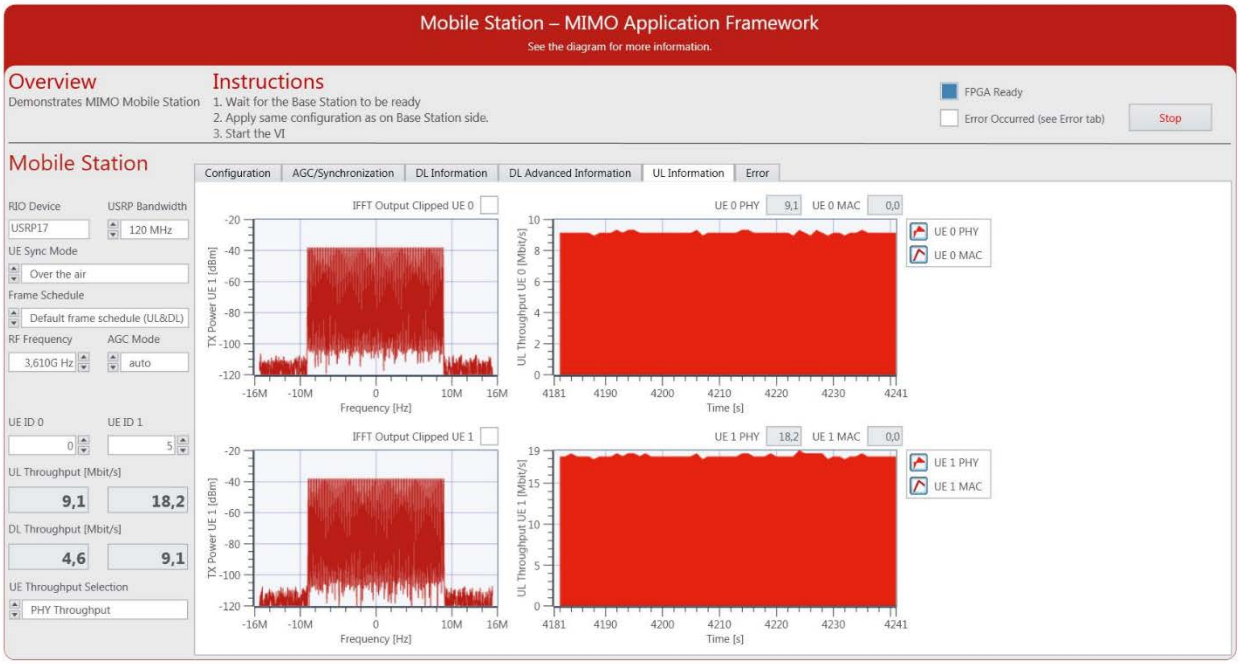
From Figure 30, the indicators on the UL Information tab of the MS are presented in Table 36.

Table 36. MS Indicators on UL Information Tab

Indicator	Description
IFFT Output Clipped UE 0	Indicates a numeric overflow after the IFFT of UE 0.
TX Power Spectrum UE 0	Indicates the power spectrum of the UL TX baseband signal transferred to the RF of UE 0.
IFFT Output Clipped UE 1	Indicates a numeric overflow after the IFFT of UE 1.
TX Power Spectrum UE 1	Indicates the power spectrum of the UL TX baseband signal transferred to the RF of UE 1.
UE 0 PHY and **UE 0 MAC**	Numerical displays showing the PHY and MAC UL throughput in Mbit/s for UE 0.

UL Throughput UE 0	Graphical indication showing the UL throughput in Mbit/s of UE 0.
UE 1 PHY and **UE 1 MAC**	Numerical displays showing the PHY and MAC UL throughput in Mbit/s for UE 1.
UL Throughput UE 1	Graphical indication showing the UL throughput in Mbit/s of UE 1.

Figure 30. Front Panel of MS (UL Information Tab)



MS Indicators on Error Tab

Such as the BS **Error** tab, there are two indicators (**Error** and **Error Report**) that are used to show the error reports in the system.

Troubleshooting

Ensure that you have verified the following:

- Your hardware devices are connected correctly.
- The USRP devices are already switched on and connected to the host before the host is switched on. Otherwise the NI USRP devices may not properly recognized by the host.
- If any device such as USRP is switched off, restart the laptop or the PXI system.

You can access the software and documentation known issues list online. Refer to the MIMO Application Framework 1.0 Known Issues at `ni.com/info` and enter the Info Code exevw4 for an up-to-date list of known issues in MIMO Application Framework 1.0.

Related Information

- NI USRP and LabVIEW Communications System Design Suite Getting Started Guide
- IEEE Standards Association: 802.11 Wireless LANs
- 3GPP TS 36.211 (Physical channels and modulation) Release 10
- 3GPP TS 36.213 (Physical layer procedure) Release 10
- Visit `ni.com/info` and enter commsmanual to access the *LabVIEW Communications System Design Suite Manual* for information about LabVIEW concepts or objects used in this sample project.
- Use the **Context Help** window to learn basic information about LabVIEW objects as you move the cursor over each object. To display the **Context Help** window in LabVIEW, select **View»Context Help**.

Appendix

Cable Connection Mapping and Labeling

Equipment Labeling Rules

Table 37. Equipment Labeling Rules

Equipment	Labeling rule
USRP RIO	**USRP**xx
CDA-2990	**OCLK**xx
CPS-8910	**CPS**xx
PXI	**PXI**xx
PXI slot	**sl**xx_**p**xx

Exception: **OCLKM**x represents OCLK Master
"**sl**"=slot, "**p**"=port

Other Labeling Rules

- All numbers should be represented as double-digit integers, that is, **xx**
- Labels should be short abbreviation of the equipment type
- Labels should be unique for the certain type of equipment
- Labels should represent the type of the equipment
- No dots ("**.**") are allowed
- No spaces (" ") are allowed

Red text = REF
Blue text = PPS / TRIG
Green text = MXI

Table 38. 16-Antenna MIMO System Cable Connection Mapping

Cable name	Side 1		Cable type	Side 2		Label on Cable End 1	Label on Cable End 2	Description
	Equip-ment	Port/Slot		Equip-ment	Port/Slot			
REF1	USRP01	RefIn	RF_coax	OCLK01	10MHzOut01	**OCLK01_10MHzOut01**	**USRP01_RefIn**	Ref.Clock for USRP01
REF2	USRP02	RefIn	RF_coax	OCLK01	10MHzOut02	**OCLK01_10MHzOut02**	**USRP02_RefIn**	Ref.Clock for USRP02
REF3	USRP03	RefIn	RF_coax	OCLK01	10MHzOut03	**OCLK01_10MHzOut03**	**USRP03_RefIn**	Ref.Clock for USRP03
REF4	USRP04	RefIn	RF_coax	OCLK01	10MHzOut04	**OCLK01_10MHzOut04**	**USRP04_RefIn**	Ref.Clock for USRP04
REF5	USRP05	RefIn	RF_coax	OCLK01	10MHzOut05	**OCLK01_10MHzOut05**	**USRP05_RefIn**	Ref.Clock for USRP05
REF6	USRP06	RefIn	RF_coax	OCLK01	10MHzOut06	**OCLK01_10MHzOut06**	**USRP06_RefIn**	Ref.Clock for USRP06
REF7	USRP07	RefIn	RF_coax	OCLK01	10MHzOut07	**OCLK01_10MHzOut07**	**USRP07_RefIn**	Ref.Clock for USRP07
REF8	USRP08	RefIn	RF_coax	OCLK01	10MHzOut08	**OCLK01_10MHzOut08**	**USRP08_RefIn**	Ref.Clock for USRP08
C1REF	PXI01	sl10_CLKout	RF_coax	OCLK01	Ext10MHzInput	**OCLK01_Ext10MHzInput**	**PXI01_sl10_CLKout**	Ref.Clock for OCLK01 from PXI01
PPS1	USRP01	PPSIn	RF_coax	OCLK01	PPSout01	**OCLK01_PPSout01**	**USRP01_PPSIn**	PPS for USRP01
PPS2	USRP02	PPSIn	RF_coax	OCLK01	PPSout02	**OCLK01_PPSout02**	**USRP02_PPSIn**	PPS for USRP02
PPS3	USRP03	PPSIn	RF_coax	OCLK01	PPSout03	**OCLK01_PPSout03**	**USRP03_PPSIn**	PPS for USRP03
PPS4	USRP04	PPSIn	RF_coax	OCLK01	PPSout04	**OCLK01_PPSout04**	**USRP04_PPSIn**	PPS for USRP04
PPS5	USRP05	PPSIn	RF_coax	OCLK01	PPSout05	**OCLK01_PPSout05**	**USRP05_PPSIn**	PPS for USRP05
PPS6	USRP06	PPSIn	RF_coax	OCLK01	PPSout06	**OCLK01_PPSout06**	**USRP06_PPSIn**	PPS for USRP06
PPS7	USRP07	PPSIn	RF_coax	OCLK01	PPSout07	**OCLK01_PPSout07**	**USRP07_PPSIn**	PPS for USRP07
PPS8	USRP08	PPSIn	RF_coax	OCLK01	PPSout08	**OCLK01_PPSout08**	**USRP08_PPSIn**	PPS for USRP08
C1PPS	PXI01	sl10_PFI3	RF_coax	OCLK01	PPSin	**OCLK01_PPSin**	**PXI01_sl10_PFI3**	PPS for OCLK01 from PXI01
MTRIG	USRP01	TRIGout	RF_coax	PXI01	sl10_PFI1	**PXI01_sl10_PFI1**	**USRP01_TRIGout**	Master TRIG for PXI01 from USRP01
MXI1	USRP01	MXI01	MXI	CPS01	MXIx4_p01	**CPS01_MXIx4_p01**	**USRP01_MXI01**	MXI for USRP01
MXI2	USRP02	MXI01	MXI	CPS01	MXIx4_p02	**CPS01_MXIx4_p02**	**USRP02_MXI01**	MXI for USRP02
MXI3	USRP03	MXI01	MXI	CPS01	MXIx4_p03	**CPS01_MXIx4_p03**	**USRP03_MXI01**	MXI for USRP03
MXI4	USRP04	MXI01	MXI	CPS01	MXIx4_p04	**CPS01_MXIx4_p04**	**USRP04_MXI01**	MXI for USRP04
MXI5	USRP05	MXI01	MXI	CPS01	MXIx4_p05	**CPS01_MXIx4_p05**	**USRP05_MXI01**	MXI for USRP05
MXI6	USRP06	MXI01	MXI	CPS01	MXIx4_p06	**CPS01_MXIx4_p06**	**USRP06_MXI01**	MXI for USRP06
MXI7	USRP07	MXI01	MXI	CPS01	MXIx4_p07	**CPS01_MXIx4_p07**	**USRP07_MXI01**	MXI for USRP07
MXI8	USRP08	MXI01	MXI	CPS01	MXIx4_p08	**CPS01_MXIx4_p08**	**USRP08_MXI01**	MXI for USRP08
C1MXI	PXI01	sl02_MXI1	MXI	CPS01	MXIx8	**CPS01_MXIx8**	**PXI01_sl02_MXI1**	MXI for CPS01 from PXI01

Table 39. 32-Antenna MIMO System Cable Connection Mapping

Cable name	Side 1		Cable type	Side 2		Label on Cable End 1	Label on Cable End 2	Description
	Equip-ment	Port/Slot		Equip-ment	Port/Slot			
REF1	USRP01	RefIn	RF_coax	OCLK01	10MHzOut 01	**OCLK01_10MHzOut01**	**USRP01_RefIn**	Ref.Clock for USRP01
REF2	USRP02	RefIn	RF_coax	OCLK01	10MHzOut02	**OCLK01_10MHzOut02**	**USRP02_RefIn**	Ref.Clock for USRP02
REF3	USRP03	RefIn	RF_coax	OCLK01	10MHzOut03	**OCLK01_10MHzOut03**	**USRP03_RefIn**	Ref.Clock for USRP03
REF4	USRP04	RefIn	RF_coax	OCLK01	10MHzOut04	**OCLK01_10MHzOut04**	**USRP04_RefIn**	Ref.Clock for USRP04
REF5	USRP05	RefIn	RF_coax	OCLK01	10MHzOut05	**OCLK01_10MHzOut05**	**USRP05_RefIn**	Ref.Clock for USRP05
REF6	USRP06	RefIn	RF_coax	OCLK01	10MHzOut06	**OCLK01_10MHzOut06**	**USRP06_RefIn**	Ref.Clock for USRP06
REF7	USRP07	RefIn	RF_coax	OCLK01	10MHzOut07	**OCLK01_10MHzOut07**	**USRP07_RefIn**	Ref.Clock for USRP07
REF8	USRP08	RefIn	RF_coax	OCLK01	10MHzOut08	**OCLK01_10MHzOut08**	**USRP08_RefIn**	Ref.Clock for USRP08
REF9	USRP09	RefIn	RF_coax	OCLK02	10MHzOut01	**OCLK02_10MHzOut01**	**USRP09_RefIn**	Ref.Clock for USRP09
REF10	USRP10	RefIn	RF_coax	OCLK02	10MHzOut02	**OCLK02_10MHzOut02**	**USRP10_RefIn**	Ref.Clock for USRP10
REF11	USRP11	RefIn	RF_coax	OCLK02	10MHzOut03	**OCLK02_10MHzOut03**	**USRP11_RefIn**	Ref.Clock for USRP11
REF12	USRP12	RefIn	RF_coax	OCLK02	10MHzOut04	**OCLK02_10MHzOut04**	**USRP12_RefIn**	Ref.Clock for USRP12
REF13	USRP13	RefIn	RF_coax	OCLK02	10MHzOut05	**OCLK02_10MHzOut05**	**USRP13_RefIn**	Ref.Clock for USRP13
REF14	USRP14	RefIn	RF_coax	OCLK02	10MHzOut06	**OCLK02_10MHzOut06**	**USRP14_RefIn**	Ref.Clock for USRP14
REF15	USRP15	RefIn	RF_coax	OCLK02	10MHzOut07	**OCLK02_10MHzOut07**	**USRP15_RefIn**	Ref.Clock for USRP15
REF16	USRP16	RefIn	RF_coax	OCLK02	10MHzOut08	**OCLK02_10MHzOut08**	**USRP16_RefIn**	Ref.Clock for USRP16
C1REF	OCLKM1	10MHzOut01	RF_coax	OCLK01	Ext10MHzInput	**OCLK01_Ext10MHzInput**	**OCLKM1_10MHzOut01**	Ref.Clock for OCLK01 from OCLKM1
C2REF	OCLKM1	10MHzOut02	RF_coax	OCLK02	Ext10MHzInput	**OCLK02_Ext10MHzInput**	**OCLKM1_10MHzOut02**	Ref.Clock for OCLK02 from OCLKM1
CMREF	PXI01	sl10_CLKout	RF_coax	OCLKM1	Ext10MHzInput	**OCLKM1_Ext10MHzInput**	**PXI01_sl10_CLKout**	Ref.Clock for OCLKM1 from PXI01
PPS1	USRP01	PPSIn	RF_coax	OCLK01	PPSout01	**OCLK01_PPSout01**	**USRP01_PPSIn**	PPS for USRP01
PPS2	USRP02	PPSIn	RF_coax	OCLK01	PPSout02	**OCLK01_PPSout02**	**USRP02_PPSIn**	PPS for USRP02
PPS3	USRP03	PPSIn	RF_coax	OCLK01	PPSout03	**OCLK01_PPSout03**	**USRP03_PPSIn**	PPS for USRP03
PPS4	USRP04	PPSIn	RF_coax	OCLK01	PPSout04	**OCLK01_PPSout04**	**USRP04_PPSIn**	PPS for USRP04
PPS5	USRP05	PPSIn	RF_coax	OCLK01	PPSout05	**OCLK01_PPSout05**	**USRP05_PPSIn**	PPS for USRP05
PPS6	USRP06	PPSIn	RF_coax	OCLK01	PPSout06	**OCLK01_PPSout06**	**USRP06_PPSIn**	PPS for USRP06
PPS7	USRP07	PPSIn	RF_coax	OCLK01	PPSout07	**OCLK01_PPSout07**	**USRP07_PPSIn**	PPS for USRP07

PPS8	USRP08	PPSIn	RF_coax	OCLK01	PPSout08	**OCLK01_PPSout08**	**USRP08_PPSIn**	PPS for USRP08
PPS9	USRP09	PPSIn	RF_coax	OCLK02	PPSout01	**OCLK02_PPSout01**	**USRP09_PPSIn**	PPS for USRP09
PPS10	USRP10	PPSIn	RF_coax	OCLK02	PPSout02	**OCLK02_PPSout02**	**USRP10_PPSIn**	PPS for USRP10
PPS11	USRP11	PPSIn	RF_coax	OCLK02	PPSout03	**OCLK02_PPSout03**	**USRP11_PPSIn**	PPS for USRP11
PPS12	USRP12	PPSIn	RF_coax	OCLK02	PPSout04	**OCLK02_PPSout04**	**USRP12_PPSIn**	PPS for USRP12
PPS13	USRP13	PPSIn	RF_coax	OCLK02	PPSout05	**OCLK02_PPSout05**	**USRP13_PPSIn**	PPS for USRP13
PPS14	USRP14	PPSIn	RF_coax	OCLK02	PPSout06	**OCLK02_PPSout06**	**USRP14_PPSIn**	PPS for USRP14
PPS15	USRP15	PPSIn	RF_coax	OCLK02	PPSout07	**OCLK02_PPSout07**	**USRP15_PPSIn**	PPS for USRP15
PPS16	USRP16	PPSIn	RF_coax	OCLK02	PPSout08	**OCLK02_PPSout08**	**USRP16_PPSIn**	PPS for USRP16
C1PPS	OCLKM1	PPSout01	RF_coax	OCLK01	PPSin	**OCLK01_PPSin**	**OCLKM1_PPSout01**	PPS for OCLK01 from OCLKM1
C2PPS	OCLKM1	PPSout02	RF_coax	OCLK02	PPSin	**OCLK02_PPSin**	**OCLKM1_PPSout02**	PPS for OCLK02 from OCLKM1
CMPPS	PXI01	sl10_PFI3	RF_coax	OCLKM1	PPSin	**OCLKM1_PPSin**	**PXI01_sl10_PFI3**	PPS for OCLKM1 from PXI01
MTRIG	USRP01	TRIGout	RF_coax	PXI01	sl10_PFI1	**PXI01_sl10_PFI1**	**USRP01_TRIGout**	Master TRIG for PXI01 from USRP01
MXI1	USRP01	MXI01	MXI	CPS01	MXIx4_p01	**CPS01_MXIx4_p01**	**USRP01_MXI01**	MXI for USRP01
MXI2	USRP02	MXI01	MXI	CPS01	MXIx4_p02	**CPS01_MXIx4_p02**	**USRP02_MXI01**	MXI for USRP02
MXI3	USRP03	MXI01	MXI	CPS01	MXIx4_p03	**CPS01_MXIx4_p03**	**USRP03_MXI01**	MXI for USRP03
MXI4	USRP04	MXI01	MXI	CPS01	MXIx4_p04	**CPS01_MXIx4_p04**	**USRP04_MXI01**	MXI for USRP04
MXI5	USRP05	MXI01	MXI	CPS01	MXIx4_p05	**CPS01_MXIx4_p05**	**USRP05_MXI01**	MXI for USRP05
MXI6	USRP06	MXI01	MXI	CPS01	MXIx4_p06	**CPS01_MXIx4_p06**	**USRP06_MXI01**	MXI for USRP06
MXI7	USRP07	MXI01	MXI	CPS01	MXIx4_p07	**CPS01_MXIx4_p07**	**USRP07_MXI01**	MXI for USRP07
MXI8	USRP08	MXI01	MXI	CPS01	MXIx4_p08	**CPS01_MXIx4_p08**	**USRP08_MXI01**	MXI for USRP08
MXI9	USRP09	MXI01	MXI	CPS02	MXIx4_p01	**CPS02_MXIx4_p01**	**USRP09_MXI01**	MXI for USRP09
MXI10	USRP10	MXI01	MXI	CPS02	MXIx4_p02	**CPS02_MXIx4_p02**	**USRP10_MXI01**	MXI for USRP10
MXI11	USRP11	MXI01	MXI	CPS02	MXIx4_p03	**CPS02_MXIx4_p03**	**USRP11_MXI01**	MXI for USRP11
MXI12	USRP12	MXI01	MXI	CPS02	MXIx4_p04	**CPS02_MXIx4_p04**	**USRP12_MXI01**	MXI for USRP12
MXI13	USRP13	MXI01	MXI	CPS02	MXIx4_p05	**CPS02_MXIx4_p05**	**USRP13_MXI01**	MXI for USRP13
MXI14	USRP14	MXI01	MXI	CPS02	MXIx4_p06	**CPS02_MXIx4_p06**	**USRP14_MXI01**	MXI for USRP14
MXI15	USRP15	MXI01	MXI	CPS02	MXIx4_p07	**CPS02_MXIx4_p07**	**USRP15_MXI01**	MXI for USRP15
MXI16	USRP16	MXI01	MXI	CPS02	MXIx4_p08	**CPS02_MXIx4_p08**	**USRP16_MXI01**	MXI for USRP16
C1MXI	PXI01	sl02_MXI1	MXI	CPS01	MXIx8	**CPS01_MXIx8**	**PXI01_sl02_MXI1**	MXI for CPS01 from PXI01
C2MXI	PXI01	sl18_MXI1	MXI	CPS02	MXIx8	**CPS02_MXIx8**	**PXI01_sl18_MXI1**	MXI for CPS02 from PXI01

Table 40. 64-Antenna MIMO System Cable Connection Mapping

Cable name	Side 1		Cable type	Side 2		Label on Cable End 1	Label on Cable End 2	Description
	Equip-ment	Port/Slot		Equip-ment	Port/Slot			
REF1	USRP01	RefIn	RF_coax	OCLK01	10MHzOut01	**OCLK01_10MHzOut01**	**USRP01_RefIn**	Ref.Clock for USRP01
REF2	USRP02	RefIn	RF_coax	OCLK01	10MHzOut02	**OCLK01_10MHzOut02**	**USRP02_RefIn**	Ref.Clock for USRP02
REF3	USRP03	RefIn	RF_coax	OCLK01	10MHzOut03	**OCLK01_10MHzOut03**	**USRP03_RefIn**	Ref.Clock for USRP03
REF4	USRP04	RefIn	RF_coax	OCLK01	10MHzOut04	**OCLK01_10MHzOut04**	**USRP04_RefIn**	Ref.Clock for USRP04
REF5	USRP05	RefIn	RF_coax	OCLK01	10MHzOut05	**OCLK01_10MHzOut05**	**USRP05_RefIn**	Ref.Clock for USRP05
REF6	USRP06	RefIn	RF_coax	OCLK01	10MHzOut06	**OCLK01_10MHzOut06**	**USRP06_RefIn**	Ref.Clock for USRP06
REF7	USRP07	RefIn	RF_coax	OCLK01	10MHzOut07	**OCLK01_10MHzOut07**	**USRP07_RefIn**	Ref.Clock for USRP07
REF8	USRP08	RefIn	RF_coax	OCLK01	10MHzOut08	**OCLK01_10MHzOut08**	**USRP08_RefIn**	Ref.Clock for USRP08
REF9	USRP09	RefIn	RF_coax	OCLK02	10MHzOut01	**OCLK02_10MHzOut01**	**USRP09_RefIn**	Ref.Clock for USRP09
REF10	USRP10	RefIn	RF_coax	OCLK02	10MHzOut02	**OCLK02_10MHzOut02**	**USRP10_RefIn**	Ref.Clock for USRP10
REF11	USRP11	RefIn	RF_coax	OCLK02	10MHzOut03	**OCLK02_10MHzOut03**	**USRP11_RefIn**	Ref.Clock for USRP11
REF12	USRP12	RefIn	RF_coax	OCLK02	10MHzOut04	**OCLK02_10MHzOut04**	**USRP12_RefIn**	Ref.Clock for USRP12
REF13	USRP13	RefIn	RF_coax	OCLK02	10MHzOut05	**OCLK02_10MHzOut05**	**USRP13_RefIn**	Ref.Clock for USRP13
REF14	USRP14	RefIn	RF_coax	OCLK02	10MHzOut06	**OCLK02_10MHzOut06**	**USRP14_RefIn**	Ref.Clock for USRP14
REF15	USRP15	RefIn	RF_coax	OCLK02	10MHzOut07	**OCLK02_10MHzOut07**	**USRP15_RefIn**	Ref.Clock for USRP15
REF16	USRP16	RefIn	RF_coax	OCLK02	10MHzOut08	**OCLK02_10MHzOut08**	**USRP16_RefIn**	Ref.Clock for USRP16
REF17	USRP17	RefIn	RF_coax	OCLK03	10MHzOut01	**OCLK03_10MHzOut01**	**USRP17_RefIn**	Ref.Clock for USRP17
REF18	USRP18	RefIn	RF_coax	OCLK03	10MHzOut02	**OCLK03_10MHzOut02**	**USRP18_RefIn**	Ref.Clock for USRP18
REF19	USRP19	RefIn	RF_coax	OCLK03	10MHzOut03	**OCLK03_10MHzOut03**	**USRP19_RefIn**	Ref.Clock for USRP19
REF20	USRP20	RefIn	RF_coax	OCLK03	10MHzOut04	**OCLK03_10MHzOut04**	**USRP20_RefIn**	Ref.Clock for USRP20
REF21	USRP21	RefIn	RF_coax	OCLK03	10MHzOut05	**OCLK03_10MHzOut05**	**USRP21_RefIn**	Ref.Clock for USRP21
REF22	USRP22	RefIn	RF_coax	OCLK03	10MHzOut06	**OCLK03_10MHzOut06**	**USRP22_RefIn**	Ref.Clock for USRP22
REF23	USRP23	RefIn	RF_coax	OCLK03	10MHzOut07	**OCLK03_10MHzOut07**	**USRP23_RefIn**	Ref.Clock for USRP23
REF24	USRP24	RefIn	RF_coax	OCLK03	10MHzOut08	**OCLK03_10MHzOut08**	**USRP24_RefIn**	Ref.Clock for USRP24
REF25	USRP25	RefIn	RF_coax	OCLK04	10MHzOut01	**OCLK04_10MHzOut01**	**USRP25_RefIn**	Ref.Clock for USRP25
REF26	USRP26	RefIn	RF_coax	OCLK04	10MHzOut02	**OCLK04_10MHzOut02**	**USRP26_RefIn**	Ref.Clock for USRP26

REF27	USRP27	RefIn	RF_coax	OCLK04	10MHzOut03	**OCLK04_10MHzOut03**	**USRP27_RefIn**	Ref.Clock for USRP27
REF28	USRP28	RefIn	RF_coax	OCLK04	10MHzOut04	**OCLK04_10MHzOut04**	**USRP28_RefIn**	Ref.Clock for USRP28
REF29	USRP29	RefIn	RF_coax	OCLK04	10MHzOut05	**OCLK04_10MHzOut05**	**USRP29_RefIn**	Ref.Clock for USRP29
REF30	USRP30	RefIn	RF_coax	OCLK04	10MHzOut06	**OCLK04_10MHzOut06**	**USRP30_RefIn**	Ref.Clock for USRP30
REF31	USRP31	RefIn	RF_coax	OCLK04	10MHzOut07	**OCLK04_10MHzOut07**	**USRP31_RefIn**	Ref.Clock for USRP31
REF32	USRP32	RefIn	RF_coax	OCLK04	10MHzOut08	**OCLK04_10MHzOut08**	**USRP32_RefIn**	Ref.Clock for USRP32
C1REF	OCLKM1	10MHzOut01	RF_coax	OCLK01	Ext10MHzInput	**OCLK01_Ext10MHzInput**	**OCLKM1_10MHzOut01**	Ref.Clock for OCLK01 from OCLKM1
C2REF	OCLKM1	10MHzOut02	RF_coax	OCLK02	Ext10MHzInput	**OCLK02_Ext10MHzInput**	**OCLKM1_10MHzOut02**	Ref.Clock for OCLK02 from OCLKM1
C3REF	OCLKM1	10MHzOut03	RF_coax	OCLK03	Ext10MHzInput	**OCLK03_Ext10MHzInput**	**OCLKM1_10MHzOut03**	Ref.Clock for OCLK03 from OCLKM1
C4REF	OCLKM1	10MHzOut04	RF_coax	OCLK04	Ext10MHzInput	**OCLK04_Ext10MHzInput**	**OCLKM1_10MHzOut04**	Ref.Clock for OCLK04 from OCLKM1
CMREF	PXI01	sl10_CLKout	RF_coax	OCLKM1	Ext10MHzInput	**OCLKM1_Ext10MHzInput**	**PXI01_sl10_CLKout**	Ref.Clock for OCLKM1 from PXI01
PPS1	USRP01	PPSIn	RF_coax	OCLK01	PPSout01	**OCLK01_PPSout01**	**USRP01_PPSIn**	PPS for USRP01
PPS2	USRP02	PPSIn	RF_coax	OCLK01	PPSout02	**OCLK01_PPSout02**	**USRP02_PPSIn**	PPS for USRP02
PPS3	USRP03	PPSIn	RF_coax	OCLK01	PPSout03	**OCLK01_PPSout03**	**USRP03_PPSIn**	PPS for USRP03
PPS4	USRP04	PPSIn	RF_coax	OCLK01	PPSout04	**OCLK01_PPSout04**	**USRP04_PPSIn**	PPS for USRP04
PPS5	USRP05	PPSIn	RF_coax	OCLK01	PPSout05	**OCLK01_PPSout05**	**USRP05_PPSIn**	PPS for USRP05
PPS6	USRP06	PPSIn	RF_coax	OCLK01	PPSout06	**OCLK01_PPSout06**	**USRP06_PPSIn**	PPS for USRP06
PPS7	USRP07	PPSIn	RF_coax	OCLK01	PPSout07	**OCLK01_PPSout07**	**USRP07_PPSIn**	PPS for USRP07
PPS8	USRP08	PPSIn	RF_coax	OCLK01	PPSout08	**OCLK01_PPSout08**	**USRP08_PPSIn**	PPS for USRP08
PPS9	USRP09	PPSIn	RF_coax	OCLK02	PPSout01	**OCLK02_PPSout01**	**USRP09_PPSIn**	PPS for USRP09
PPS10	USRP10	PPSIn	RF_coax	OCLK02	PPSout02	**OCLK02_PPSout02**	**USRP10_PPSIn**	PPS for USRP10
PPS11	USRP11	PPSIn	RF_coax	OCLK02	PPSout03	**OCLK02_PPSout03**	**USRP11_PPSIn**	PPS for USRP11
PPS12	USRP12	PPSIn	RF_coax	OCLK02	PPSout04	**OCLK02_PPSout04**	**USRP12_PPSIn**	PPS for USRP12
PPS13	USRP13	PPSIn	RF_coax	OCLK02	PPSout05	**OCLK02_PPSout05**	**USRP13_PPSIn**	PPS for USRP13
PPS14	USRP14	PPSIn	RF_coax	OCLK02	PPSout06	**OCLK02_PPSout06**	**USRP14_PPSIn**	PPS for USRP14
PPS15	USRP15	PPSIn	RF_coax	OCLK02	PPSout07	**OCLK02_PPSout07**	**USRP15_PPSIn**	PPS for USRP15
PPS16	USRP16	PPSIn	RF_coax	OCLK02	PPSout08	**OCLK02_PPSout08**	**USRP16_PPSIn**	PPS for USRP16

PPS17	USRP17	PPSIn	RF_coax	OCLK03	PPSout01	**OCLK03_PPSout01**	**USRP17_PPSIn**	PPS for USRP17
PPS18	USRP18	PPSIn	RF_coax	OCLK03	PPSout02	**OCLK03_PPSout02**	**USRP18_PPSIn**	PPS for USRP18
PPS19	USRP19	PPSIn	RF_coax	OCLK03	PPSout03	**OCLK03_PPSout03**	**USRP19_PPSIn**	PPS for USRP19
PPS20	USRP20	PPSIn	RF_coax	OCLK03	PPSout04	**OCLK03_PPSout04**	**USRP20_PPSIn**	PPS for USRP20
PPS21	USRP21	PPSIn	RF_coax	OCLK03	PPSout05	**OCLK03_PPSout05**	**USRP21_PPSIn**	PPS for USRP21
PPS22	USRP22	PPSIn	RF_coax	OCLK03	PPSout06	**OCLK03_PPSout06**	**USRP22_PPSIn**	PPS for USRP22
PPS23	USRP23	PPSIn	RF_coax	OCLK03	PPSout07	**OCLK03_PPSout07**	**USRP23_PPSIn**	PPS for USRP23
PPS24	USRP24	PPSIn	RF_coax	OCLK03	PPSout08	**OCLK03_PPSout08**	**USRP24_PPSIn**	PPS for USRP24
PPS25	USRP25	PPSIn	RF_coax	OCLK04	PPSout01	**OCLK04_PPSout01**	**USRP25_PPSIn**	PPS for USRP25
PPS26	USRP26	PPSIn	RF_coax	OCLK04	PPSout02	**OCLK04_PPSout02**	**USRP26_PPSIn**	PPS for USRP26
PPS27	USRP27	PPSIn	RF_coax	OCLK04	PPSout03	**OCLK04_PPSout03**	**USRP27_PPSIn**	PPS for USRP27
PPS28	USRP28	PPSIn	RF_coax	OCLK04	PPSout04	**OCLK04_PPSout04**	**USRP28_PPSIn**	PPS for USRP28
PPS29	USRP29	PPSIn	RF_coax	OCLK04	PPSout05	**OCLK04_PPSout05**	**USRP29_PPSIn**	PPS for USRP29
PPS30	USRP30	PPSIn	RF_coax	OCLK04	PPSout06	**OCLK04_PPSout06**	**USRP30_PPSIn**	PPS for USRP30
PPS31	USRP31	PPSIn	RF_coax	OCLK04	PPSout07	**OCLK04_PPSout07**	**USRP31_PPSIn**	PPS for USRP31
PPS32	USRP32	PPSIn	RF_coax	OCLK04	PPSout08	**OCLK04_PPSout08**	**USRP32_PPSIn**	PPS for USRP32
C1PPS	OCLKM1	PPSout01	RF_coax	OCLK01	PPSin	**OCLK01_PPSin**	**OCLKM1_PPSout01**	PPS for OCLK01 from OCLKM1
C2PPS	OCLKM1	PPSout02	RF_coax	OCLK02	PPSin	**OCLK02_PPSin**	**OCLKM1_PPSout02**	PPS for OCLK02 from OCLKM1
C3PPS	OCLKM1	PPSout03	RF_coax	OCLK03	PPSin	**OCLK03_PPSin**	**OCLKM1_PPSout03**	PPS for OCLK03 from OCLKM1
C4PPS	OCLKM1	PPSout04	RF_coax	OCLK04	PPSin	**OCLK04_PPSin**	**OCLKM1_PPSout04**	PPS for OCLK04 from OCLKM1
CMPPS	PXI01	sl10_PFI3	RF_coax	OCLKM1	PPSin	**OCLKM1_PPSin**	**PXI01_sl10_PFI3**	PPS for OCLKM1 from PXI01
MTRIG	USRP01	TRIGout	RF_coax	PXI01	sl10_PFI1	**PXI01_sl10_PFI1**	**USRP01_TRIGout**	Master TRIG for PXI01 from USRP01
MXI1	USRP01	MXI01	MXI	CPS01	MXIx4_p01	**CPS01_MXIx4_p01**	**USRP01_MXI01**	MXI for USRP01
MXI2	USRP02	MXI01	MXI	CPS01	MXIx4_p02	**CPS01_MXIx4_p02**	**USRP02_MXI01**	MXI for USRP02
MXI3	USRP03	MXI01	MXI	CPS01	MXIx4_p03	**CPS01_MXIx4_p03**	**USRP03_MXI01**	MXI for USRP03
MXI4	USRP04	MXI01	MXI	CPS01	MXIx4_p04	**CPS01_MXIx4_p04**	**USRP04_MXI01**	MXI for USRP04
MXI5	USRP05	MXI01	MXI	CPS01	MXIx4_p05	**CPS01_MXIx4_p05**	**USRP05_MXI01**	MXI for USRP05
MXI6	USRP06	MXI01	MXI	CPS01	MXIx4_p06	**CPS01_MXIx4_p06**	**USRP06_MXI01**	MXI for USRP06
MXI7	USRP07	MXI01	MXI	CPS01	MXIx4_p07	**CPS01_MXIx4_p07**	**USRP07_MXI01**	MXI for USRP07
MXI8	USRP08	MXI01	MXI	CPS01	MXIx4_p08	**CPS01_MXIx4_p08**	**USRP08_MXI01**	MXI for USRP08
MXI9	USRP09	MXI01	MXI	CPS02	MXIx4_p01	**CPS02_MXIx4_p01**	**USRP09_MXI01**	MXI for USRP09

MXI10	USRP10	MXI01	MXI	CPS02	MXIx4_p02	**CPS02_MXIx4_p02**	**USRP10_MXI01**	MXI for USRP10
MXI11	USRP11	MXI01	MXI	CPS02	MXIx4_p03	**CPS02_MXIx4_p03**	**USRP11_MXI01**	MXI for USRP11
MXI12	USRP12	MXI01	MXI	CPS02	MXIx4_p04	**CPS02_MXIx4_p04**	**USRP12_MXI01**	MXI for USRP12
MXI13	USRP13	MXI01	MXI	CPS02	MXIx4_p05	**CPS02_MXIx4_p05**	**USRP13_MXI01**	MXI for USRP13
MXI14	USRP14	MXI01	MXI	CPS02	MXIx4_p06	**CPS02_MXIx4_p06**	**USRP14_MXI01**	MXI for USRP14
MXI15	USRP15	MXI01	MXI	CPS02	MXIx4_p07	**CPS02_MXIx4_p07**	**USRP15_MXI01**	MXI for USRP15
MXI16	USRP16	MXI01	MXI	CPS02	MXIx4_p08	**CPS02_MXIx4_p08**	**USRP16_MXI01**	MXI for USRP16
MXI17	USRP17	MXI01	MXI	CPS03	MXIx4_p01	**CPS03_MXIx4_p01**	**USRP17_MXI01**	MXI for USRP17
MXI18	USRP18	MXI01	MXI	CPS03	MXIx4_p02	**CPS03_MXIx4_p02**	**USRP18_MXI01**	MXI for USRP18
MXI19	USRP19	MXI01	MXI	CPS03	MXIx4_p03	**CPS03_MXIx4_p03**	**USRP19_MXI01**	MXI for USRP19
MXI20	USRP20	MXI01	MXI	CPS03	MXIx4_p04	**CPS03_MXIx4_p04**	**USRP20_MXI01**	MXI for USRP20
MXI21	USRP21	MXI01	MXI	CPS03	MXIx4_p05	**CPS03_MXIx4_p05**	**USRP21_MXI01**	MXI for USRP21
MXI22	USRP22	MXI01	MXI	CPS03	MXIx4_p06	**CPS03_MXIx4_p06**	**USRP22_MXI01**	MXI for USRP22
MXI23	USRP23	MXI01	MXI	CPS03	MXIx4_p07	**CPS03_MXIx4_p07**	**USRP23_MXI01**	MXI for USRP23
MXI24	USRP24	MXI01	MXI	CPS03	MXIx4_p08	**CPS03_MXIx4_p08**	**USRP24_MXI01**	MXI for USRP24
MXI25	USRP25	MXI01	MXI	CPS04	MXIx4_p01	**CPS04_MXIx4_p01**	**USRP25_MXI01**	MXI for USRP25
MXI26	USRP26	MXI01	MXI	CPS04	MXIx4_p02	**CPS04_MXIx4_p02**	**USRP26_MXI01**	MXI for USRP26
MXI27	USRP27	MXI01	MXI	CPS04	MXIx4_p03	**CPS04_MXIx4_p03**	**USRP27_MXI01**	MXI for USRP27
MXI28	USRP28	MXI01	MXI	CPS04	MXIx4_p04	**CPS04_MXIx4_p04**	**USRP28_MXI01**	MXI for USRP28
MXI29	USRP29	MXI01	MXI	CPS04	MXIx4_p05	**CPS04_MXIx4_p05**	**USRP29_MXI01**	MXI for USRP29
MXI30	USRP30	MXI01	MXI	CPS04	MXIx4_p06	**CPS04_MXIx4_p06**	**USRP30_MXI01**	MXI for USRP30
MXI31	USRP31	MXI01	MXI	CPS04	MXIx4_p07	**CPS04_MXIx4_p07**	**USRP31_MXI01**	MXI for USRP31
MXI32	USRP32	MXI01	MXI	CPS04	MXIx4_p08	**CPS04_MXIx4_p08**	**USRP32_MXI01**	MXI for USRP32
C1MXI	PXI01	sl02_MXI1	MXI	CPS01	MXIx8	**CPS01_MXIx8**	**PXI01_sl02_MXI1**	MXI for CPS01 from PXI01
C2MXI	PXI01	sl03_MXI1	MXI	CPS02	MXIx8	**CPS02_MXIx8**	**PXI01_sl03_MXI1**	MXI for CPS02 from PXI01
C3MXI	PXI01	sl17_MXI1	MXI	CPS03	MXIx8	**CPS03_MXIx8**	**PXI01_sl17_MXI1**	MXI for CPS03 from PXI01
C4MXI	PXI01	sl18_MXI1	MXI	CPS04	MXIx8	**CPS04_MXIx8**	**PXI01_sl18_MXI1**	MXI for CPS04 from PXI01

Table 41. 128-Antenna MIMO System Cable Connection Mapping

Cable name	Side 1		Cable type	Side 2		Label on Cable End 1	Label on Cable End 2	Description
	Equipment	Port/Slot		Equipment	Port/Slot			
REF1	USRP01	RefIn	RF_coax	OCLK01	10MHzOut01	**OCLK01_10MHzOut01**	**USRP01_RefIn**	Ref.Clock for USRP01
REF2	USRP02	RefIn	RF_coax	OCLK01	10MHzOut02	**OCLK01_10MHzOut02**	**USRP02_RefIn**	Ref.Clock for USRP02
REF3	USRP03	RefIn	RF_coax	OCLK01	10MHzOut03	**OCLK01_10MHzOut03**	**USRP03_RefIn**	Ref.Clock for USRP03
REF4	USRP04	RefIn	RF_coax	OCLK01	10MHzOut04	**OCLK01_10MHzOut04**	**USRP04_RefIn**	Ref.Clock for USRP04
REF5	USRP05	RefIn	RF_coax	OCLK01	10MHzOut05	**OCLK01_10MHzOut05**	**USRP05_RefIn**	Ref.Clock for USRP05
REF6	USRP06	RefIn	RF_coax	OCLK01	10MHzOut06	**OCLK01_10MHzOut06**	**USRP06_RefIn**	Ref.Clock for USRP06
REF7	USRP07	RefIn	RF_coax	OCLK01	10MHzOut07	**OCLK01_10MHzOut07**	**USRP07_RefIn**	Ref.Clock for USRP07
REF8	USRP08	RefIn	RF_coax	OCLK01	10MHzOut08	**OCLK01_10MHzOut08**	**USRP08_RefIn**	Ref.Clock for USRP08
REF9	USRP09	RefIn	RF_coax	OCLK02	10MHzOut01	**OCLK02_10MHzOut01**	**USRP09_RefIn**	Ref.Clock for USRP09
REF10	USRP10	RefIn	RF_coax	OCLK02	10MHzOut02	**OCLK02_10MHzOut02**	**USRP10_RefIn**	Ref.Clock for USRP10
REF11	USRP11	RefIn	RF_coax	OCLK02	10MHzOut03	**OCLK02_10MHzOut03**	**USRP11_RefIn**	Ref.Clock for USRP11
REF12	USRP12	RefIn	RF_coax	OCLK02	10MHzOut04	**OCLK02_10MHzOut04**	**USRP12_RefIn**	Ref.Clock for USRP12
REF13	USRP13	RefIn	RF_coax	OCLK02	10MHzOut05	**OCLK02_10MHzOut05**	**USRP13_RefIn**	Ref.Clock for USRP13
REF14	USRP14	RefIn	RF_coax	OCLK02	10MHzOut06	**OCLK02_10MHzOut06**	**USRP14_RefIn**	Ref.Clock for USRP14
REF15	USRP15	RefIn	RF_coax	OCLK02	10MHzOut07	**OCLK02_10MHzOut07**	**USRP15_RefIn**	Ref.Clock for USRP15
REF16	USRP16	RefIn	RF_coax	OCLK02	10MHzOut08	**OCLK02_10MHzOut08**	**USRP16_RefIn**	Ref.Clock for USRP16
REF17	USRP17	RefIn	RF_coax	OCLK03	10MHzOut01	**OCLK03_10MHzOut01**	**USRP17_RefIn**	Ref.Clock for USRP17
REF18	USRP18	RefIn	RF_coax	OCLK03	10MHzOut02	**OCLK03_10MHzOut02**	**USRP18_RefIn**	Ref.Clock for USRP18
REF19	USRP19	RefIn	RF_coax	OCLK03	10MHzOut03	**OCLK03_10MHzOut03**	**USRP19_RefIn**	Ref.Clock for USRP19
REF20	USRP20	RefIn	RF_coax	OCLK03	10MHzOut04	**OCLK03_10MHzOut04**	**USRP20_RefIn**	Ref.Clock for USRP20
REF21	USRP21	RefIn	RF_coax	OCLK03	10MHzOut05	**OCLK03_10MHzOut05**	**USRP21_RefIn**	Ref.Clock for USRP21
REF22	USRP22	RefIn	RF_coax	OCLK03	10MHzOut06	**OCLK03_10MHzOut06**	**USRP22_RefIn**	Ref.Clock for USRP22
REF23	USRP23	RefIn	RF_coax	OCLK03	10MHzOut07	**OCLK03_10MHzOut07**	**USRP23_RefIn**	Ref.Clock for USRP23
REF24	USRP24	RefIn	RF_coax	OCLK03	10MHzOut08	**OCLK03_10MHzOut08**	**USRP24_RefIn**	Ref.Clock for USRP24
REF25	USRP25	RefIn	RF_coax	OCLK04	10MHzOut01	**OCLK04_10MHzOut01**	**USRP25_RefIn**	Ref.Clock for USRP25
REF26	USRP26	RefIn	RF_coax	OCLK04	10MHzOut02	**OCLK04_10MHzOut02**	**USRP26_RefIn**	Ref.Clock for USRP26
REF27	USRP27	RefIn	RF_coax	OCLK04	10MHzOut03	**OCLK04_10MHzOut03**	**USRP27_RefIn**	Ref.Clock for USRP27
REF28	USRP28	RefIn	RF_coax	OCLK04	10MHzOut04	**OCLK04_10MHzOut04**	**USRP28_RefIn**	Ref.Clock for USRP28

REF29	USRP29	RefIn	RF_coax	OCLK04	10MHzOut05	**OCLK04_10MHzOut05**	**USRP29_RefIn**	Ref.Clock for USRP29
REF30	USRP30	RefIn	RF_coax	OCLK04	10MHzOut06	**OCLK04_10MHzOut06**	**USRP30_RefIn**	Ref.Clock for USRP30
REF31	USRP31	RefIn	RF_coax	OCLK04	10MHzOut07	**OCLK04_10MHzOut07**	**USRP31_RefIn**	Ref.Clock for USRP31
REF32	USRP32	RefIn	RF_coax	OCLK04	10MHzOut08	**OCLK04_10MHzOut08**	**USRP32_RefIn**	Ref.Clock for USRP32
REF33	USRP33	RefIn	RF_coax	OCLK05	10MHzOut01	**OCLK05_10MHzOut01**	**USRP33_RefIn**	Ref.Clock for USRP33
REF34	USRP34	RefIn	RF_coax	OCLK05	10MHzOut02	**OCLK05_10MHzOut02**	**USRP34_RefIn**	Ref.Clock for USRP34
REF35	USRP35	RefIn	RF_coax	OCLK05	10MHzOut03	**OCLK05_10MHzOut03**	**USRP35_RefIn**	Ref.Clock for USRP35
REF36	USRP36	RefIn	RF_coax	OCLK05	10MHzOut04	**OCLK05_10MHzOut04**	**USRP36_RefIn**	Ref.Clock for USRP36
REF37	USRP37	RefIn	RF_coax	OCLK05	10MHzOut05	**OCLK05_10MHzOut05**	**USRP37_RefIn**	Ref.Clock for USRP37
REF38	USRP38	RefIn	RF_coax	OCLK05	10MHzOut06	**OCLK05_10MHzOut06**	**USRP38_RefIn**	Ref.Clock for USRP38
REF39	USRP39	RefIn	RF_coax	OCLK05	10MHzOut07	**OCLK05_10MHzOut07**	**USRP39_RefIn**	Ref.Clock for USRP39
REF40	USRP40	RefIn	RF_coax	OCLK05	10MHzOut08	**OCLK05_10MHzOut08**	**USRP40_RefIn**	Ref.Clock for USRP40
REF41	USRP41	RefIn	RF_coax	OCLK06	10MHzOut01	**OCLK06_10MHzOut01**	**USRP41_RefIn**	Ref.Clock for USRP41
REF42	USRP42	RefIn	RF_coax	OCLK06	10MHzOut02	**OCLK06_10MHzOut02**	**USRP42_RefIn**	Ref.Clock for USRP42
REF43	USRP43	RefIn	RF_coax	OCLK06	10MHzOut03	**OCLK06_10MHzOut03**	**USRP43_RefIn**	Ref.Clock for USRP43
REF44	USRP44	RefIn	RF_coax	OCLK06	10MHzOut04	**OCLK06_10MHzOut04**	**USRP44_RefIn**	Ref.Clock for USRP44
REF45	USRP45	RefIn	RF_coax	OCLK06	10MHzOut05	**OCLK06_10MHzOut05**	**USRP45_RefIn**	Ref.Clock for USRP45
REF46	USRP46	RefIn	RF_coax	OCLK06	10MHzOut06	**OCLK06_10MHzOut06**	**USRP46_RefIn**	Ref.Clock for USRP46
REF47	USRP47	RefIn	RF_coax	OCLK06	10MHzOut07	**OCLK06_10MHzOut07**	**USRP47_RefIn**	Ref.Clock for USRP47
REF48	USRP48	RefIn	RF_coax	OCLK06	10MHzOut08	**OCLK06_10MHzOut08**	**USRP48_RefIn**	Ref.Clock for USRP48
REF49	USRP49	RefIn	RF_coax	OCLK07	10MHzOut01	**OCLK07_10MHzOut01**	**USRP49_RefIn**	Ref.Clock for USRP49
REF50	USRP50	RefIn	RF_coax	OCLK07	10MHzOut02	**OCLK07_10MHzOut02**	**USRP50_RefIn**	Ref.Clock for USRP50
REF51	USRP51	RefIn	RF_coax	OCLK07	10MHzOut03	**OCLK07_10MHzOut03**	**USRP51_RefIn**	Ref.Clock for USRP51
REF52	USRP52	RefIn	RF_coax	OCLK07	10MHzOut04	**OCLK07_10MHzOut04**	**USRP52_RefIn**	Ref.Clock for USRP52
REF53	USRP53	RefIn	RF_coax	OCLK07	10MHzOut05	**OCLK07_10MHzOut05**	**USRP53_RefIn**	Ref.Clock for USRP53
REF54	USRP54	RefIn	RF_coax	OCLK07	10MHzOut06	**OCLK07_10MHzOut06**	**USRP54_RefIn**	Ref.Clock for USRP54
REF55	USRP55	RefIn	RF_coax	OCLK07	10MHzOut07	**OCLK07_10MHzOut07**	**USRP55_RefIn**	Ref.Clock for USRP55
REF56	USRP56	RefIn	RF_coax	OCLK07	10MHzOut08	**OCLK07_10MHzOut08**	**USRP56_RefIn**	Ref.Clock for USRP56
REF57	USRP57	RefIn	RF_coax	OCLK08	10MHzOut01	**OCLK08_10MHzOut01**	**USRP57_RefIn**	Ref.Clock for USRP57
REF58	USRP58	RefIn	RF_coax	OCLK08	10MHzOut02	**OCLK08_10MHzOut02**	**USRP58_RefIn**	Ref.Clock for USRP58
REF59	USRP59	RefIn	RF_coax	OCLK08	10MHzOut03	**OCLK08_10MHzOut03**	**USRP59_RefIn**	Ref.Clock for USRP59
REF60	USRP60	RefIn	RF_coax	OCLK08	10MHzOut04	**OCLK08_10MHzOut04**	**USRP60_RefIn**	Ref.Clock for USRP60

REF61	USRP61	RefIn	RF_coax	OCLK08	10MHzOut05	**OCLK08_10MHzOut05**	**USRP61_RefIn**	Ref.Clock for USRP61
REF62	USRP62	RefIn	RF_coax	OCLK08	10MHzOut06	**OCLK08_10MHzOut06**	**USRP62_RefIn**	Ref.Clock for USRP62
REF63	USRP63	RefIn	RF_coax	OCLK08	10MHzOut07	**OCLK08_10MHzOut07**	**USRP63_RefIn**	Ref.Clock for USRP63
REF64	USRP64	RefIn	RF_coax	OCLK08	10MHzOut08	**OCLK08_10MHzOut08**	**USRP64_RefIn**	Ref.Clock for USRP64
C1REF	OCLKM1	10MHzOut01	RF_coax	OCLK01	Ext10MHzInput	**OCLK01_Ext10MHzInput**	**OCLKM1_10MHzOut 01**	Ref.Clock for OCLK01 from OCLKM1
C2REF	OCLKM1	10MHzOut02	RF_coax	OCLK02	Ext10MHzInput	**OCLK02_Ext10MHzInput**	**OCLKM1_10MHzOut 02**	Ref.Clock for OCLK02 from OCLKM1
C3REF	OCLKM1	10MHzOut03	RF_coax	OCLK03	Ext10MHzInput	**OCLK03_Ext10MHzInput**	**OCLKM1_10MHzOut 03**	Ref.Clock for OCLK03 from OCLKM1
C4REF	OCLKM1	10MHzOut04	RF_coax	OCLK04	Ext10MHzInput	**OCLK04_Ext10MHzInput**	**OCLKM1_10MHzOut 04**	Ref.Clock for OCLK04 from OCLKM1
C5REF	OCLKM1	10MHzOut05	RF_coax	OCLK05	Ext10MHzInput	**OCLK05_Ext10MHzInput**	**OCLKM1_10MHzOut 05**	Ref.Clock for OCLK05 from OCLKM1
C6REF	OCLKM1	10MHzOut06	RF_coax	OCLK06	Ext10MHzInput	**OCLK06_Ext10MHzInput**	**OCLKM1_10MHzOut 06**	Ref.Clock for OCLK06 from OCLKM1
C7REF	OCLKM1	10MHzOut07	RF_coax	OCLK07	Ext10MHzInput	**OCLK07_Ext10MHzInput**	**OCLKM1_10MHzOut 07**	Ref.Clock for OCLK07 from OCLKM1
C8REF	OCLKM1	10MHzOut08	RF_coax	OCLK08	Ext10MHzInput	**OCLK08_Ext10MHzInput**	**OCLKM1_10MHzOut 08**	Ref.Clock for OCLK08 from OCLKM1
CMREF	PXI01	sl10_CLKout	RF_coax	OCLKM1	Ext10MHzInput	**OCLKM1_Ext10MHzInput**	**PXI01_sl10_CLKout**	Ref.Clock for OCLKM1 from PXI01
PPS1	USRP01	PPSIn	RF_coax	OCLK01	PPSout01	**OCLK01_PPSout01**	**USRP01_PPSIn**	PPS for USRP01
PPS2	USRP02	PPSIn	RF_coax	OCLK01	PPSout02	**OCLK01_PPSout02**	**USRP02_PPSIn**	PPS for USRP02
PPS3	USRP03	PPSIn	RF_coax	OCLK01	PPSout03	**OCLK01_PPSout03**	**USRP03_PPSIn**	PPS for USRP03
PPS4	USRP04	PPSIn	RF_coax	OCLK01	PPSout04	**OCLK01_PPSout04**	**USRP04_PPSIn**	PPS for USRP04
PPS5	USRP05	PPSIn	RF_coax	OCLK01	PPSout05	**OCLK01_PPSout05**	**USRP05_PPSIn**	PPS for USRP05
PPS6	USRP06	PPSIn	RF_coax	OCLK01	PPSout06	**OCLK01_PPSout06**	**USRP06_PPSIn**	PPS for USRP06
PPS7	USRP07	PPSIn	RF_coax	OCLK01	PPSout07	**OCLK01_PPSout07**	**USRP07_PPSIn**	PPS for USRP07
PPS8	USRP08	PPSIn	RF_coax	OCLK01	PPSout08	**OCLK01_PPSout08**	**USRP08_PPSIn**	PPS for USRP08
PPS9	USRP09	PPSIn	RF_coax	OCLK02	PPSout01	**OCLK02_PPSout01**	**USRP09_PPSIn**	PPS for USRP09
PPS10	USRP10	PPSIn	RF_coax	OCLK02	PPSout02	**OCLK02_PPSout02**	**USRP10_PPSIn**	PPS for USRP10
PPS11	USRP11	PPSIn	RF_coax	OCLK02	PPSout03	**OCLK02_PPSout03**	**USRP11_PPSIn**	PPS for USRP11

PPS12	USRP12	PPSIn	RF_coax	OCLK02	PPSout04	**OCLK02_PPSout04**	**USRP12_PPSIn**	PPS for USRP12
PPS13	USRP13	PPSIn	RF_coax	OCLK02	PPSout05	**OCLK02_PPSout05**	**USRP13_PPSIn**	PPS for USRP13
PPS14	USRP14	PPSIn	RF_coax	OCLK02	PPSout06	**OCLK02_PPSout06**	**USRP14_PPSIn**	PPS for USRP14
PPS15	USRP15	PPSIn	RF_coax	OCLK02	PPSout07	**OCLK02_PPSout07**	**USRP15_PPSIn**	PPS for USRP15
PPS16	USRP16	PPSIn	RF_coax	OCLK02	PPSout08	**OCLK02_PPSout08**	**USRP16_PPSIn**	PPS for USRP16
PPS17	USRP17	PPSIn	RF_coax	OCLK03	PPSout01	**OCLK03_PPSout01**	**USRP17_PPSIn**	PPS for USRP17
PPS18	USRP18	PPSIn	RF_coax	OCLK03	PPSout02	**OCLK03_PPSout02**	**USRP18_PPSIn**	PPS for USRP18
PPS19	USRP19	PPSIn	RF_coax	OCLK03	PPSout03	**OCLK03_PPSout03**	**USRP19_PPSIn**	PPS for USRP19
PPS20	USRP20	PPSIn	RF_coax	OCLK03	PPSout04	**OCLK03_PPSout04**	**USRP20_PPSIn**	PPS for USRP20
PPS21	USRP21	PPSIn	RF_coax	OCLK03	PPSout05	**OCLK03_PPSout05**	**USRP21_PPSIn**	PPS for USRP21
PPS22	USRP22	PPSIn	RF_coax	OCLK03	PPSout06	**OCLK03_PPSout06**	**USRP22_PPSIn**	PPS for USRP22
PPS23	USRP23	PPSIn	RF_coax	OCLK03	PPSout07	**OCLK03_PPSout07**	**USRP23_PPSIn**	PPS for USRP23
PPS24	USRP24	PPSIn	RF_coax	OCLK03	PPSout08	**OCLK03_PPSout08**	**USRP24_PPSIn**	PPS for USRP24
PPS25	USRP25	PPSIn	RF_coax	OCLK04	PPSout01	**OCLK04_PPSout01**	**USRP25_PPSIn**	PPS for USRP25
PPS26	USRP26	PPSIn	RF_coax	OCLK04	PPSout02	**OCLK04_PPSout02**	**USRP26_PPSIn**	PPS for USRP26
PPS27	USRP27	PPSIn	RF_coax	OCLK04	PPSout03	**OCLK04_PPSout03**	**USRP27_PPSIn**	PPS for USRP27
PPS28	USRP28	PPSIn	RF_coax	OCLK04	PPSout04	**OCLK04_PPSout04**	**USRP28_PPSIn**	PPS for USRP28
PPS29	USRP29	PPSIn	RF_coax	OCLK04	PPSout05	**OCLK04_PPSout05**	**USRP29_PPSIn**	PPS for USRP29
PPS30	USRP30	PPSIn	RF_coax	OCLK04	PPSout06	**OCLK04_PPSout06**	**USRP30_PPSIn**	PPS for USRP30
PPS31	USRP31	PPSIn	RF_coax	OCLK04	PPSout07	**OCLK04_PPSout07**	**USRP31_PPSIn**	PPS for USRP31
PPS32	USRP32	PPSIn	RF_coax	OCLK04	PPSout08	**OCLK04_PPSout08**	**USRP32_PPSIn**	PPS for USRP32
PPS33	USRP33	PPSIn	RF_coax	OCLK05	PPSout01	**OCLK05_PPSout01**	**USRP33_PPSIn**	PPS for USRP33
PPS34	USRP34	PPSIn	RF_coax	OCLK05	PPSout02	**OCLK05_PPSout02**	**USRP34_PPSIn**	PPS for USRP34
PPS35	USRP35	PPSIn	RF_coax	OCLK05	PPSout03	**OCLK05_PPSout03**	**USRP35_PPSIn**	PPS for USRP35
PPS36	USRP36	PPSIn	RF_coax	OCLK05	PPSout04	**OCLK05_PPSout04**	**USRP36_PPSIn**	PPS for USRP36
PPS37	USRP37	PPSIn	RF_coax	OCLK05	PPSout05	**OCLK05_PPSout05**	**USRP37_PPSIn**	PPS for USRP37
PPS38	USRP38	PPSIn	RF_coax	OCLK05	PPSout06	**OCLK05_PPSout06**	**USRP38_PPSIn**	PPS for USRP38
PPS39	USRP39	PPSIn	RF_coax	OCLK05	PPSout07	**OCLK05_PPSout07**	**USRP39_PPSIn**	PPS for USRP39
PPS40	USRP40	PPSIn	RF_coax	OCLK05	PPSout08	**OCLK05_PPSout08**	**USRP40_PPSIn**	PPS for USRP40
PPS41	USRP41	PPSIn	RF_coax	OCLK06	PPSout01	**OCLK06_PPSout01**	**USRP41_PPSIn**	PPS for USRP41
PPS42	USRP42	PPSIn	RF_coax	OCLK06	PPSout02	**OCLK06_PPSout02**	**USRP42_PPSIn**	PPS for USRP42
PPS43	USRP43	PPSIn	RF_coax	OCLK06	PPSout03	**OCLK06_PPSout03**	**USRP43_PPSIn**	PPS for USRP43

PPS44	USRP44	PPSIn	RF_coax	OCLK06	PPSout04	**OCLK06_PPSout04**	**USRP44_PPSIn**	PPS for USRP44
PPS45	USRP45	PPSIn	RF_coax	OCLK06	PPSout05	**OCLK06_PPSout05**	**USRP45_PPSIn**	PPS for USRP45
PPS46	USRP46	PPSIn	RF_coax	OCLK06	PPSout06	**OCLK06_PPSout06**	**USRP46_PPSIn**	PPS for USRP46
PPS47	USRP47	PPSIn	RF_coax	OCLK06	PPSout07	**OCLK06_PPSout07**	**USRP47_PPSIn**	PPS for USRP47
PPS48	USRP48	PPSIn	RF_coax	OCLK06	PPSout08	**OCLK06_PPSout08**	**USRP48_PPSIn**	PPS for USRP48
PPS49	USRP49	PPSIn	RF_coax	OCLK07	PPSout01	**OCLK07_PPSout01**	**USRP49_PPSIn**	PPS for USRP49
PPS50	USRP50	PPSIn	RF_coax	OCLK07	PPSout02	**OCLK07_PPSout02**	**USRP50_PPSIn**	PPS for USRP50
PPS51	USRP51	PPSIn	RF_coax	OCLK07	PPSout03	**OCLK07_PPSout03**	**USRP51_PPSIn**	PPS for USRP51
PPS52	USRP52	PPSIn	RF_coax	OCLK07	PPSout04	**OCLK07_PPSout04**	**USRP52_PPSIn**	PPS for USRP52
PPS53	USRP53	PPSIn	RF_coax	OCLK07	PPSout05	**OCLK07_PPSout05**	**USRP53_PPSIn**	PPS for USRP53
PPS54	USRP54	PPSIn	RF_coax	OCLK07	PPSout06	**OCLK07_PPSout06**	**USRP54_PPSIn**	PPS for USRP54
PPS55	USRP55	PPSIn	RF_coax	OCLK07	PPSout07	**OCLK07_PPSout07**	**USRP55_PPSIn**	PPS for USRP55
PPS56	USRP56	PPSIn	RF_coax	OCLK07	PPSout08	**OCLK07_PPSout08**	**USRP56_PPSIn**	PPS for USRP56
PPS57	USRP57	PPSIn	RF_coax	OCLK08	PPSout01	**OCLK08_PPSout01**	**USRP57_PPSIn**	PPS for USRP57
PPS58	USRP58	PPSIn	RF_coax	OCLK08	PPSout02	**OCLK08_PPSout02**	**USRP58_PPSIn**	PPS for USRP58
PPS59	USRP59	PPSIn	RF_coax	OCLK08	PPSout03	**OCLK08_PPSout03**	**USRP59_PPSIn**	PPS for USRP59
PPS60	USRP60	PPSIn	RF_coax	OCLK08	PPSout04	**OCLK08_PPSout04**	**USRP60_PPSIn**	PPS for USRP60
PPS61	USRP61	PPSIn	RF_coax	OCLK08	PPSout05	**OCLK08_PPSout05**	**USRP61_PPSIn**	PPS for USRP61
PPS62	USRP62	PPSIn	RF_coax	OCLK08	PPSout06	**OCLK08_PPSout06**	**USRP62_PPSIn**	PPS for USRP62
PPS63	USRP63	PPSIn	RF_coax	OCLK08	PPSout07	**OCLK08_PPSout07**	**USRP63_PPSIn**	PPS for USRP63
PPS64	USRP64	PPSIn	RF_coax	OCLK08	PPSout08	**OCLK08_PPSout08**	**USRP64_PPSIn**	PPS for USRP64
C1PPS	OCLKM1	PPSout01	RF_coax	OCLK01	PPSin	**OCLK01_PPSin**	**OCLKM1_PPSout01**	PPS for OCLK01 from OCLKM1
C2PPS	OCLKM1	PPSout02	RF_coax	OCLK02	PPSin	**OCLK02_PPSin**	**OCLKM1_PPSout02**	PPS for OCLK02 from OCLKM1
C3PPS	OCLKM1	PPSout03	RF_coax	OCLK03	PPSin	**OCLK03_PPSin**	**OCLKM1_PPSout03**	PPS for OCLK03 from OCLKM1
C4PPS	OCLKM1	PPSout04	RF_coax	OCLK04	PPSin	**OCLK04_PPSin**	**OCLKM1_PPSout04**	PPS for OCLK04 from OCLKM1
C5PPS	OCLKM1	PPSout01	RF_coax	OCLK05	PPSin	**OCLK05_PPSin**	**OCLKM1_PPSout01**	PPS for OCLK05 from OCLKM1
C6PPS	OCLKM1	PPSout02	RF_coax	OCLK06	PPSin	**OCLK06_PPSin**	**OCLKM1_PPSout02**	PPS for OCLK06 from OCLKM1

C7PPS	OCLKM1	PPSout03	RF_coax	OCLK07	PPSin	**OCLK07_PPSin**	**OCLKM1_PPSout03**	PPS for OCLK07 from OCLKM1
C8PPS	OCLKM1	PPSout04	RF_coax	OCLK08	PPSin	**OCLK08_PPSin**	**OCLKM1_PPSout04**	PPS for OCLK08 from OCLKM1
CMPPS	PXI01	sl10_PFI3	RF_coax	OCLKM1	PPSin	**OCLKM1_PPSin**	**PXI01_sl10_PFI3**	PPS for OCLKM1 from PXI01
MTRIG	USRP01	TRIGout	RF_coax	PXI01	sl10_PFI1	**PXI01_sl10_PFI1**	**USRP01_TRIGout**	Master TRIG for PXI01 from USRP01
MXI1	USRP01	MXI01	MXI	CPS01	MXIx4_p01	**CPS01_MXIx4_p01**	**USRP01_MXI01**	MXI for USRP01
MXI2	USRP02	MXI01	MXI	CPS01	MXIx4_p02	**CPS01_MXIx4_p02**	**USRP02_MXI01**	MXI for USRP02
MXI3	USRP03	MXI01	MXI	CPS01	MXIx4_p03	**CPS01_MXIx4_p03**	**USRP03_MXI01**	MXI for USRP03
MXI4	USRP04	MXI01	MXI	CPS01	MXIx4_p04	**CPS01_MXIx4_p04**	**USRP04_MXI01**	MXI for USRP04
MXI5	USRP05	MXI01	MXI	CPS01	MXIx4_p05	**CPS01_MXIx4_p05**	**USRP05_MXI01**	MXI for USRP05
MXI6	USRP06	MXI01	MXI	CPS01	MXIx4_p06	**CPS01_MXIx4_p06**	**USRP06_MXI01**	MXI for USRP06
MXI7	USRP07	MXI01	MXI	CPS01	MXIx4_p07	**CPS01_MXIx4_p07**	**USRP07_MXI01**	MXI for USRP07
MXI8	USRP08	MXI01	MXI	CPS01	MXIx4_p08	**CPS01_MXIx4_p08**	**USRP08_MXI01**	MXI for USRP08
MXI9	USRP09	MXI01	MXI	CPS02	MXIx4_p01	**CPS02_MXIx4_p01**	**USRP09_MXI01**	MXI for USRP09
MXI10	USRP10	MXI01	MXI	CPS02	MXIx4_p02	**CPS02_MXIx4_p02**	**USRP10_MXI01**	MXI for USRP10
MXI11	USRP11	MXI01	MXI	CPS02	MXIx4_p03	**CPS02_MXIx4_p03**	**USRP11_MXI01**	MXI for USRP11
MXI12	USRP12	MXI01	MXI	CPS02	MXIx4_p04	**CPS02_MXIx4_p04**	**USRP12_MXI01**	MXI for USRP12
MXI13	USRP13	MXI01	MXI	CPS02	MXIx4_p05	**CPS02_MXIx4_p05**	**USRP13_MXI01**	MXI for USRP13
MXI14	USRP14	MXI01	MXI	CPS02	MXIx4_p06	**CPS02_MXIx4_p06**	**USRP14_MXI01**	MXI for USRP14
MXI15	USRP15	MXI01	MXI	CPS02	MXIx4_p07	**CPS02_MXIx4_p07**	**USRP15_MXI01**	MXI for USRP15
MXI16	USRP16	MXI01	MXI	CPS02	MXIx4_p08	**CPS02_MXIx4_p08**	**USRP16_MXI01**	MXI for USRP16
MXI17	USRP17	MXI01	MXI	CPS03	MXIx4_p01	**CPS03_MXIx4_p01**	**USRP17_MXI01**	MXI for USRP17
MXI18	USRP18	MXI01	MXI	CPS03	MXIx4_p02	**CPS03_MXIx4_p02**	**USRP18_MXI01**	MXI for USRP18
MXI19	USRP19	MXI01	MXI	CPS03	MXIx4_p03	**CPS03_MXIx4_p03**	**USRP19_MXI01**	MXI for USRP19
MXI20	USRP20	MXI01	MXI	CPS03	MXIx4_p04	**CPS03_MXIx4_p04**	**USRP20_MXI01**	MXI for USRP20
MXI21	USRP21	MXI01	MXI	CPS03	MXIx4_p05	**CPS03_MXIx4_p05**	**USRP21_MXI01**	MXI for USRP21
MXI22	USRP22	MXI01	MXI	CPS03	MXIx4_p06	**CPS03_MXIx4_p06**	**USRP22_MXI01**	MXI for USRP22
MXI23	USRP23	MXI01	MXI	CPS03	MXIx4_p07	**CPS03_MXIx4_p07**	**USRP23_MXI01**	MXI for USRP23
MXI24	USRP24	MXI01	MXI	CPS03	MXIx4_p08	**CPS03_MXIx4_p08**	**USRP24_MXI01**	MXI for USRP24

MXI25	USRP25	MXI01	MXI	CPS04	MXIx4_p01	**CPS04_MXIx4_p01**	**USRP25_MXI01**	MXI for USRP25
MXI26	USRP26	MXI01	MXI	CPS04	MXIx4_p02	**CPS04_MXIx4_p02**	**USRP26_MXI01**	MXI for USRP26
MXI27	USRP27	MXI01	MXI	CPS04	MXIx4_p03	**CPS04_MXIx4_p03**	**USRP27_MXI01**	MXI for USRP27
MXI28	USRP28	MXI01	MXI	CPS04	MXIx4_p04	**CPS04_MXIx4_p04**	**USRP28_MXI01**	MXI for USRP28
MXI29	USRP29	MXI01	MXI	CPS04	MXIx4_p05	**CPS04_MXIx4_p05**	**USRP29_MXI01**	MXI for USRP29
MXI30	USRP30	MXI01	MXI	CPS04	MXIx4_p06	**CPS04_MXIx4_p06**	**USRP30_MXI01**	MXI for USRP30
MXI31	USRP31	MXI01	MXI	CPS04	MXIx4_p07	**CPS04_MXIx4_p07**	**USRP31_MXI01**	MXI for USRP31
MXI32	USRP32	MXI01	MXI	CPS04	MXIx4_p08	**CPS04_MXIx4_p08**	**USRP32_MXI01**	MXI for USRP32
MXI33	USRP33	MXI01	MXI	CPS05	MXIx4_p01	**CPS05_MXIx4_p01**	**USRP33_MXI01**	MXI for USRP33
MXI34	USRP34	MXI01	MXI	CPS05	MXIx4_p02	**CPS05_MXIx4_p02**	**USRP34_MXI01**	MXI for USRP34
MXI35	USRP35	MXI01	MXI	CPS05	MXIx4_p03	**CPS05_MXIx4_p03**	**USRP35_MXI01**	MXI for USRP35
MXI36	USRP36	MXI01	MXI	CPS05	MXIx4_p04	**CPS05_MXIx4_p04**	**USRP36_MXI01**	MXI for USRP36
MXI37	USRP37	MXI01	MXI	CPS05	MXIx4_p05	**CPS05_MXIx4_p05**	**USRP37_MXI01**	MXI for USRP37
MXI38	USRP38	MXI01	MXI	CPS05	MXIx4_p06	**CPS05_MXIx4_p06**	**USRP38_MXI01**	MXI for USRP38
MXI39	USRP39	MXI01	MXI	CPS05	MXIx4_p07	**CPS05_MXIx4_p07**	**USRP39_MXI01**	MXI for USRP39
MXI40	USRP40	MXI01	MXI	CPS05	MXIx4_p08	**CPS05_MXIx4_p08**	**USRP40_MXI01**	MXI for USRP40
MXI41	USRP41	MXI01	MXI	CPS06	MXIx4_p01	**CPS06_MXIx4_p01**	**USRP41_MXI01**	MXI for USRP41
MXI42	USRP42	MXI01	MXI	CPS06	MXIx4_p02	**CPS06_MXIx4_p02**	**USRP42_MXI01**	MXI for USRP42
MXI43	USRP43	MXI01	MXI	CPS06	MXIx4_p03	**CPS06_MXIx4_p03**	**USRP43_MXI01**	MXI for USRP43
MXI44	USRP44	MXI01	MXI	CPS06	MXIx4_p04	**CPS06_MXIx4_p04**	**USRP44_MXI01**	MXI for USRP44
MXI45	USRP45	MXI01	MXI	CPS06	MXIx4_p05	**CPS06_MXIx4_p05**	**USRP45_MXI01**	MXI for USRP45
MXI46	USRP46	MXI01	MXI	CPS06	MXIx4_p06	**CPS06_MXIx4_p06**	**USRP46_MXI01**	MXI for USRP46
MXI47	USRP47	MXI01	MXI	CPS06	MXIx4_p07	**CPS06_MXIx4_p07**	**USRP47_MXI01**	MXI for USRP47
MXI48	USRP48	MXI01	MXI	CPS06	MXIx4_p08	**CPS06_MXIx4_p08**	**USRP48_MXI01**	MXI for USRP48
MXI49	USRP49	MXI01	MXI	CPS07	MXIx4_p01	**CPS07_MXIx4_p01**	**USRP49_MXI01**	MXI for USRP49
MXI50	USRP50	MXI01	MXI	CPS07	MXIx4_p02	**CPS07_MXIx4_p02**	**USRP50_MXI01**	MXI for USRP50
MXI51	USRP51	MXI01	MXI	CPS07	MXIx4_p03	**CPS07_MXIx4_p03**	**USRP51_MXI01**	MXI for USRP51
MXI52	USRP52	MXI01	MXI	CPS07	MXIx4_p04	**CPS07_MXIx4_p04**	**USRP52_MXI01**	MXI for USRP52
MXI53	USRP53	MXI01	MXI	CPS07	MXIx4_p05	**CPS07_MXIx4_p05**	**USRP53_MXI01**	MXI for USRP53
MXI54	USRP54	MXI01	MXI	CPS07	MXIx4_p06	**CPS07_MXIx4_p06**	**USRP54_MXI01**	MXI for USRP54
MXI55	USRP55	MXI01	MXI	CPS07	MXIx4_p07	**CPS07_MXIx4_p07**	**USRP55_MXI01**	MXI for USRP55
MXI56	USRP56	MXI01	MXI	CPS07	MXIx4_p08	**CPS07_MXIx4_p08**	**USRP56_MXI01**	MXI for USRP56

MXI57	USRP57	MXI01	MXI	CPS08	MXIx4_p01	**CPS08_MXIx4_p01**	**USRP57_MXI01**	MXI for USRP57
MXI58	USRP58	MXI01	MXI	CPS08	MXIx4_p02	**CPS08_MXIx4_p02**	**USRP58_MXI01**	MXI for USRP58
MXI59	USRP59	MXI01	MXI	CPS08	MXIx4_p03	**CPS08_MXIx4_p03**	**USRP59_MXI01**	MXI for USRP59
MXI60	USRP60	MXI01	MXI	CPS08	MXIx4_p04	**CPS08_MXIx4_p04**	**USRP60_MXI01**	MXI for USRP60
MXI61	USRP61	MXI01	MXI	CPS08	MXIx4_p05	**CPS08_MXIx4_p05**	**USRP61_MXI01**	MXI for USRP61
MXI62	USRP62	MXI01	MXI	CPS08	MXIx4_p06	**CPS08_MXIx4_p06**	**USRP62_MXI01**	MXI for USRP62
MXI63	USRP63	MXI01	MXI	CPS08	MXIx4_p07	**CPS08_MXIx4_p07**	**USRP63_MXI01**	MXI for USRP63
MXI64	USRP64	MXI01	MXI	CPS08	MXIx4_p08	**CPS08_MXIx4_p08**	**USRP64_MXI01**	MXI for USRP64
C1MXI	PXI01	sl02_MXI1	MXI	CPS01	MXIx8	**CPS01_MXIx8**	**PXI01_sl02_MXI1**	MXI for CPS01 from PXI01
C2MXI	PXI01	sl03_MXI1	MXI	CPS02	MXIx8	**CPS02_MXIx8**	**PXI01_sl03_MXI1**	MXI for CPS02 from PXI01
C3MXI	PXI01	sl04_MXI1	MXI	CPS03	MXIx8	**CPS03_MXIx8**	**PXI01_sl04_MXI1**	MXI for CPS03 from PXI01
C4MXI	PXI01	sl05_MXI1	MXI	CPS04	MXIx8	**CPS04_MXIx8**	**PXI01_sl05_MXI1**	MXI for CPS04 from PXI01
C5MXI	PXI01	sl15_MXI1	MXI	CPS05	MXIx8	**CPS05_MXIx8**	**PXI01_sl15_MXI1**	MXI for CPS05 from PXI01
C6MXI	PXI01	sl16_MXI1	MXI	CPS06	MXIx8	**CPS06_MXIx8**	**PXI01_sl16_MXI1**	MXI for CPS06 from PXI01
C7MXI	PXI01	sl17_MXI1	MXI	CPS07	MXIx8	**CPS07_MXIx8**	**PXI01_sl17_MXI1**	MXI for CPS07 from PXI01
C8MXI	PXI01	sl18_MXI1	MXI	CPS08	MXIx8	**CPS08_MXIx8**	**PXI01_sl18_MXI1**	MXI for CPS08 from PXI01

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