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Getting Results with the NI 5752R

This document explains how to install and configure an NI FlexRIO™ FPGA module (NI PXI/PXIe-79*xx*R) and an NI FlexRIO adapter module (NI 5752) to form the NI 5752R. This document also contains tutorial sections that demonstrate how to acquire samples using a LabVIEW FPGA example VI and how to create and run your own LabVIEW project.

The form factor of the FPGA module (PXI or PXI Express) determines the form factor of the combined NI 5752R module, as shown in Figure 1.

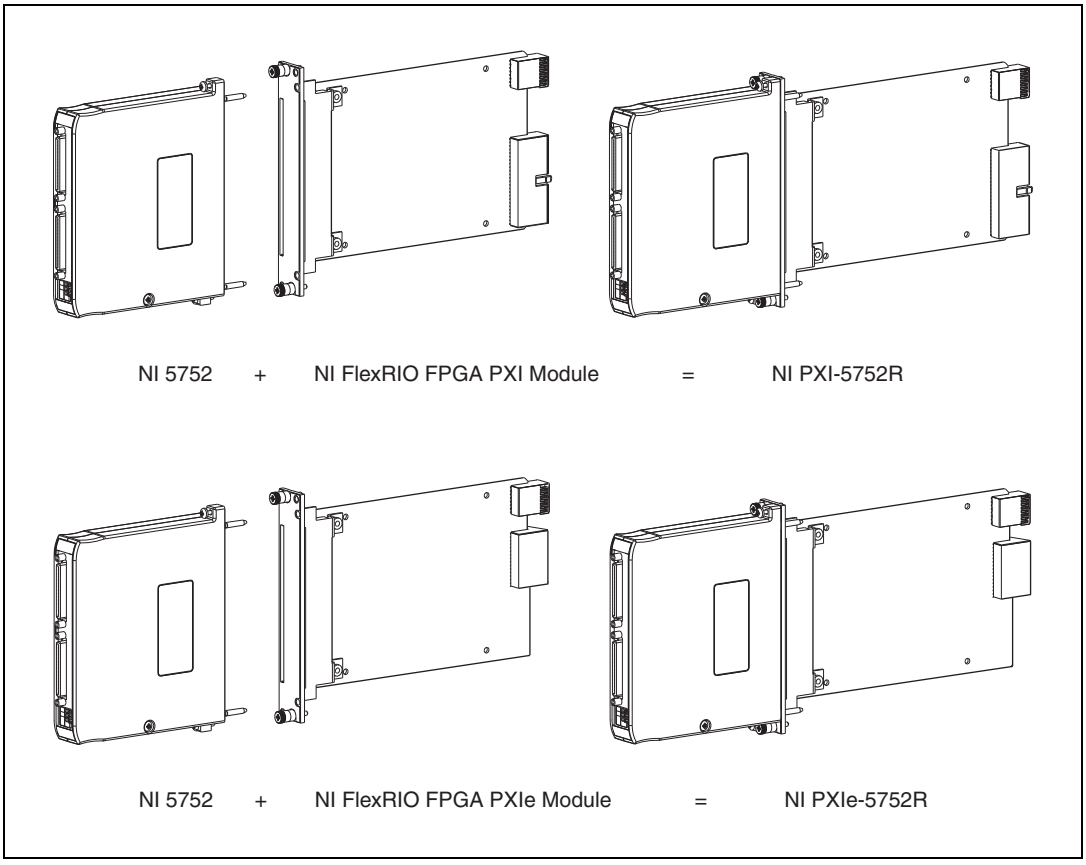


Figure 1. FPGA Module and NI 5752 Adapter Module

Required Components

The following items are required to set up and use the NI 5752R:

- ❑ The hardware kit containing the following items:
  - NI PXI/PXIe-79*xx*R FlexRIO FPGA module
  - NI FlexRIO adapter module (NI 5752)
- ❑ The following software packages:
  - LabVIEW
  - LabVIEW FPGA Module
  - NI-RIO device drivers
  - NI FlexRIO Adapter Module Support CD or the document *Downloading the NI FlexRIO Adapter Module Software Note to Users*
  - (Optional) LabVIEW Real-Time Module

  Refer to *Step 1. Install the Application Software and Instrument Driver*, for information about NI FlexRIO software support.
- ❑ One of the following systems:
  - PXI/CompactPCI or PXI Express/CompactPCI Express chassis with a PXI/CompactPCI or a PXI Express/CompactPCI Express embedded controller
  - MXI kit and a PC, running one of the following operating systems:
    - Windows Vista/2000
    - Windows XP Pro x32 Service Pack 1 or 2
    - Windows 7
- ❑ At least one cable for connecting signals to the NI 5752R. Refer to the *Connectivity Options* section for more information about cables.

Step 1. Install the Application Software and Instrument Driver

Before installing the NI 5752, you must install the application software and device driver. Visit `ni.com/info` and enter `rdsoftwareversion` as the Info Code to determine which minimum software versions you need for your device. Install the software in the following order:

1. **LabVIEW**—Refer to the *LabVIEW Release Notes* for installation instructions for LabVIEW and system requirements for the LabVIEW software. Refer to the *LabVIEW Upgrade Notes* for additional information about upgrading to the most recent version of LabVIEW for Windows.

   Documentation for LabVIEW is available by selecting **Start»All Programs»National Instruments»LabVIEW»LabVIEW Manuals**.
2. **LabVIEW FPGA Module**—Refer to the *LabVIEW FPGA Module Release and Upgrade Notes* for installation instructions and information about getting started with the LabVIEW FPGA Module.

   Documentation for the LabVIEW FPGA Module is available by selecting **Start»All Programs»National Instruments»LabVIEW»LabVIEW Manuals**.
3. **LabVIEW Real-Time Module (optional)**—Refer to the *LabVIEW Real-Time Module Release and Upgrade Notes* for system requirements, installation instructions, and additional information about using the LabVIEW Real-Time Module.

4. **NI-RIO**—Refer to the *NI-RIO Readme* on the NI-RIO installation media for system requirements and installation instructions for the NI-RIO driver.

   Documentation for the NI-RIO driver software is available by selecting **Start»All Programs» National Instruments»NI-RIO**.

5. **NI FlexRIO Adapter Module Support**—Refer to the *NI FlexRIO Adapter Module Support Readme* on the NI FlexRIO Adapter Module Support installation media for system requirements and installation instructions.

The LabVIEW documents are available from `ni.com/manuals`. You can also view the LabVIEW Manuals directory that contains these documents by selecting **Start»All Programs»National Instruments»LabVIEW»LabVIEW Manuals**.

Step 2. Install the Hardware

This section describes how to unpack and install the NI FlexRIO FPGA module and the NI 5752.

Note You must install LabVIEW, the LabVIEW FPGA Module, NI-RIO, and NI FlexRIO Adapter Module Support before installing the hardware.

Unpacking

The NI FlexRIO FPGA module and the NI 5752 adapter module are shipped in antistatic packages to prevent electrostatic discharge from damaging device components. To prevent such damage when handling the device, take the following precautions:

- Ground yourself using a grounding strap or by holding a grounded object, such as your computer chassis.
- Touch the antistatic package to a metal part of the computer chassis before removing the device from the package.

Caution *Never* touch the exposed pins of connectors.

Remove the device from the package and inspect it for loose components or any other sign of damage. Notify NI if the device appears damaged in any way. Do *not* install a damaged device into the chassis.

Store the NI FlexRIO FPGA module and NI 5752 adapter module in the antistatic envelopes when not in use.

Installing the NI FlexRIO FPGA Module

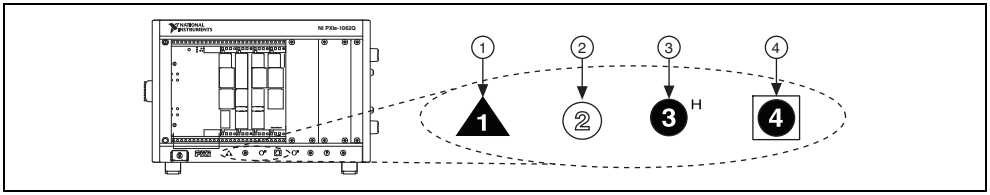
Complete the following steps to install an NI FlexRIO FPGA module:

Note You must install the software before installing the hardware. For software installation information, refer to *Step 1. Install the Application Software and Instrument Driver*.

Caution Refer to the *Read Me First: Safety and Electromagnetic Compatibility* document packaged with your PXI chassis or device before removing equipment covers or connecting or disconnecting any signal wires.

1. Power off and unplug the PXI/PXI Express chassis. Refer to your chassis manual to install or configure the chassis.

2. Identify a supported PXI/PXI Express slot in the chassis. Figure 2 shows the symbols that indicate the slot types for a PXI/PXI Express chassis.

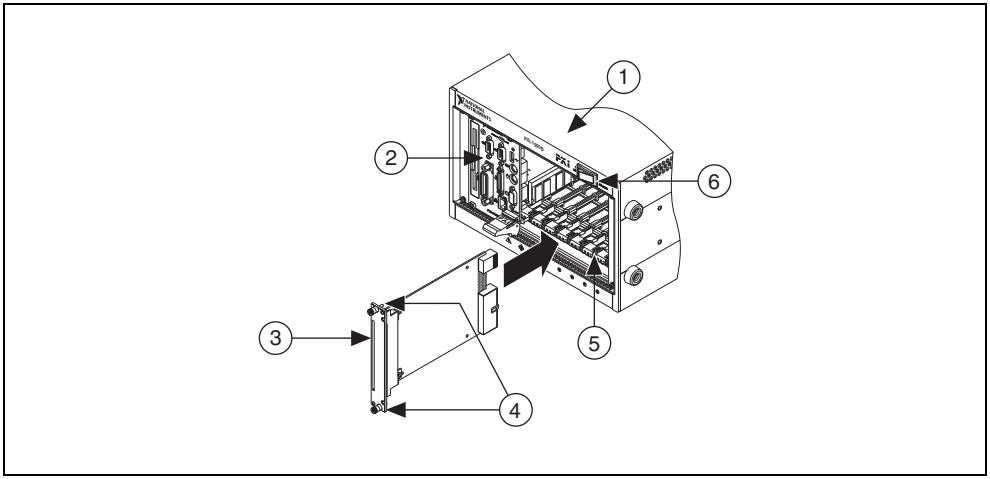


1	PXI Express System Controller Slot	3	PXI Express Hybrid Peripheral Slot
2	PXI Peripheral Slot	4	PXI Express System Timing Slot

Figure 2. Symbols for PXI Express/PXI Express Hybrid/PXI Slots

If you are using a PXI Express chassis, you can place PXI devices in the PXI slots. If a PXI device is hybrid slot compatible, you can use the PXI Express Hybrid slots. PXI Express devices can be placed only in PXI Express slots and PXI Express Hybrid slots. Refer to the chassis documentation for details.

3. Remove the filler panel of an unused PXI/PXI Express slot.
4. Touch any metal part of the chassis to discharge any static electricity.
5. Place the PXI/PXI Express module edges into the module guides at the top and bottom of the chassis and slide the module into the chassis until the module is fully inserted, as shown in Figure 3.



1	PXI/PXI Express Chassis	4	Front-Panel Mounting Screws
2	PXI/PXI Express System Controller	5	Module Guides
3	NI FlexRIO FPGA Module (PXI shown)	6	Power Switch

Figure 3. Installing an NI FlexRIO FPGA Module in a PXI/PXI Express Chassis

6. Secure the device front panel to the chassis front panel mounting rail using the front-panel mounting screws.
7. Plug in and power on the PXI/PXI Express chassis.

Confirming That the Device Is Recognized

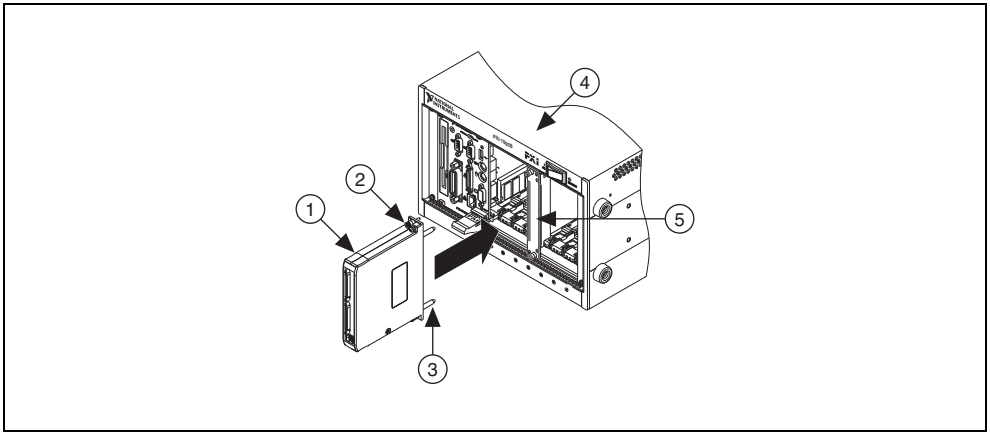
To confirm that the NI FlexRIO FPGA module is recognized, complete the following steps.

1. Select **Start»All Programs»National Instruments»Measurement & Automation** to open Measurement & Automation Explorer (MAX).
2. Expand **Devices and Interfaces**.
3. Verify that the device appears under **Devices and Interfaces»RIO Devices**.

Installing the NI 5752

Complete the following steps to connect the NI 5752 adapter module to the NI FlexRIO FPGA module.

1. Gently insert the guide pins and the high-density card edge of the NI 5752 into the corresponding connectors of the NI FlexRIO FPGA module, as shown in Figure 4. The connection may be tight, but do *not* force the adapter module into place.



1	NI FlexRIO Adapter Module (NI 5752)	4	PXI Chassis
2	Captive Screw	5	NI FlexRIO FPGA Module
3	Guide Pin		

Figure 4. Installing the NI 5752

2. Tighten the captive screws on the adapter module to secure it to the NI FlexRIO FPGA module.

Step 3. Connect Signals

Refer to the *NI 5752 Specifications* document for descriptions of the connectors on your adapter module and for information about connecting I/O signals.

Connectivity Options

NI recommends using the following cables with the NI 5752.

Signal	Cable Description	Part Number
Analog	SHC68-C68-D3	188143B-01
Digital	SHC68-C68-D4	196275A-01

These cables connect directly to the analog and digital connectors on the NI 5752.

Caution Connections that exceed any of the maximum ratings of input or output signals on the adapter module can damage the device and the chassis. NI is *not* liable for any damage resulting from such signal connections. For the maximum input and output ratings for each signal, refer to the *NI 5752 Specifications*, available from `ni.com/manuals`.

Step 4. Use Your Hardware with a LabVIEW FPGA Example VI

The NI FlexRIO Adapter Module Support installation includes a variety of example projects to help get you started. This section demonstrates how to use an existing LabVIEW FPGA example project to generate or acquire samples with your hardware.

Note Examples available for your device are dependent on the device-specific minimum software requirements. For more information about software requirements for your device, refer to *Step 1. Install the Application Software and Instrument Driver*.

Each example project includes the following components:

- A LabVIEW FPGA VI that can be compiled and run embedded in FPGA hardware
- A Host VI that runs in LabVIEW for Windows and interacts with the LabVIEW FPGA VI

Note In software, NI FlexRIO adapter modules are referred to as *IO Modules*.

Complete the following steps to run an example that acquires a waveform on an analog input channel:

1. Connect one end of an SHC68-C68-D3 cable to the analog input connector on the NI 5752.
2. Launch LabVIEW.
3. In the **Getting Started** window, click **Find Examples** to display the NI Example Finder.
4. In the **NI Example Finder** window, select **Hardware Input and Output»FlexRIO»IO Modules» NI 5752**. This directory holds several example projects designed to help you get started using the NI 5752R.
5. Select **NI 5752 Finite Acquisition with External Clock.lvproj**.
6. In the **Project Explorer** window, double-click **NI 5752 Finite Acquisition with External Clock (Host).vi** under My Computer to open the host VI. The VI uses the NI PXI-7952R as the FPGA target by default. If you are not using an NI PXI-7952R, complete the following steps to change to an FPGA VI that supports your target.

Note All example projects are configured for RIO0. If your device is not RIO0, you must update the target device name by right-clicking your device in the **Project Explorer** window, selecting **Properties**, and entering the correct target device name in the Resource text box. You can find your target device name in MAX by following the steps listed in the *Confirming That the Device Is Recognized* section.

   a. Select **Window»Show Block Diagram** to open the VI block diagram.
   b. On the block diagram, right-click the **Open FPGA** icon (NI PXI-7952R) and select **Configure Open FPGA VI Reference**.
   c. In the **Configure Open FPGA VI Reference** window, click the **Select Bitfile** button in the Open Bitfile section.
   d. Select the appropriate bitfile for your target device in the FPGA Bitfiles folder under the example directory. FPGA bitfiles are named by the compiler with the format `<Project Name>_<Target Name>_<VI Name>.vi.lvbitx`.
   e. Click **OK** in the **Configure Open FPGA VI Reference** window.
   f. Save the VI.

7. On the front panel, enter appropriate values in the **Num Samples** box. Leave the **Sample Clk Source** set to `50 MHz Internal`.
8. Click the **Run** button to run the VI and acquire data from the selected analog input channel.

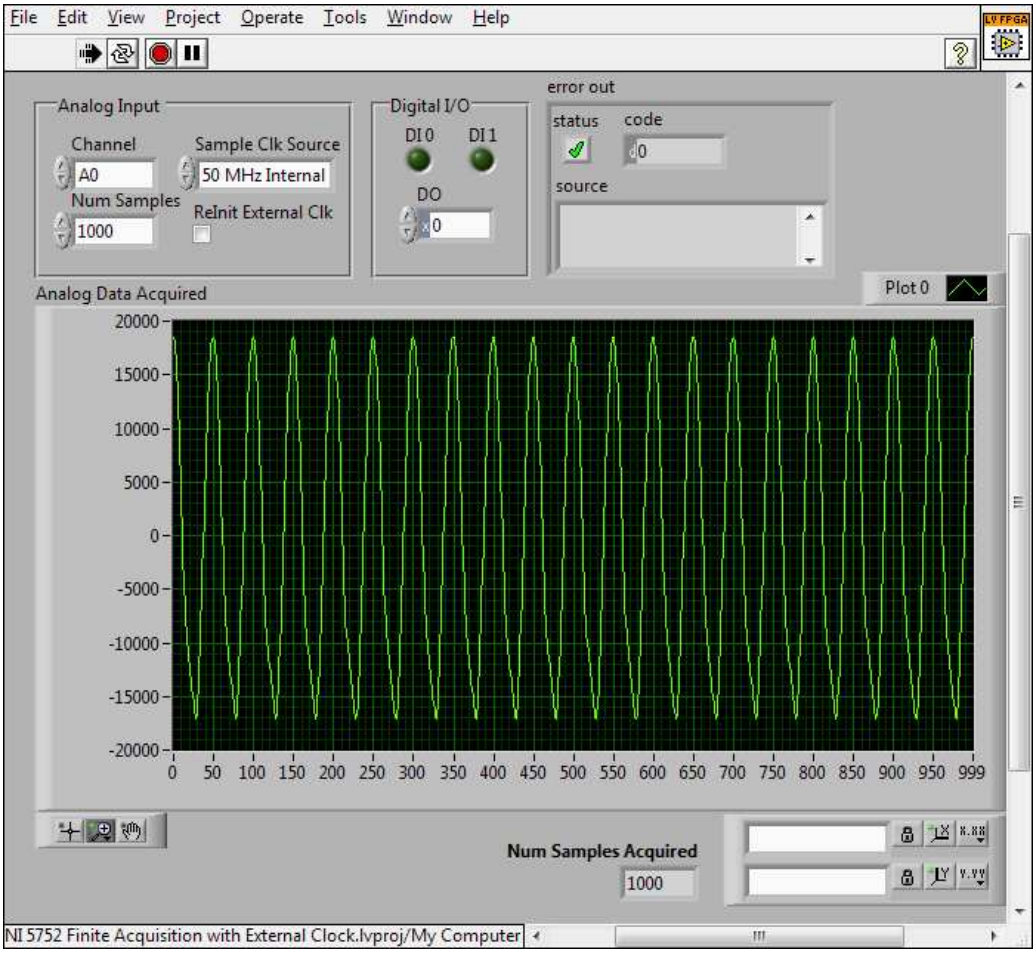


Figure 5. NI 5752 Finite Acquisition with External Clock (Host) VI Front Panel

9. Close the VI.

Step 5. Create a LabVIEW Project and Run a VI on an FPGA Target

This section demonstrates how to create a LabVIEW project, FPGA VI, and host VI that reads the analog and digital inputs and writes to the digital outputs of the NI 5752. This exercise also demonstrates how to compile the FPGA VI onto your target and run a VI on the host machine.

Creating a Project

1. Launch LabVIEW, or if LabVIEW is already running, select **File»New**.
2. In the **New** dialog box, select **Project»Empty Project**. Click **OK**. The new project opens in the **Project Explorer** window.
3. Save the project as `5752 RW.lvproj`.

Creating an FPGA Target VI

1. In the **Project Explorer** window, right-click **My Computer** and select **New»Targets and Devices**.
2. In the **Add Targets and Devices on My Computer** dialog box, select the **Existing Target or Device** radio button and expand the **FPGA Target**. The target is displayed.
3. Select your device and click **OK**. The target and target properties are loaded into the project tree.
4. In the **Project Explorer** window, expand **FPGA Target (RIOx, NI 79xxR)**.
5. Right-click **FPGA Target (RIOx, NI 79xxR)** and select **New»FPGA Base Clock**. In the General category, select **200 MHz Clock** as the Resource and click **OK**. The 200 MHz Clock is now added to the project. The 200 MHz Clock is required to configure the CLIP for the NI 5752.
6. Right-click **IO Module** and select **Properties**. In the General category, you can see the available CLIP for the device in the Component Level IP pane. If the category information is dimmed, select the **Enable IO Module** checkbox.
7. Select **NI 5752 IO Module**.
8. In the Clock Selections category, select the **40 MHz Onboard Clock** for CLIP Clock40 and the **200 MHz Clock** for CLIP Clock200. Click **OK**.

Note For more information about CLIP (component-level intellectual property) for your device, refer to the *Component-Level Intellectual Property* section.

9. Right-click **FPGA Target (RIOx, NI 79xxR)** and select **New»FPGA Base Clock**. In the General category, select **IO Module Clock0** as the resource and click **OK**. **IO Module Clock0** is now added to the project.
10. In the **Project Explorer** window, right-click the FPGA target and select **New»VI**. A blank VI opens. Select **Window»Show Block Diagram**.
11. In the **Project Explorer** window, expand the **IO Module (NI 5752: NI 5752 IO Module)** tree view.
12. Select **AI, A0**, **DI 0**, and **DO 0** and drag them onto the block diagram.
13. Add a Timed Loop around the three, as shown in Figure 6.
14. Wire an indicator from the output terminal of the **IO Module\AI A0** node.
15. Wire an indicator from the output of the **IO Module\DI 0** node.
16. Wire a control to the write input of the **IO Module\DO** node.
17. Wire **IO Module Clock0** to the source name input node of the Timed Loop.

18. Add a Flat Sequence Structure around the Timed Loop, as shown in Figure 6.
19. Right click on the Flat Sequence Structure and select **Add Frame Before** to add another frame.
20. Under the IO Module tree view, select **InitDone** and drag it into the new sequence frame.
21. Wire an indicator from the output terminal of the **IO Module\InitDone** node.
22. Add a While Loop around the I/O Node and wire the output terminal of **IO Module\InitDone** to the stop condition of the loop. This loop ensures that the CLIP is initialized before the adapter module I/O is written or read.

Your block diagram should now resemble the block diagram in Figure 6.

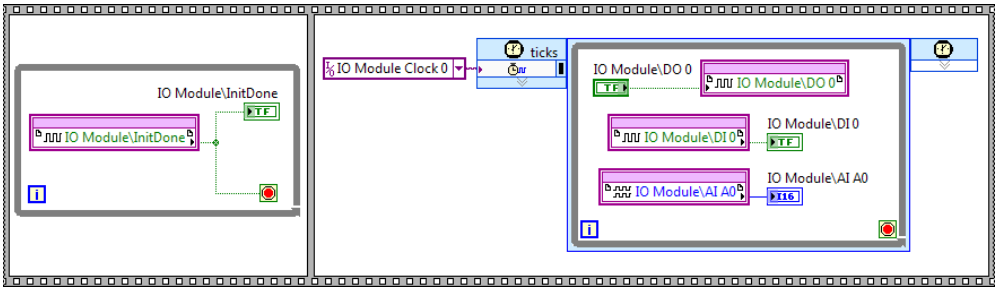


Figure 6. 5752 RW (FPGA).vi Block Diagram

Tip Click the **Clean Up Diagram** button on the toolbar to clean up VI block diagrams.

23. Save the VI as `5752 RW (FPGA).vi`.
24. Close the VI.
25. In the **Project Explorer** window under **My Computer**, expand the tree view for your device, right-click **5752 RW (FPGA).vi** and select **Compile** to compile the files for your target. The **Generating Intermediate Files** window opens and displays the compilation progress. The **LabVIEW FPGA Compile Server** window opens and runs.

Note The compilation takes several minutes to complete.

26. When the compilation finishes, click the **Stop Server** button.
27. Click **OK** in the **Successful Compile Report** window. Close the VI without saving changes.

Creating a Host VI

1. In the **Project Explorer** window, right-click **My Computer** and select **New»VI**. A blank VI opens. Select **Window»Show Block Diagram**.
2. Add the Open FPGA VI Reference function, located on the **FPGA Interface** palette, to the block diagram.
3. Right-click the Open FPGA VI Reference function labeled `No Target` and select **Configure Open FPGA VI Reference**.
4. In the **Configure Open FPGA VI Reference** dialog box, click the **VI** button.
5. In the **Select VI** window that opens, select **5752 RW (FPGA).vi** under your device, and click **OK**.
6. Click **OK** in the **Configure Open FPGA VI Reference** dialog box. The new target name appears under the Open FPGA VI Reference function in the block diagram.
7. Add a While Loop to the block diagram and delete the stop control.
8. Add a Read/Write Control, located on the FPGA Interface function palette, inside the While Loop.

9. Wire in the FPGA VI Reference and the error cluster from the Open FPGA VI Reference VI.
10. Click the **Unselected** node of Read/Write Control and select **IO Module\InitDone**.
11. Wire the output of **IO Module\InitDone** to the stop condition of the loop. This loop ensures that the CLIP is initialized before I/O is written or read in a dependent clock domain.
12. Add a While Loop to the block diagram with a control on the loop condition, as shown in Figure 7.
13. Add the Read/Write Control function, located on the **FPGA Interface** palette, inside the While Loop.
14. Wire in the FPGA VI Reference and the error cluster from the first Read/Write Control.
15. Click the **Unselected** node of Read/Write Control function and select **IO Module\AI A0**.
16. Wire an indicator to the **IO Module\AI A0** output terminal.
17. Expand the bottom of the Read/Write Control function to expose another node. Click the new node and select **IO Module\DI 0**.
18. Wire an indicator from the **IO Module\DI 0** output terminal.
19. Expand the bottom of the Read/Write Control to expose another node. Click the new node and select **IO Module\DO 0**.
20. Wire a control to the **IO Module\DO** input terminal.
21. Add the Close FPGA VI Reference VI function, located on the FPGA Interface palette, outside the While Loop.
22. Wire in the FPGA VI Reference and the error cluster from the second Read/Write Control function.
23. Wire an error indicator to the error out output of the Close FPGA VI Reference VI.

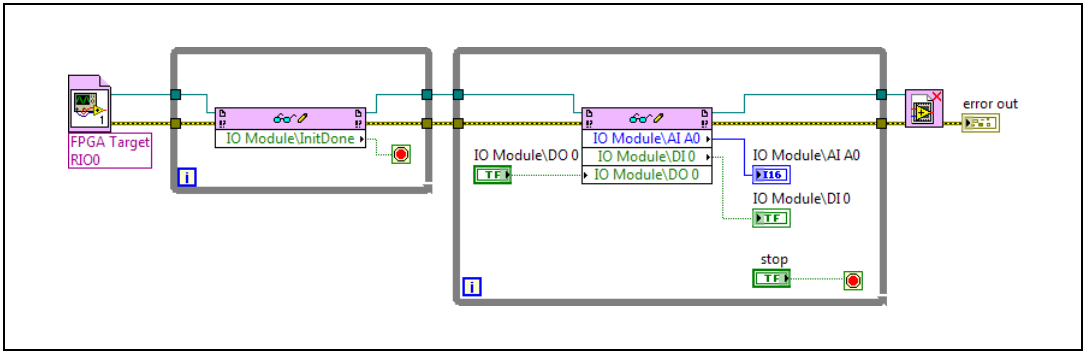


Figure 7. 5752 RW (Host).vi Block Diagram

24. Save the VI as `5752 RW (Host).vi`.

Running the Host VI

1. Open the front panel of `5752 RW (Host).vi`.
2. Click the **Run** button to run the VI.
3. Enter a number into the **IO Module\DO 0** control to send different values to the digital outputs. The values of **IO Module\AI A0** and **IO Module\DI 0** reflect the values being driven on those lines.
4. Click the **STOP** button on the front panel and close the VI.

Component-Level Intellectual Property

The LabVIEW FPGA Module includes a feature for HDL IP integration called component-level intellectual property (CLIP).

NI FlexRIO devices support two types of CLIP: user-defined and socketed.

- User-defined CLIP allows users to insert HDL IP into an FPGA target, enabling VHDL code to communicate directly with an FPGA VI.
- Socketed CLIP provides the same IP integration functionality of the user-defined CLIP while also allowing the CLIP to communicate directly with circuitry external to the FPGA. Adapter module socketed CLIP allows your IP to communicate directly with both the FPGA VI and the external adapter module connector interface.

Figure 8 shows the relationship between an FPGA VI and CLIP.

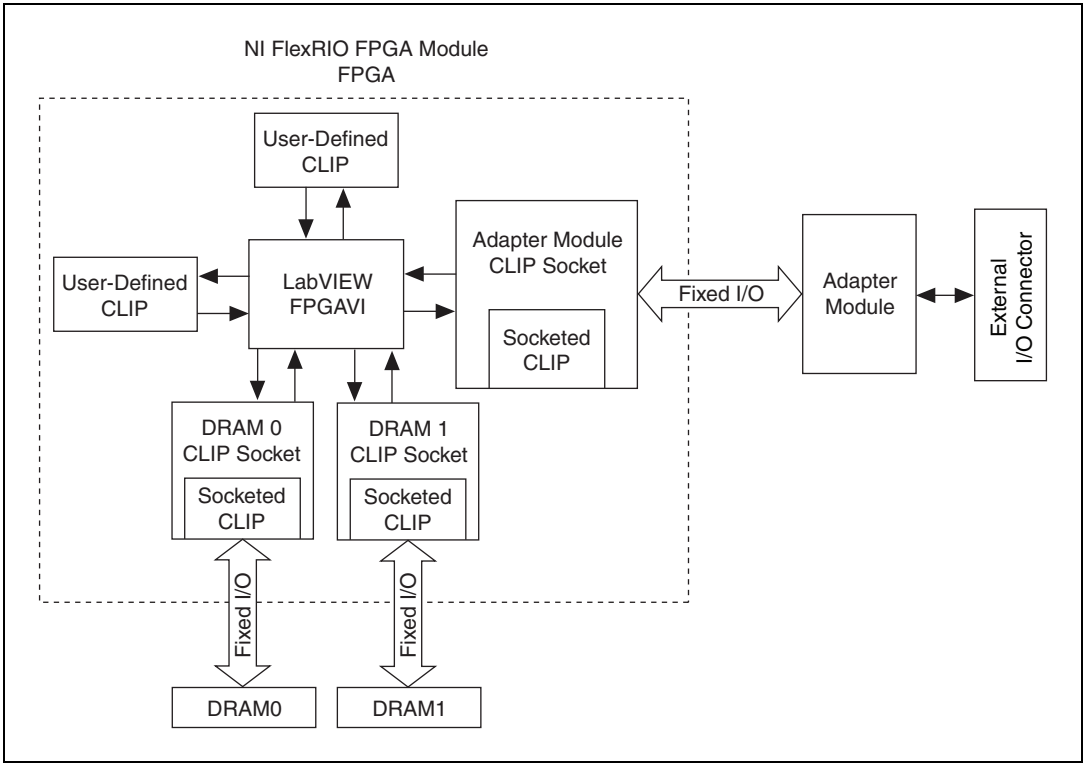


Figure 8. CLIP Relationship

The NI 5752 ships with socketed CLIP that is used to add module I/O to the LabVIEW project. The NI 5752 IO Module provides read/write access to all analog inputs (AI), digital inputs (DI), and digital outputs (DO).

Refer to the *NI FlexRIO Adapter Module Support Help* topic of the *LabVIEW Help* for information regarding NI FlexRIO CLIP items, configuring the NI 5752 with socketed CLIP, and a list of available socketed CLIP items and provided signals.

Where to Go From Here

The following resources contain information for writing applications and taking measurements with your hardware.

Software Documentation

- LabVIEW FPGA documentation:
  - *Getting Started with LabVIEW FPGA 8.x*—This KnowledgeBase, available at `ni.com/kb`, provides links to the top resources that can be used to assist in getting started with programming in LabVIEW FPGA.
  - *FPGA Module* book in the *LabVIEW Help*—Select **Help»Search the LabVIEW Help** in LabVIEW to view the *LabVIEW Help*. Browse the FPGA Module book in the Contents tab for information about how to use the FPGA Module to create VIs that run on the NI 5752R.
  - *LabVIEW FPGA Module Release and Upgrade Notes*—Contains information about installing the LabVIEW FPGA Module, describes new features, and provides upgrade information. To access this document, refer to `ni.com/manuals`. In LabVIEW 8.0 or later, you can also view the LabVIEW Manuals directory that contains this document by selecting **Start» All Programs»National Instruments»LabVIEW»LabVIEW Manuals**.
- *National Instruments Example Finder*—LabVIEW contains an extensive library of VIs and example programs for use with NI FlexRIO devices. To access the NI Example Finder, open LabVIEW and select **Help»Find Examples**, then select **Hardware Input and Output»FlexRIO**.

  You can also access device-specific examples by selecting **Add device** from the Hardware pull-down menu in the **NI Example Finder** window.
- *NI FlexRIO Reference and Procedures*—This book provides instructions for using LabVIEW and the LabVIEW FPGA Module with NI FlexRIO devices. This document is located in the *FPGA Module* in the *LabVIEW Help*.

Device-Specific Documentation

- *NI FlexRIO FPGA Module Specifications*—Lists the specifications of your NI FlexRIO FPGA module. To access this document, visit `ni.com/manuals`.
- *NI 5752 Specifications*—Lists the specifications and signal information for your hardware. To access these documents, refer to `ni.com/manuals`.

Additional Resources

- *LabVIEW FPGA IPNet*—Offers resources for browsing, understanding, and downloading LabVIEW FPGA functions or IP (Intellectual Property). Use this resource to acquire IP that you need for your application, download examples to help learn programming techniques, and explore the depth of IP offered by the LabVIEW FPGA platform. To access the LabVIEW FPGA IPNet, visit `ni.com/ipnet`.
- `ni.com/flexrio`—Contains product information, and helpful links to the NI FlexRIO forum and the NI community for NI FlexRIO devices.

Where to Go for Support

The National Instruments Web site is your complete resource for technical support. At `ni.com/support` you have access to everything from troubleshooting and application development self-help resources to email and phone assistance from NI Application Engineers.

National Instruments corporate headquarters is located at 11500 North Mopac Expressway, Austin, Texas, 78759-3504. National Instruments also has offices located around the world to help address your support needs. For telephone support in the United States, create your service request at `ni.com/support` and follow the calling instructions or dial 512 795 8248. For telephone support outside the United States, contact your local branch office:

Australia 1800 300 800, Austria 43 662 457990-0, Belgium 32 (0) 2 757 0020,
Brazil 55 11 3262 3599, Canada 800 433 3488, China 86 21 5050 9800,
Czech Republic 420 224 235 774, Denmark 45 45 76 26 00, Finland 358 (0) 9 725 72511,
France 01 57 66 24 24, Germany 49 89 7413130, India 91 80 41190000, Israel 972 3 6393737,
Italy 39 02 41309277, Japan 0120-527196, Korea 82 02 3451 3400, Lebanon 961 (0) 1 33 28 28,
Malaysia 1800 887710, Mexico 01 800 010 0793, Netherlands 31 (0) 348 433 466,
New Zealand 0800 553 322, Norway 47 (0) 66 90 76 60, Poland 48 22 328 90 10,
Portugal 351 210 311 210, Russia 7 495 783 6851, Singapore 1800 226 5886,
Slovenia 386 3 425 42 00, South Africa 27 0 11 805 8197, Spain 34 91 640 0085,
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