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USB-6259

NI 625x Specifications

Specifications listed below are typical at 25 °C unless otherwise noted. Refer to the *M Series User Manual* for more information about NI 625x devices.

Analog Input

Number of channels		Input impedance	
NI 6250/6251	8 differential or 16 single ended	Device on	
NI 6254/6259	16 differential or 32 single ended	AI+ to AI GND	>10 G Ω in parallel with 100 pF
NI 6255	40 differential or 80 single ended	AI- to AI GND	>10 G Ω in parallel with 100 pF
ADC resolution	16 bits	Device off	
DNL	No missing codes guaranteed	AI+ to AI GND	820 Ω
INL	Refer to the AI Absolute Accuracy Table	AI- to AI GND	820 Ω
Sampling rate		Input bias current	\pm 100 pA
Maximum		Crosstalk (at 100 kHz)	
NI 6250/6251/6254/6259	1.25 MS/s single channel, 1.00 MS/s multi-channel (aggregate)	Adjacent channels	-75 dB
NI 6255	1.25 MS/s single channel 750 kS/s multi-channel (aggregate)	Non-adjacent channels	-95 dB
Minimum	No minimum	Small signal bandwidth (-3 dB)	1.7 MHz
Timing accuracy	50 ppm of sample rate	Input FIFO size	4,095 samples
Timing resolution	50 ns	Scan list memory	4,095 entries
Input coupling	DC	Data transfers	
Input range	\pm 10 V, \pm 5 V, \pm 2 V, \pm 1 V, \pm 0.5 V, \pm 0.2 V, \pm 0.1 V	PCI/PCIe/PXI/PXIE devices	DMA (scatter-gather), interrupts, programmed I/O
Maximum working voltage for analog inputs (signal + common mode)	\pm 11 V of AI GND	USB devices	USB Signal Stream, programmed I/O
CMRR (DC to 60 Hz)	100 dB	Overvoltage protection (AI <0..79>, AI SENSE, AI SENSE 2)	
		Device on	\pm 25 V for up to four AI pins
		Device off	\pm 15 V for up to four AI pins
		Input current during overvoltage condition	\pm 20 mA max/AI pin

Settling Time for Multichannel Measurements

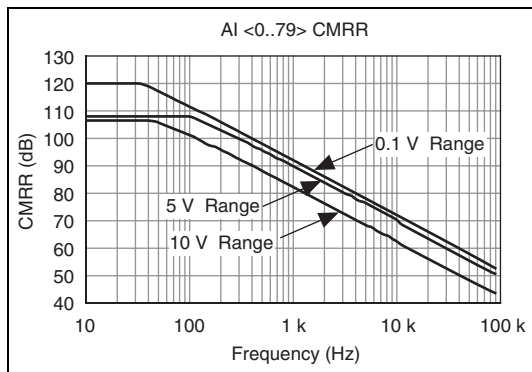
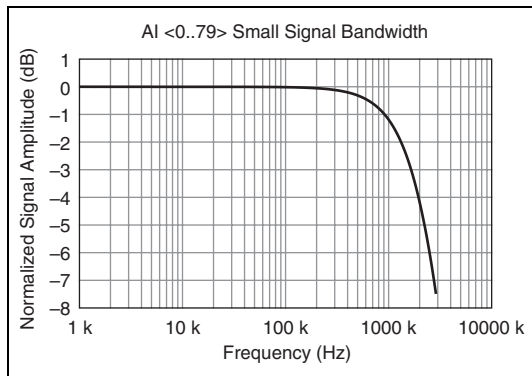
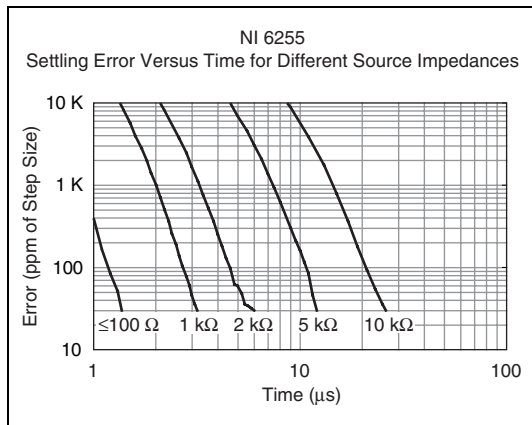
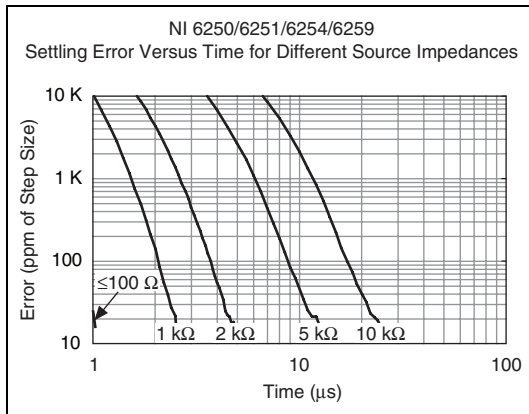
NI 6250/6251/6254/6259

Range	±60 ppm of Step (±4 LSB for Full Scale Step)	±15 ppm of Step (±1 LSB for Full Scale Step)
±10 V, ±5 V, ±2 V, ±1 V	1 μs	1.5 μs
±0.5 V	1.5 μs	2 μs
±0.2 V, ±0.1 V	2 μs	8 μs

NI 6255

Range	±60 ppm of Step (±4 LSB for Full Scale Step)	±15 ppm of Step (±1 LSB for Full Scale Step)
±10 V, ±5 V, ±2 V, ±1 V	1.3 μs	1.6 μs
±0.5 V	1.8 μs	2.5 μs
±0.2 V, ±0.1 V	3 μs	8 μs

Typical Performance Graphs



Analog Triggers

Number of triggers	1
Source	
NI 6250/6251	AI <0..15>, APFI 0
NI 6254/6259	AI <0..31>, APFI <0..1>
NI 6255	AI <0..79>, APFI 0
Functions	Start Trigger, Reference Trigger, Pause Trigger, Sample Clock, Convert Clock, Sample Clock Timebase
Source level	
AI <0..79>	±full scale
APFI <0..1>	±10 V
Resolution	10 bits, 1 in 1,024
Modes	Analog edge triggering, analog edge triggering with hysteresis, and analog window triggering
Bandwidth (–3 dB)	
AI <0..79>	3.4 MHz
APFI <0..1>	3.9 MHz
Accuracy	±1%
APFI <0..1> characteristics	
Input impedance	10 kΩ
Coupling	DC
Protection	
Power on	±30 V
Power off	±15 V

Analog Output

Number of channels	
NI 6250/6254	0
NI 6251/6255	2
NI 6259	4
DAC resolution	16 bits
DNL	±1 LSB
Monotonicity	16 bit guaranteed
Accuracy	Refer to the <i>AO Absolute Accuracy Table</i>
Maximum update rate	
1 channel	2.86 MS/s
2 channels	2.00 MS/s
3 channels	1.54 MS/s
4 channels	1.25 MS/s
Timing accuracy	50 ppm of sample rate
Timing resolution	50 ns
Output range	±10 V, ±5 V, ±external reference on APFI <0..1>
Output coupling	DC
Output impedance	0.2 Ω
Output current drive	±5 mA
Overdrive protection	±25 V
Overdrive current	20 mA
Power-on state	±5 mV ¹
Power-on glitch	1.5 V peak for 1.5 s
Output FIFO size	8,191 samples shared among channels used
Data transfers	
PCI/PCIe/PXI/PXIe devices	DMA (scatter-gather), interrupts, programmed I/O
USB devices	USB Signal Stream, programmed I/O

¹ For all USB-6251/6259 devices, when powered on, the analog output signal is not defined until after USB configuration is complete.

AO waveform modes:

- Non-periodic waveform
- Periodic waveform regeneration mode from onboard FIFO
- Periodic waveform regeneration from host buffer including dynamic update

Settling time, full scale step

15 ppm (1 LSB).....2 μ s

Slew rate20 V/ μ s

Glitch energy at midscale transition, ± 10 V range

Magnitude10 mV

Duration1 μ s

External Reference

APFI <0..1> characteristics

Input impedance.....10 k Ω

Coupling.....DC

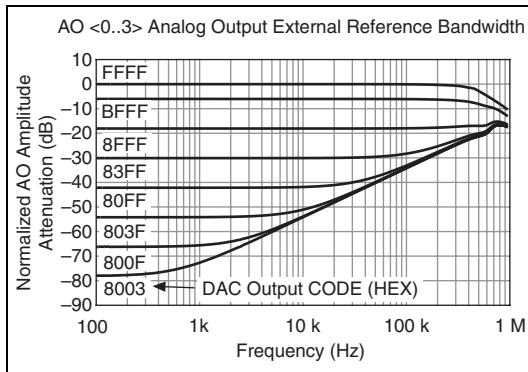
Protection

Power on..... ± 30 V

Power off ± 15 V

Range..... ± 11 V

Slew rate20 V/ μ s



Calibration (AI and AO)

Recommended warm-up time15 minutes

Calibration interval.....2 years

AI Absolute Accuracy Table

Nominal Range		Residual Gain Error (ppm of Reading)	Gain Tempco (ppm/°C)	Reference Tempco	Residual Offset Error (ppm of Range)	Offset Tempco (ppm of Range/°C)	INLError (ppm of Range)	Random Noise, σ (μ Vrms)	Absolute Accuracy at Full Scale ¹ (μ V)	Sensitivity ² (μ V)
Positive Full Scale	Negative Full Scale									
10	-10	60	13	1	20	21	60	280	1,920	112.0
5	-5	70	13	1	20	21	60	140	1,010	56.0
2	-2	70	13	1	20	24	60	57	410	22.8
1	-1	80	13	1	20	27	60	32	220	12.8
0.5	-0.5	90	13	1	40	34	60	21	130	8.4
0.2	-0.2	130	13	1	80	55	60	16	74	6.4
0.1	-0.1	150	13	1	150	90	60	15	52	6.0

Accuracies listed are valid for up to two years from the device external calibration.

AbsoluteAccuracy = Reading · (GainError) + Range · (OffsetError) + NoiseUncertainty

GainError = ResidualAIGainError + GainTempco · (TempChangeFromLastInternalCal) + ReferenceTempco · (TempChangeFromLastExternalCal)

OffsetError = ResidualAIOffsetError + OffsetTempco · (TempChangeFromLastInternalCal) + INL_Error

NoiseUncertainty = $\frac{\text{RandomNoise} \cdot 3}{\sqrt{100}}$ For a coverage factor of 3 σ and averaging 100 points.

¹ Absolute accuracy at full scale on the analog input channels is determined using the following assumptions:

TempChangeFromLastExternalCal = 10 °C

TempChangeFromLastInternalCal = 1 °C

number_of_readings = 100

CoverageFactor = 3 σ

For example, on the 10 V range, the absolute accuracy at full scale is as follows:

GainError = 60 ppm + 13 ppm · 1 + 1 ppm · 10 GainError = 83 ppm

OffsetError = 20 ppm + 21 ppm · 1 + 60 ppm OffsetError = 101 ppm

NoiseUncertainty = $\frac{275 \mu\text{V} \cdot 3}{\sqrt{100}}$ NoiseUncertainty = 83 μ V

AbsoluteAccuracy = 10 V · (GainError) + 10 V · (OffsetError) + NoiseUncertainty AbsoluteAccuracy = 1920 μ V

² Sensitivity is the smallest voltage change that can be detected. It is a function of noise.

AO Absolute Accuracy Table

Nominal Range		Residual Gain Error (ppm of Reading)	Gain Tempco (ppm/°C)	Reference Tempco	Residual Offset Error (ppm of Range)	Offset Tempco (ppm of Range/°C)	INL Error (ppm of Range)	Absolute Accuracy at Full Scale ¹ (µV)
Positive Full Scale	Negative Full Scale							
10	-10	75	17	1	40	2	64	2,080
5	-5	85	8	1	40	2	64	1,045

¹ Absolute Accuracy at full scale numbers is valid immediately following internal calibration and assumes the device is operating within 10 °C of the last external calibration. Accuracies listed are valid for up to two years from the device external calibration.

AbsoluteAccuracy = OutputValue · (GainError) + Range · (OffsetError)

GainError = ResidualGainError + GainTempco · (TempChangeFromLastInternalCal) + ReferenceTempco · (TempChangeFromLastExternalCal)

OffsetError = ResidualOffsetError + AOffsetTempco · (TempChangeFromLastInternalCal) + INL_Error

Digital I/O/PFI

Static Characteristics

Number of channels	
NI 6250/6251/6255.....	24 total, 8 (P0.<0..7>), 16 (PFI <0..7>/P1, PFI <8..15>/P2)
NI 6254/6259.....	48 total, 32 (P0.<0..31>), 16 (PFI <0..7>/P1, PFI <8..15>/P2)
Ground reference.....	D GND
Direction control.....	Each terminal individually programmable as input or output
Pull-down resistor.....	50 k Ω typ, 20 k Ω min
Input voltage protection ¹	± 20 V on up to two pins

Waveform Characteristics (Port 0 Only)

Terminals used	
NI 6250/6251/6255.....	Port 0 (P0.<0..7>)
NI 6254/6259.....	Port 0 (P0.<0..31>)
Port/sample size	
NI 6250/6251/6255.....	Up to 8 bits
NI 6254/6259.....	Up to 32 bits
Waveform generation (DO) FIFO ...	2,047 samples
Waveform acquisition (DI) FIFO ...	2,047 samples
DI Sample Clock frequency	
PCI/PCIe/PXI/PXIe devices.....	0 to 10 MHz ²
USB devices	0 to 1 MHz system dependent ²
DO Sample Clock frequency	
PCI/PCIe/PXI/PXIe devices	
Regenerate from FIFO	0 to 10 MHz
Streaming from memory	0 to 10 MHz system dependent ²
USB devices	
Regenerate from FIFO	0 to 10 MHz
Streaming from memory	0 to 1 MHz system dependent ²

Data transfers	
PCI/PCIe/PXI/PXIe devices	DMA (scatter-gather), interrupts, programmed I/O
USB devices.....	USB Signal Stream, programmed I/O
DO or DI Sample Clock source ³	Any PFI, RTSI, AI Sample or Convert Clock, AO Sample Clock, Ctr <i>n</i> Internal Output, and many other signals

PFI/Port 1/Port 2 Functionality

Functionality.....	Static digital input, static digital output, timing input, timing output
Timing output sources.....	Many AI, AO, counter, DI, DO timing signals
Debounce filter settings.....	125 ns, 6.425 μ s, 2.54 ms, disable; high and low transitions; selectable per input

¹ Stresses beyond those listed under *Input voltage protection* may cause permanent damage to the device.

² Performance can be dependent on bus latency and volume of bus activity.

³ The digital subsystem does not have its own dedicated internal timing engine. Therefore, a sample clock must be provided from another subsystem on the device or an external source.

Recommended Operation Conditions

PCI/PCIe/PXI/PXIe devices

Level	Min	Max
Input high voltage (V_{IH})	2.2 V	5.25 V
Input low voltage (V_{IL})	0 V	0.8 V
Output high current (I_{OH})		
P0.<0..31>	—	-24 mA
PFI <0..15>/P1/P2	—	-16 mA
Output low current (I_{OL})		
P0.<0..31>	—	24 mA
PFI <0..15>/P1/P2	—	16 mA

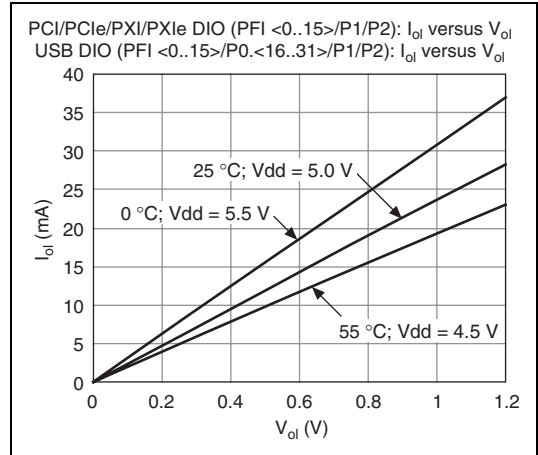
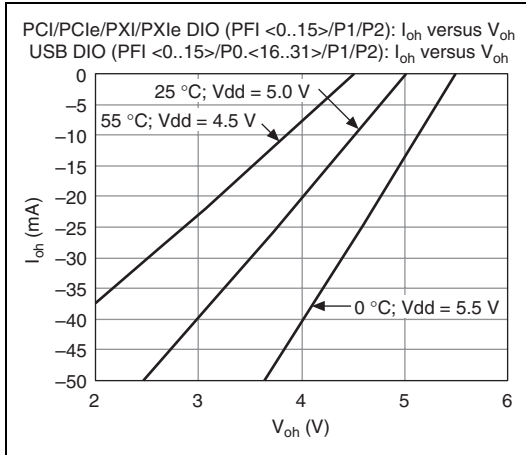
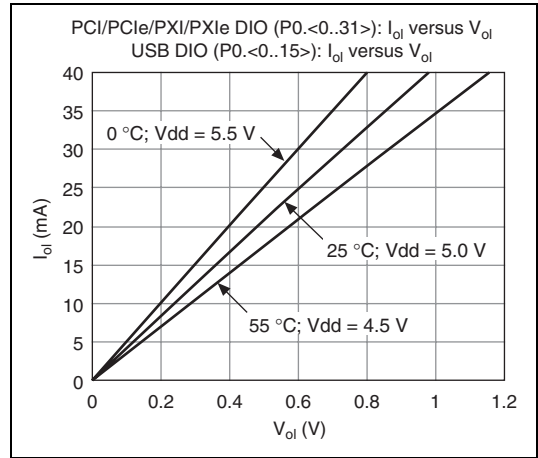
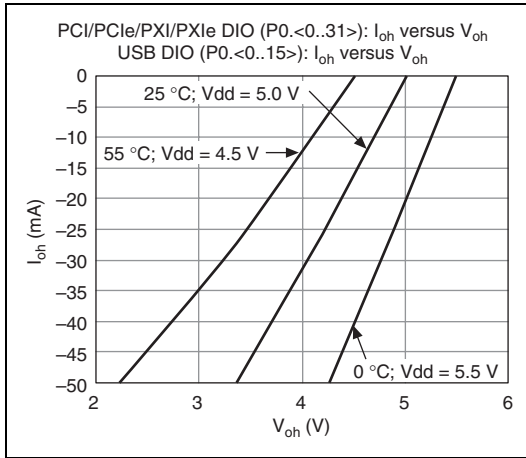
USB devices

Level	Min	Max
Input high voltage (V_{IH})	2.2 V	5.25 V
Input low voltage (V_{IL})	0 V	0.8 V
Output high current (I_{OH})		
P0.<0..15>	—	-24 mA
P0.<16..31>	—	-16 mA
PFI <0..15>/P1/P2	—	-16 mA
Output low current (I_{OL})		
P0.<0..15>	—	24 mA
P0.<16..31>	—	16 mA
PFI <0..15>/P1/P2	—	16 mA

Electrical Characteristics

Level	Min	Max
Positive-going threshold (V_{T+})	—	2.2 V
Negative-going threshold (V_{T-})	0.8 V	—
Delta VT hysteresis ($V_{T+} - V_{T-}$)	0.2 V	—
I_{IL} input low current ($V_{in} = 0$ V)	—	-10 μ A
I_{IH} input high current ($V_{in} = 5$ V)	—	250 μ A

Digital I/O Characteristics



General-Purpose Counter/Timers

Number of counter/timers	2
Resolution.....	32 bits
Counter measurements	Edge counting, pulse, semi-period, period, two-edge separation
Position measurements	X1, X2, X4 quadrature encoding with Channel Z reloading; two-pulse encoding
Output applications.....	Pulse, pulse train with dynamic updates, frequency division, equivalent time sampling
Internal base clocks	80 MHz, 20 MHz, 0.1 MHz
External base clock frequency.....	0 MHz to 20 MHz
Base clock accuracy	50 ppm
Inputs	Gate, Source, HW_Arm, Aux, A, B, Z, Up_Down
Routing options for inputs.....	Any PFI, RTSI, PXI_TRIG, PXI_STAR, analog trigger, many internal signals
FIFO	2 samples
Data transfers	
PCI/PCIe/PXI/PXIe devices	Dedicated scatter-gather DMA controller for each counter/timer; interrupts, programmed I/O
USB devices.....	USB Signal Stream, programmed I/O

Frequency Generator

Number of channels.....	1
Base clocks.....	10 MHz, 100 kHz
Divisors	1 to 16
Base clock accuracy	50 ppm
Output can be available on any PFI or RTSI terminal.	

Phase-Locked Loop (PLL)

Number of PLLs	1
Reference signal.....	PXI_STAR, PXI_CLK10, RTSI <0..7>
Output of PLL.....	80 MHz Timebase; other signals derived from 80 MHz Timebase including 20 MHz and 100 kHz Timebases

External Digital Triggers

Source	Any PFI, RTSI, PXI_TRIG, PXI_STAR
Polarity.....	Software-selectable for most signals
Analog input function	Start Trigger, Reference Trigger, Pause Trigger, Sample Clock, Convert Clock, Sample Clock Timebase
Analog output function	Start Trigger, Pause Trigger, Sample Clock, Sample Clock Timebase
Counter/timer functions	Gate, Source, HW_Arm, Aux, A, B, Z, Up_Down
Digital waveform generation (DO) function.....	Sample Clock
Digital waveform acquisition (DI) function	Sample Clock

Device-To-Device Trigger Bus

PCI/PCIe devices	RTSI <0..7> ¹
PXI/PXIe devices.....	PXI_TRIG <0..7>, PXI_STAR
USB devices.....	None
Output selections.....	10 MHz Clock; frequency generator output; many internal signals
Debounce filter settings	125 ns, 6.425 μ s, 2.54 ms, disable; high and low transitions; selectable per input

Bus Interface

PCI/PXI/PXIe devices	3.3 V or 5 V signal environment
PCIe devices	
Form factor	x1 PCI Express, specification v1.0a compliant
Slot compatibility	x1, x4, x8, and x16 PCI Express slots ²
USB devices.....	USB 2.0 Hi-Speed or full-speed ^{3,4}
DMA channels (PCI/PCIe/PXI/PXIe devices).....	6, analog input, analog output, digital input, digital output, counter/timer 0, counter/timer 1
USB Signal Stream (USB devices).....	4, can be used for analog input, analog output, digital input, digital output, counter/timer 0, counter/timer 1

All PXI-625x devices support one of the following features:

- May be installed in PXI Express hybrid slots
- Or, may be used to control SCXI in PXI/SCXI combo chassis

Table 1. PXI and PXI Express Chassis

Device	Part Number	SCXI Control in PXI/SCXI Combo Chassis	PXI Express Hybrid Slot Compatible
PXI-6250	191325D-04	No	Yes
PXI-6251	191325D-03	No	Yes
	191325D-13	Yes	No
PXI-6254	191325D-02	No	Yes
PXI-6255	193618A-01	No	Yes
PXI-6259	191325D-01	No	Yes
	191325D-11	Yes	No
Earlier versions of PXI-625x	191325C-0x 191325B-0x	Yes	No

All NI PXIe-625x devices may be installed in PXI Express slots or PXI Express hybrid slots.

Power Requirements

Current draw from bus during no-load condition⁵

PCI/PXI devices

+5 V	0.03 A
+3.3 V	0.725 A
+12 V	0.35 A

PCIe devices

+3.3 V	0.925 A
+12 V	0.35 A

¹ In other sections of this document, *RTSI* refers to *RTSI <0..7>* for PCI/PCIe devices or *PXI_TRIG <0..7>* for PXI/PXIe devices.

² Some motherboards reserve the x16 slot for graphics use. For PCI Express guidelines, refer to ni.com/pciexpress.

³ If you are using a USB M Series device in full-speed mode, device performance will be lower and you will not be able to achieve maximum sampling/update rates.

⁴ Operating on a full-speed bus may result in lower high-speed full-speed performance.

⁵ Does not include P0/PFI/P1/P2 and +5 V terminals.

PXIe devices	
+3.3 V	0.45 A
+12 V	0.5 A

Current draw from bus during AI and AO overvoltage condition¹

PCI/PXI devices	
+5 V	0.03 A
+3.3 V	1.2 A
+12 V	0.38 A

PCIe devices	
+3.3 V	1.4 A
+12 V	0.38 A

PXIe devices	
+3.3 V	0.48 A
+12 V	0.71 A



Caution USB-625x devices *must* be powered with NI offered AC adapter or a National Electric Code (NEC) Class 2 DC source that meets the power requirements for the device and has appropriate safety certification marks for country of use.

USB power supply requirements.....11 to 30 VDC, 20 W

Power Limits



Caution Exceeding the power limits may cause unpredictable behavior by the device and/or PC/chassis.

PCI devices	
+5 V terminal (connector 0).....	1 A max ²
+5 V terminal (connector 1).....	1 A max ²

PCIe devices	
Without disk drive power connector installed	
+5 V terminals combined	0.35 A max ²
P0/PFI/P1/P2 and +5 V terminals combined	0.39 A max
With disk drive power connector installed	
+5 V terminal (connector 0) ...	1 A max ²
+5 V terminal (connector 1) ...	1 A max ²
P0/PFI/P1/P2 combined	0.39 A max

PXI/PXIe devices	
+5 V terminal (connector 0).....	1 A max ²
+5 V terminal (connector 1).....	1 A max ²

P0/PFI/P1/P2 and +5 V terminals combined	2 A max
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USB devices	
+5 V terminal	1 A max ²
P0/PFI/P1/P2 and +5 V terminals combined	2 A max
Power supply fuse	2 A, 250 V

Physical Requirements

Printed circuit board dimensions	
NI PCI-6250/6251/6254/6255/6259	9.7 × 15.5 cm (3.8 × 6.1 in.)
NI PCIe-6251/6259	9.9 × 16.8 cm (3.9 × 6.6 in.) (half-length)
NI PXI/PXIe-6250/6251/6254/6255/6259	Standard 3U PXI

Enclosure dimensions (includes connectors)	
NI USB-6251/6259	26.67 × 17.09 × 4.45 cm (10.5 × 6.73 × 1.75 in.)
NI USB-6251/6259 Mass Termination.....	18.8 × 17.09 × 4.45 cm (7.4 × 6.73 × 1.75 in.)

Weight	
NI PCI-6250	142 g (5 oz)
NI PCI-6251	149 g (5.2 oz)
NI PCI-6254	152 g (5.3 oz)
NI PCI-6255	164 g (5.8 oz)
NI PCI-6259	162 g (5.6 oz)
NI PCIe-6251	161 g (5.7 oz)
NI PCIe-6259	175 g (6.1 oz)
NI PXI-6250	212 g (7.5 oz)
NI PXI-6251/6254	222 g (7.8 oz)
NI PXI-6255	236 g (8.3 oz)
NI PXI-6259	233 g (8.2 oz)
NI PXIe-6251	215 g (7.5 oz)
NI PXIe-6259	226 g (7.9 oz)
NI USB-6251	1.2 kg (2 lb 10 oz)
NI USB-6259	1.24 kg (2 lb 11 oz)
NI USB-6251/6259 Mass Termination.....	907 g (2 lb)
NI USB-6251 OEM.....	140 g (4.9 oz)
NI USB-6259 OEM.....	172 g (6.1 oz)

¹ Does not include P0/PFI/P1/P2 and +5 V terminals.

² Has a self-resetting fuse that opens when current exceeds this specification.

I/O connector

NI PCI/PCIe/PXI/PXIe-6250/6251	1 68-pin VHDCI
NI PCI/PCIe/PXI/PXIe-6254/6255/6259	2 68-pin VHDCI
NI USB-6251	64 screw terminals
NI USB-6259	128 screw terminals
NI USB-6251	
Mass Termination	1 68-pin SCSI
NI USB-6259	
Mass Termination	2 68-pin SCSI

Disk drive power connector

(PCIe devices)	Standard ATX peripheral connector (not serial ATA)
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Maximum Working Voltage¹

NI 6250/6251/6254/6255/6259	
Channel-to-earth	11 V, Measurement Category I



Caution Do *not* use for measurements within Categories II, III, or IV.

Environmental

Operating temperature

PCI/PXI/PXIe devices	0 to 55 °C
PCIe devices	0 to 50 °C
USB devices	0 to 45 °C

Storage temperature

.....	-20 to 70 °C
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Humidity

.....	10 to 90% RH, noncondensing
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Maximum altitude

.....	2,000 m
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Pollution Degree

(indoor use only)

.....	2
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Shock and Vibration (PXI/PXIe Devices Only)

Operational shock	30 g peak, half-sine, 11 ms pulse (Tested in accordance with IEC-60068-2-27. Test profile developed in accordance with MIL-PRF-28800F.)
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Random vibration

Operating	5 to 500 Hz, 0.3 g _{rms}
Nonoperating	5 to 500 Hz, 2.4 g _{rms} (Tested in accordance with IEC-60068-2-64. Nonoperating test profile exceeds the requirements of MIL-PRF-28800F, Class 3.)

Safety

This product is designed to meet the requirements of the following standards of safety for electrical equipment for measurement, control, and laboratory use:

- IEC 61010-1, EN 61010-1
- UL 61010-1, CSA 61010-1



Note For UL and other safety certifications, refer to the product label or visit ni.com/certification, search by model number or product line, and click the appropriate link in the Certification column.

Electromagnetic Compatibility

This product is designed to meet the requirements of the following standards of EMC for electrical equipment for measurement, control, and laboratory use:

- EN 61326 EMC requirements; Minimum Immunity
- EN 55011 Emissions; Group 1, Class A
- CE, C-Tick, ICES, and FCC Part 15 Emissions; Class A



Note For EMC compliance, operate this device according to product documentation.

CE Compliance

This product meets the essential requirements of applicable European Directives, as amended for CE marking, as follows:

- 73/23/EEC; Low-Voltage Directive (safety)
- 89/336/EEC; Electromagnetic Compatibility Directive (EMC)



Note Refer to the Declaration of Conformity (DoC) for this product for any additional regulatory compliance information. To obtain the DoC for this product, visit ni.com/certification, search by model number or product line, and click the appropriate link in the Certification column.

¹ *Maximum working voltage* refers to the signal voltage plus the common-mode voltage.

Waste Electrical and Electronic Equipment (WEEE)



EU Customers At the end of their life cycle, all products must be sent to a WEEE recycling center. For more information about WEEE recycling centers and National Instruments WEEE initiatives, visit ni.com/environment/weee.htm.

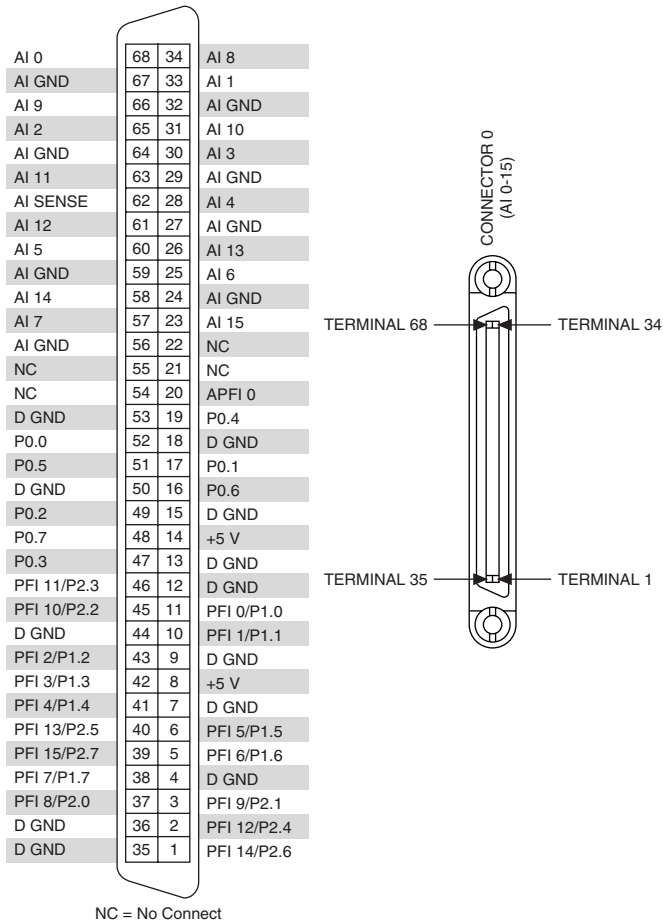


Figure 1. NI PCI/PXI-6250 Pinout

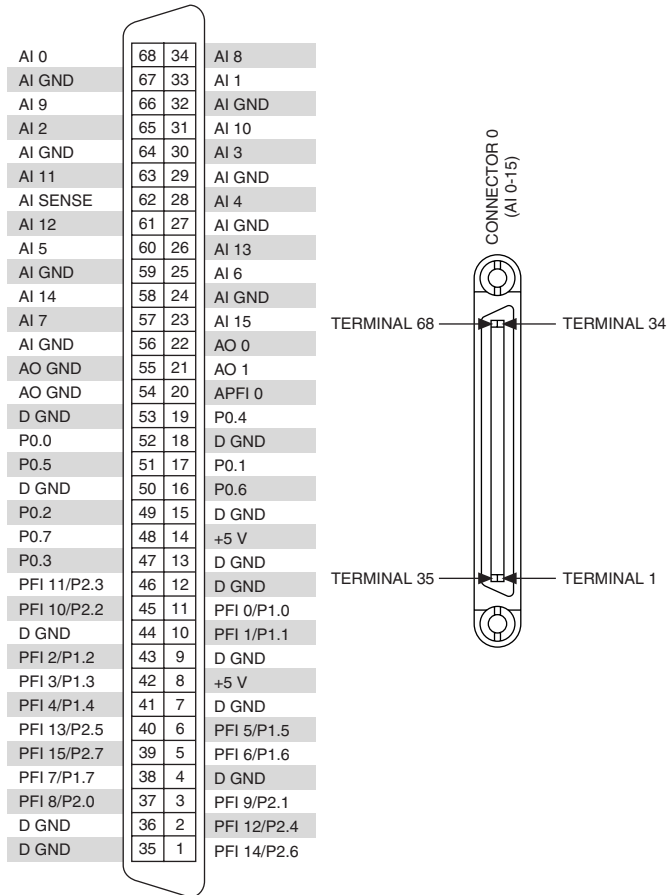


Figure 2. NI PCI/PCIe/PXI/PXIe-6251 Pinout

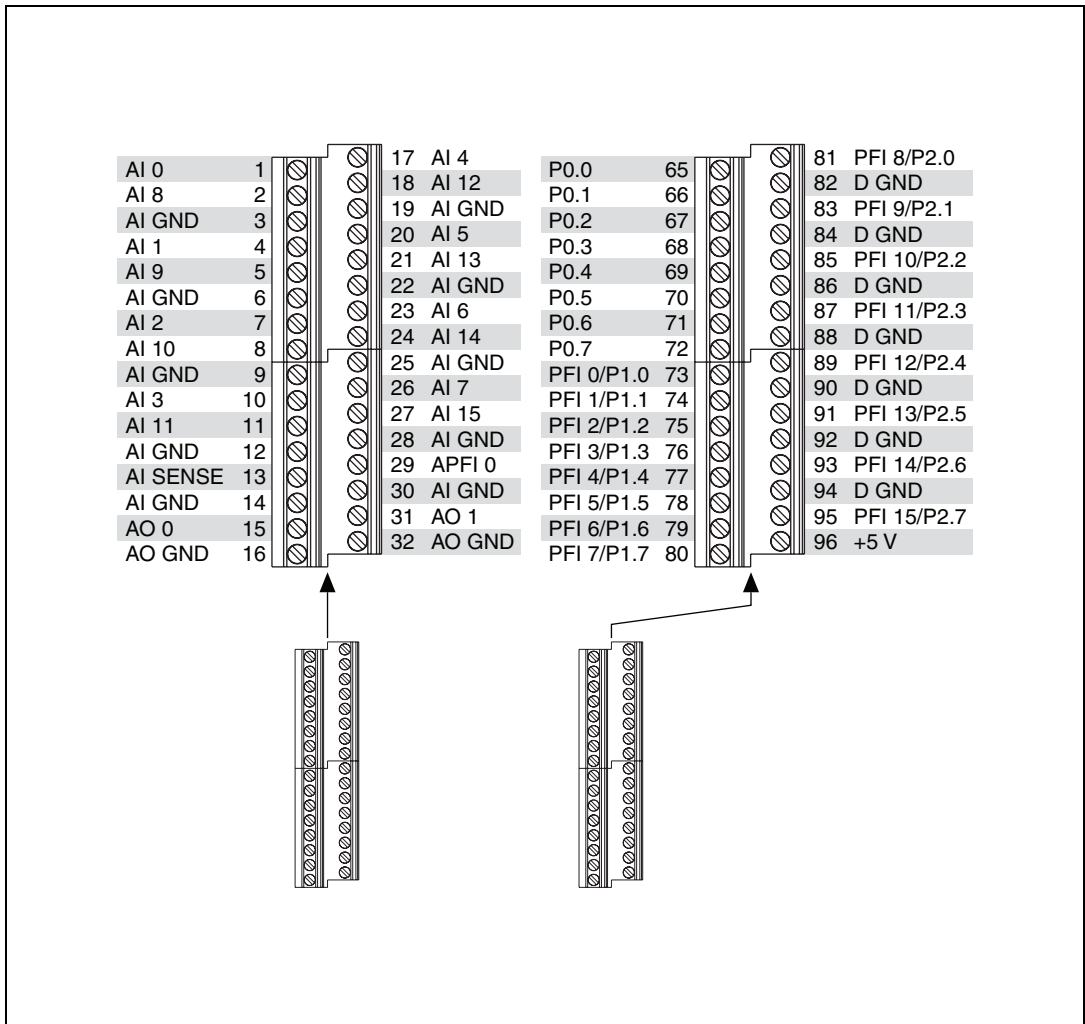


Figure 3. NI USB-6251 Pinout

AI 8	34	68	AI 0
AI 1	33	67	AI GND
AI GND	32	66	AI 9
AI 10	31	65	AI 2
AI 3	30	64	AI GND
AI GND	29	63	AI 11
AI 4	28	62	AI SENSE
AI GND	27	61	AI 12
AI 13	26	60	AI 5
AI 6	25	59	AI GND
AI GND	24	58	AI 14
AI 15	23	57	AI 7
AO 0	22	56	AI GND
AO 1	21	55	AO GND
APFI 0	20	54	AO GND
P0.4	19	53	D GND
D GND	18	52	P0.0
P0.1	17	51	P0.5
P0.6	16	50	D GND
D GND	15	49	P0.2
+5 V	14	48	P0.7
D GND	13	47	P0.3
D GND	12	46	PFI 11/P2.3
PFI 0/P1.0	11	45	PFI 10/P2.2
PFI 1/P1.1	10	44	D GND
D GND	9	43	PFI 2/P1.2
+5 V	8	42	PFI 3/P1.3
D GND	7	41	PFI 4/P1.4
PFI 5/P1.5	6	40	PFI 13/P2.5
PFI 6/P1.6	5	39	PFI 15/P2.7
D GND	4	38	PFI 7/P1.7
PFI 9/P2.1	3	37	PFI 8/P2.0
PFI 12/P2.4	2	36	D GND
PFI 14/P2.6	1	35	D GND

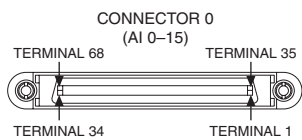


Figure 4. NI USB-6251 Mass Termination Pinout

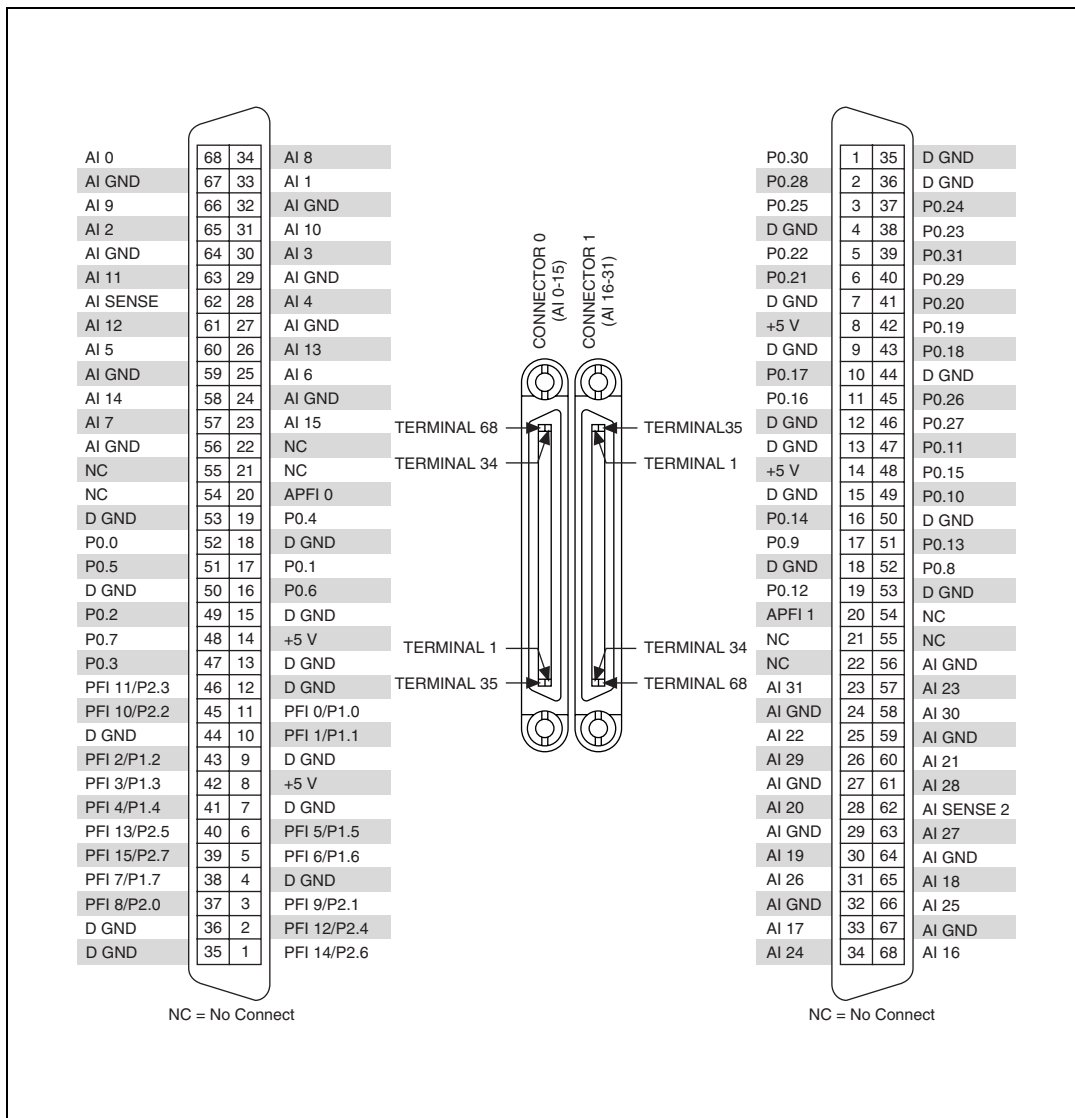


Figure 5. NI PCI/PXI-6254 Pinout

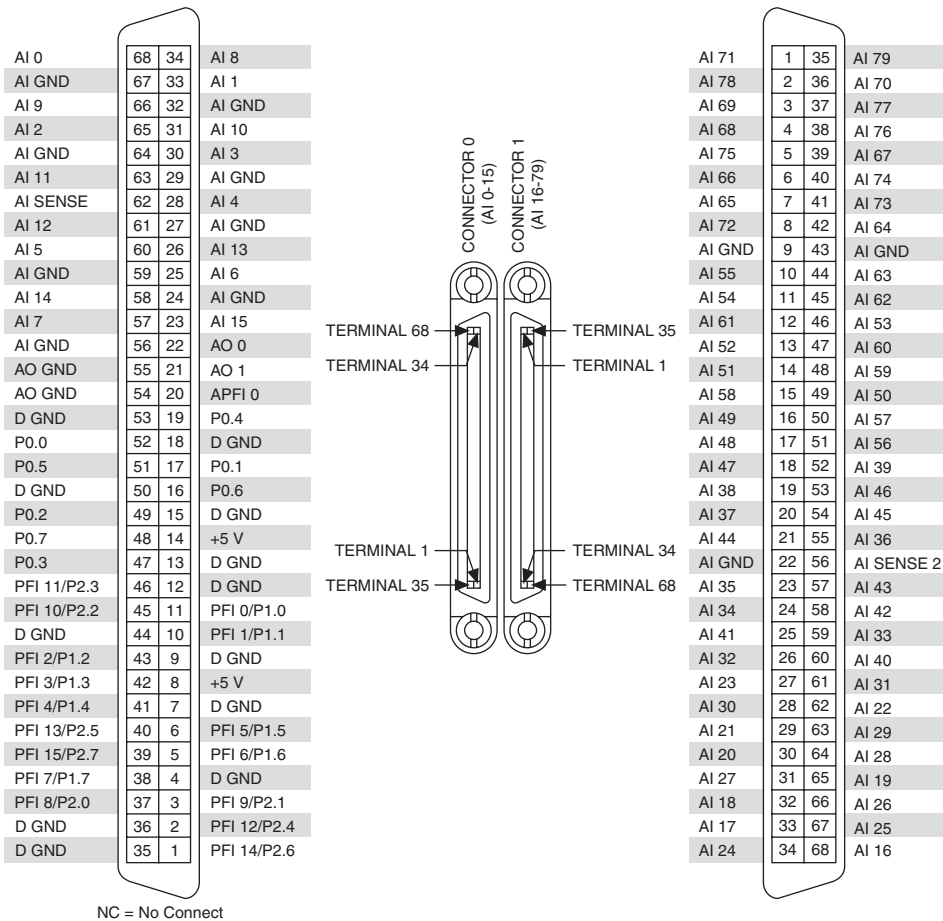


Figure 6. NI PCI/PXI-6255 Pinout

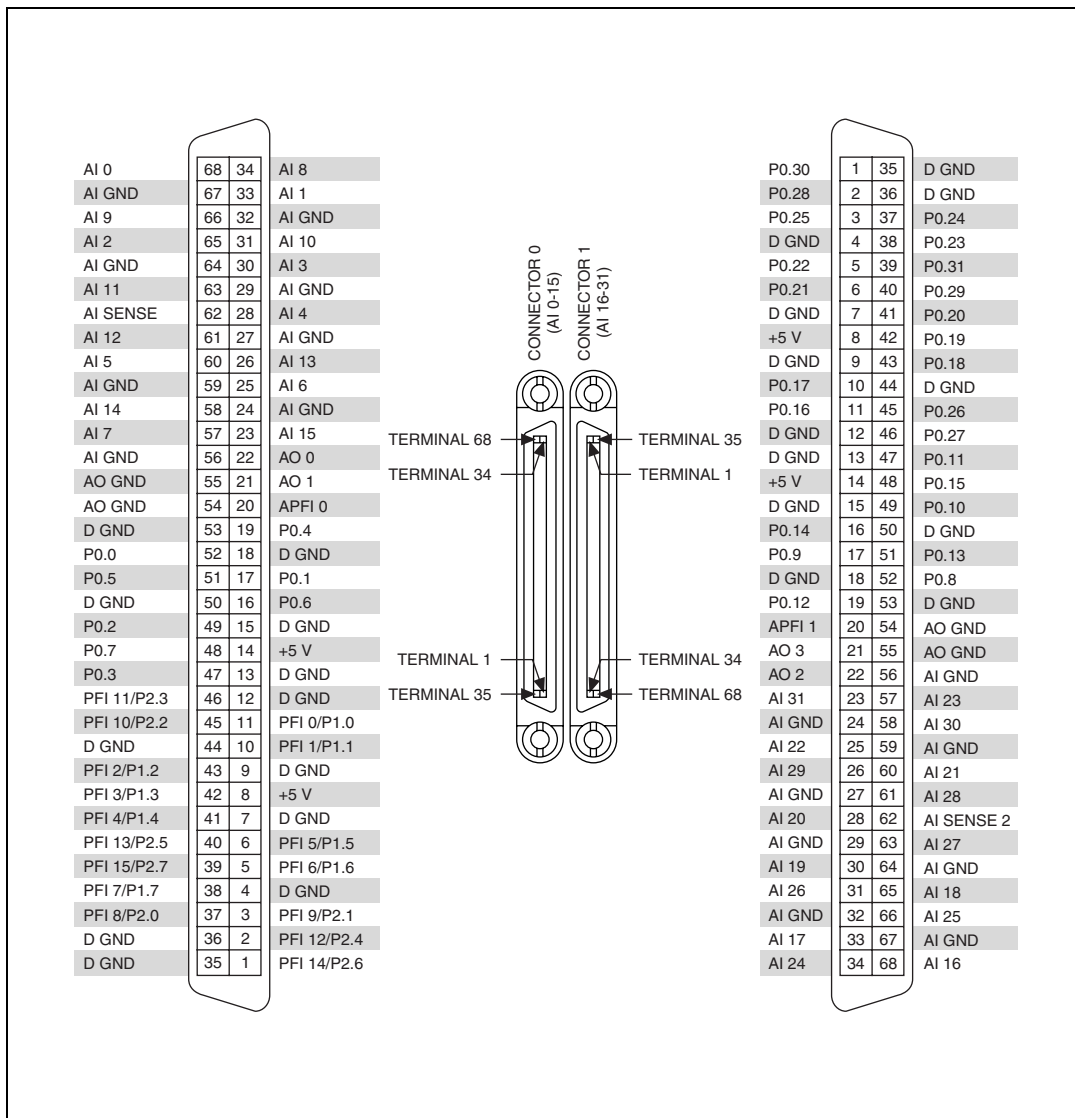
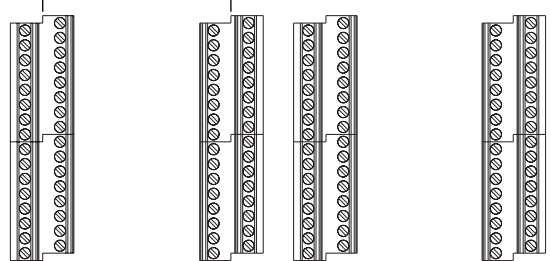


Figure 7. NI PCI/PCIe/PXI/PXIe-6259 Pinout

AI 0	1	17 AI 4	49 AI 20
AI 8	2	18 AI 12	50 AI 28
AI GND	3	19 AI GND	51 AI GND
AI 1	4	20 AI 5	52 AI 21
AI 9	5	21 AI 13	53 AI 29
AI GND	6	22 AI GND	54 AI GND
AI 2	7	23 AI 6	55 AI 22
AI 10	8	24 AI 14	56 AI 30
AI GND	9	25 AI GND	57 AI GND
AI 3	10	26 AI 7	58 AI 23
AI 11	11	27 AI 15	59 AI 31
AI GND	12	28 AI GND	60 AI GND
AI SENSE	13	29 APFI 0	61 APFI 1
AI GND	14	30 AI GND	62 AI GND
AO 0	15	31 AO 1	63 AO 3
AO GND	16	32 AO GND	64 AO GND
AI 16	33	AI 17	36
AI 24	34	AI 25	37
AI GND	35	AI GND	38
AI 18	39	AI 26	40
AI GND	41	AI GND	42
AI 19	42	AI 27	43
AI GND	44	AI GND	45
AI SENSE 2	45	AI GND	46
AI GND	46	AO 2	47
AO GND	48	AO GND	48



P0.0	65	81 PFI 8/P2.0	113 P0.24
P0.1	66	82 D GND	114 D GND
P0.2	67	83 PFI 9/P2.1	115 P0.25
P0.3	68	84 D GND	116 D GND
P0.4	69	85 PFI 10/P2.2	117 P0.26
P0.5	70	86 D GND	118 D GND
P0.6	71	87 PFI 11/P2.3	119 P0.27
P0.7	72	88 D GND	120 D GND
PFI 0/P1.0	73	89 PFI 12/P2.4	121 P0.28
PFI 1/P1.1	74	90 D GND	122 D GND
PFI 2/P1.2	75	91 PFI 13/P2.5	123 P0.29
PFI 3/P1.3	76	92 D GND	124 D GND
PFI 4/P1.4	77	93 PFI 14/P2.6	125 P0.30
PFI 5/P1.5	78	94 D GND	126 D GND
PFI 6/P1.6	79	95 PFI 15/P2.7	127 P0.31
PFI 7/P1.7	80	96 +5 V	128 D GND
P0.8	97	P0.9	98
P0.10	99	P0.11	100
P0.12	101	P0.13	102
P0.14	103	P0.15	104
P0.16	105	P0.17	106
P0.18	107	P0.19	108
P0.20	109	P0.21	110
P0.22	111	P0.23	112

Figure 8. NI USB-6259 Pinout

AI 8	34	68	AI 0	34	68	AI 16
AI 1	33	67	AI GND	33	67	AI GND
AI GND	32	66	AI 9	32	66	AI 25
AI 10	31	65	AI 2	31	65	AI 18
AI 3	30	64	AI GND	30	64	AI GND
AI GND	29	63	AI 11	29	63	AI 27
AI 4	28	62	AI SENSE	28	62	AI SENSE 2
AI GND	27	61	AI 12	27	61	AI 28
AI 13	26	60	AI 5	26	60	AI 21
AI 6	25	59	AI GND	25	59	AI GND
AI GND	24	58	AI 14	24	58	AI 30
AI 15	23	57	AI 7	23	57	AI 23
AO 0	22	56	AI GND	22	56	AI GND
AO 1	21	55	AO GND	21	55	AO GND
APFI 0	20	54	AO GND	20	54	AO GND
P0.4	19	53	D GND	19	53	D GND
D GND	18	52	P0.0	18	52	P0.8
P0.1	17	51	P0.5	17	51	P0.13
P0.6	16	50	D GND	16	50	D GND
D GND	15	49	P0.2	15	49	P0.10
+5 V	14	48	P0.7	14	48	P0.15
D GND	13	47	P0.3	13	47	P0.11
D GND	12	46	PFI 11/P2.3	12	46	P0.27
PFI 0/P1.0	11	45	PFI 10/P2.2	11	45	P0.26
PFI 1/P1.1	10	44	D GND	10	44	D GND
D GND	9	43	PFI 2/P1.2	9	43	P0.18
+5 V	8	42	PFI 3/P1.3	8	42	P0.19
D GND	7	41	PFI 4/P1.4	7	41	P0.20
PFI 5/P1.5	6	40	PFI 13/P2.5	6	40	P0.29
PFI 6/P1.6	5	39	PFI 15/P2.7	5	39	P0.31
D GND	4	38	PFI 7/P1.7	4	38	P0.23
PFI 9/P2.1	3	37	PFI 8/P2.0	3	37	P0.24
PFI 12/P2.4	2	36	D GND	2	36	D GND
PFI 14/P2.6	1	35	D GND	1	35	D GND

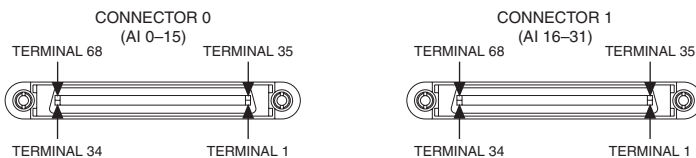


Figure 9. NI USB-6259 Mass Termination Pinout

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